CSE:215 EDA

Digital Access Control Physical Synthesis Project 3

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Department: CESS

Introduction:

This is a report for Part 3 of the Project of Electronic Design Automation which is developing the physical Synthesis of my design to produce the code_chip.cif file which will be sent to factory to manufacture the IC and to produce this file I passed by 4 parts which are:

1. High-Level Design.
2. Low-Level Synthesis.
3. Design for test.
4. Placement and Routing (this document)

I passed by some Alliance tools such as :

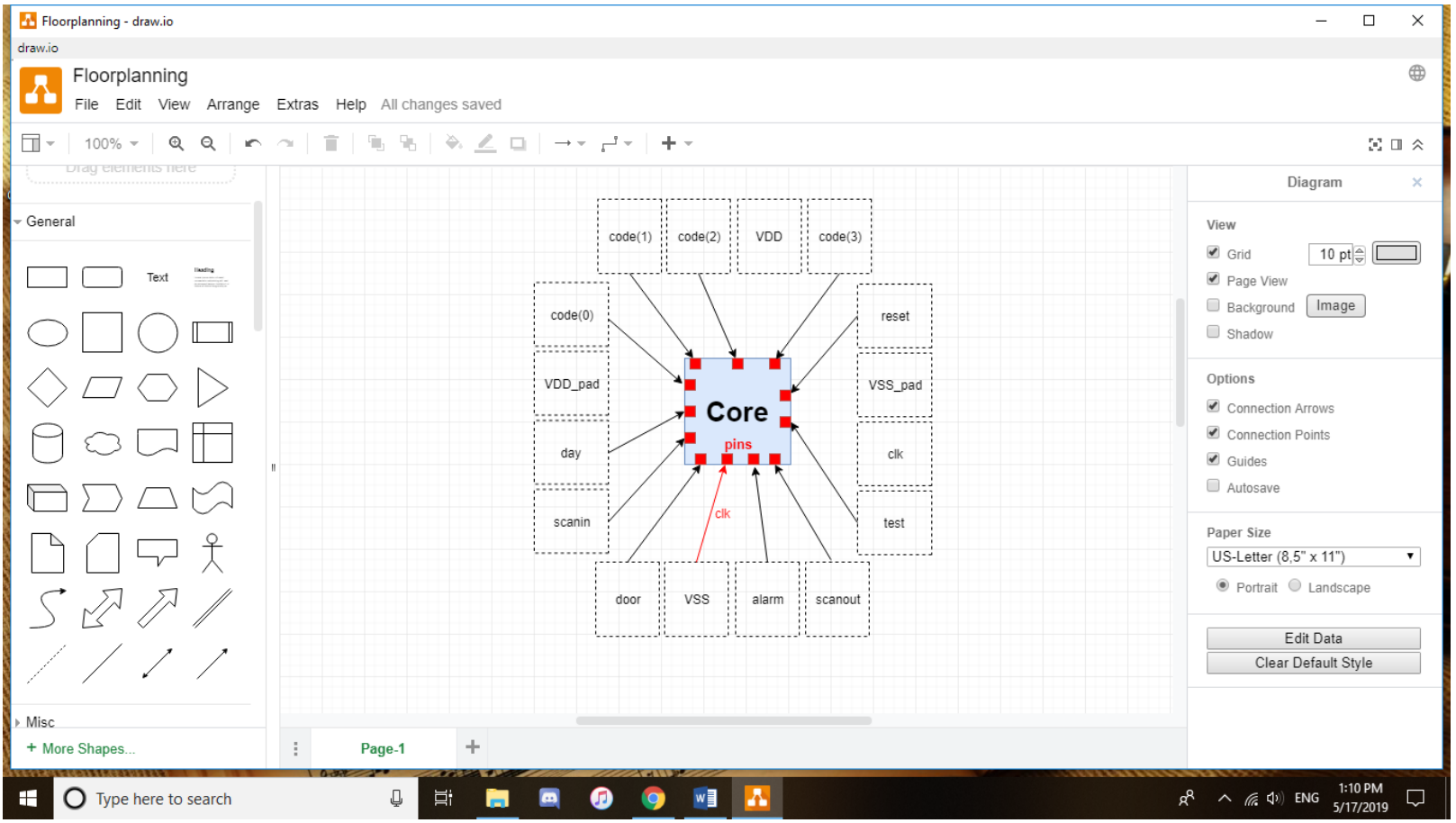
- ocp: Standard Cell Placer.
- nero: Over-Cell Router.
- cougar: Symbolic Netlist Extractor.
- lvx: Netlist comparator.
- graal: Symbolic layout editor.
- druc: Symbolic Design-rule checker.
- Ring: Pad ring router.
- s2r : Symbolic-to-Real layout converter.

- dreal : Real layout editor.

This Report consist of :

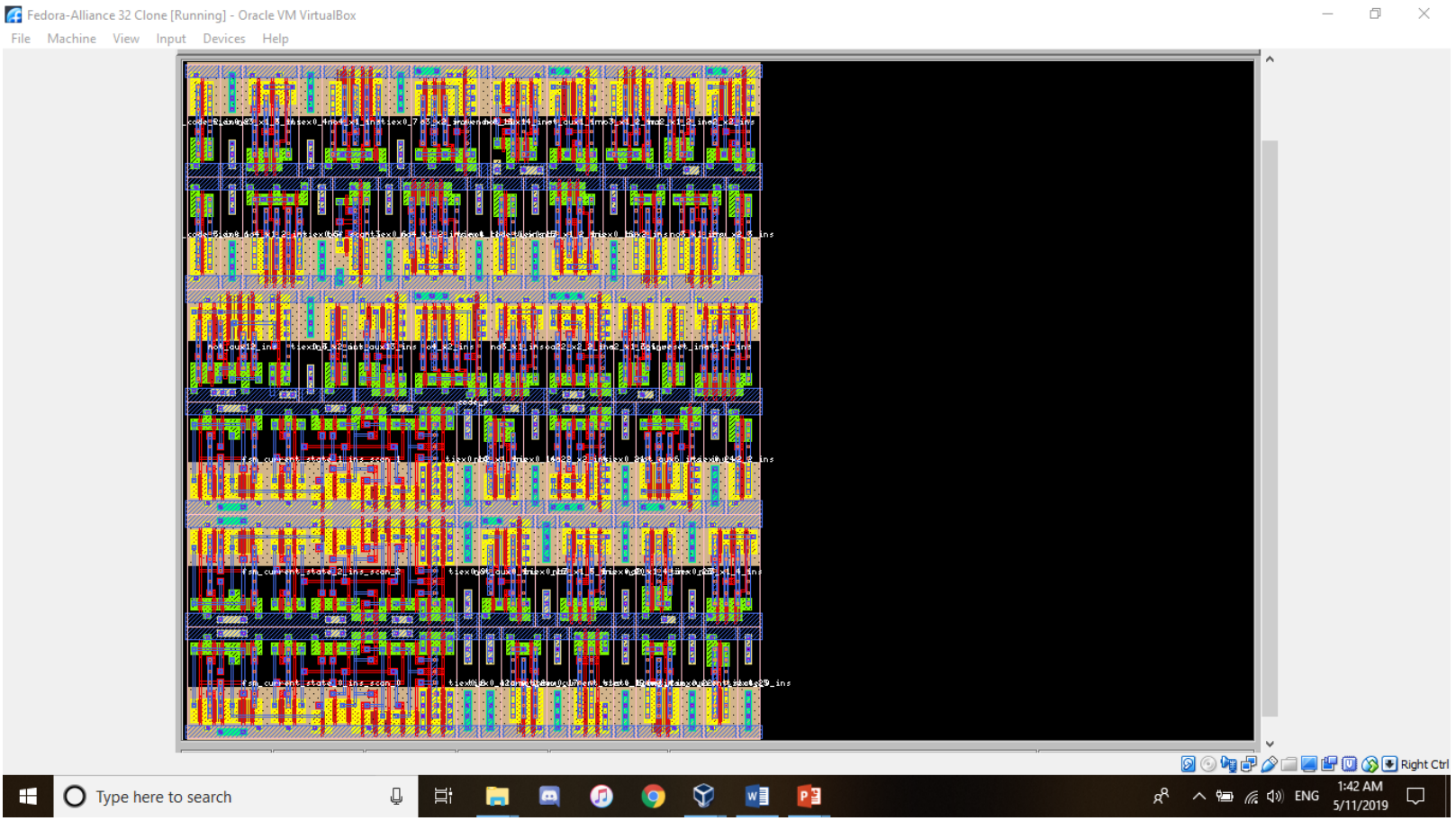
1. Floorplanning
2. Placement (graal)
3. Placement(Flattened)
4. Routing(graal)
5. Final cif layout (dreal)
6. Final cif layout (flattened)
7. .out files of the tools output
8. Appendices(Makefile + code.ioc)

1.Floorplanning



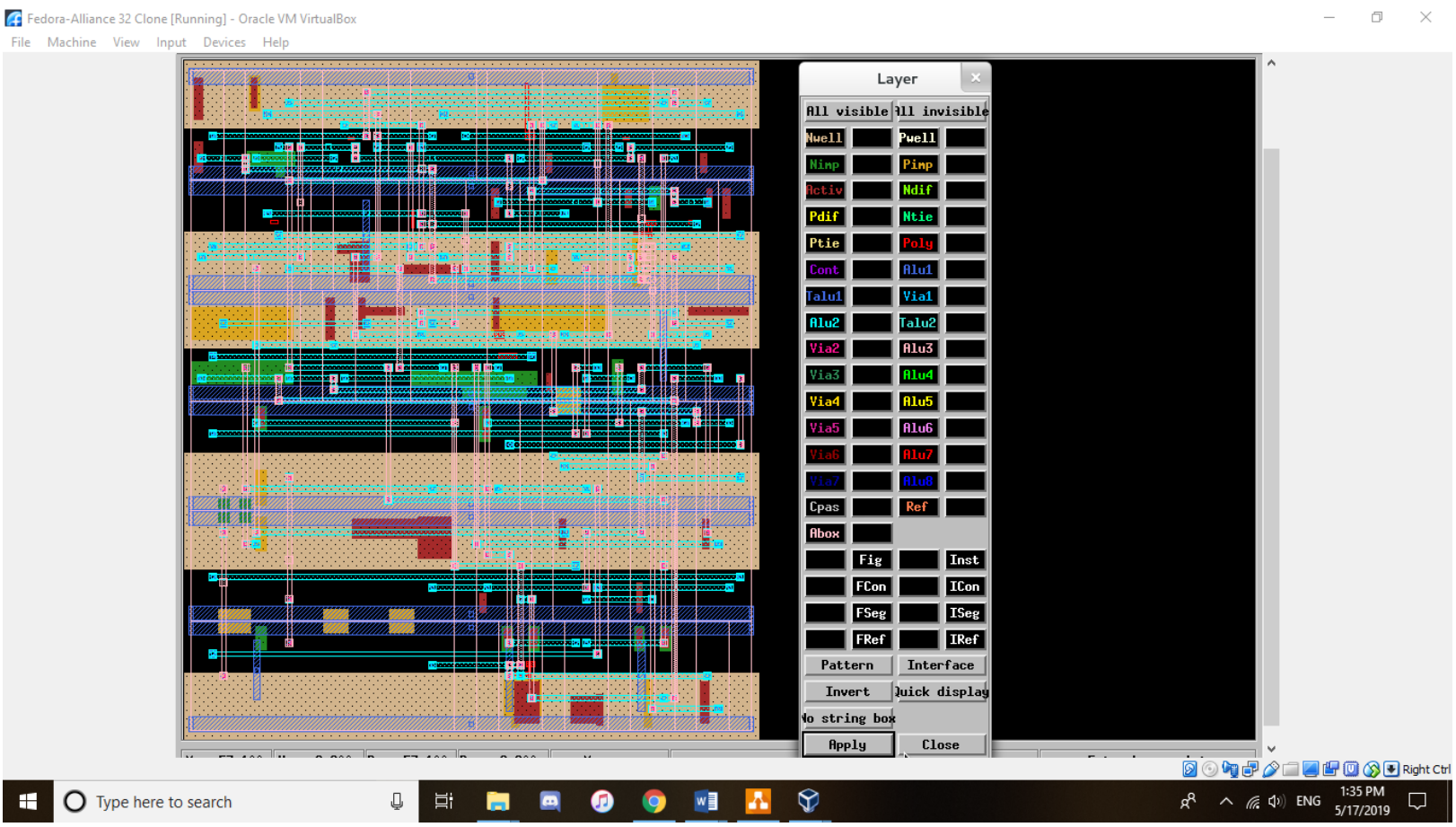
2.Placemet (graal)

3. Placement (flattened)

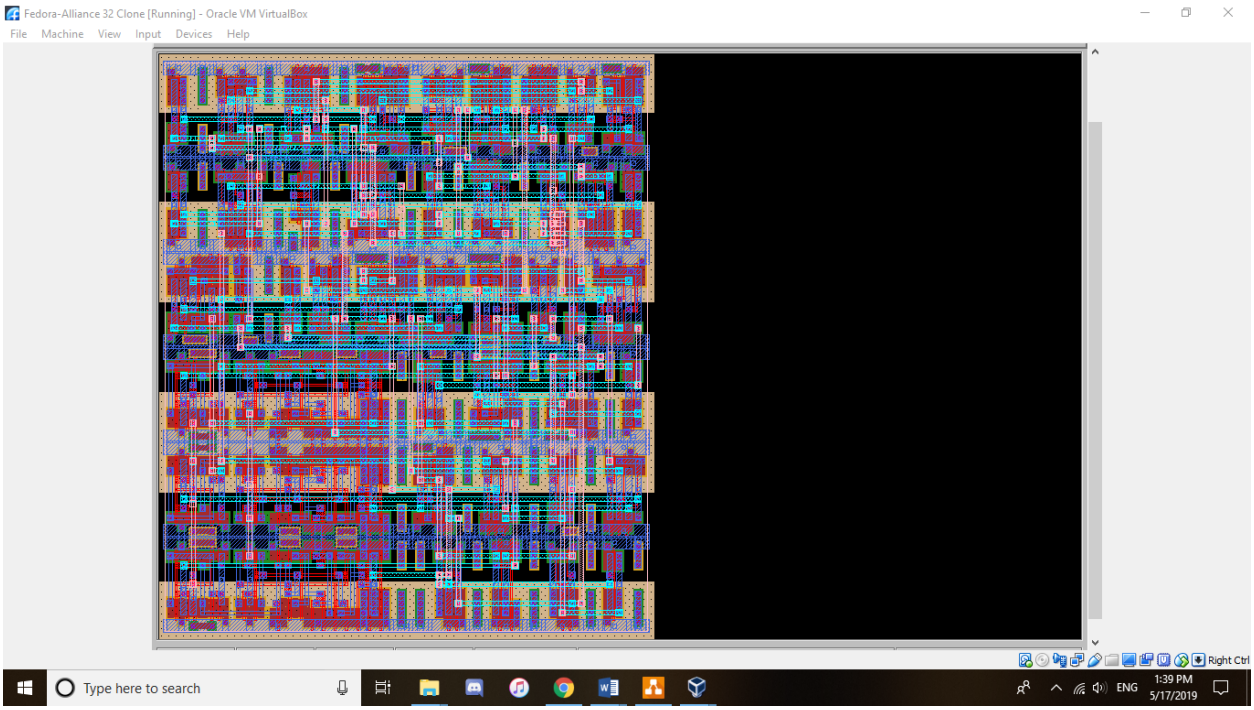


4. Routing (graal)

5.Final cif layout (dreal)

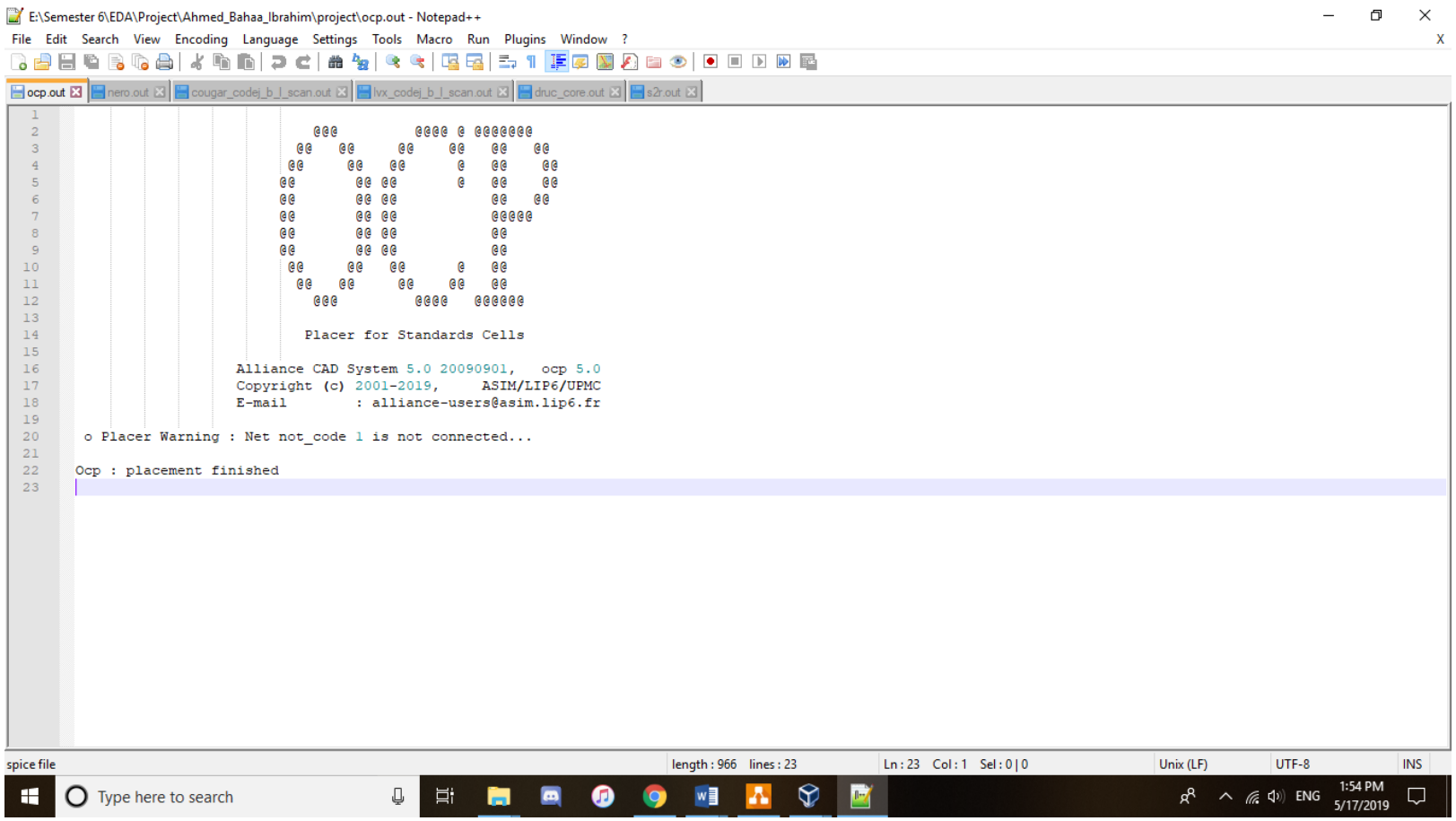


6.Final cif layout (flattened)

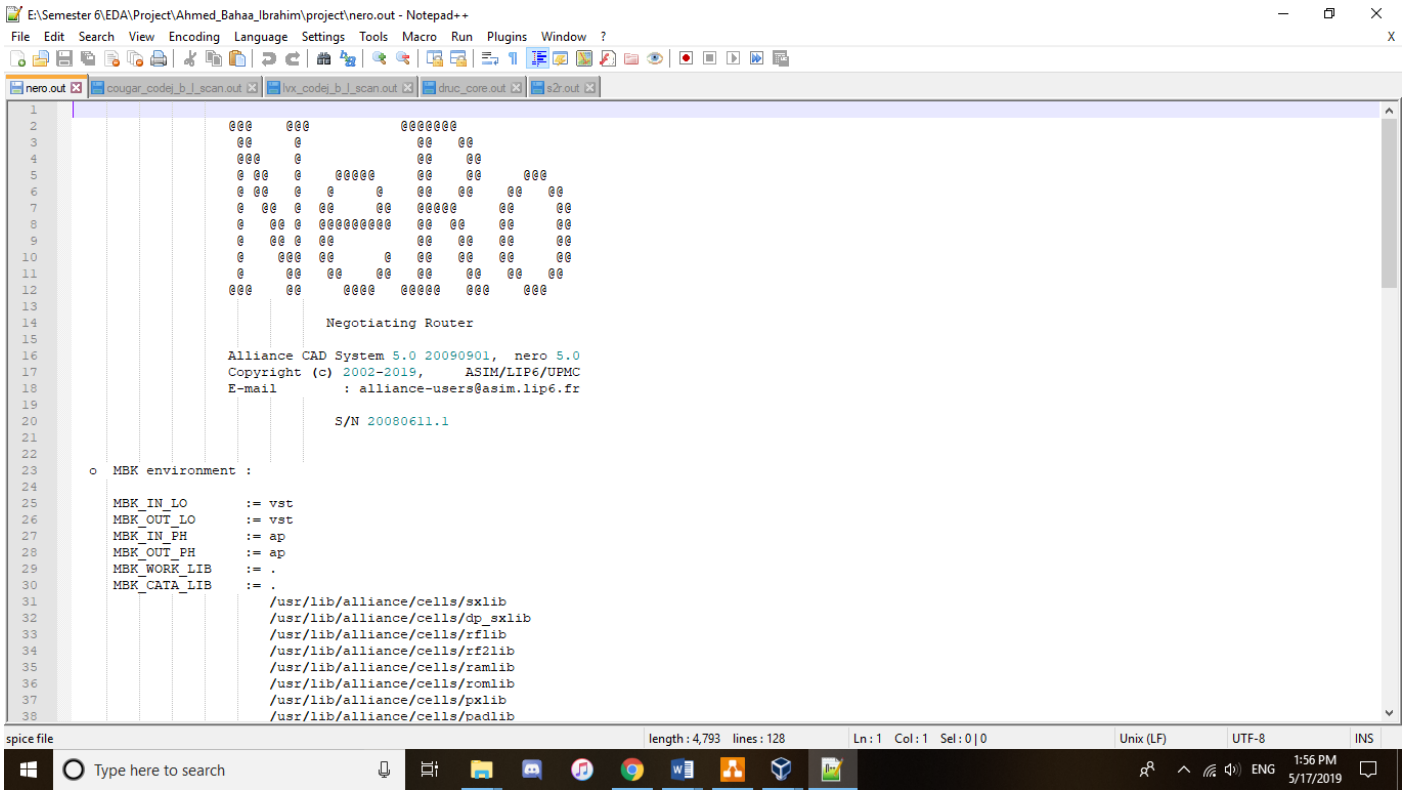


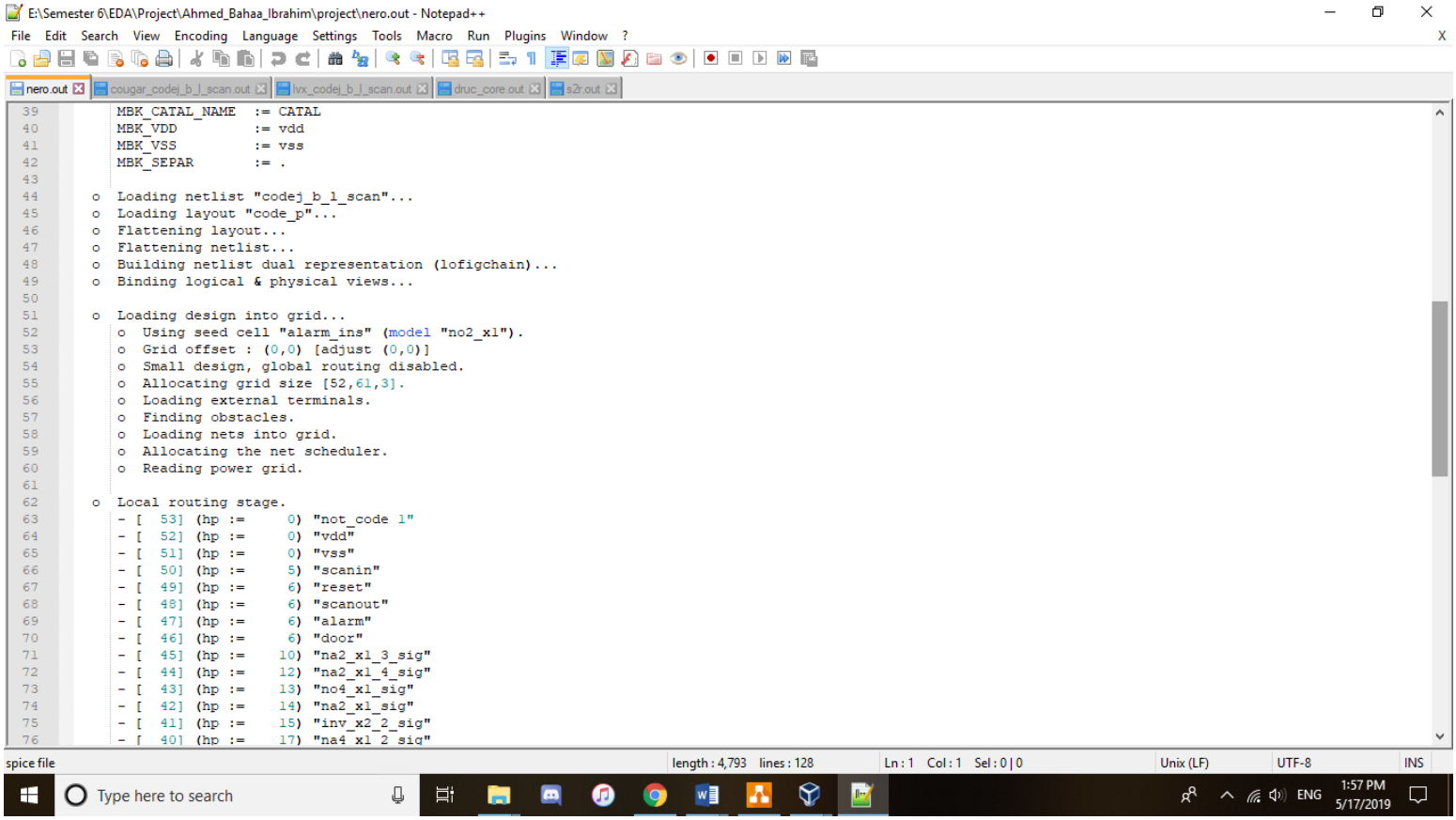
7. .out files of the tools output

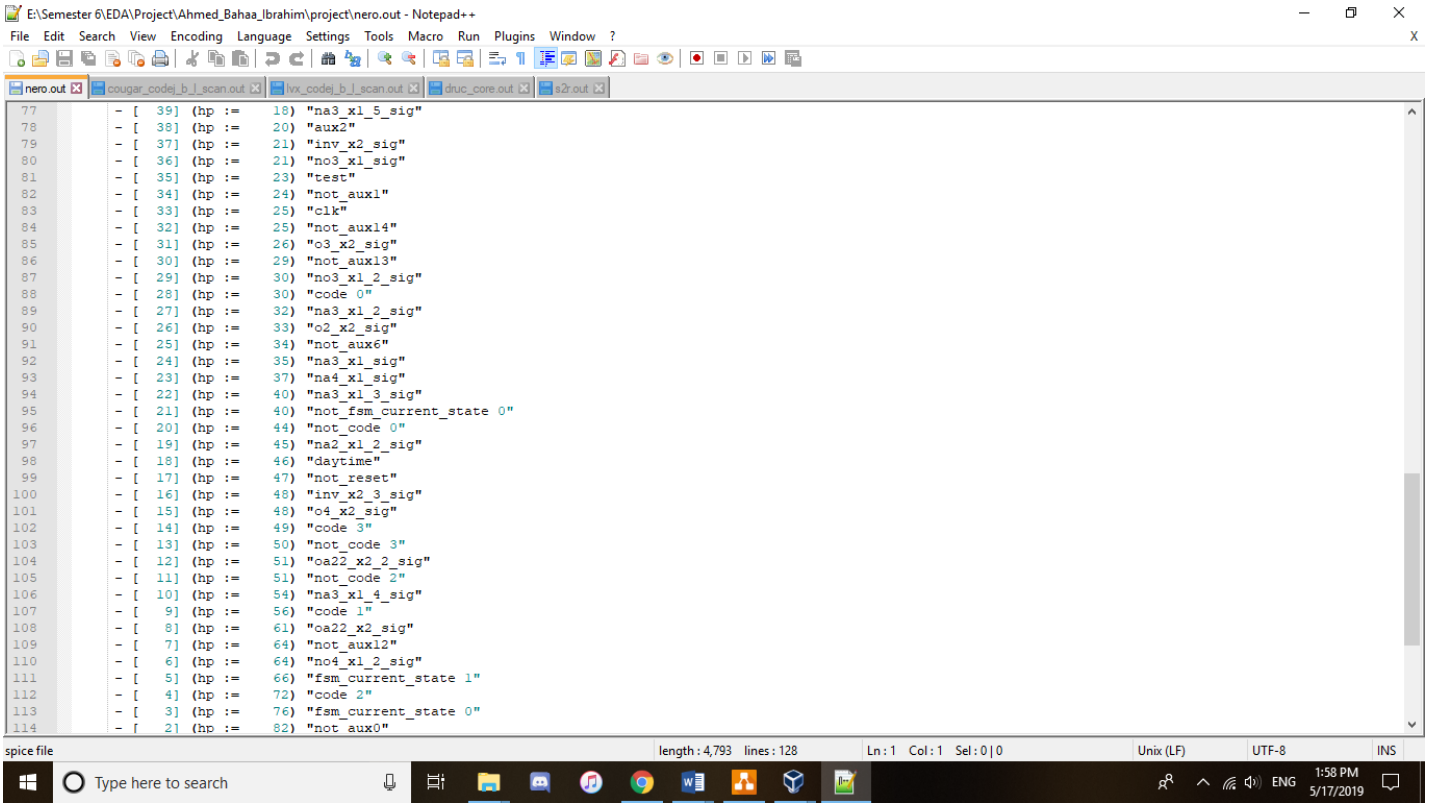
7.1 OCP.out

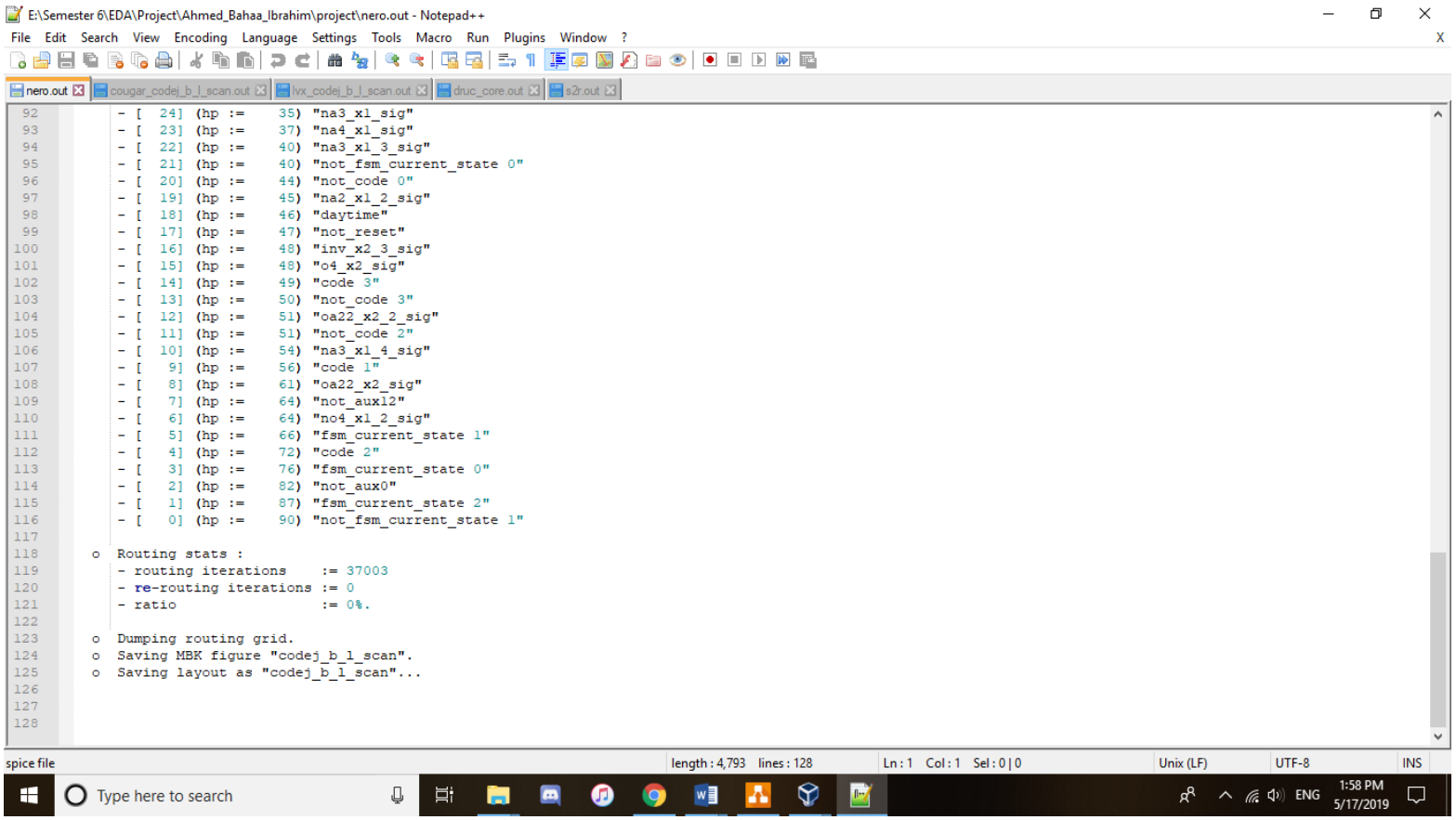


7.2 NERO.out

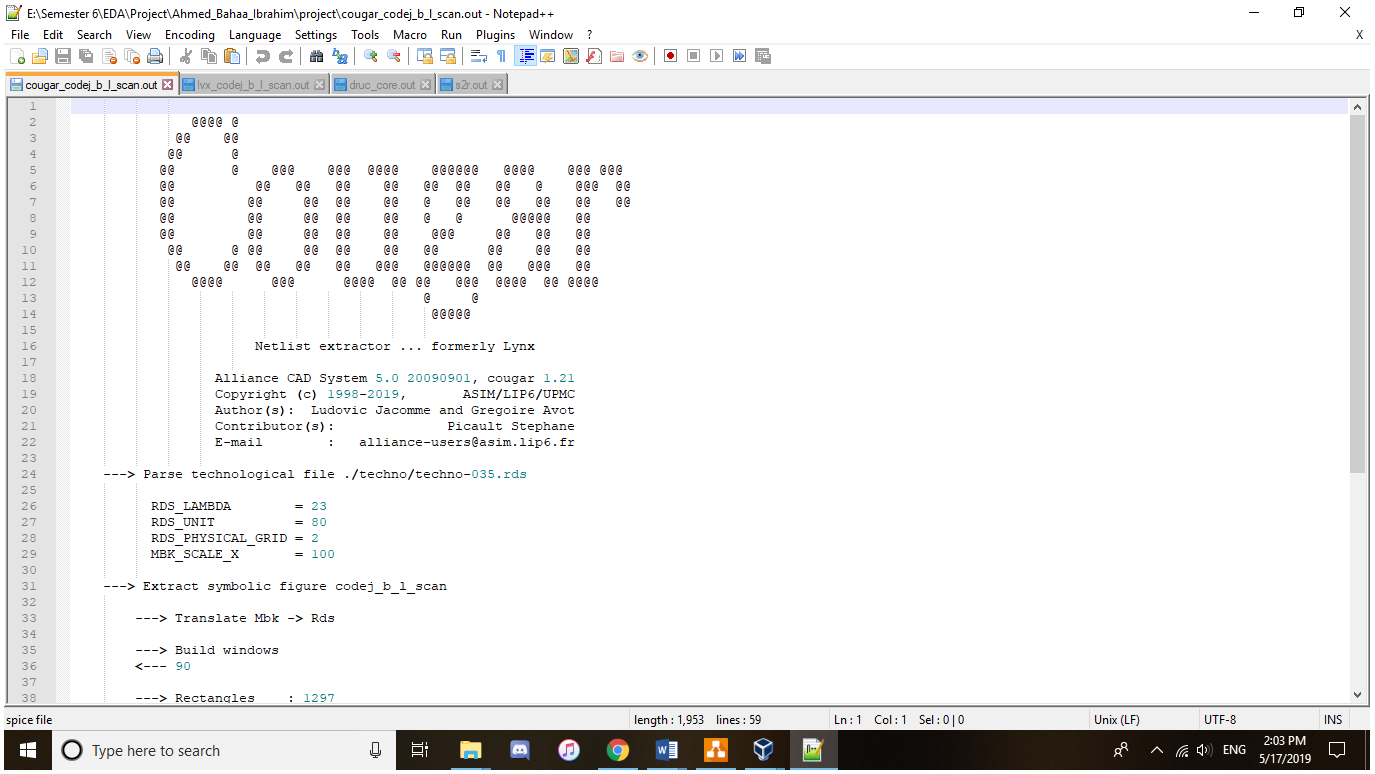

E:\Semester 6\EDA\Project\Ahmed_Bahaa_Ibrahim\project\nero.out - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
nero.out
cougar_codej_b_l_scan.out
lvx_codej_b_l_scan.out
druc_core.out
s2r.out
Negotiating Router
Alliance CAD System 5.0 20090901, nero 5.0
Copyright (c) 2002-2019, ASIM/LIP6/UPMC
E-mail : alliance-users@asim.lip6.fr
S/N 20080611.1
o MBK environment :
MBK_IN_LO := vst
MBK_OUT_LO := vst
MBK_IN_PH := ap
MBK_OUT_PH := ap
MBK_WORK_LIB := .
MBK_CATA_LIB := .
/usr/lib/alliance/cells/sxlib
/usr/lib/alliance/cells/dp_sxlib
/usr/lib/alliance/cells/rflib
/usr/lib/alliance/cells/rf2lib
/usr/lib/alliance/cells/ramlib
/usr/lib/alliance/cells/romlib
/usr/lib/alliance/cells/pxlib
/usr/lib/alliance/cells/padlib
spice file
length : 4,793 lines : 128
Ln : 1 Col : 1 Sel : 0 | 0
Unix (LF)
UTF-8
INS
Type here to search
ENG
1:56 PM
5/17/2019


E:\Semester 6\EDA\Project\Ahmed_Bahaa_Ibrahim\project\nero.out - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
nero.out
cougar_codej_b_l_scan.out
lvx_codej_b_l_scan.out
druc_core.out
s2r.out
MBK_CATAL_NAME := CATAL
MBK_VDD := vdd
MBK_VSS := vss
MBK_SEPAR := .
o Loading netlist "codej_b_l_scan"...
o Loading layout "code_p"...
o Flattening layout...
o Flattening netlist...
o Building netlist dual representation (lofigchain)...
o Binding logical & physical views...
o Loading design into grid...
o Using seed cell "alarm_ins" (model "no2_x1").
o Grid offset : (0,0) [adjust (0,0)]
o Small design, global routing disabled.
o Allocating grid size [52,61,3].
o Loading external terminals.
o Finding obstacles.
o Loading nets into grid.
o Allocating the net scheduler.
o Reading power grid.
o Local routing stage.
- [53] (hp := 0) "not_code 1"
- [52] (hp := 0) "vdd"
- [51] (hp := 0) "vss"
- [50] (hp := 5) "scanin"
- [49] (hp := 6) "reset"
- [48] (hp := 6) "scanout"
- [47] (hp := 6) "alarm"
- [46] (hp := 6) "door"
- [45] (hp := 10) "na2_x1_3_sig"
- [44] (hp := 12) "na2_x1_4_sig"
- [43] (hp := 13) "no4_x1_sig"
- [42] (hp := 14) "na2_x1_sig"
- [41] (hp := 15) "inv_x2_2_sig"
- [40] (hp := 17) "na4_x1_2_sig"
spice file
length : 4,793 lines : 128
Ln : 1 Col : 1 Sel : 0 | 0
Unix (LF)
UTF-8
INS
Type here to search
ENG
1:57 PM
5/17/2019

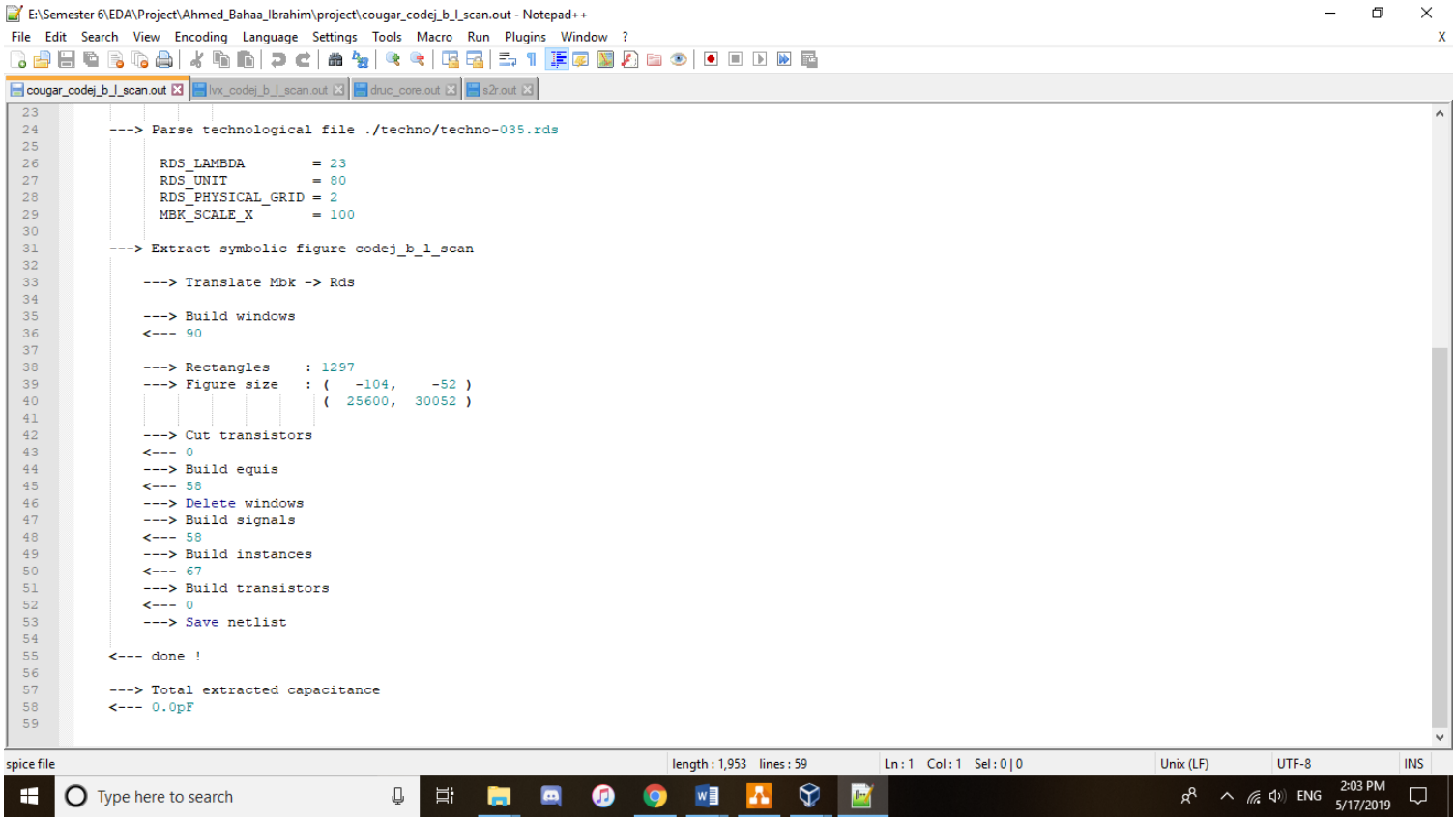

E:\Semester 6\EDA\Project\Ahmed_Bahaa_Ibrahim\project\nero.out - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
nero.out
cougar_codej_b_l_scan.out
lvx_codej_b_l_scan.out
druc_core.out
s2r.out
- [39] (hp := 18) "na3_xl_5_sig"
- [38] (hp := 20) "aux2"
- [37] (hp := 21) "inv_x2_sig"
- [36] (hp := 21) "no3_xl_sig"
- [35] (hp := 23) "test"
- [34] (hp := 24) "not_aux1"
- [33] (hp := 25) "clk"
- [32] (hp := 25) "not_aux14"
- [31] (hp := 26) "o3_x2_sig"
- [30] (hp := 29) "not_aux13"
- [29] (hp := 30) "no3_xl_2_sig"
- [28] (hp := 30) "code 0"
- [27] (hp := 32) "na3_xl_2_sig"
- [26] (hp := 33) "o2_x2_sig"
- [25] (hp := 34) "not_aux6"
- [24] (hp := 35) "na3_xl_sig"
- [23] (hp := 37) "na4_xl_sig"
- [22] (hp := 40) "na3_xl_3_sig"
- [21] (hp := 40) "not_fsm_current_state 0"
- [20] (hp := 44) "not_code 0"
- [19] (hp := 45) "na2_xl_2_sig"
- [18] (hp := 46) "daytime"
- [17] (hp := 47) "not_reset"
- [16] (hp := 48) "inv_x2_3_sig"
- [15] (hp := 48) "o4_x2_sig"
- [14] (hp := 49) "code 3"
- [13] (hp := 50) "not_code 3"
- [12] (hp := 51) "oa22_x2_2_sig"
- [11] (hp := 51) "not_code 2"
- [10] (hp := 54) "na3_xl_4_sig"
- [9] (hp := 56) "code 1"
- [8] (hp := 61) "oa22_x2_sig"
- [7] (hp := 64) "not_aux12"
- [6] (hp := 64) "no4_xl_2_sig"
- [5] (hp := 66) "fsm_current_state 1"
- [4] (hp := 72) "code 2"
- [3] (hp := 76) "fsm_current_state 0"
- [2] (hp := 82) "not_aux0"
spice file
length : 4,793 lines : 128
Ln : 1 Col : 1 Sel : 0 | 0
Unix (LF)
UTF-8
INS
Type here to search
ENG
1:58 PM
5/17/2019


E:\Semester 6\EDA\Project\Ahmed_Bahaa_Ibrahim\project\nero.out - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
nero.out
cougar_codej_b_l_scan.out
lvx_codej_b_l_scan.out
druc_core.out
s2r.out
- [24] (hp := 35) "na3_xl_sig"
- [23] (hp := 37) "na4_xl_sig"
- [22] (hp := 40) "na3_xl_3_sig"
- [21] (hp := 40) "not_fsm_current_state 0"
- [20] (hp := 44) "not_code 0"
- [19] (hp := 45) "na2_xl_2_sig"
- [18] (hp := 46) "daytime"
- [17] (hp := 47) "not_reset"
- [16] (hp := 48) "inv_x2_3_sig"
- [15] (hp := 48) "o4_x2_sig"
- [14] (hp := 49) "code 3"
- [13] (hp := 50) "not_code 3"
- [12] (hp := 51) "oa22_x2_2_sig"
- [11] (hp := 51) "not_code 2"
- [10] (hp := 54) "na3_xl_4_sig"
- [9] (hp := 56) "code 1"
- [8] (hp := 61) "oa22_x2_sig"
- [7] (hp := 64) "not_aux12"
- [6] (hp := 64) "no4_xl_2_sig"
- [5] (hp := 66) "fsm_current_state 1"
- [4] (hp := 72) "code 2"
- [3] (hp := 76) "fsm_current_state 0"
- [2] (hp := 82) "not_aux0"
- [1] (hp := 87) "fsm_current_state 2"
- [0] (hp := 90) "not_fsm_current_state 1"
o Routing stats :
- routing iterations := 37003
- re-routing iterations := 0
- ratio := 0%.
o Dumping routing grid.
o Saving MBK figure "codej_b_l_scan".
o Saving layout as "codej_b_l_scan"...
spice file
length : 4,793 lines : 128
Ln : 1 Col : 1 Sel : 0 | 0
Unix (LF)
UTF-8
INS
Type here to search
ENG
1:58 PM
5/17/2019

7.3 cougar_codej_b_l_scan.out

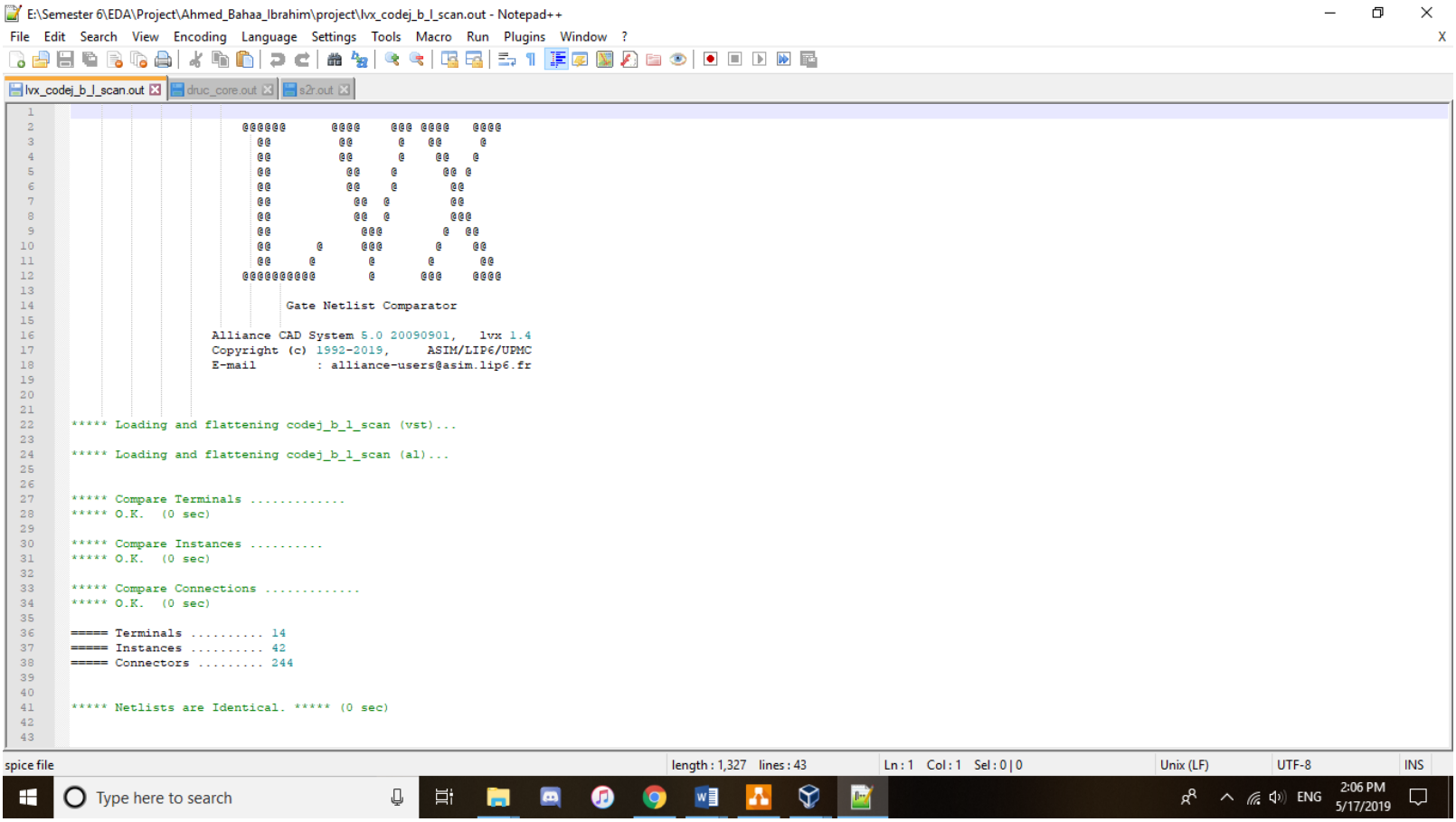


```
E:\Semester 6\EDA\Project\Ahmed_Bahaa_Ibrahim\project\cougar_codej_b_l_scan.out - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
cougar_codej_b_l_scan.out | lvx_codej_b_l_scan.out | druc_core.out | s2r.out

                  @@@@ @
                 @@    @@
                @@      @
               @@       @    @@@    @@@  @@@@    @@@@@@   @@@@    @@@ @@@
               @@          @@   @@   @@    @@   @@   @@   @@   @    @@@  @@
               @@          @@     @@  @@    @@   @    @@   @@   @@   @@   @@
               @@          @@     @@  @@    @@   @    @@     @@@@@   @@
               @@          @@     @@  @@    @@    @@@     @@   @@   @@
                @@       @ @@     @@  @@    @@       @@    @@   @@   @@
                 @@     @@  @@    @@   @@    @@@   @@@@@@  @@   @@@   @@
                   @@@@      @@@      @@@@  @@ @@   @@@  @@@@  @@ @@@@
                                                    @     @
                                                     @@@@@

                          Netlist extractor ... formerly Lynx

                    Alliance CAD System 5.0 20090901, cougar 1.21
                    Copyright (c) 1998-2019,       ASIM/LIP6/UPMC
                    Author(s):  Ludovic Jacomme and Gregoire Avot
                    Contributor(s):             Picault Stephane
                    E-mail        :   alliance-users@asim.lip6.fr

      ---> Parse technological file ./techno/techno-035.rds

           RDS_LAMBDA        = 23
           RDS_UNIT          = 80
           RDS_PHYSICAL_GRID = 2
           MBK_SCALE_X       = 100

      ---> Extract symbolic figure codej_b_l_scan

          ---> Translate Mbk -> Rds

          ---> Build windows
          <--- 90

          ---> Rectangles    : 1297

spice file   length : 1,953   lines : 59   Ln : 1   Col : 1   Sel : 0 | 0   Unix (LF)   UTF-8   INS
Type here to search   ENG   2:03 PM   5/17/2019
```

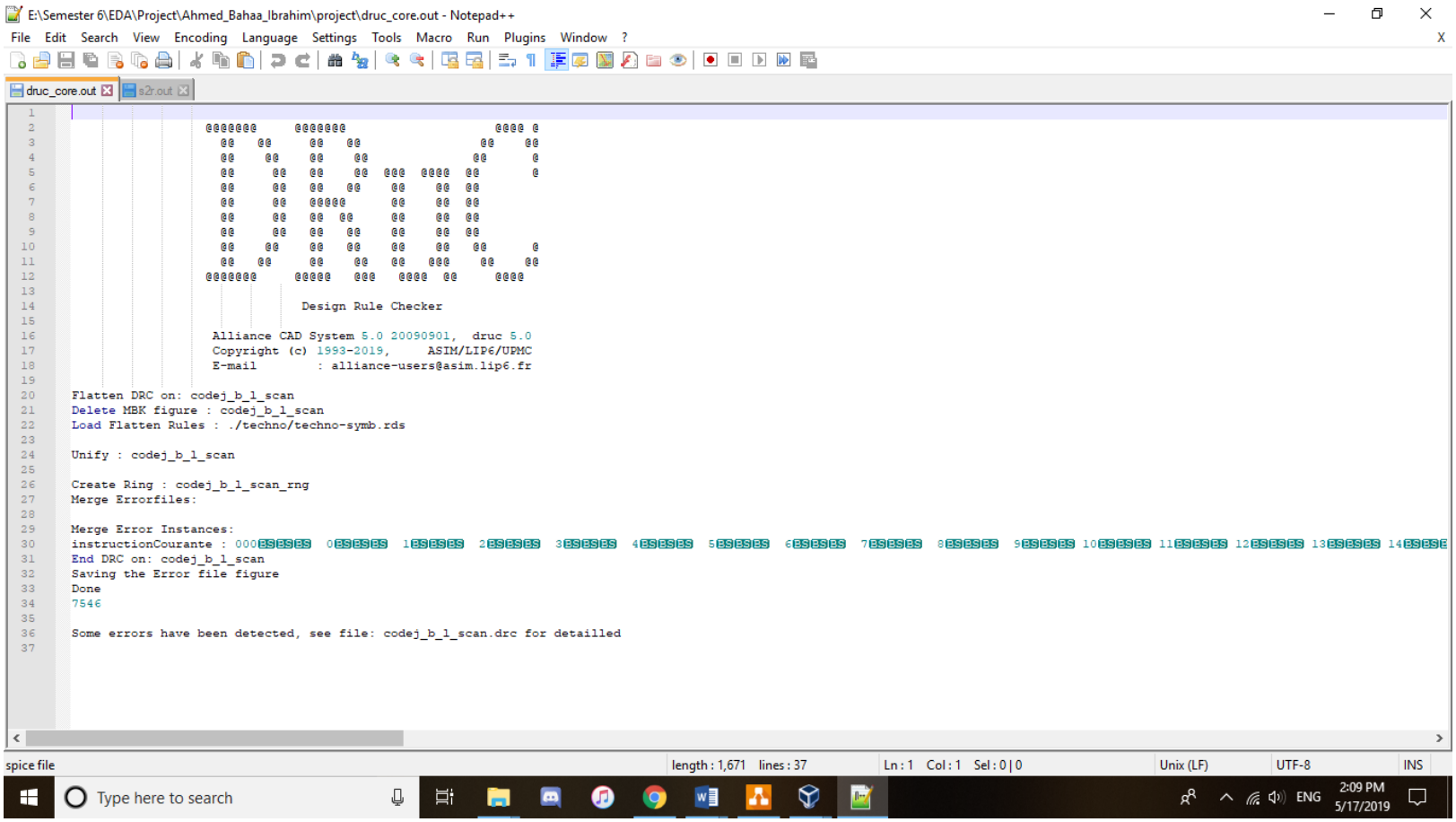


```
E:\Semester 6\EDA\Project\Ahmed_Bahaa_Ibrahim\project\cougar_codej_b_l_scan.out - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
cougar_codej_b_l_scan.out | lvx_codej_b_l_scan.out | druc_core.out | s2r.out

      ---> Parse technological file ./techno/techno-035.rds

           RDS_LAMBDA        = 23
           RDS_UNIT          = 80
           RDS_PHYSICAL_GRID = 2
           MBK_SCALE_X       = 100

      ---> Extract symbolic figure codej_b_l_scan

          ---> Translate Mbk -> Rds

          ---> Build windows
          <--- 90

          ---> Rectangles    : 1297
          ---> Figure size   : (   -104,    -52 )
                               (  25600,  30052 )

          ---> Cut transistors
          <--- 0
          ---> Build equis
          <--- 58
          ---> Delete windows
          ---> Build signals
          <--- 58
          ---> Build instances
          <--- 67
          ---> Build transistors
          <--- 0
          ---> Save netlist

      <--- done !

      ---> Total extracted capacitance
      <--- 0.0pF

spice file   length : 1,953   lines : 59   Ln : 1   Col : 1   Sel : 0 | 0   Unix (LF)   UTF-8   INS
Type here to search   ENG   2:03 PM   5/17/2019
```

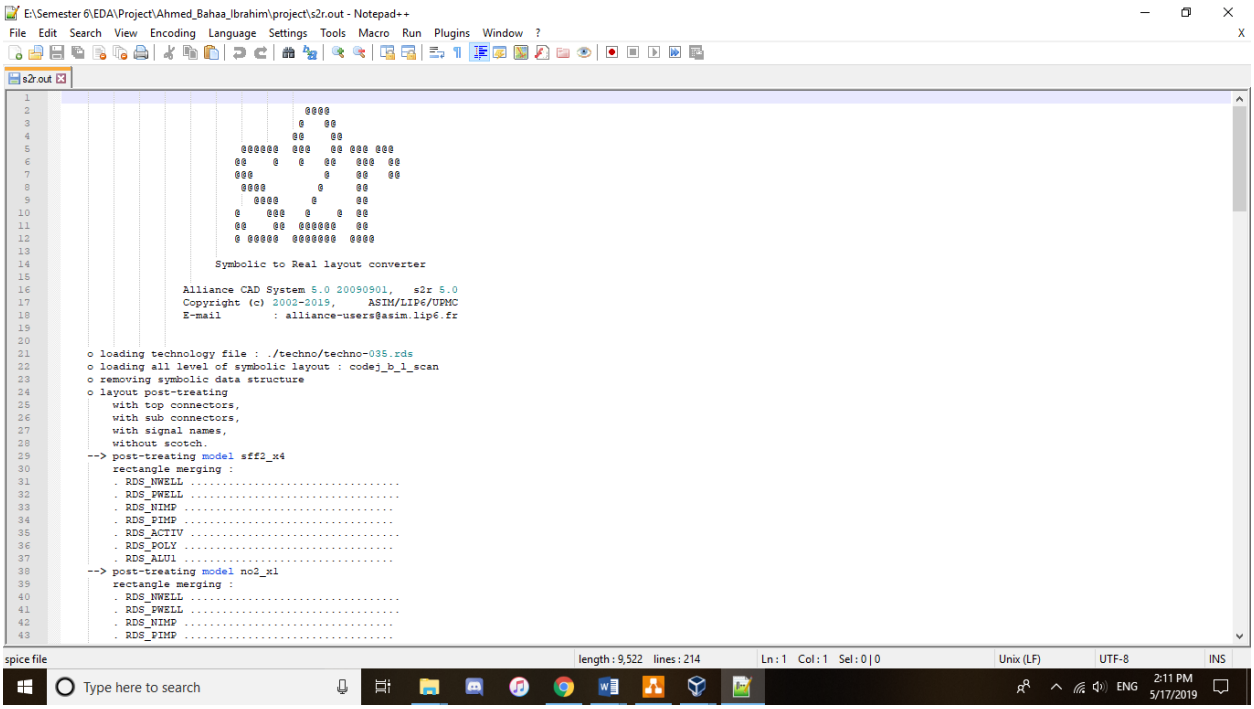
7.4 lvx_codej_b_l_scan.out

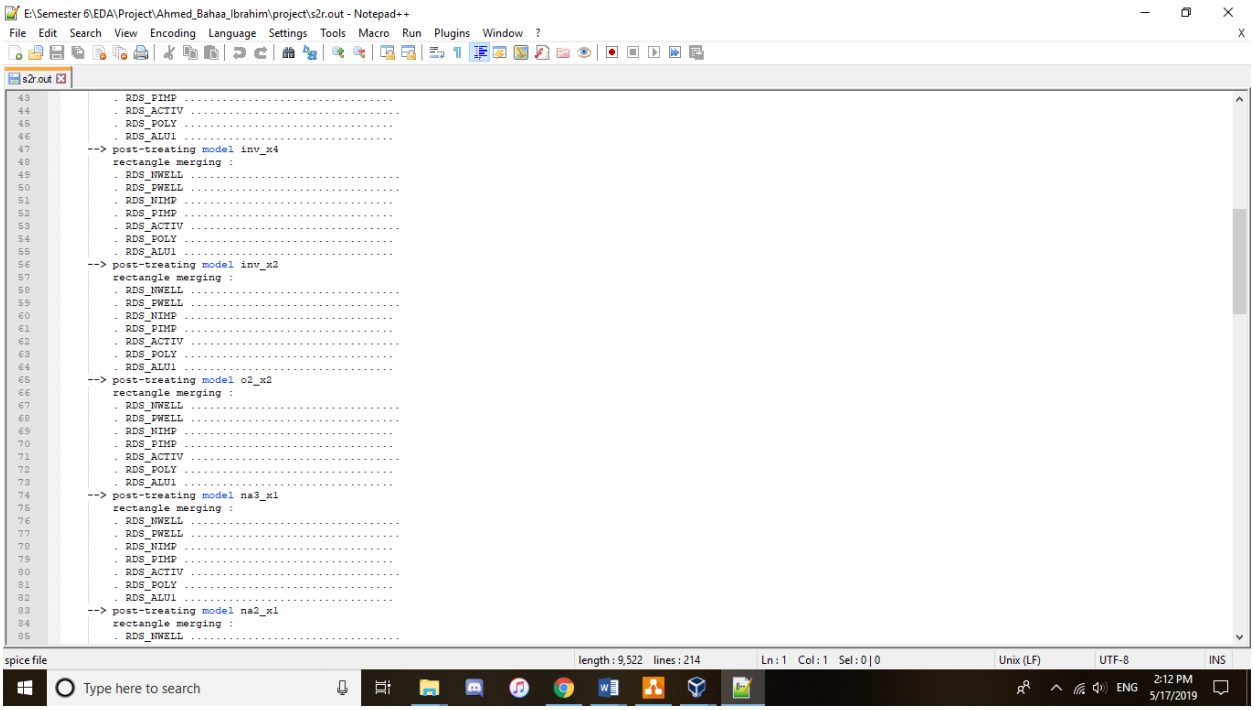


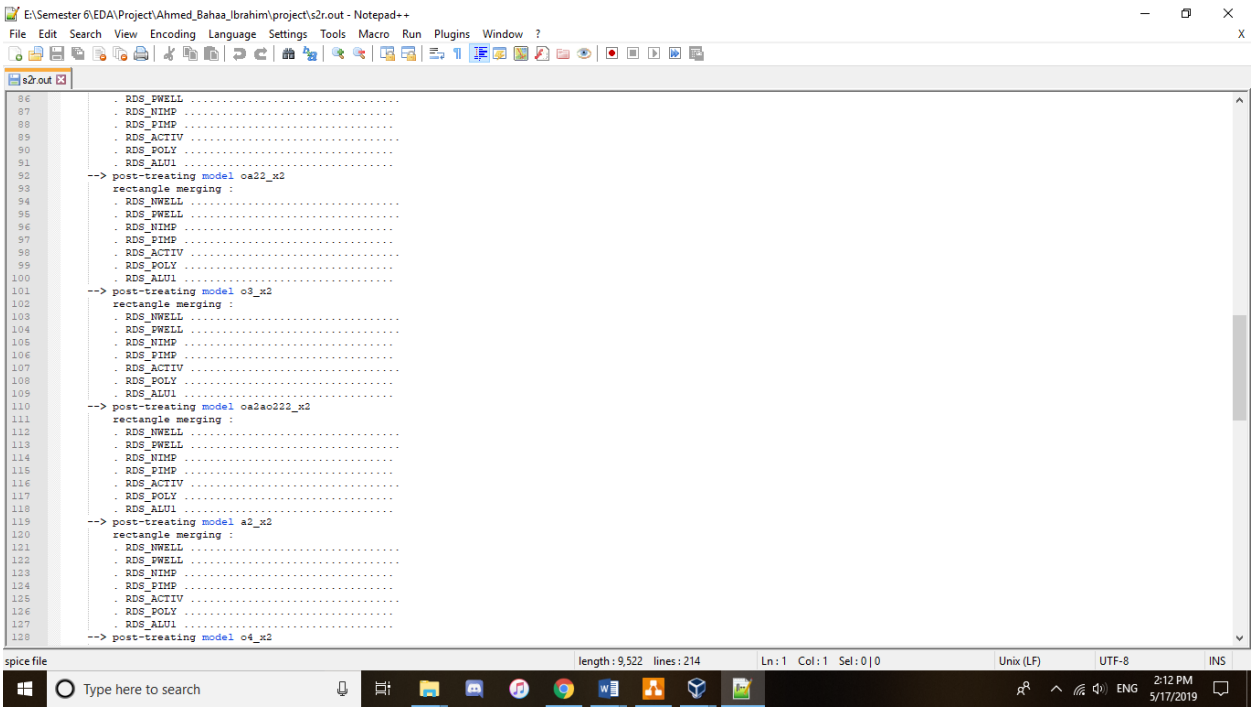
7.5 druc_core.out

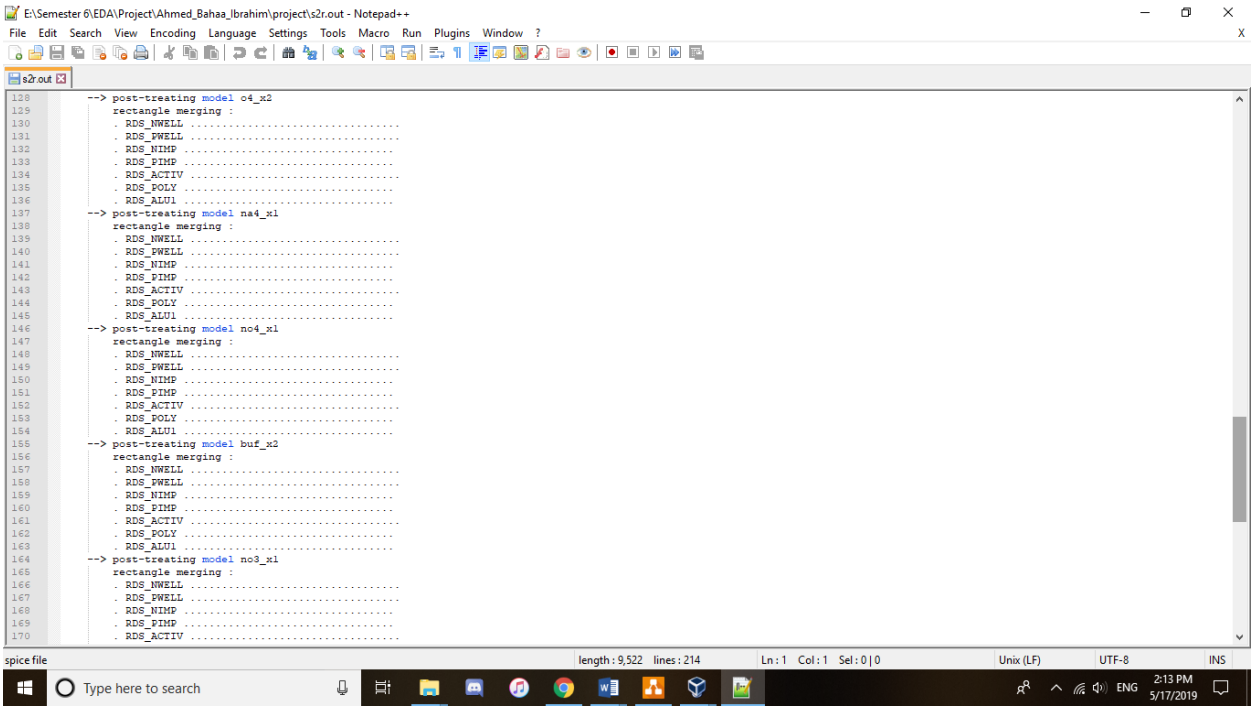


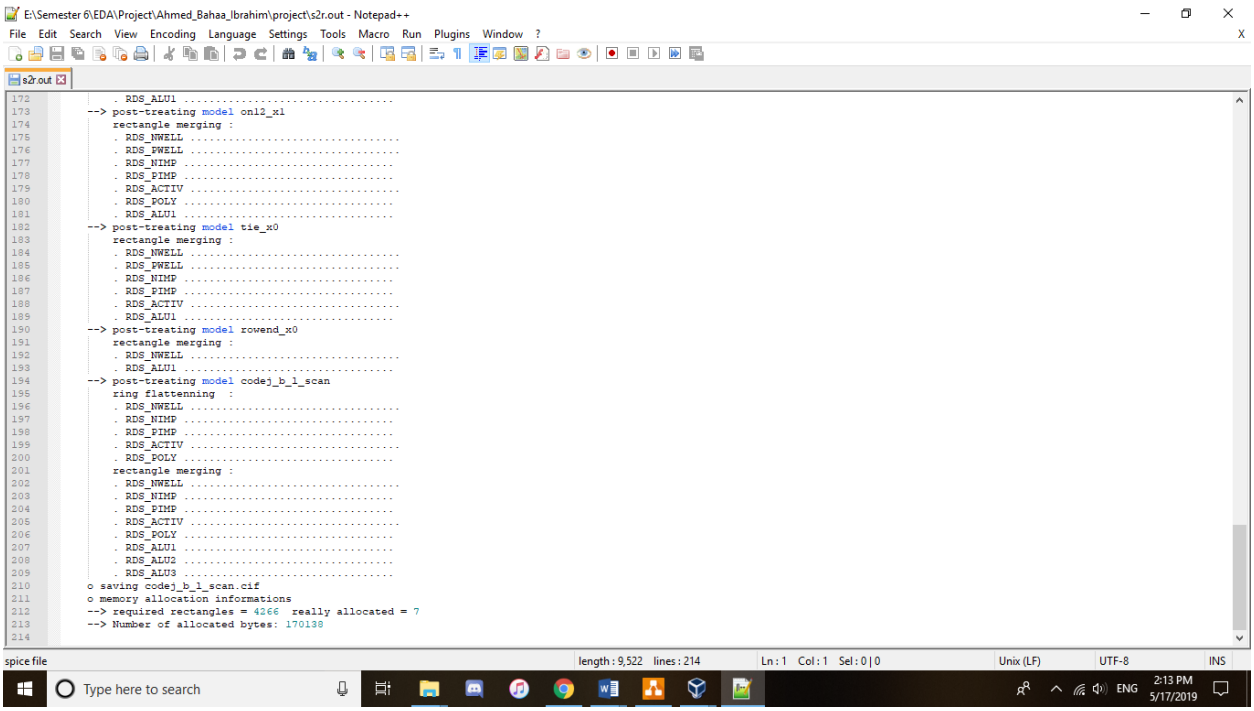
7.6 s2r.out


E:\Semester 6\EDA\Project\Ahmed_Bahaa_Ibrahim\project\s2r.out - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
s2r.out
Symbolic to Real layout converter
Alliance CAD System 5.0 20090901, s2r 5.0
Copyright (c) 2002-2019, ASIM/LIP6/UPMC
E-mail : alliance-users@asim.lip6.fr
o loading technology file : ./techno/techno-035.rds
o loading all level of symbolic layout : codej_b_l_scan
o removing symbolic data structure
o layout post-treating
with top connectors,
with sub connectors,
with signal names,
without scotch.
--> post-treating model sff2_x4
rectangle merging :
. RDS_NWELL .....
. RDS_PWELL .....
. RDS_NIMP .....
. RDS_PIMP .....
. RDS_ACTIV .....
. RDS_POLY .....
. RDS_ALU1 .....
--> post-treating model no2_x1
rectangle merging :
. RDS_NWELL .....
. RDS_PWELL .....
. RDS_NIMP .....
. RDS_PIMP .....
spice file
length : 9,522 lines : 214
Ln : 1 Col : 1 Sel : 0 | 0
Unix (LF)
UTF-8
INS
Type here to search
ENG
2:11 PM
5/17/2019


E:\Semester 6\EDA\Project\Ahmed_Bahaa_Ibrahim\project\s2r.out - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
s2r.out
. RDS_PIMP .....
. RDS_ACTIV .....
. RDS_POLY .....
. RDS_ALU1 .....
--> post-treating model inv_x4
rectangle merging :
. RDS_NWELL .....
. RDS_PWELL .....
. RDS_NIMP .....
. RDS_PIMP .....
. RDS_ACTIV .....
. RDS_POLY .....
. RDS_ALU1 .....
--> post-treating model inv_x2
rectangle merging :
. RDS_NWELL .....
. RDS_PWELL .....
. RDS_NIMP .....
. RDS_PIMP .....
. RDS_ACTIV .....
. RDS_POLY .....
. RDS_ALU1 .....
--> post-treating model o2_x2
rectangle merging :
. RDS_NWELL .....
. RDS_PWELL .....
. RDS_NIMP .....
. RDS_PIMP .....
. RDS_ACTIV .....
. RDS_POLY .....
. RDS_ALU1 .....
--> post-treating model na3_x1
rectangle merging :
. RDS_NWELL .....
. RDS_PWELL .....
. RDS_NIMP .....
. RDS_PIMP .....
. RDS_ACTIV .....
. RDS_POLY .....
. RDS_ALU1 .....
--> post-treating model na2_x1
rectangle merging :
. RDS_NWELL .....
spice file
length : 9,522 lines : 214
Ln : 1 Col : 1 Sel : 0 | 0
Unix (LF)
UTF-8
INS
Type here to search
ENG
2:12 PM
5/17/2019


E:\Semester 6\EDA\Project\Ahmed_Bahaa_Ibrahim\project\s2r.out - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
s2r.out
. RDS_PWELL .....
. RDS_NIMP .....
. RDS_PIMP .....
. RDS_ACTIV .....
. RDS_POLY .....
. RDS_ALU1 .....
--> post-treating model oa22_x2
rectangle merging :
. RDS_NWELL .....
. RDS_PWELL .....
. RDS_NIMP .....
. RDS_PIMP .....
. RDS_ACTIV .....
. RDS_POLY .....
. RDS_ALU1 .....
--> post-treating model o3_x2
rectangle merging :
. RDS_NWELL .....
. RDS_PWELL .....
. RDS_NIMP .....
. RDS_PIMP .....
. RDS_ACTIV .....
. RDS_POLY .....
. RDS_ALU1 .....
--> post-treating model oa2ao222_x2
rectangle merging :
. RDS_NWELL .....
. RDS_PWELL .....
. RDS_NIMP .....
. RDS_PIMP .....
. RDS_ACTIV .....
. RDS_POLY .....
. RDS_ALU1 .....
--> post-treating model a2_x2
rectangle merging :
. RDS_NWELL .....
. RDS_PWELL .....
. RDS_NIMP .....
. RDS_PIMP .....
. RDS_ACTIV .....
. RDS_POLY .....
. RDS_ALU1 .....
--> post-treating model o4_x2
spice file
length : 9,522 lines : 214
Ln : 1 Col : 1 Sel : 0 | 0
Unix (LF)
UTF-8
INS
Type here to search
ENG
2:12 PM
5/17/2019


E:\Semester 6\EDA\Project\Ahmed_Bahaa_Ibrahim\project\s2r.out - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
s2r.out
--> post-treating model o4_x2
rectangle merging :
. RDS_NWELL .....
. RDS_PWELL .....
. RDS_NIMP .....
. RDS_PIMP .....
. RDS_ACTIV .....
. RDS_POLY .....
. RDS_ALU1 .....
--> post-treating model na4_x1
rectangle merging :
. RDS_NWELL .....
. RDS_PWELL .....
. RDS_NIMP .....
. RDS_PIMP .....
. RDS_ACTIV .....
. RDS_POLY .....
. RDS_ALU1 .....
--> post-treating model no4_x1
rectangle merging :
. RDS_NWELL .....
. RDS_PWELL .....
. RDS_NIMP .....
. RDS_PIMP .....
. RDS_ACTIV .....
. RDS_POLY .....
. RDS_ALU1 .....
--> post-treating model buf_x2
rectangle merging :
. RDS_NWELL .....
. RDS_PWELL .....
. RDS_NIMP .....
. RDS_PIMP .....
. RDS_ACTIV .....
. RDS_POLY .....
. RDS_ALU1 .....
--> post-treating model no3_x1
rectangle merging :
. RDS_NWELL .....
. RDS_PWELL .....
. RDS_NIMP .....
. RDS_PIMP .....
. RDS_ACTIV .....
spice file
length : 9,522 lines : 214
Ln : 1 Col : 1 Sel : 0 | 0
Unix (LF)
UTF-8
INS
Type here to search
ENG
2:13 PM
5/17/2019


E:\Semester 6\EDA\Project\Ahmed_Bahaa_Ibrahim\project\s2r.out - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
s2r.out
. RDS_ALU1 .....
--> post-treating model onl2_x1
rectangle merging :
. RDS_NWELL .....
. RDS_PWELL .....
. RDS_NIMP .....
. RDS_PIMP .....
. RDS_ACTIV .....
. RDS_POLY .....
. RDS_ALU1 .....
--> post-treating model tie_x0
rectangle merging :
. RDS_NWELL .....
. RDS_PWELL .....
. RDS_NIMP .....
. RDS_PIMP .....
. RDS_ACTIV .....
. RDS_ALU1 .....
--> post-treating model rowend_x0
rectangle merging :
. RDS_NWELL .....
. RDS_ALU1 .....
--> post-treating model codej_b_1_scan
ring flattenning :
. RDS_NWELL .....
. RDS_NIMP .....
. RDS_PIMP .....
. RDS_ACTIV .....
. RDS_POLY .....
rectangle merging :
. RDS_NWELL .....
. RDS_NIMP .....
. RDS_PIMP .....
. RDS_ACTIV .....
. RDS_POLY .....
. RDS_ALU1 .....
. RDS_ALU2 .....
. RDS_ALU3 .....
o saving codej_b_1_scan.cif
o memory allocation informations
--> required rectangles = 4266 / really allocated = 7
--> Number of allocated bytes: 170138
spice file
length : 9,522 lines : 214
Ln : 1 Col : 1 Sel : 0 | 0
Unix (LF)
UTF-8
INS
Type here to search
ENG
2:13 PM
5/17/2019

8. Appendecies

8.1 Makefile

```
#-------Sdet-----------------------------------------#

all: codea.vbe \
    codej.vbe \
    codem.vbe \
    codeo.vbe \
    coder.vbe \
    code_boom \
    code_loon
                                @echo "<-- Generated"

#-------Finite State Machine Synthesis-----------------#

vhd_to_fsm:
                            rename .vhd .fsm *.vhd

codea.vbe: code.fsm
                            @echo "    Encoding Synthesis -> codea.vbe"
                            syf -CEV -a code

codej.vbe: code.fsm
                            @echo "    Encoding Synthesis  -> codej.vbe"
                            syf -CEV -j code

codem.vbe: code.fsm
                            @echo "    Encoding Synthesis  -> codem.vbe"
                            syf -CEV -m code

codeo.vbe: code.fsm
                            @echo "    Encoding Synthesis  -> codeo.vbe"
                            syf -CEV -o code

coder.vbe: code.fsm
                            @echo "    Encoding Synthesis  -> coder.vbe"
                            syf -CEV -r code
```

```
code_boom: codea_b.vbe codej_b.vbe codem_b.vbe \
                        codeo_b.vbe coder_b.vbe

%_b.vbe: %.vbe
                        @echo "   Boolean Optimiztaion -> $@  "
                        boom -V -d 50 $* $*_b > $*_boom.out

code_boog: codea_b.vst codej_b.vst codem_b.vst \
                        codeo_b.vst coder_b.vst

code_loon: codea_b_l.vst codej_b_l.vst codem_b_l.vst \
                        codeo_b_l.vst coder_b_l.vst

%.vst : %.vbe paramfile.lax
                        @echo "  Logical Synsthesis -> $@ "
                        boog -x 1 -l paramfile $* > $*_boog.out

%_l.vst : %.vst paramfile.lax
                        @echo "  Netlist OPtimization -> $@ "
                        loon -x 1 -l paramfile $* $*_l > $*_loon.out

%_b_l_net.vbe : %_b_l.vst %.vbe
                        @echo " Formal checking -> $@ "
                        flatbeh $*_b_l $*_b_l_net > $*_flatbeh.out
                        proof -d $* $*_b_l_net > $*_proof.out

ac_scapin_registers:
                        cat codej_b_l.vst | grep sff

%_scan.vst : %.vst scan.path
                        @echo " scan-path insertion -> $@ "
                        scapin -VRB $* scan $*_scan > scapin.out

code_p.ap : code.ioc codej_b_l_scan.vst
                        MBK_IN_LO=vst; export MBK_IN_LO; \
                        MBK_OUT_PH=ap; export MBK_OUT_PH; \
                        ocp –v –ring –ioc code.ioc codej_b_l_scan code_p > ocp.out

codej_b_l_scan.ap: code_p.ap codej_b_l_scan.vst
                        nero -V -p code_p codej_b_l_scan codej_b_l_scan > nero.out

%.al : %.ap
                        MBK_OUT_LO=al; export MBK_OUT_LO; \
                        RDS_TECHNO_NAME=./techno/techno-035.rds; \
```

```
                        export RDS_TECHNO_NAME; \
                        cougar -v $* > cougar_$*.out
                        lvx vst al $* $* -f > lvx_$*.out

druc_core : codej_b_l_scan.ap
                        RDS_TECHNO_NAME=./techno/techno-symb.rds; \
                        export RDS_TECHNO_NAME; \
                        druc codej_b_l_scan > druc_core.out

code_chip.cif : codej_b_l_scan.ap
                        RDS_TECHNO_NAME=./techno/techno-035.rds; \
                        export RDS_TECHNO_NAME; \
                        RDS_OUT=cif; export RDS_OUT; \
                        s2r -v -r codej_b_l_scan code_chip

#-------Clean Up----------------------------------------#

clean :
                        rm -f  *.vbe *.enc *~
                        @echo "Erase all the files generated by the makefile"
```

8.2 Code.ioc

```
LEFT ( # IOs from bottom to top
(IOPIN scanin.0 );
(IOPIN daytime.0 );
(IOPIN code(0).0 );
)
TOP ( # IOs from left to right
(IOPIN code(1).0 );
(IOPIN code(2).0 );
(IOPIN code(3).0 );
)
RIGHT( # IOs from bottom to top
(IOPIN test.0 );
(IOPIN reset.0 );
)
BOTTOM ( # IOs from left to right
(IOPIN door.0 );
(IOPIN clk.0 );
(IOPIN alarm.0 );
(IOPIN scanout.0 ); )
```