



CSE:215 EDA

Digital Access Control
Physical Synthesis
Project 3

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Department: CESS

Introduction:

This is a report for Part 3 of the Project of Electronic Design Automation which is developing the physical Synthesis of my design to produce the `code_chip.cif` file which will be sent to factory to manufacture the IC and to produce this file I passed by 4 parts which are:

1. High-Level Design.
2. Low-Level Synthesis.
3. Design for test.
4. Placement and Routing (this document)

I passed by some Alliance tools such as :

- ocp: Standard Cell Placer.
- nero: Over-Cell Router.
- cougar: Symbolic Netlist Extractor.
- lvx: Netlist comparator.
- graal: Symbolic layout editor.
- druc: Symbolic Design-rule checker.
- Ring: Pad ring router.
- s2r : Symbolic-to-Real layout converter.

- `dreal` : Real layout editor.

This Report consist of :

1. Floorplanning

2. Placement (`graal`)

3. Placement(Flattened)

4. Routing(`graal`)

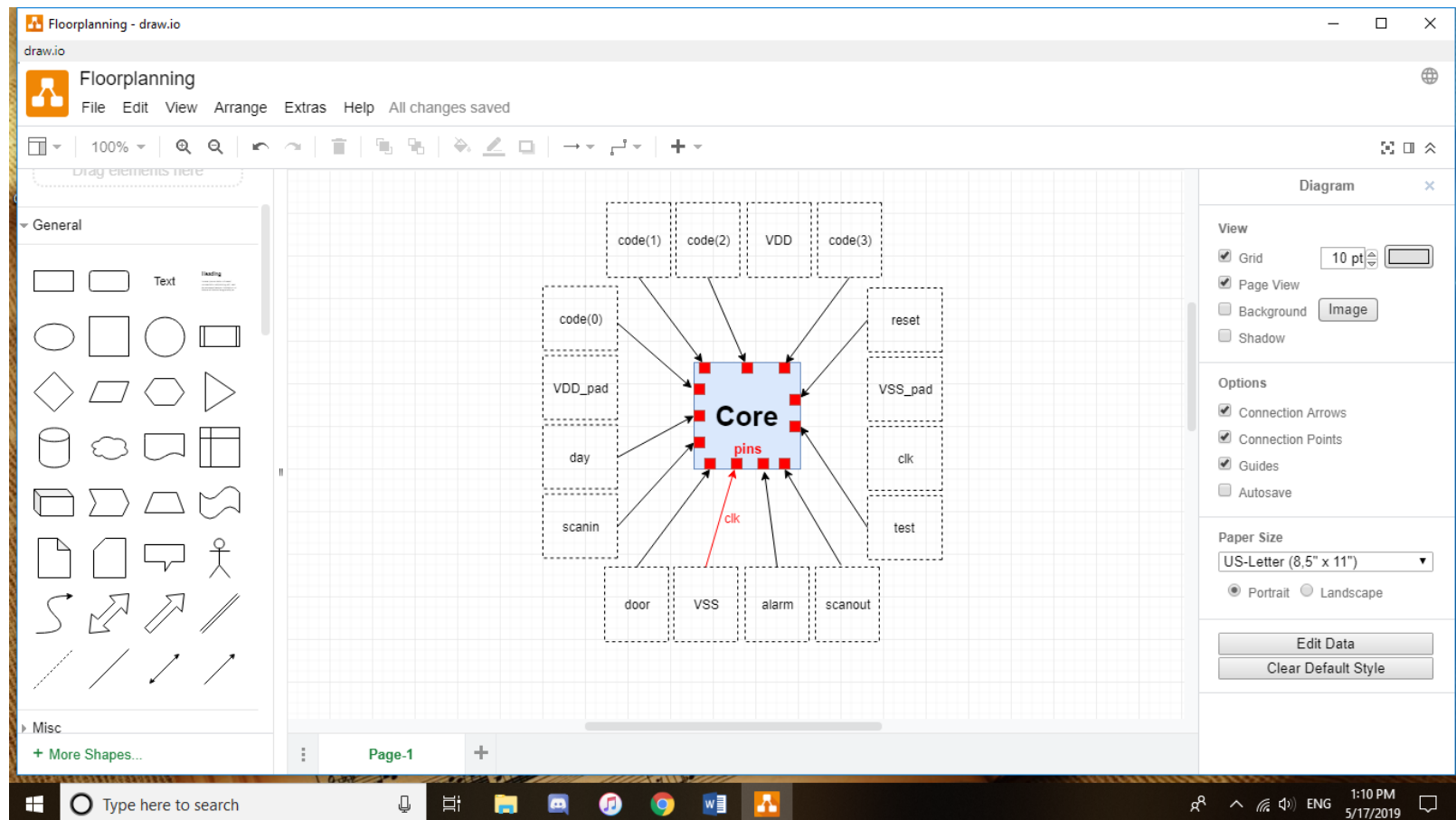
5. Final cif layout (`dreal`)

6. Final cif layout (flattened)

7. .out files of the tools output

8. Appendices(Makefile + `code.ioc`)

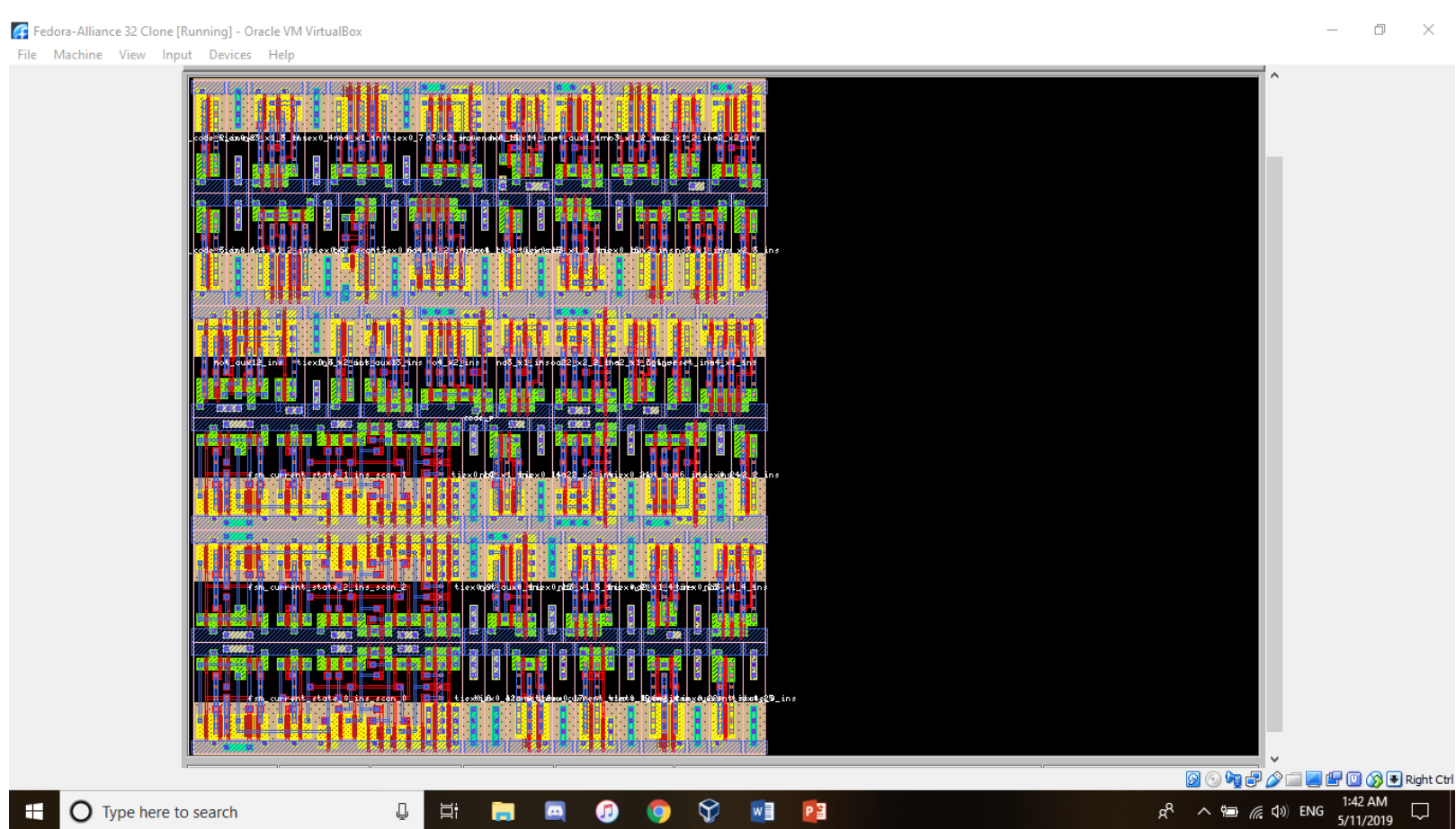
1. Floorplanning



2.Placemet (graal)



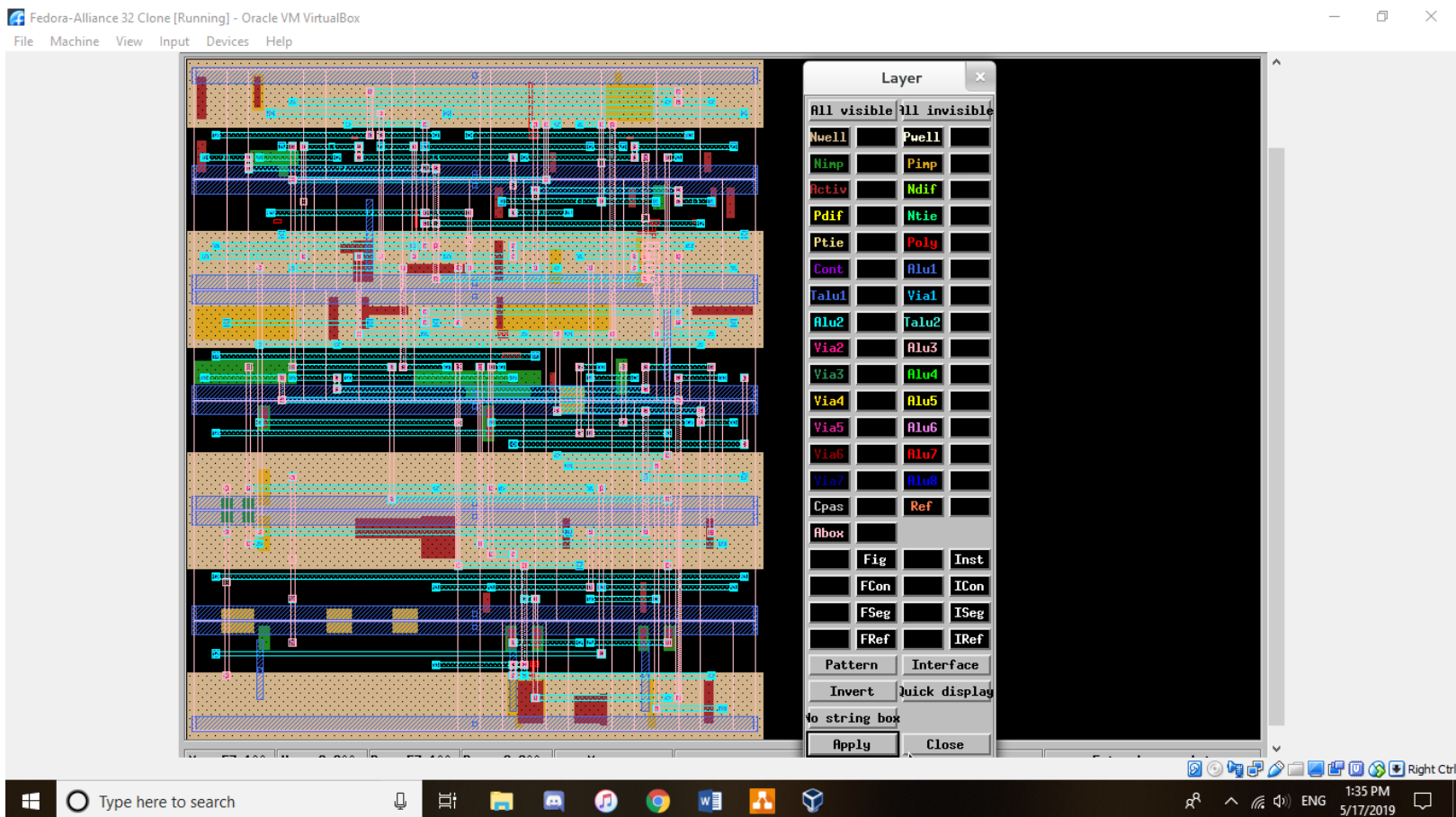
3. Placement (flattened)



4. Routing (graal)



5. Final cif layout (dreal)



6. Final cif layout (flattened)



7.1 OCP.out

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7.2 NERO.out

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E:\Semester 6\EDA\Project\Ahmed_Bahaa_Ibrahim\project\nero.out - Notepad++
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nero.out x cougar_codej_b_l_scan.out x lvx_codej_b_l_scan.out x druc_core.out x s2r.out x

1
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3      000 000      0000000
4      00 0      00 00
5      000 0      00 00
6      0 00 0 0 0000 00 00 000
7      0 00 0 00 00 0000 00 00
8      0 00 00000000 00 00 00 00
9      0 00 0 00 00 00 00 00
10     0 000 00 00 00 00 00 00
11     0 00 00 00 00 00 00 00
12     000 00 0000 0000 000 000
13
14      Negotiating Router
15
16      Alliance CAD System 5.0 20090901, nero 5.0
17      Copyright (c) 2002-2019, ASIM/LIP6/UFMC
18      E-mail : alliance-users@asim.lip6.fr
19
20      S/N 20080611.1
21
22      o MBK environment :
23
24      MBK_IN_LO      := vst
25      MBK_OUT_LO     := vst
26      MBK_IN_PH      := ap
27      MBK_OUT_PH     := ap
28      MBK_WORK_LIB   := .
29      MBK_CATA_LIB   := .
30
31      /usr/lib/alliance/cells/sxlib
32      /usr/lib/alliance/cells/dp_sxlib
33      /usr/lib/alliance/cells/rflib
34      /usr/lib/alliance/cells/rf2lib
35      /usr/lib/alliance/cells/ramlib
36      /usr/lib/alliance/cells/romlib
37      /usr/lib/alliance/cells/pxlib
38      /usr/lib/alliance/cells/padlib

spice file      length: 4,793 lines: 128 Ln: 1 Col: 1 Sel: 0|0 Unix (LF) UTF-8 INS
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nero.out x cougar_codej_b_l_scan.out x lvx_codej_b_l_scan.out x druc_core.out x s2r.out x

39      MBK_CATAL_NAME := CATAL
40      MBK_VDD         := vdd
41      MBK_VSS         := vss
42      MBK_SEPAR       := .
43
44      o Loading netlist "codej_b_l_scan"...
45      o Loading layout "code_p"...
46      o Flattening layout...
47      o Flattening netlist...
48      o Building netlist dual representation (lofigchain)...
49      o Binding logical & physical views...
50
51      o Loading design into grid...
52      o Using seed cell "alarm_ins" (model "no2_x1").
53      o Grid offset : (0,0) [adjust (0,0)]
54      o Small design, global routing disabled.
55      o Allocating grid size [52,61,3].
56      o Loading external terminals.
57      o Finding obstacles.
58      o Loading nets into grid.
59      o Allocating the net scheduler.
60      o Reading power grid.
61
62      o Local routing stage.
63      - [ 53] (hp := 0) "not_code 1"
64      - [ 52] (hp := 0) "vdd"
65      - [ 51] (hp := 0) "vss"
66      - [ 50] (hp := 5) "scanin"
67      - [ 49] (hp := 6) "reset"
68      - [ 48] (hp := 6) "scanout"
69      - [ 47] (hp := 6) "alarm"
70      - [ 46] (hp := 6) "door"
71      - [ 45] (hp := 10) "na2_x1_3_sig"
72      - [ 44] (hp := 12) "na2_x1_4_sig"
73      - [ 43] (hp := 13) "na1_x1_sig"
74      - [ 42] (hp := 14) "na2_x1_sig"
75      - [ 41] (hp := 15) "inv_x2_2_sig"
76      - [ 40] (hp := 17) "na4_x1_2_sig"

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nero.out x cougar_codej_b_l_scan.out x lvx_codej_b_l_scan.out x druc_core.out x s2r.out x

```
77 - [ 39] (hp := 18) "na3_x1_5_sig"
78 - [ 38] (hp := 20) "aux2"
79 - [ 37] (hp := 21) "inv_x2_sig"
80 - [ 36] (hp := 21) "no3_x1_sig"
81 - [ 35] (hp := 23) "test"
82 - [ 34] (hp := 24) "not_aux1"
83 - [ 33] (hp := 25) "clk"
84 - [ 32] (hp := 25) "not_aux14"
85 - [ 31] (hp := 26) "o3_x2_sig"
86 - [ 30] (hp := 29) "not_aux13"
87 - [ 29] (hp := 30) "no3_x1_2_sig"
88 - [ 28] (hp := 30) "code 0"
89 - [ 27] (hp := 32) "na3_x1_2_sig"
90 - [ 26] (hp := 33) "o2_x2_sig"
91 - [ 25] (hp := 34) "not_aux6"
92 - [ 24] (hp := 35) "na3_x1_sig"
93 - [ 23] (hp := 37) "na4_x1_sig"
94 - [ 22] (hp := 40) "na3_x1_3_sig"
95 - [ 21] (hp := 40) "not_fsm_current_state 0"
96 - [ 20] (hp := 44) "not_code 0"
97 - [ 19] (hp := 45) "na2_x1_2_sig"
98 - [ 18] (hp := 46) "daytime"
99 - [ 17] (hp := 47) "not_reset"
100 - [ 16] (hp := 48) "inv_x2_3_sig"
101 - [ 15] (hp := 48) "o4_x2_sig"
102 - [ 14] (hp := 49) "code 3"
103 - [ 13] (hp := 50) "not_code 3"
104 - [ 12] (hp := 51) "oa22_x2_2_sig"
105 - [ 11] (hp := 51) "not_code 2"
106 - [ 10] (hp := 54) "na3_x1_4_sig"
107 - [ 9] (hp := 56) "code 1"
108 - [ 8] (hp := 61) "oa22_x2_sig"
109 - [ 7] (hp := 64) "not_aux12"
110 - [ 6] (hp := 64) "no4_x1_2_sig"
111 - [ 5] (hp := 66) "fsm_current_state 1"
112 - [ 4] (hp := 72) "code 2"
113 - [ 3] (hp := 76) "fsm_current_state 0"
114 - [ 2] (hp := 82) "not_aux0"
```

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nero.out x cougar_codej_b_l_scan.out x lvx_codej_b_l_scan.out x druc_core.out x s2r.out x

```
92 - [ 24] (hp := 35) "na3_x1_sig"
93 - [ 23] (hp := 37) "na4_x1_sig"
94 - [ 22] (hp := 40) "na3_x1_3_sig"
95 - [ 21] (hp := 40) "not_fsm_current_state 0"
96 - [ 20] (hp := 44) "not_code 0"
97 - [ 19] (hp := 45) "na2_x1_2_sig"
98 - [ 18] (hp := 46) "daytime"
99 - [ 17] (hp := 47) "not_reset"
100 - [ 16] (hp := 48) "inv_x2_3_sig"
101 - [ 15] (hp := 48) "o4_x2_sig"
102 - [ 14] (hp := 49) "code 3"
103 - [ 13] (hp := 50) "not_code 3"
104 - [ 12] (hp := 51) "oa22_x2_2_sig"
105 - [ 11] (hp := 51) "not_code 2"
106 - [ 10] (hp := 54) "na3_x1_4_sig"
107 - [ 9] (hp := 56) "code 1"
108 - [ 8] (hp := 61) "oa22_x2_sig"
109 - [ 7] (hp := 64) "not_aux12"
110 - [ 6] (hp := 64) "no4_x1_2_sig"
111 - [ 5] (hp := 66) "fsm_current_state 1"
112 - [ 4] (hp := 72) "code 2"
113 - [ 3] (hp := 76) "fsm_current_state 0"
114 - [ 2] (hp := 82) "not_aux0"
115 - [ 1] (hp := 87) "fsm_current_state 2"
116 - [ 0] (hp := 90) "not_fsm_current_state 1"

o Routing stats :
- routing iterations := 37003
- re-routing iterations := 0
- ratio := 0%.

o Dumping routing grid.
o Saving MBK figure "codej_b_l_scan".
o Saving layout as "codej_b_l_scan"...
```

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7.3 cougar_codej_b_l_scan.out

```
E:\Semester 6\EDA\Project\Ahmed_Bahaa_Ibrahim\project\cougar_codej_b_l_scan.out - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?

cougar_codej_b_l_scan.out | hvx_codej_b_l_scan.out | druc_core.out | s2r.out |

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      00 00 00 00 00 0 0 0000 00
      00 00 00 00 00 000 00 00 00
      00 00 00 00 00 0000 00 00 00
      0000 000 0000 00 0000 00 0000
      0
      00000

Netlist extractor ... formerly Lynx

Alliance CAD System 5.0 20090901, cougar 1.21
Copyright (c) 1998-2019, ASIM/LIP6/UPMC
Author(s): Ludovic Jacomme and Gregoire Avot
Contributor(s): Picault Stephane
E-mail : alliance-users@asim.lip6.fr

---> Parse technological file ./techno/techno-035.rds

RDS_LAMBDA = 23
RDS_UNIT = 80
RDS_PHYSICAL_GRID = 2
MBK_SCALE_X = 100

---> Extract symbolic figure codej_b_l_scan

---> Translate MbK -> Rds

---> Build windows
<--- 90

---> Rectangles : 1297

spice file length: 1,953 lines: 59 Ln: 1 Col: 1 Sel: 0 | 0 Unix (LF) UTF-8 INS
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```

```
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cougar_codej_b_l_scan.out | hvx_codej_b_l_scan.out | druc_core.out | s2r.out |

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---> Parse technological file ./techno/techno-035.rds

RDS_LAMBDA = 23
RDS_UNIT = 80
RDS_PHYSICAL_GRID = 2
MBK_SCALE_X = 100

---> Extract symbolic figure codej_b_l_scan

---> Translate MbK -> Rds

---> Build windows
<--- 90

---> Rectangles : 1297
---> Figure size : ( -104, -52 )
                  ( 25600, 30052 )

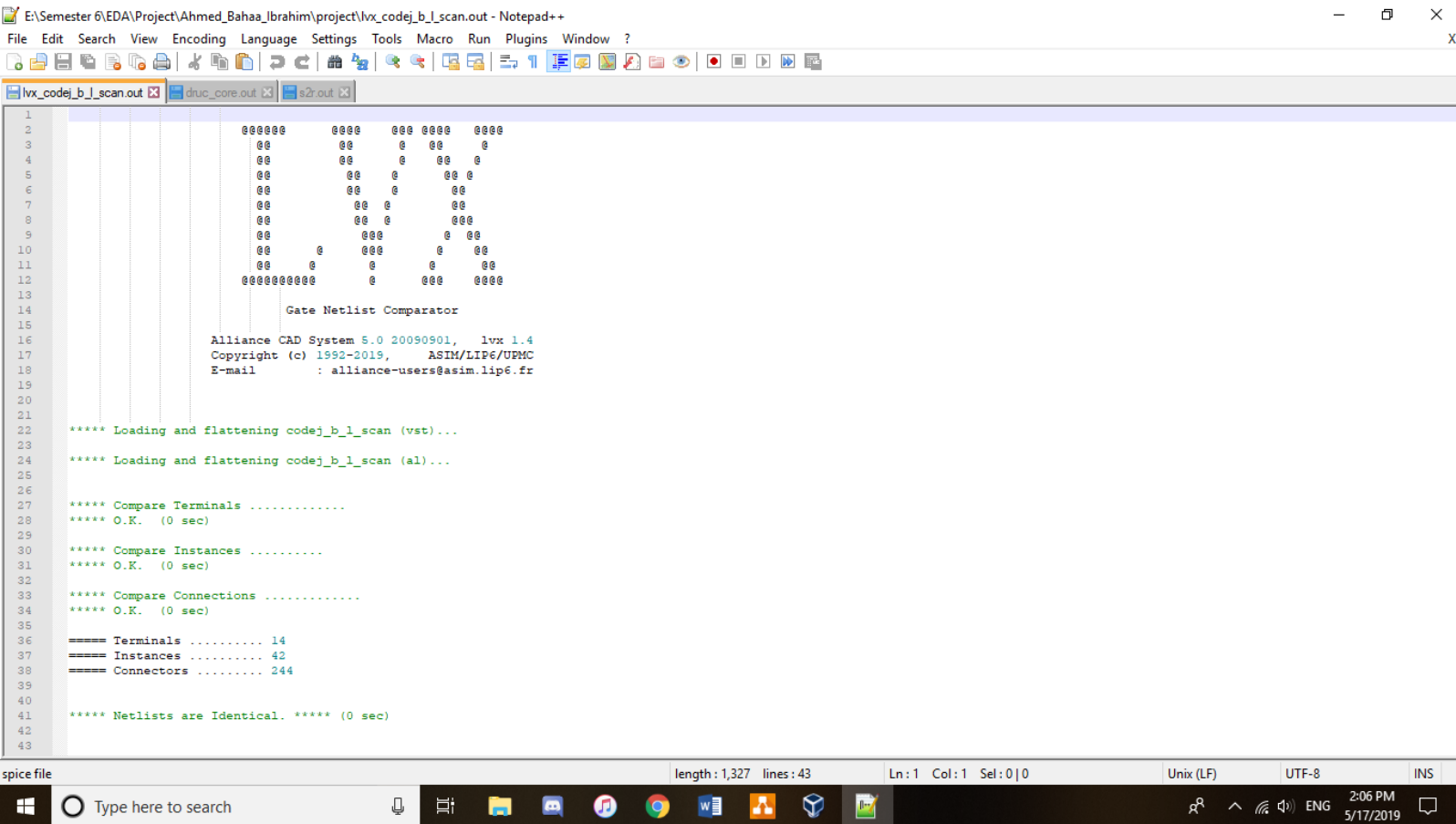
---> Cut transistors
<--- 0
---> Build equis
<--- 58
---> Delete windows
---> Build signals
<--- 58
---> Build instances
<--- 67
---> Build transistors
<--- 0
---> Save netlist

<--- done !

---> Total extracted capacitance
<--- 0.0pF

spice file length: 1,953 lines: 59 Ln: 1 Col: 1 Sel: 0 | 0 Unix (LF) UTF-8 INS
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```

7.4 lvx_codej_b_l_scan.out



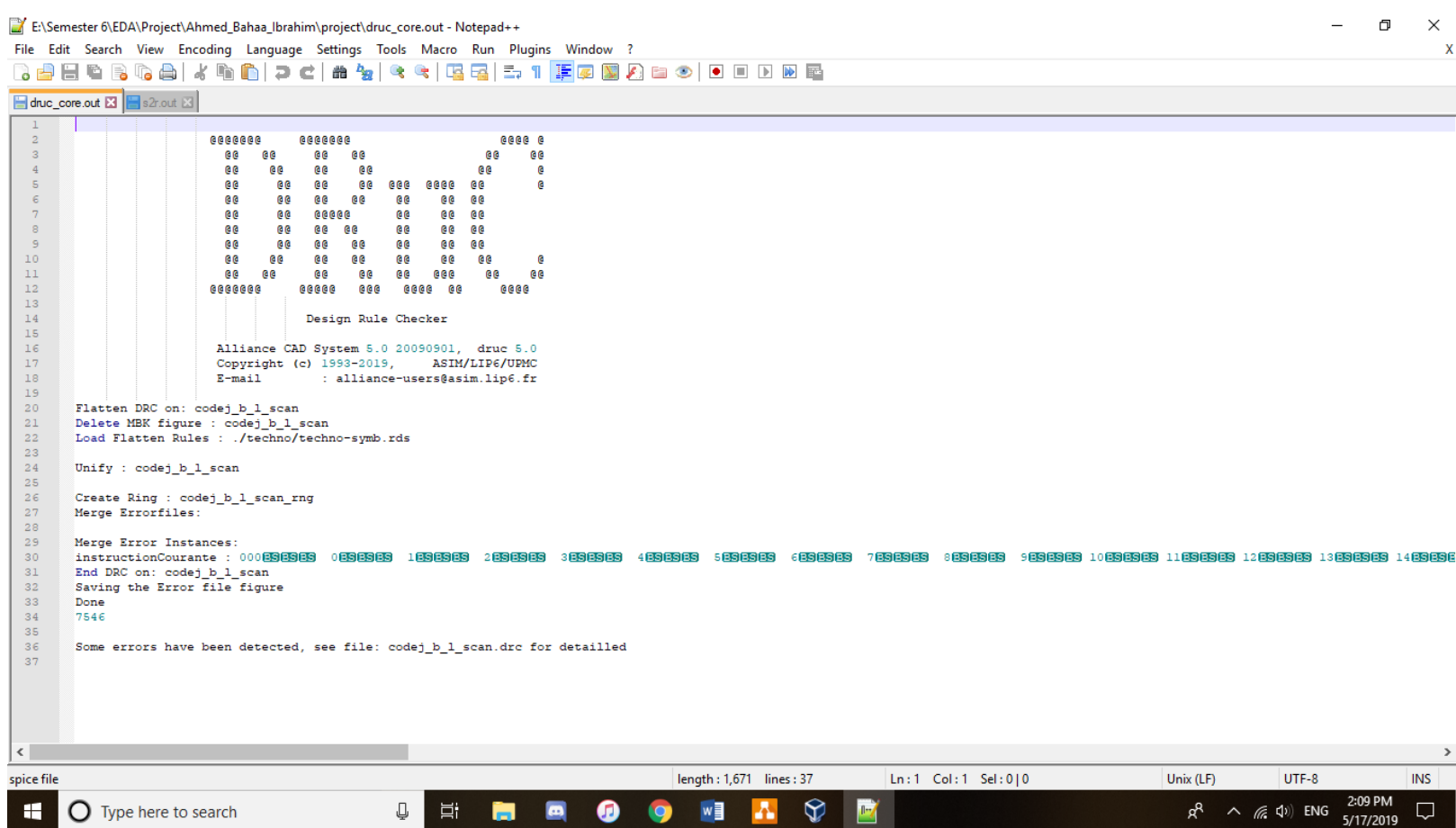
```
1
2
3      000000  0000  000 0000  0000
4      00      00  0  00  0
5      00      00  0  00  0
6      00      00  0  00  0
7      00      00  0  00  0
8      00      00  0  000
9      00      000  0  00
10     00      000  0  00
11     00      0  0  0  00
12     000000000  0  000 0000
13
14      Gate Netlist Comparator
15
16      Alliance CAD System 5.0 20090901,  lvx 1.4
17      Copyright (c) 1992-2019,  ASIM/LIP6/UPMC
18      E-mail      : alliance-users@asim.lip6.fr
19
20
21
22      ***** Loading and flattening codej_b_l_scan (vst)...
23
24      ***** Loading and flattening codej_b_l_scan (al)...
25
26
27      ***** Compare Terminals .....
28      ***** O.K. (0 sec)
29
30      ***** Compare Instances .....
31      ***** O.K. (0 sec)
32
33      ***** Compare Connections .....
34      ***** O.K. (0 sec)
35
36      ===== Terminals ..... 14
37      ===== Instances ..... 42
38      ===== Connectors ..... 244
39
40
41      ***** Netlists are Identical. ***** (0 sec)
42
43
```

spice file length: 1,327 lines: 43 Ln: 1 Col: 1 Sel: 0 | 0 Unix (LF) UTF-8 INS

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7.5 druc_core.out



```
1
2      00000000 00000000          0000 0
3      00 00 00 00          00 00
4      00 00 00 00          0
5      00 00 00 00 000 0000 00 0
6      00 00 00 00 00 00 00
7      00 00 00000 00 00 00
8      00 00 00 00 00 00 00
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10     00 00 00 00 00 00 00 0
11     00 00 00 00 00 000 00 00
12     00000000 00000 000 0000 00 0000
13
14     Design Rule Checker
15
16     Alliance CAD System 5.0 20090901, druc 5.0
17     Copyright (c) 1993-2019, ASIM/LIP6/UPMC
18     E-mail      : alliance-users@asim.lip6.fr
19
20     Flatten DRC on: codej_b_l_scan
21     Delete MBK figure : codej_b_l_scan
22     Load Flatten Rules : ./techno/techno-symb.rds
23
24     Unify : codej_b_l_scan
25
26     Create Ring : codej_b_l_scan_rng
27     Merge Errorfiles:
28
29     Merge Error Instances:
30     instructionCourante : 00000000 00000000 10000000 20000000 30000000 40000000 50000000 60000000 70000000 80000000 90000000 10000000 11000000 12000000 13000000 14000000
31     End DRC on: codej_b_l_scan
32     Saving the Error file figure
33     Done
34     7546
35
36     Some errors have been detected, see file: codej_b_l_scan.drc for detailed
37
```

spice file length: 1,671 lines: 37 Ln: 1 Col: 1 Sel: 0 | 0 Unix (LF) UTF-8 INS

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7.6 s2r.out

```
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192 --> post-treating model oa22_x2
193 rectangle merging :
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219 --> post-treating model a2_x2
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228 --> post-treating model o4_x2

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spice file
128 --> post-treating model o4_x2
129 rectangle merging :
130 . RDS_NWELL .....
131 . RDS_PWELL .....
132 . RDS_NIMP .....
133 . RDS_PIMP .....
134 . RDS_ACTIV .....
135 . RDS_POLY .....
136 . RDS_ALU1 .....
137 --> post-treating model na4_x1
138 rectangle merging :
139 . RDS_NWELL .....
140 . RDS_PWELL .....
141 . RDS_NIMP .....
142 . RDS_PIMP .....
143 . RDS_ACTIV .....
144 . RDS_POLY .....
145 . RDS_ALU1 .....
146 --> post-treating model no4_x1
147 rectangle merging :
148 . RDS_NWELL .....
149 . RDS_PWELL .....
150 . RDS_NIMP .....
151 . RDS_PIMP .....
152 . RDS_ACTIV .....
153 . RDS_POLY .....
154 . RDS_ALU1 .....
155 --> post-treating model buf_x2
156 rectangle merging :
157 . RDS_NWELL .....
158 . RDS_PWELL .....
159 . RDS_NIMP .....
160 . RDS_PIMP .....
161 . RDS_ACTIV .....
162 . RDS_POLY .....
163 . RDS_ALU1 .....
164 --> post-treating model no3_x1
165 rectangle merging :
166 . RDS_NWELL .....
167 . RDS_PWELL .....
168 . RDS_NIMP .....
169 . RDS_PIMP .....
170 . RDS_ACTIV .....

spice file length: 9,522 lines: 214 Ln: 1 Col: 1 Sel: 0 | 0 Unix (LF) UTF-8 INS
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```

E:\Semester 6\EDA\Project\Ahmed_Bahaa_Ibrahim\project\szr.out - Notepad++

File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?

szr.out

```
172 . RDS_ALU1 .....
173 --> post-treating model onl2_x1
174 rectangle merging :
175 . RDS_NWELL .....
176 . RDS_PWELL .....
177 . RDS_NIMP .....
178 . RDS_PIMP .....
179 . RDS_ACTIV .....
180 . RDS_POLY .....
181 . RDS_ALU1 .....
182 --> post-treating model tie_w0
183 rectangle merging :
184 . RDS_NWELL .....
185 . RDS_PWELL .....
186 . RDS_NIMP .....
187 . RDS_PIMP .....
188 . RDS_ACTIV .....
189 . RDS_ALU1 .....
190 --> post-treating model rowend_x0
191 rectangle merging :
192 . RDS_NWELL .....
193 . RDS_ALU1 .....
194 --> post-treating model codej_b_l_scan
195 ring flattening :
196 . RDS_NWELL .....
197 . RDS_NIMP .....
198 . RDS_PIMP .....
199 . RDS_ACTIV .....
200 . RDS_POLY .....
201 rectangle merging :
202 . RDS_NWELL .....
203 . RDS_NIMP .....
204 . RDS_PIMP .....
205 . RDS_ACTIV .....
206 . RDS_POLY .....
207 . RDS_ALU1 .....
208 . RDS_ALU2 .....
209 . RDS_ALU3 .....
210 o saving codej_b_l_scan.cif
211 o memory allocation informations
212 --> required rectangles = 4266 really allocated = 7
213 --> Number of allocated bytes: 170138
214
```

spice file length: 9,522 lines: 214 Ln: 1 Col: 1 Sel: 0 | 0 Unix (LF) UTF-8 INS

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8. Appendecies

8.1 Makefile

```
#-----Sdet-----#

all: codea.vbe \
    codej.vbe \
    codem.vbe \
    codeo.vbe \
    coder.vbe \
    code_boom \
    code_loon

                                @echo "<-- Generated"

#-----Finite State Machine Synthesis-----#

vhd_to_fsm:

                                rename .vhd .fsm *.vhd

codea.vbe: code.fsm

                                @echo "  Encoding Synthesis -> codea.vbe"
                                syf -CEV -a code

codej.vbe: code.fsm

                                @echo "  Encoding Synthesis -> codej.vbe"
                                syf -CEV -j code

codem.vbe: code.fsm

                                @echo "  Encoding Synthesis -> codem.vbe"
                                syf -CEV -m code

codeo.vbe: code.fsm

                                @echo "  Encoding Synthesis -> codeo.vbe"
                                syf -CEV -o code

coder.vbe: code.fsm

                                @echo "  Encoding Synthesis -> coder.vbe"
                                syf -CEV -r code
```

```
MBK_OUT_LO=al; export MBK_OUT_LO; \
RDS TECHNO NAME=./techno/techno-035.rds; \
```

```
export RDS_TECHNO_NAME; \  
cougar -v $* > cougar_$.out  
lvx vst al $* $* -f > lvx_$.out
```

```
druc_core : codej_b_l_scan.ap  
RDS_TECHNO_NAME=./techno/techno-symb.rds; \  
export RDS_TECHNO_NAME; \  
druc codej_b_l_scan > druc_core.out
```

```
code_chip.cif : codej_b_l_scan.ap  
RDS_TECHNO_NAME=./techno/techno-035.rds; \  
export RDS_TECHNO_NAME; \  
RDS_OUT=cif; export RDS_OUT; \  
s2r -v -r codej_b_l_scan code_chip
```

```
#-----Clean Up-----#
```

```
clean :  
rm -f *.vbe *.enc *~  
@echo "Erase all the files generated by the makefile"
```

8.2 Code.ioc

```
LEFT ( # IOs from bottom to top
(IOPIN scanin.0 );
(IOPIN daytime.0 );
(IOPIN code(0).0 );
)
TOP ( # IOs from left to right
(IOPIN code(1).0 );
(IOPIN code(2).0 );
(IOPIN code(3).0 );
)
RIGHT( # IOs from bottom to top
(IOPIN test.0 );
(IOPIN reset.0 );
)
BOTTOM ( # IOs from left to right
(IOPIN door.0 );
(IOPIN clk.0 );
(IOPIN alarm.0 );
(IOPIN scanout.0 ); )
```