	1	2	3	4	5	6	7	8
A	HT1_TX_CADn07	HT1_TX_CTLp0	HT1_TX_CTLn0	VDDE_1V2	HT1_REXT	HT1_TX_CTLp1	HT1CLKp	HT1_RX_CTLn0
B	HT1_TX_CADp07	VDDE_1V2	VDDE_1V2	HT1_TX_CADn15	HT1_TX_CADp15	HT1_TX_CTLn1	HT1CLKn	VDDE_1V2
C	HT1_TX_CADn05	HT1_TX_CADp06	HT1_TX_CADn06	GNDE	GNDE	HT1_TX_CADn14	HT1_PLL_AVDD	VDDE_1V2
D	HT1_TX_CADp05	GNDE	GNDE	HT1_TX_CADn13	HT1_TX_CADp13	HT1_TX_CADp14	HT1_PLL_GND	HT1_RX_CTLp0
E	HT1_TX_CLKn0	HT1_TX_CADp04	HT1_TX_CADn04	VDDE_1V2	VDDE_1V2	HT1_TX_CADn12	HT1_PLL_DVDD	HT1_RX_CTLn1
F	HT1_TX_CLKp0	VDDE_1V2	VDDE_1V2	HT1_TX_CLKn1	HT1_TX_CLKp1	HT1_TX_CADp12	HT1_PLL_GND	HT1_RX_CADn15
G	HT1_TX_CADn02	HT1_TX_CADp03	HT1_TX_CADn03	GNDE	GNDE	HT1_TX_CADn11	GND	VDD
H	HT1_TX_CADp02	GNDE	GNDE	HT1_TX_CADn10	HT1_TX_CADp10	HT1_TX_CADp11	GND	
J	HT1_TX_CADn00	HT1_TX_CADp01	HT1_TX_CADn01	VDDE_1V2	VDDE_1V2	HT1_TX_CADn09	VDD	
K	HT1_TX_CADp00	VDDE_1V2	VDDE_1V2	HT1_TX_CADn08	HT1_TX_CADp08	HT1_TX_CADp09	VDD	
L	UART0_RI	UART1_DCD	PCI_CONFIG7	PCI_CONFIG6	PCI_CONFIG5	VDDE_1V8	GNDE	
M	UART1_RTS	UART0_DTR	UART0_RXD	PCI_CONFIG0	PCI_CONFIG3	GNDE	VDDE_1V8	
N	UART1_DTR	UART0_CTS	PCI_CONFIG2	PCI_CONFIG1	PCI_CONFIG4	VDDE_1V8	GNDE	
P	UART1_RXD	UART1_DSR	UART0_RTS	UART0_DSR	UART0_DCD	UART0_TXD	VDDE_1V8	
R	NODE_ID0	UART1_RI	CLKSEL15	ICCC_EN	UART1_TXD	UART1_CTS	GNDE	
T	CLKSEL11	CLKSEL08	CLKSEL14	CLKSEL10	CLKSEL13	NODE_ID1	GNDE	
U	CLKSEL07	CLKSEL06	CLKSEL09	CLKSEL05	CLKSEL12	VDD	VDD	
V	CLKSEL02	CLKSEL01	CLKSEL04	CLKSEL00	CLKSEL03	GND	GND	
W	GND	VDD	GND	VDD	GND	VDD	VDD	
Y	MC1_DDR_DQ01	MC1_DDR_DQ00	MC1_DDR_DQM0	GNDE	MC1_DDR_DQ05	MC1_DDR_DQ04	GND	
AA	MC1_DDR_DQSp0	MC1_DDR_DQSn0	MC1_DDR_DQ06	MC1_DDR_DQ03	VDDE_DDR	MC1_DDR_DQ07	MC1_DDR_DQ02	
AB	MC1_DDR_DQM1	MC1_DDR_DQ13	MC1_DDR_DQ09	GNDE	MC1_DDR_DQ08	MC1_DDR_DQ12	VDD	
AC	MC1_DDR_DQSn1	MC1_DDR_DQSp1	VDDE_DDR	MC1_DDR_CLKp1	MC1_DDR_CLKn1	MC1_DDR_DQ14	MC1_DDR_DQ10	
AD	MC1_DDR_CLKp0	MC1_DDR_CLKn0	GNDE	MC1_DDR_DQ15	MC1_DDR_DQ11	MC1_DDR_DQ20	GND	
AE	MC1_DDR_DQSn2	MC1_DDR_DQSp2	MC1_DDR_DQM2	VDDE_DDR	MC1_DDR_DQ17	MC1_DDR_DQ21	MC1_DDR_DQ16	
AF	MC1_DDR_DQ23	MC1_DDR_DQ19	MC1_DDR_DQ28	MC1_DDR_DQ18	GNDE	MC1_DDR_DQ22	VDD	
AG	MC1_DDR_DQSn3	MC1_DDR_DQSp3	MC1_DDR_DQ25	VDDE_DDR	MC1_DDR_DQ29	MC1_DDR_DQ24	GND	
AH	MC1_DDR_DQ27	MC1_DDR_DQ31	GNDE	MC1_DDR_DQM3	MC1_DDR_DQ26	MC1_DDR_DQ30	VDD	
AJ	MC1_DDR_DQM8	MC1_DDR_CB1	MC1_DDR_CB0	MC1_DDR_CB5	VDDE_DDR	MC1_DDR_CB4	GND	
AK	MC1_DDR_DQSn8	MC1_DDR_DQSp8	MC1_DDR_CB3	MC1_DDR_CB2	MC1_DDR_CB7	GNDE	MC1_DDR_CB6	
AL	MC1_DDR_CKE2	MC1_DDR_BA2	MC1_DDR_CKE0	VDDE_DDR	MC1_DDR_CKE1	MC1_DDR_CKE3	VDD	
AM	MC1_DDR_A09	MC1_DDR_A11	GNDE	MC1_DDR_A12	MC1_DDR_A14	MC1_DDR_RESETn	MC1_DDR_A15	
AN	MC1_DDR_A04	MC1_DDR_A06	MC1_DDR_A05	VDDE_DDR	MC1_DDR_A07	MC1_DDR_A08	MC1_DDR_REXT	MC1_DDR_DQ46
AP	MC1_DDR_A00	MC1_DDR_CLKn3	MC1_DDR_CLKp3	MC1_DDR_A01	MC1_DDR_A02	MC1_DDR_A03	GND	MC1_DDR_DQ42
AR	MC1_DDR_CLKn2	MC1_DDR_CLKp2	MC1_DDR_RASn	MC1_DDR_BA0	MC1_DDR_BA1	MC1_DDR_A10	MC1_DDR_DQ44	MC1_DDR_DQ47
AT	MC1_DDR_SCSn0	MC1_DDR_WEn	MC1_DDR_SCSn2	MC1_DDR_CASn	MC1_DDR_ODT0	MC1_DDR_ODT2	MC1_DDR_DQ40	VDDE_DDR
AU	MC1_DDR_SCSn3	MC1_DDR_SCSn1	GNDE	MC1_DDR_A13	MC1_DDR_ODT1	MC1_DDR_ODT3	MC1_DDR_DQ45	MC1_DDR_DQSn5
AV	MC1_DDR_DQ33	MC1_DDR_DQM4	MC1_DDR_DQ37	VDDE_DDR	MC1_DDR_DQ32	MC1_DDR_DQ36	MC1_DDR_DQ41	MC1_DDR_DQSp5
AW	MC1_DDR_DQSn4	MC1_DDR_DQSp4	MC1_DDR_DQ38	MC1_DDR_DQ39	MC1_DDR_DQ34	MC1_DDR_DQ35	MC1_DDR_DQM5	MC1_DDR_DQ43
	1	2	3	4	5	6	7	8