33	34	35	36	37	38	39	
HT0CLKp	HT0_TX_CTLp1	HT0_REXT	VDDE_1V2	HT0_TX_CTLn0	HT0_TX_CTLp0	HT0_TX_CADn07	A
HT0CLKn	HT0_TX_CTLn1	HT0_TX_CADp15	HT0_TX_CADn15	VDDE_1V2	VDDE_1V2	HT0_TX_CADp07	B
HT0_PLL_AVDD	HT0_TX_CADn14	GNDE	GNDE	HT0_TX_CADn06	HT0_TX_CADp06	HT0_TX_CADn05	C
HT0_PLL_GND	HT0_TX_CADp14	HT0_TX_CADp13	HT0_TX_CADn13	GNDE	GNDE	HT0_TX_CADp05	D
HT0_PLL_DVDD	HT0_TX_CADn12	VDDE_1V2	VDDE_1V2	HT0_TX_CADn04	HT0_TX_CADp04	HT0_TX_CLKn0	E
HT0_PLL_GND	HT0_TX_CADp12	HT0_TX_CLKp1	HT0_TX_CLKn1	VDDE_1V2	VDDE_1V2	HT0_TX_CLKp0	F
GND	HT0_TX_CADn11	GNDE	GNDE	HT0_TX_CADn03	HT0_TX_CADp03	HT0_TX_CADn02	G
GND	HT0_TX_CADp11	HT0_TX_CADp10	HT0_TX_CADn10	GNDE	GNDE	HT0_TX_CADp02	H
VDD	HT0_TX_CADn09	VDDE_1V2	VDDE_1V2	HT0_TX_CADn01	HT0_TX_CADp01	HT0_TX_CADn00	J
VDD	HT0_TX_CADp09	HT0_TX_CADp08	HT0_TX_CADn08	VDDE_1V2	VDDE_1V2	HT0_TX_CADp00	K
GNDE	VDDE_1V8	INTn1	NMIn	INTn0	SPI_SDO	HTCLK	L
VDDE_1V8	GNDE	INTn3	INTn2	SPI_SDI	DOTEST	TMS	M
GNDE	VDDE_1V8	SPI_SCK	TDO	TESTCLK	TDI	TRST	N
VDDE_1V8	EJTAG_TDO	TCK	EJTAG_TCK	EJTAG_TMS	EJTAG_TDI	EJTAG_TRST	P
GNDE	GPIO15	GPIO12	GPIO14	GPIO13	GPIO10	GPIO11	R
VDDE_1V8	GNDE	GPIO07	GPIO09	GPIO08	GPIO05	GPIO06	T
GNDE	VDDE_1V8	GPIO02	GPIO03	GPIO04	GPIO00	GPIO01	U
VDDE_1V8	GNDE	LPC_LAD1	LPC_LAD3	LPC_LAD2	LPC_LAD0	LPC_SERIRQ	V
GNDE	VDDE_1V8	GNDE	GNDE	LPC_ROM8MBITS	LPC_ROMINTEL	LPC_LFRAMEn	W
GNDE	MC0_DDR_DQ04	MC0_DDR_DQ05	GNDE	MC0_DDR_DQM0	MC0_DDR_DQ00	MC0_DDR_DQ01	Y
MC0_DDR_DQ02	MC0_DDR_DQ07	VDDE_DDR	MC0_DDR_DQ03	MC0_DDR_DQ06	MC0_DDR_DQSn0	MC0_DDR_DQSp0	AA
VDD	MC0_DDR_DQ12	MC0_DDR_DQ08	GNDE	MC0_DDR_DQ09	MC0_DDR_DQ13	MC0_DDR_DQM1	AB
MC0_DDR_DQ10	MC0_DDR_DQ14	MC0_DDR_CLKn1	MC0_DDR_CLKp1	VDDE_DDR	MC0_DDR_DQSp1	MC0_DDR_DQSn1	AC
GND	MC0_DDR_DQ20	MC0_DDR_DQ11	MC0_DDR_DQ15	GNDE	MC0_DDR_CLKn0	MC0_DDR_CLKp0	AD
MC0_DDR_DQ16	MC0_DDR_DQ21	MC0_DDR_DQ17	VDDE_DDR	MC0_DDR_DQM2	MC0_DDR_DQSp2	MC0_DDR_DQSn2	AE
VDD	MC0_DDR_DQ22	GNDE	MC0_DDR_DQ18	MC0_DDR_DQ28	MC0_DDR_DQ19	MC0_DDR_DQ23	AF
GND	MC0_DDR_DQ24	MC0_DDR_DQ29	VDDE_DDR	MC0_DDR_DQ25	MC0_DDR_DQSp3	MC0_DDR_DQSn3	AG
VDD	MC0_DDR_DQ30	MC0_DDR_DQ26	MC0_DDR_DQM3	GNDE	MC0_DDR_DQ31	MC0_DDR_DQ27	AH
GND	MC0_DDR_CB4	VDDE_DDR	MC0_DDR_CB5	MC0_DDR_CB0	MC0_DDR_CB1	MC0_DDR_DQM8	AJ
MC0_DDR_CB6	GNDE	MC0_DDR_CB7	MC0_DDR_CB2	MC0_DDR_CB3	MC0_DDR_DQSp8	MC0_DDR_DQSn8	AK
VDD	MC0_DDR_CKE3	MC0_DDR_CKE1	VDDE_DDR	MC0_DDR_CKE0	MC0_DDR_BA2	MC0_DDR_CKE2	AL
MC0_DDR_A15	MC0_DDR_RESETn	MC0_DDR_A14	MC0_DDR_A12	GNDE	MC0_DDR_A11	MC0_DDR_A09	AM
MC0_DDR_REXT	MC0_DDR_A08	MC0_DDR_A07	VDDE_DDR	MC0_DDR_A05	MC0_DDR_A06	MC0_DDR_A04	AN
GND	MC0_DDR_A03	MC0_DDR_A02	MC0_DDR_A01	MC0_DDR_CLKp3	MC0_DDR_CLKn3	MC0_DDR_A00	AP
MC0_DDR_DQ44	MC0_DDR_A10	MC0_DDR_BA1	MC0_DDR_BA0	MC0_DDR_RASn	MC0_DDR_CLKp2	MC0_DDR_CLKn2	AR
MC0_DDR_DQ40	MC0_DDR_ODT2	MC0_DDR_ODT0	MC0_DDR_CASn	MC0_DDR_SCSn2	MC0_DDR_WEn	MC0_DDR_SCSn0	AT
MC0_DDR_DQ45	MC0_DDR_ODT3	MC0_DDR_ODT1	MC0_DDR_A13	GNDE	MC0_DDR_SCSn1	MC0_DDR_SCSn3	AU
MC0_DDR_DQ41	MC0_DDR_DQ36	MC0_DDR_DQ32	VDDE_DDR	MC0_DDR_DQ37	MC0_DDR_DQM4	MC0_DDR_DQ33	AV
MC0_DDR_DQM5	MC0_DDR_DQ35	MC0_DDR_DQ34	MC0_DDR_DQ39	MC0_DDR_DQ38	MC0_DDR_DQSp4	MC0_DDR_DQSn4	AW
33	34	35	36	37	38	39	