	9	10	11	12	13	14	15	16
A	HT1_RX_CTLp0	HT1_RX_CADn06	HT1_RX_CADp06	HT1_RX_CADn04	HT1_RX_CADp04	HT1_RX_CADn03	HT1_RX_CADp03	HT1_RX_CADnO
В	$\tt HT1\_RX\_CADn07$	$VDDE_{-}1V2$	HT1_RX_CADn05	$VDDE_{-}1V2$	HT1_RX_CLKn0	$VDDE_{-}1V2$	HT1_RX_CADn02	$VDDE_{-}1V2$
C	HT1_RX_CADp07	VDDE_1V2	HT1_RX_CADp05	VDDE_1V2	HT1_RX_CLKp0	VDDE_1V2	HT1_RX_CADp02	VDDE_1V2
D	GNDE	$\tt HT1\_RX\_CADp14$	GNDE	HT1_RX_CADp12	GNDE	HT1_RX_CADp11	GNDE	HT1_RX_CADp0
E	GNDE	HT1_RX_CADn14	GNDE	HT1_RX_CADn12	GNDE	HT1_RX_CADn11	GNDE	HT1_RX_CADnO
F	HT1_RX_CADp15	HT1_RX_CADn13	HT1_RX_CADp13	HT1_RX_CLKp1	HT1_RX_CLKn1	HT1_RX_CADn10	HT1_RX_CADp10	HT1_RX_CADnO
G	VDD	GND	GND	VDD	VDD	GND	GND	VDD
Н								
J								
K								
L								
М								
N					GND	VDD	GND	VDD
P					VDD	GND	VDD	GND
R					GND	$VDD_{-}N1$	GND	VDD_N1
T					VDD_N1	GND	VDD_N1	GND
U					GND	VDD_N1	GND	VDD_N1
V					VDD_N1	GND	$VDD_N1$	GND
W					GND	VDD_N1	GND	VDD_N1
Y					VDD_N1	GND	VDD_N1	GND
AA					GND	$VDD_{-}N1$	GND	$VDD_{-}N1$
AB					VDD	GND	VDD	GND
AC					GND	VDD	GND	VDD
AD					VDD	GND	VDD	GND
ΑE					GND	VDD	GND	VDD
AF					VDD	GND	VDD	GND
AG					GND	VDD	GND	VDD
AH								
AJ								
AK								
AL								
AM								
AN	MC1_DDR_DQ52	VDD	GND	VDDE_VREF	VDDE_VREF	$PCI_IRQnD$	GNDE	GNDE
AP	MC1_DDR_DQ48	MC1_DDR_DQM6	MC1_DDR_DQ54	MC1_DDR_DQ58	MC1_DDR_DQ63	PCI_IRQnB	PCI_GNTn2	PCI_REQn5
AR	MC1_DDR_DQ53	VDDE_DDR	MC1_DDR_DQ50	MC1_DDR_DQ56	MC1_DDR_DQ59	PCI_RESETn	PCI_REQn2	PCI_GNTn4
AT	MC1_DDR_DQ49	MC1_DDR_DQSn6	MC1_DDR_DQ55	VDDE_DDR	GNDE	VDDE_1V8	PCI_GNTn1	VDDE_1V8
AU	GNDE	MC1_DDR_DQSp6	GNDE	MC1_DDR_DQ61	MC1_DDR_DQSn7	PCI_IRQnA	PCI_REQn1	PCI_REQn4
AV	MC1_DDR_CLKn4	MC1_DDR_CLKp5	MC1_DDR_DQ51	MC1_DDR_DQ57	MC1_DDR_DQSp7	PCI_IRQnC	PCI_GNTn0	PCI_GNTn3
AW	MC1_DDR_CLKp4	MC1_DDR_CLKn5	MC1_DDR_DQ60	MC1_DDR_DQM7	MC1_DDR_DQ62	PCI_CLK	PCI_REQn0	PCI_REQn3
	9	10	11	12	13	14	15	16