Schematic: Expansion Accessory

SHEET	SHEET NAME
01	Title/Revision History
02	System Block Diagram
03	Power Tree Diagram
04	Power Supply
05	LPDDR4
06	eMMC/SD
07	JTAG/SPI Flash
08	Gigabit Ethernet
09	USB OTG TYPE C
10	USB HOST/ADC
11	M.2 Key E/XCVR
12	SoC BANK0/BANK2
13	SoC BANK1
14	SoC Power
15	MISC
16	Exp Conn

Revision History

DATE	REVISION	DESCRIPTION
May. 21 2021	v0.1	1. Initial

MAIN

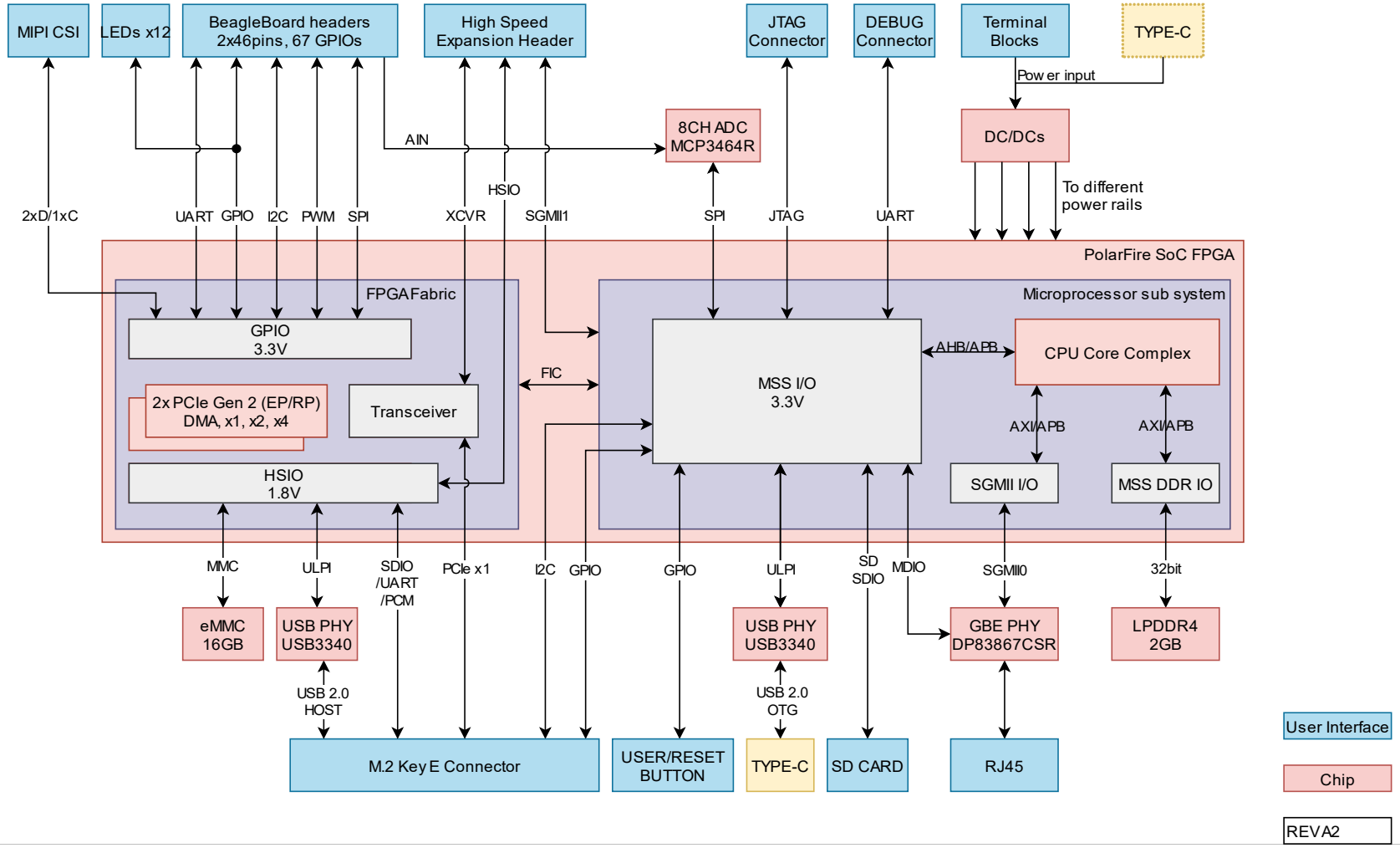
seeed The IoT Hardware Enabler

https://www.seeedstudio.com

Title: Beagleboard FPGA

Size: A3	Document Number: 01_Title/Revision History	Rev: v0.1
Draw By: Xiangnan	Date: Monday, August 23, 2021	Sheet: 1 of 17

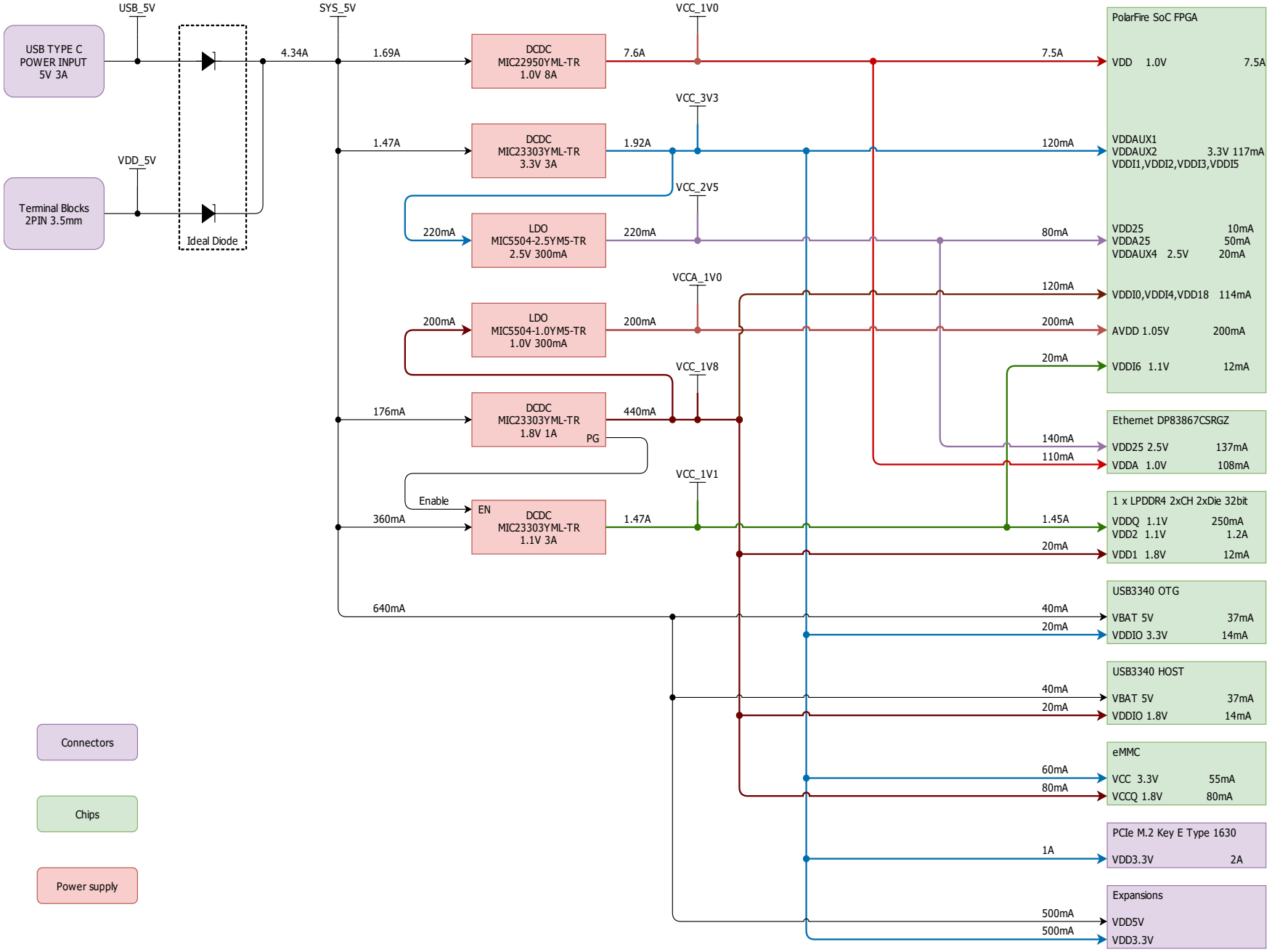
System Block Diagram



MAIN

seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: Beagleboard FPGA	
Size: A3	Document Number: 02_System Block Diagram	Rev: v0.1
Draw By: Xiangnan	Date: Monday, August 23, 2021	Sheet: 2 of 17

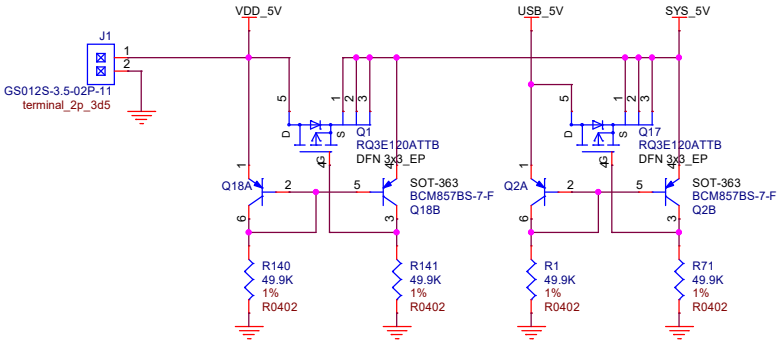
Power Tree Diagram



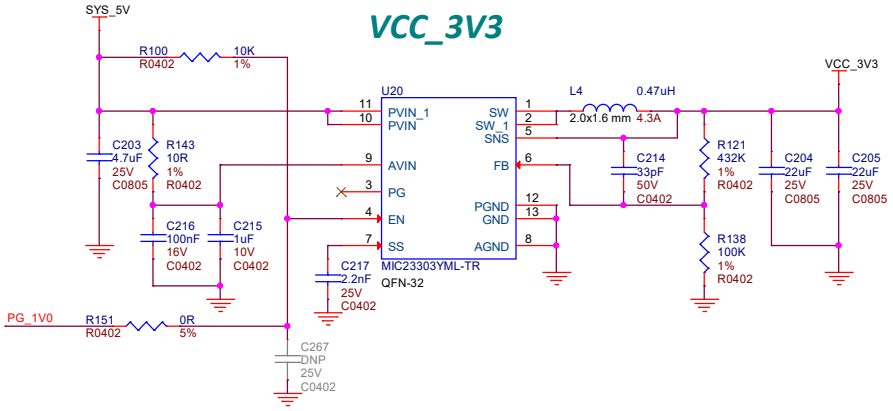
MAIN

seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: Beagleboard FPGA	
Size: A3	Document Number: 03_Power Tree Diagram	Rev: v0.1
Draw By: Xiangnan	Date: Monday, August 23, 2021	Sheet: 3 of 17

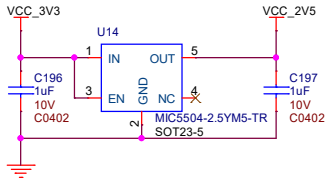
DC IN/Ideal Diode



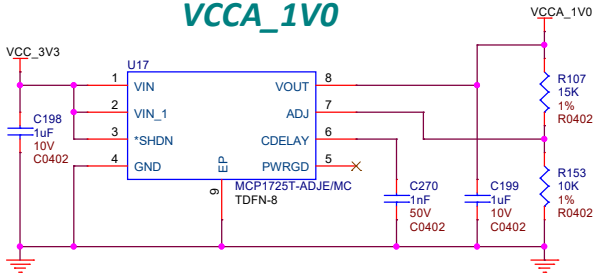
VCC_3V3



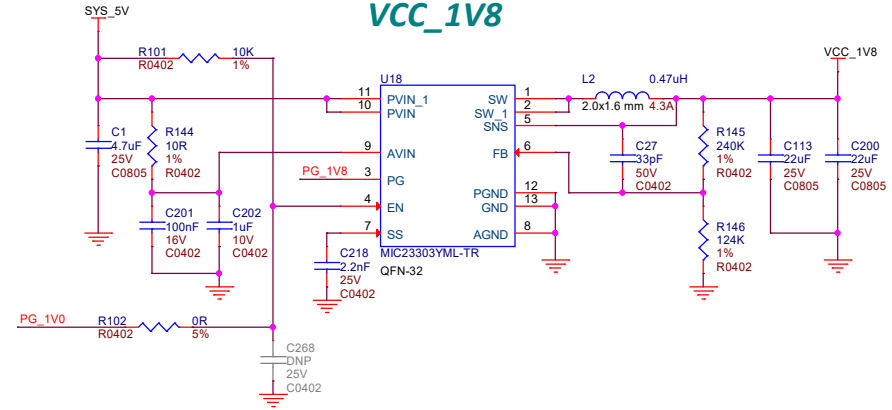
VCC_2V5



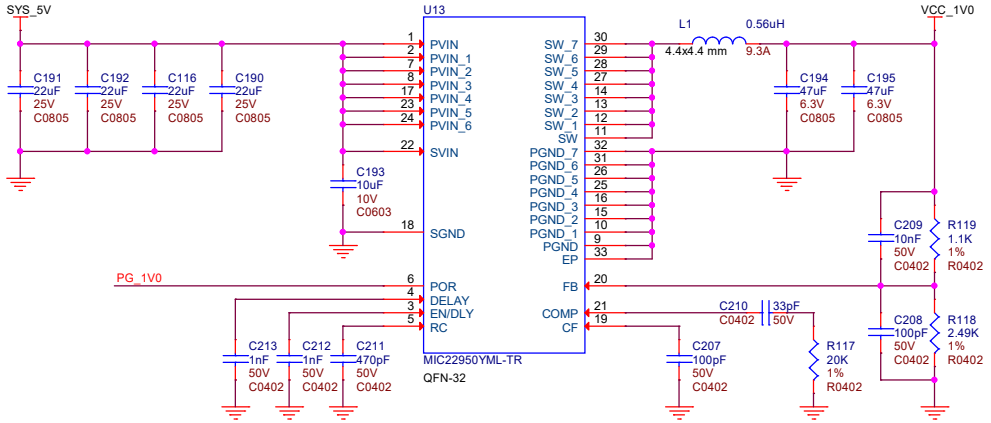
VCCA_1V0



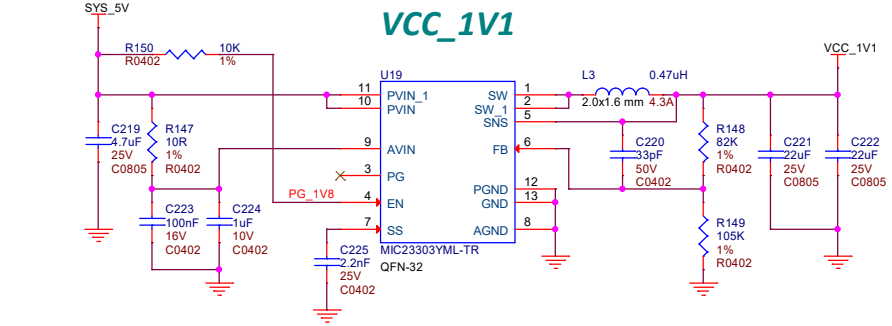
VCC_1V8



VCC_1V0



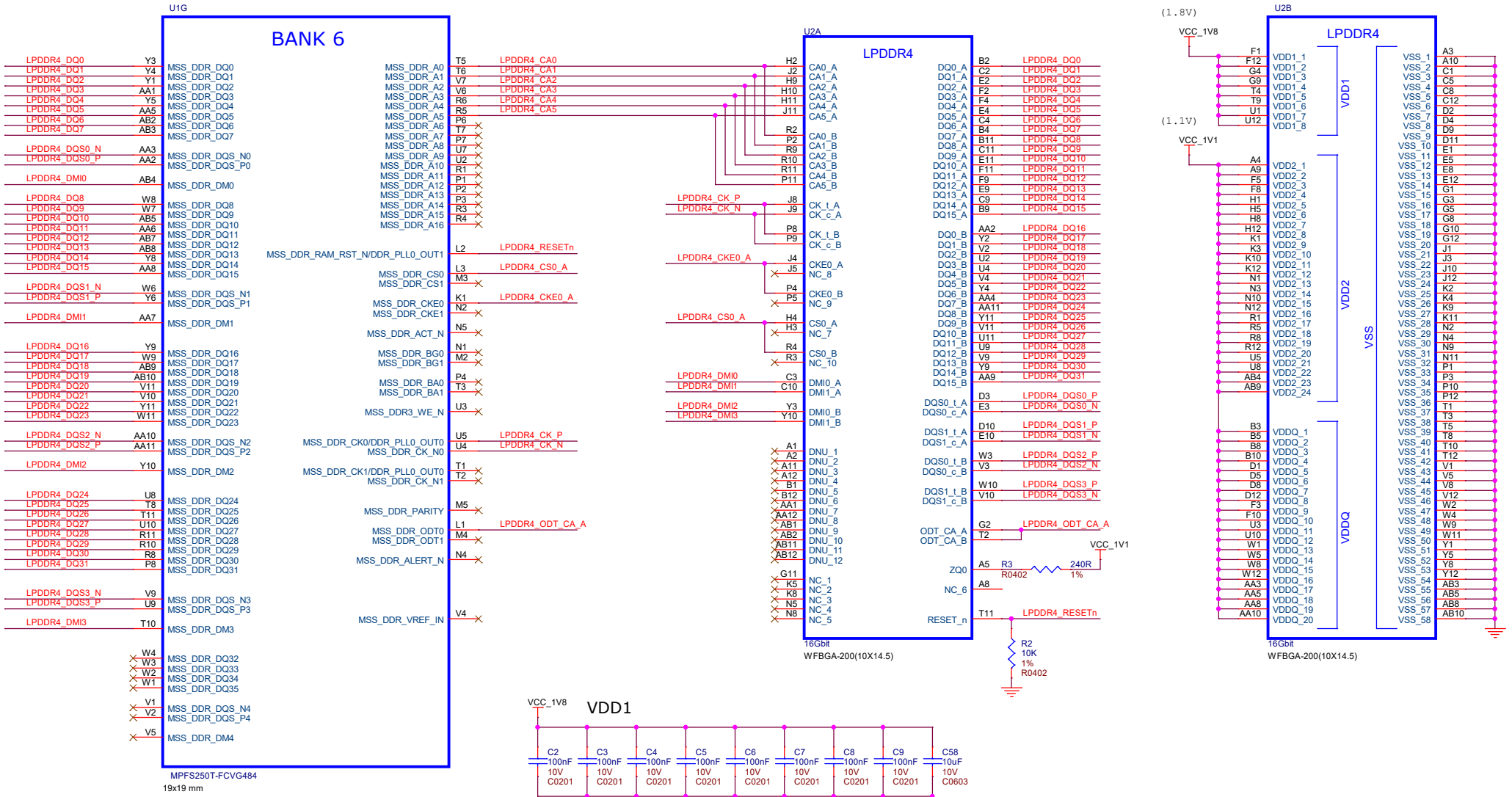
VCC_1V1



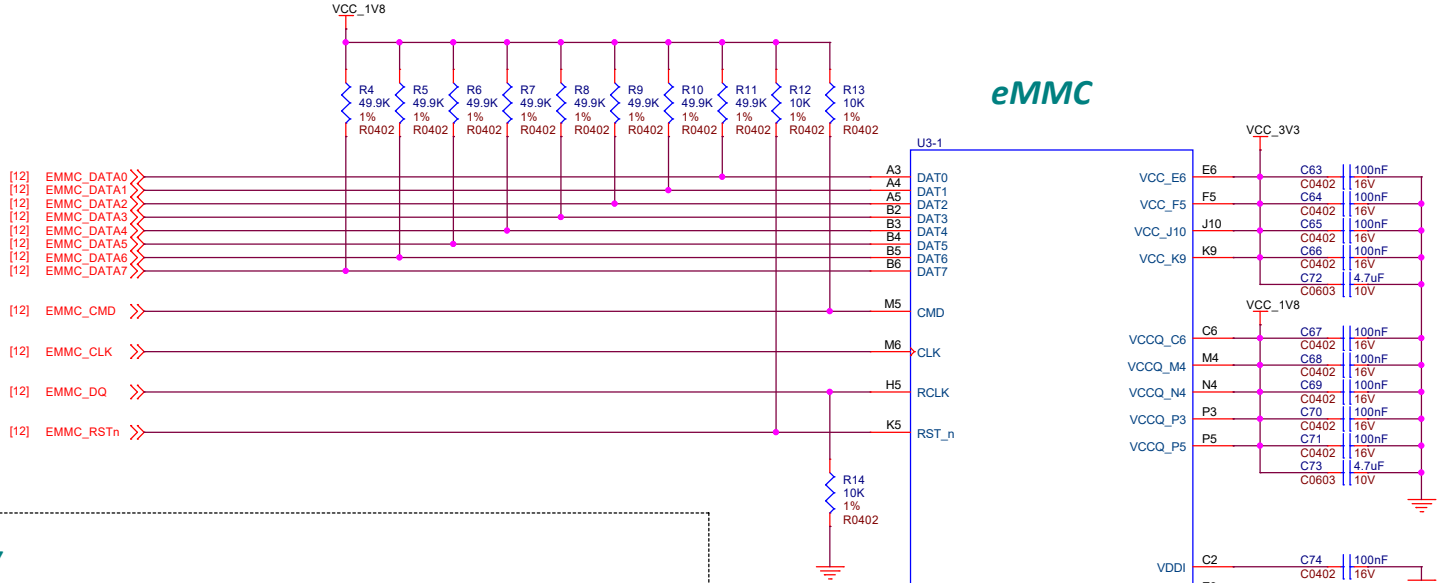
MAIN

seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: Beagleboard FPGA	
Size: A3	Document Number: 04_Power Supply	Rev: v0.1
Draw By: Xiangnan	Date: Monday, August 23, 2021	Sheet: 4 of 17

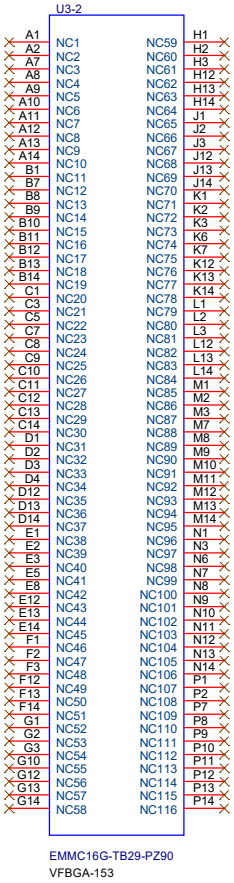
LPDDR4_CONNECTION



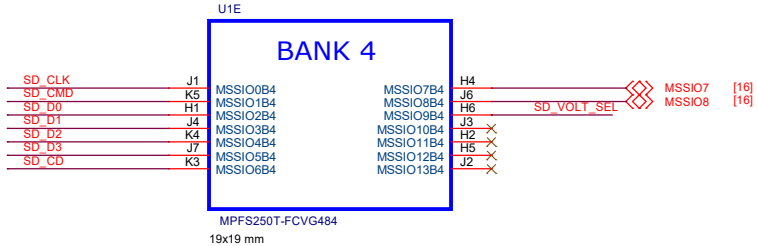
eMMC/SD



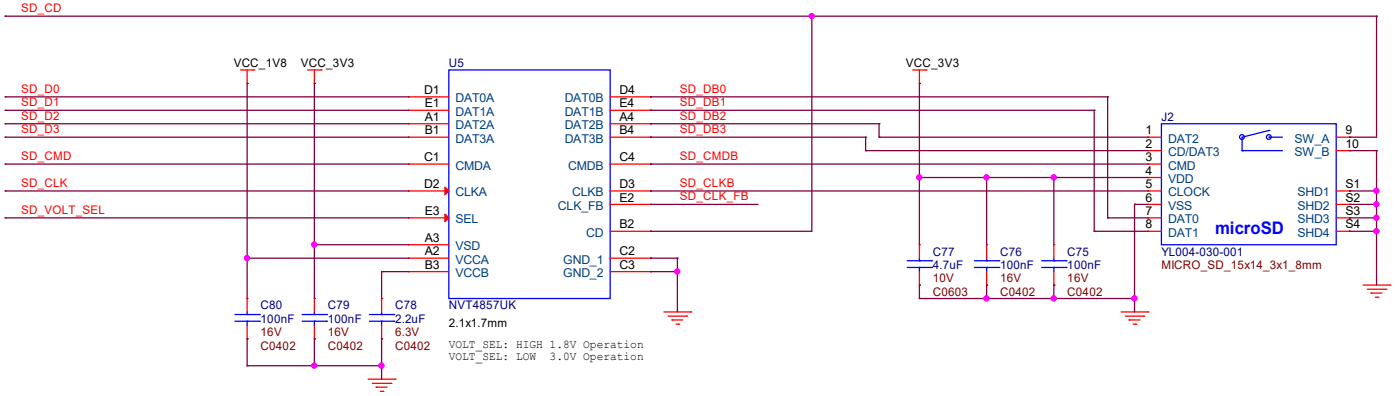
eMMC



BANK4 1.8V



MICRO SD CARD

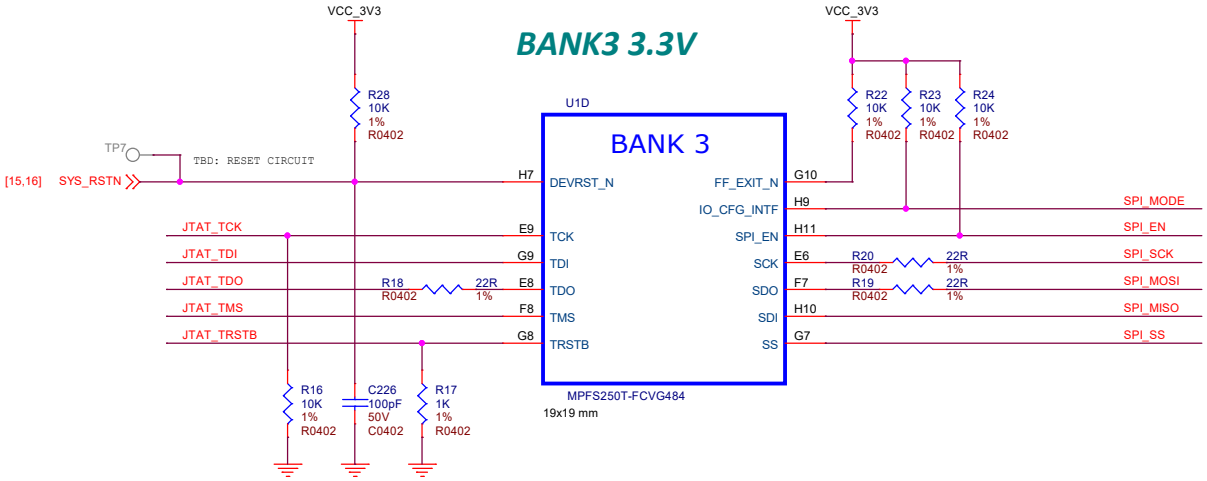


MAIN

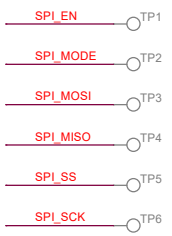
seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: Beagleboard FPGA	
Size: A3	Document Number: 06_eMMC/SD	Rev: v0.1
Draw By: Xiangnan	Date: Monday, August 23, 2021	Sheet: 6 of 17

JTAG/SPI Flash

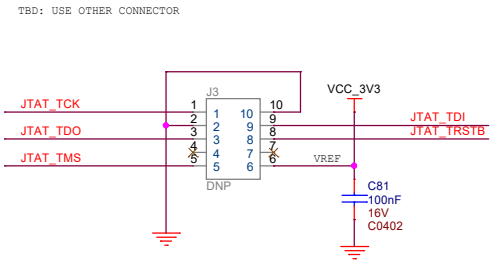
BANK3 3.3V



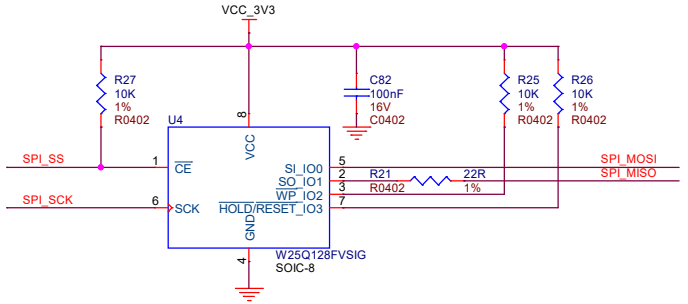
Programming the SPI Flash Using External Master



JTAG for Tag-Connect cable



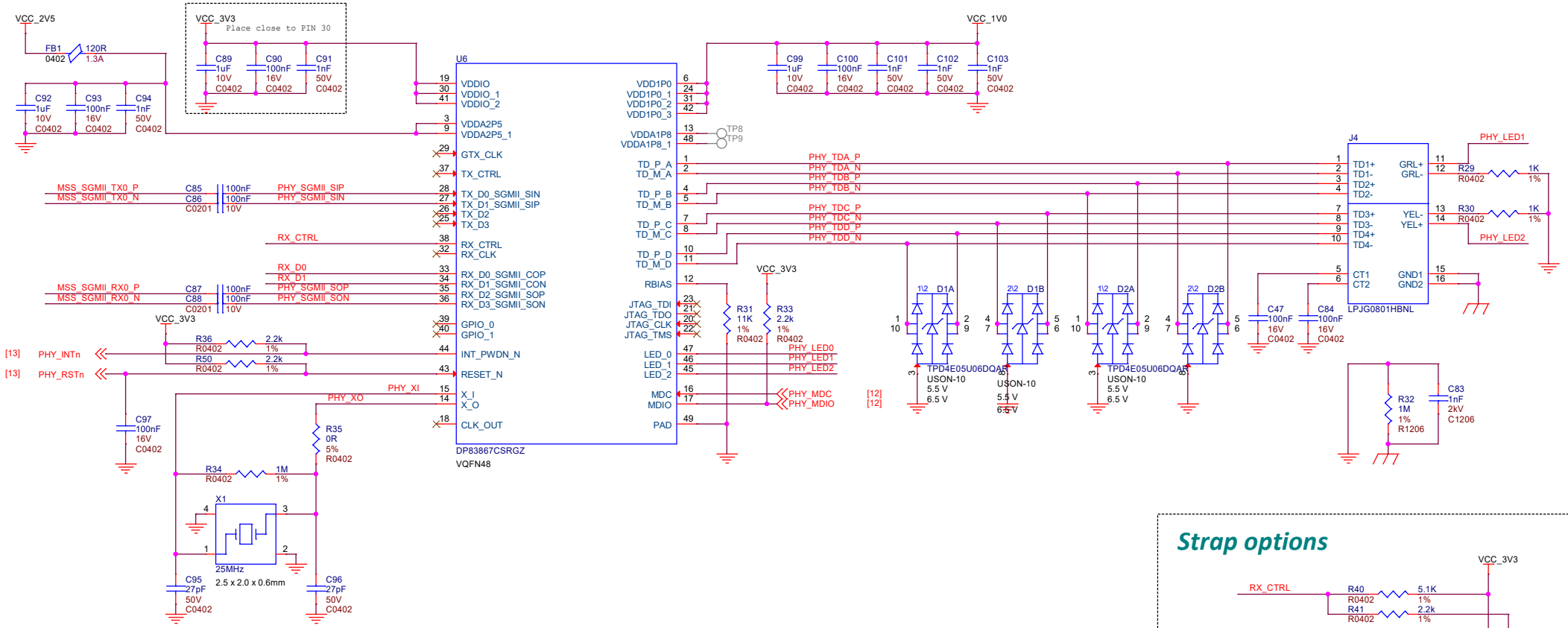
SPI Flash



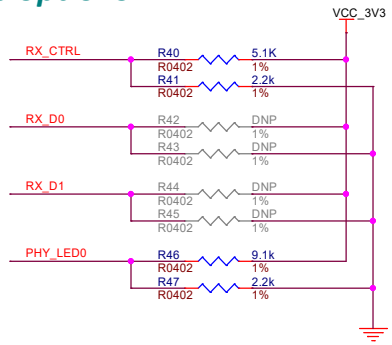
MAIN

seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: Beagleboard FPGA	
Size: A3	Document Number: 07_JTAG/SPI Flash	Rev: v0.1
Draw By: Xiangnan	Date: Monday, August 23, 2021	Sheet: 7 of 17

Gigabit Ethernet

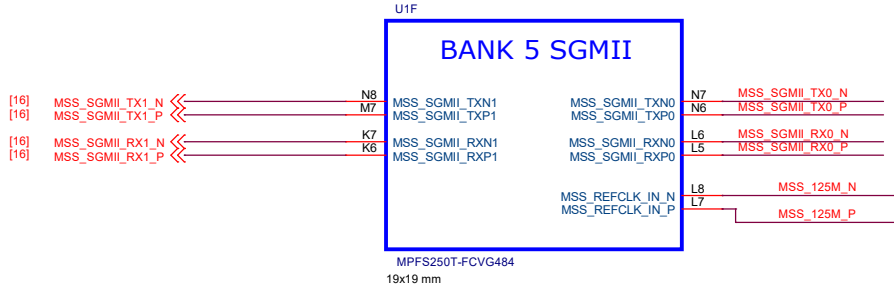


Strap options

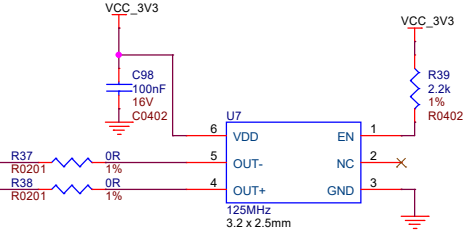


Strap options
GPIO_0,GPIO_1: MODE1, using internal pulldown
RX_CTRL: MODE3, Autoneg Disable = 0
LED_0: MODE2, SGMII Enable =1, Mirror Enable = 0
LED_1: MODE1, ANEG_SEL = 0, using internal pulldown
LED_2: MODE1, using internal pulldown
RX_D2: MODE1, PHY_ADD[3:2] = 00, using internal pulldown
RX_D0: MODE1, PHY_ADD[1:0] = 00, can be setup with external resistors

BACNK5



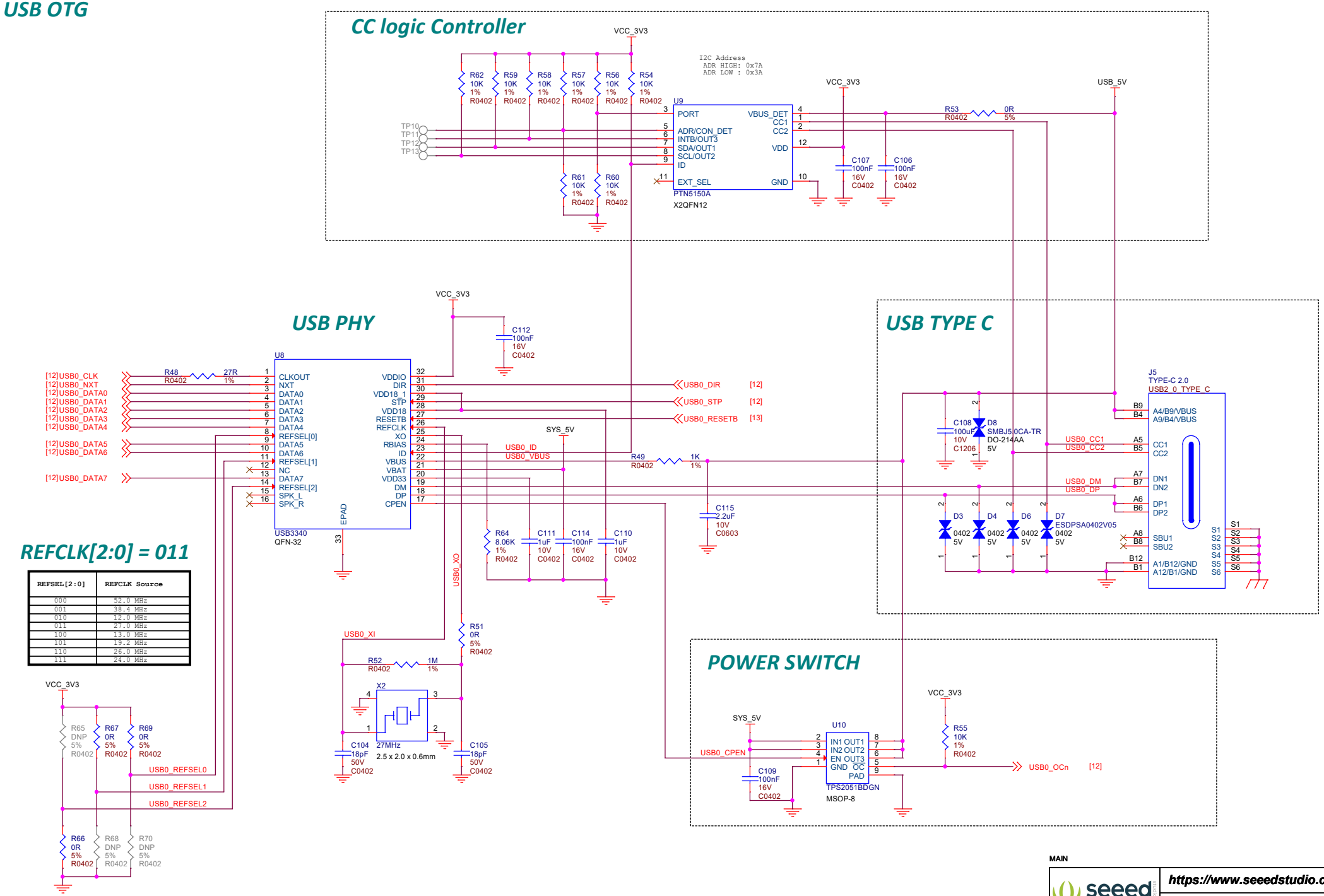
125MHz Oscillator



MAIN

seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: Beagleboard FPGA	
Size: A3	Document Number: 08_Gigabit Ethernet	Rev: v0.1
Draw By: Xiangnan	Date: Friday, September 10, 2021	Sheet: 8 of 17

USB OTG

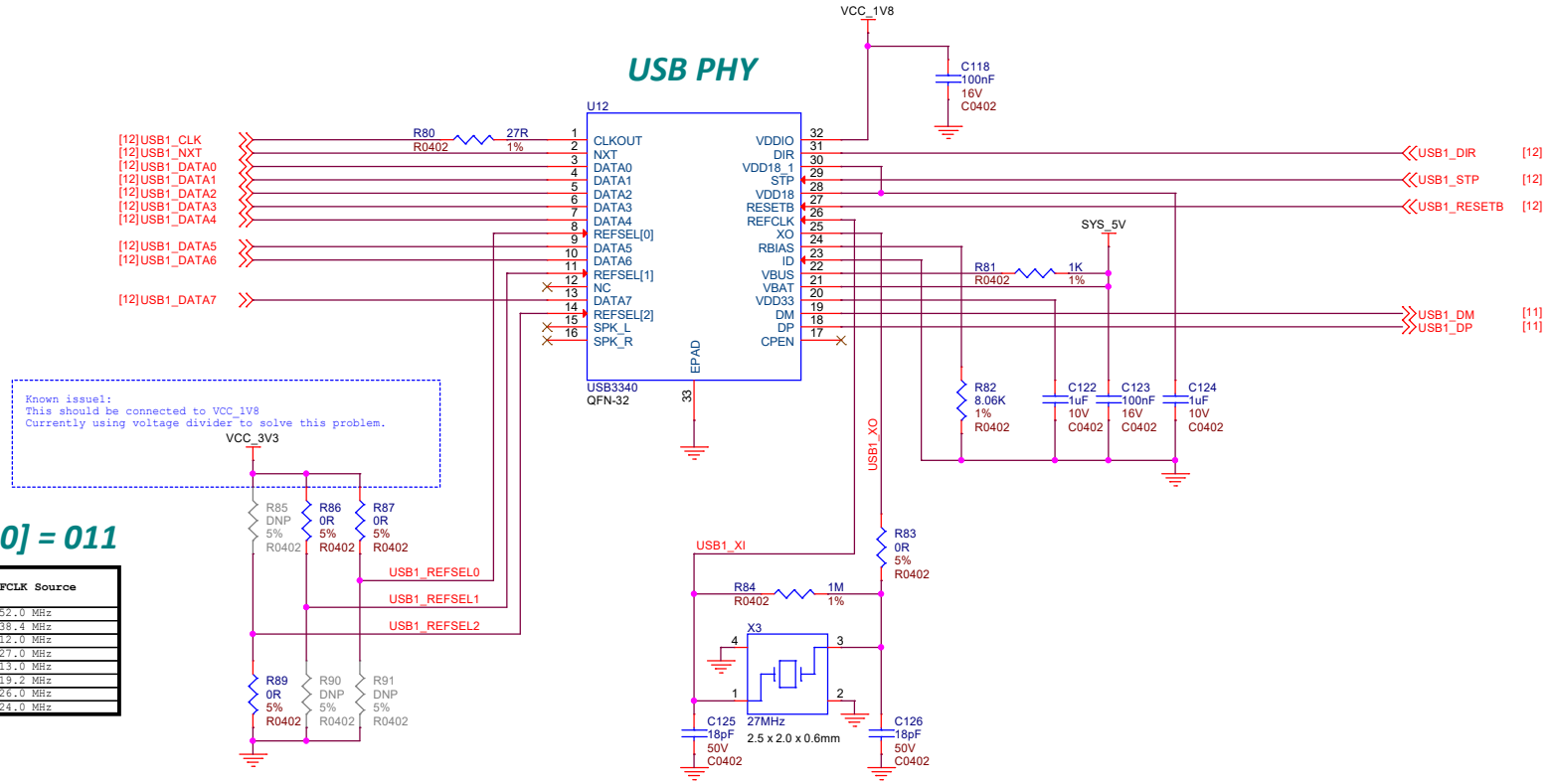


MAIN

seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: Beagleboard FPGA	
Size: A3	Document Number: 09_USB OTG TYPE C	Rev: v0.1
Draw By: Xiangnan	Date: Monday, August 23, 2021	Sheet: 9 of 17

USB HOST/ADC

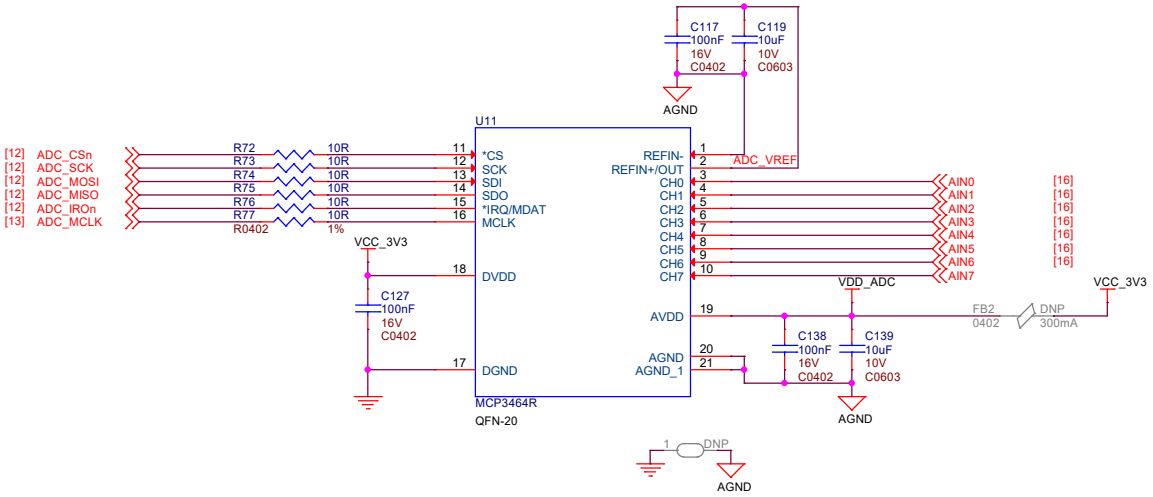
USB PHY



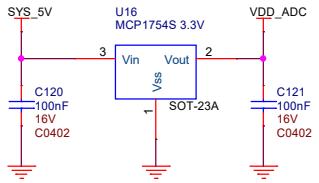
REFCLK[2:0] = 011

REFSEL[2:0]	REFCLK Source
000	52.0 MHz
001	38.4 MHz
010	12.0 MHz
011	27.0 MHz
100	13.0 MHz
101	19.2 MHz
110	26.0 MHz
111	24.0 MHz

16-bit Delta-Sigma ADC



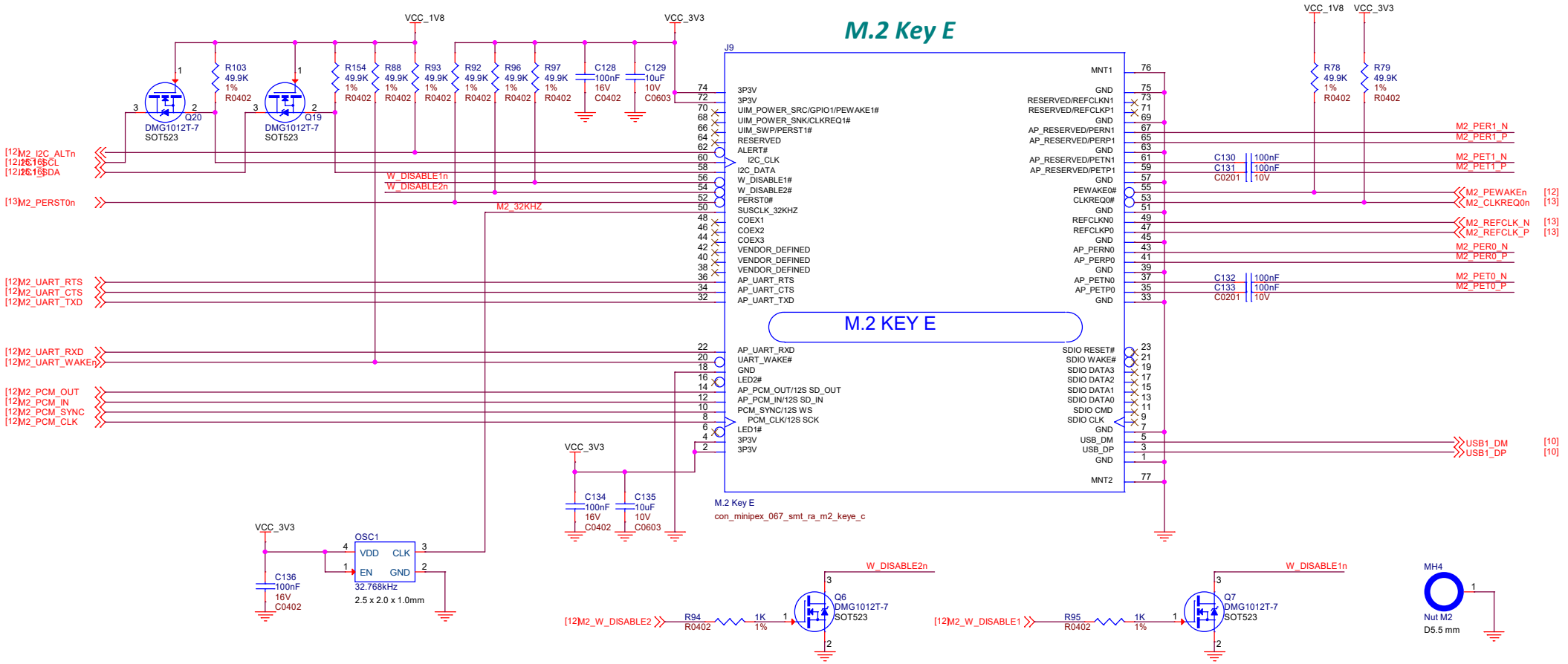
High PSRR LDO



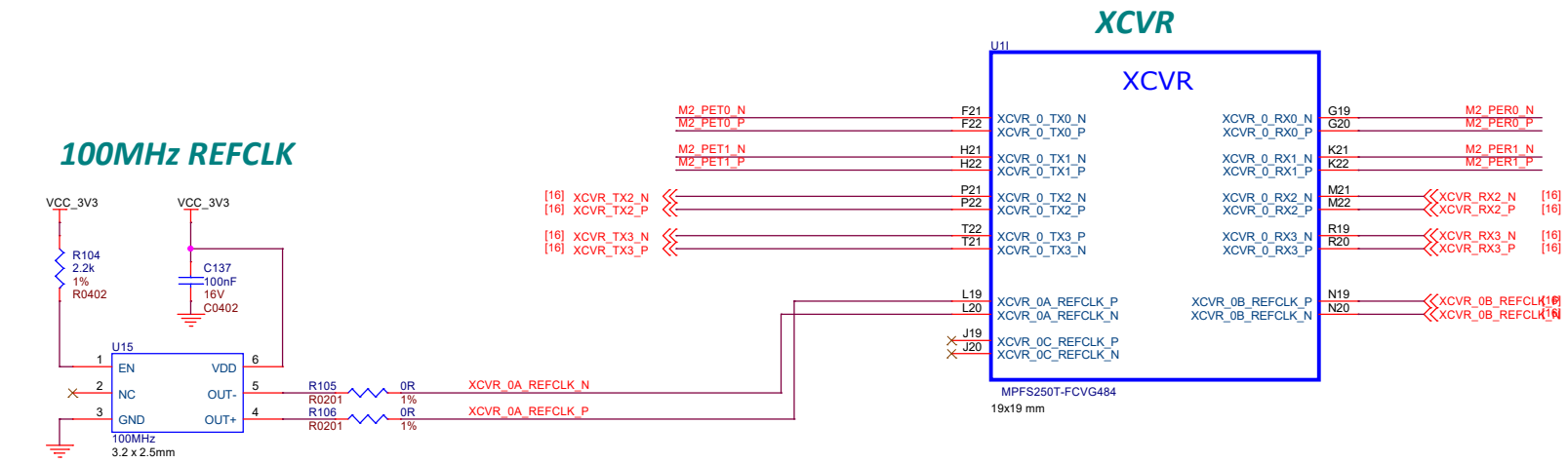
MAIN

seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: Beagleboard FPGA	
Size: A3	Document Number: 10_USB HOST/ADC	Rev: v0.1
Draw By: Xiangnan	Date: Saturday, September 18, 2021	Sheet: 10 of 17

M.2 Key E/XCVR



XCVR

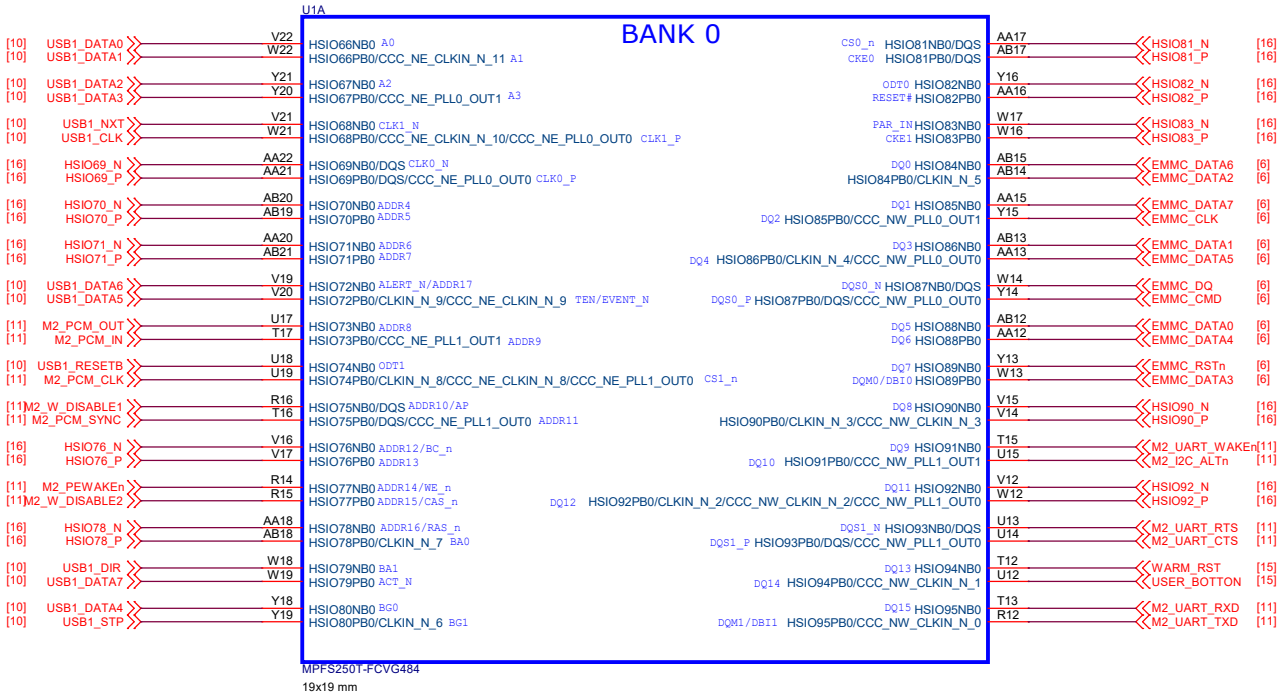


MAIN

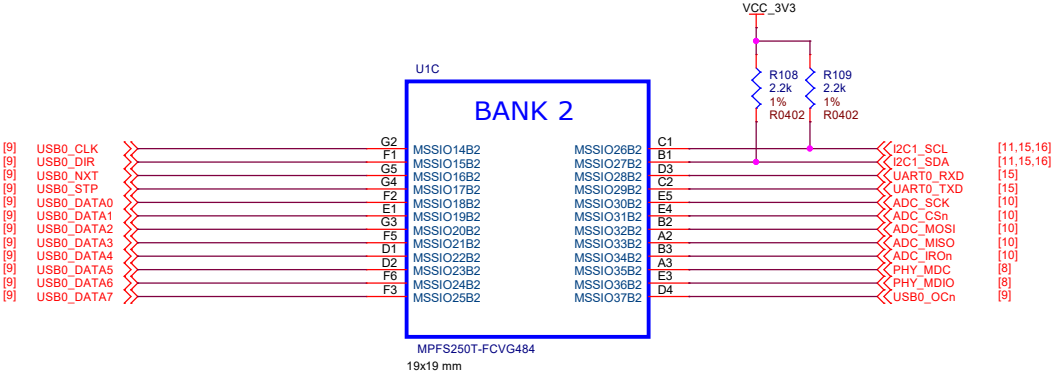
seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: Beagleboard FPGA	
Size: A3	Document Number: 11_M.2 Key E/XCVR	Rev: v0.1
Draw By: Xiangnan	Date: Monday, August 23, 2021	Sheet: 11 of 17

SoC Back0/Bank2

BANK0 HSIO 1.8V



BANK2 MSSIO 3.3V



MAIN

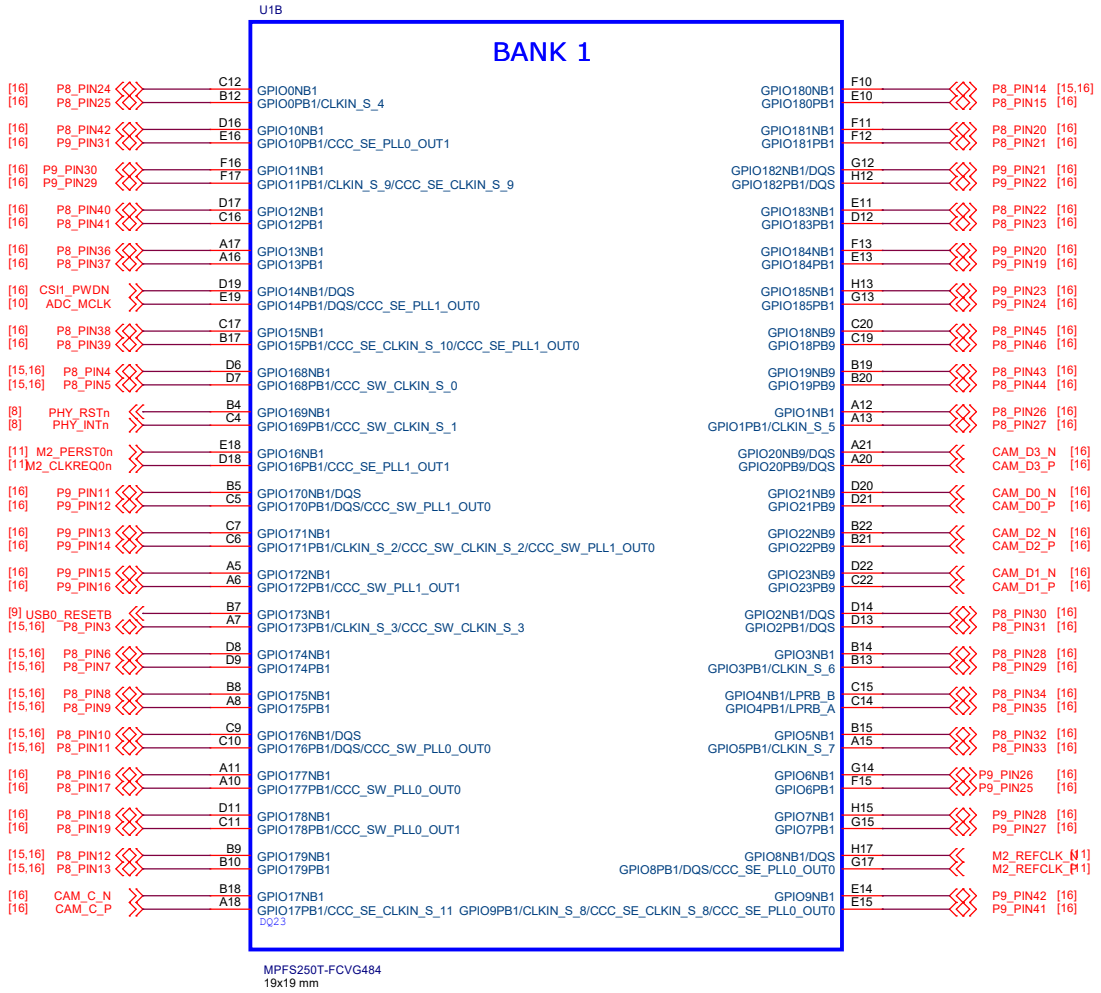
https://www.seeedstudio.com

Title: Beagleboard FPGA

Size:	Document Number:	Rev:
A3	12_SoC BANK0/BANK2	v0.1

Draw By:	Date:	Sheet:
Xiangnan	Monday, August 23, 2021	12 of 17

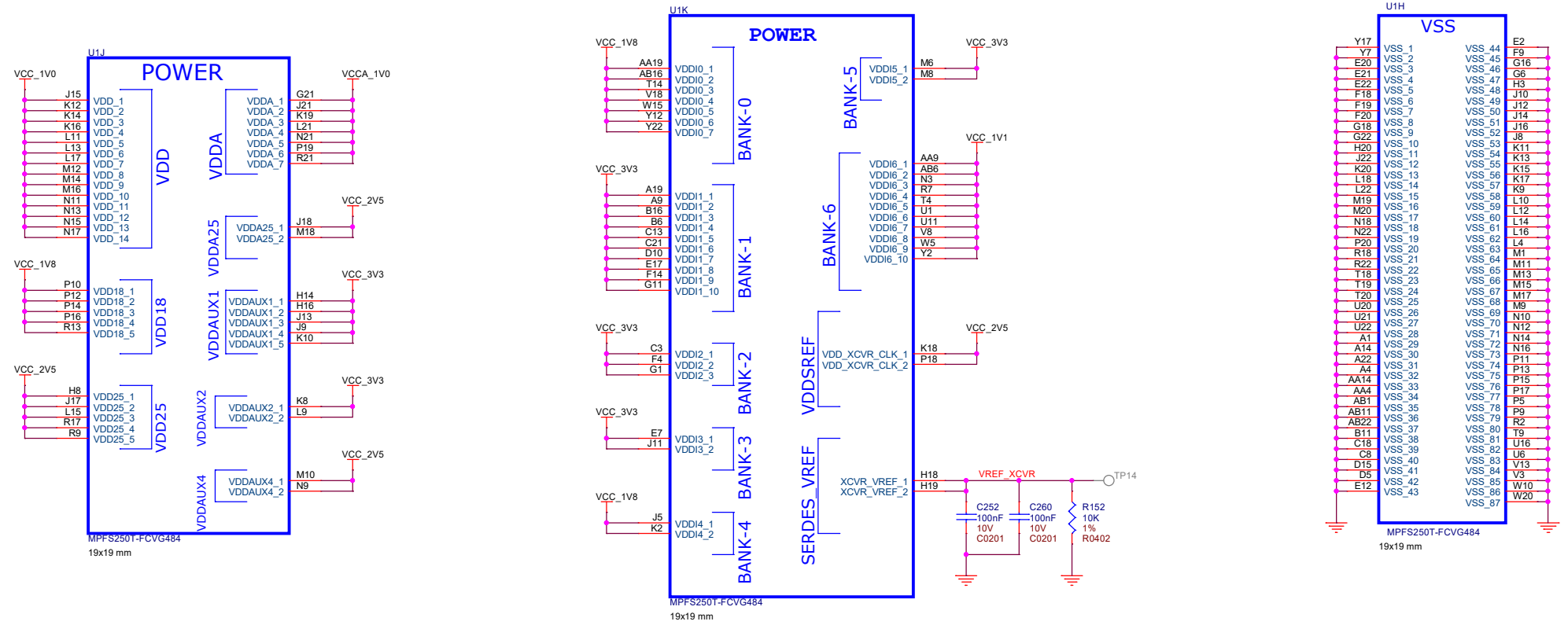
SoC BANK1

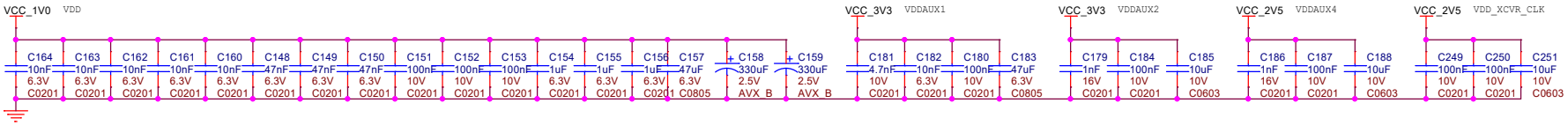


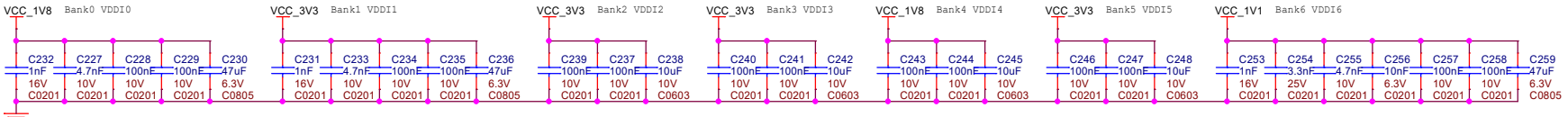
MAIN

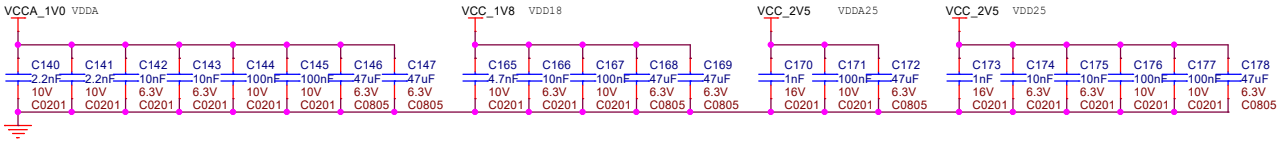
seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: Beagleboard FPGA	
Size: A3	Document Number: 13_SoC BANK1	Rev: v0.1
Draw By: Xiangnan	Date: Monday, August 23, 2021	Sheet: 13 of 17

SoC Power





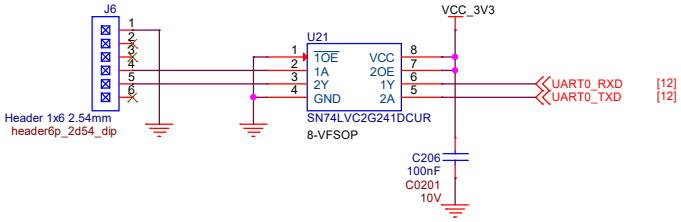




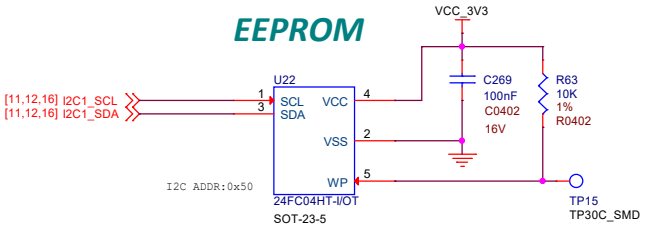
MAIN

seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: Beagleboard FPGA	
Size: A3	Document Number: 14_SoC Power	Rev: v0.1
Draw By: Xiangnan	Date: Monday, August 23, 2021	Sheet: 14 of 17

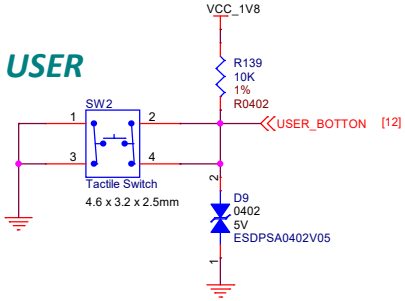
Debug



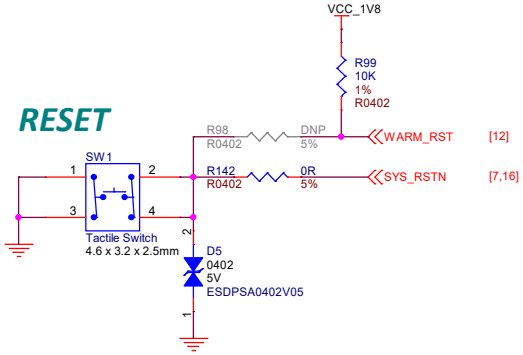
EEPROM



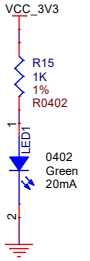
USER



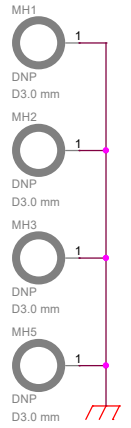
RESET



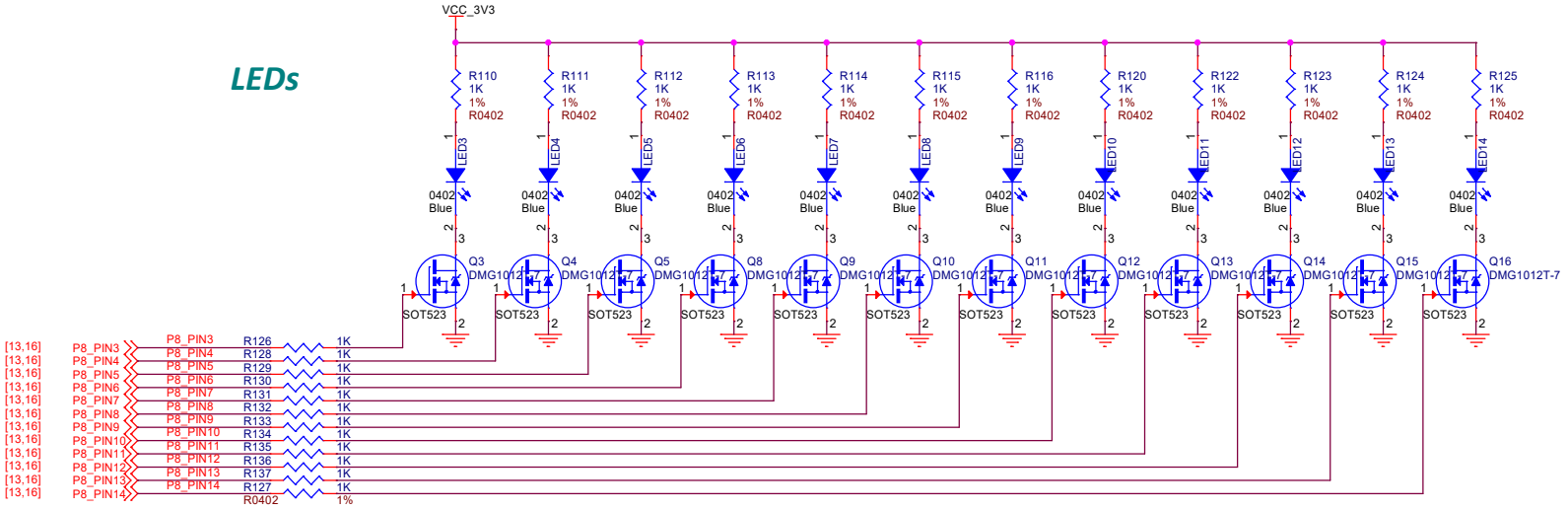
Power LED



MHoles



LEDs



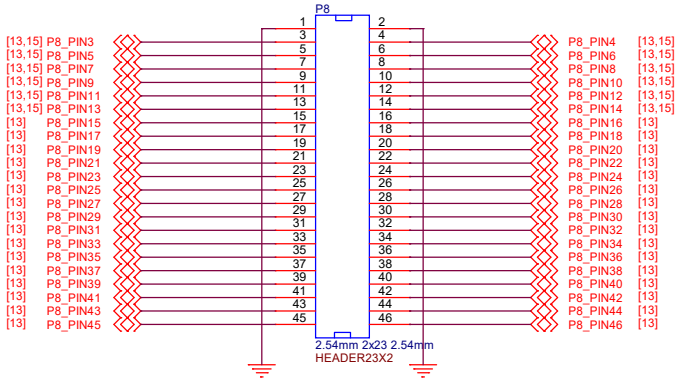
MAIN

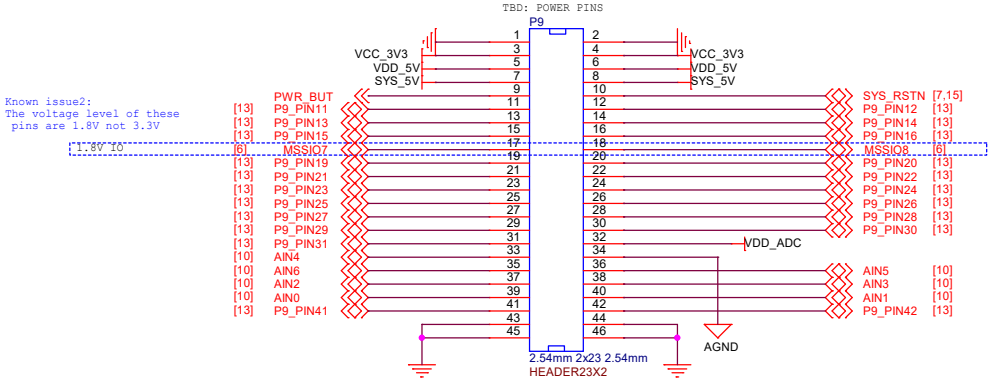
seeed The IoT Hardware Enabler

https://www.seeedstudio.com

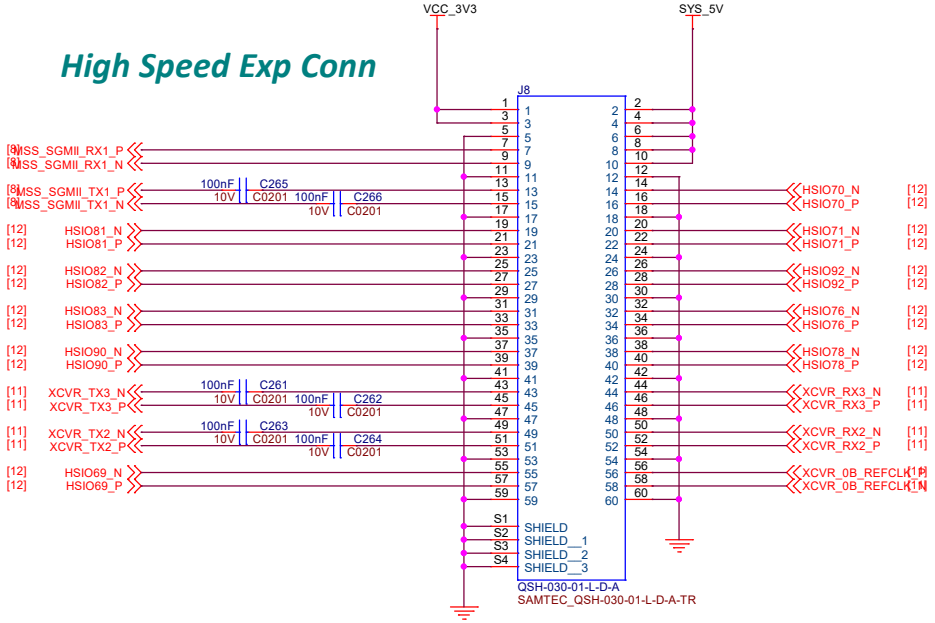
Title: Beagleboard FPGA		
Size: A3	Document Number: 15_MISC	Rev: v0.1
Draw By: Xiangnan	Date: Tuesday, August 24, 2021	Sheet: 15 of 17

BeagleBoard Header

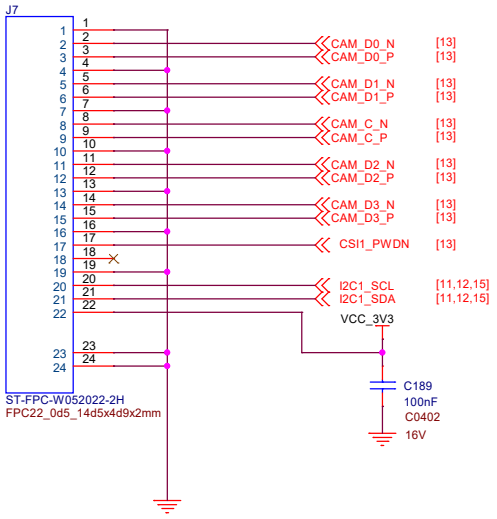




High Speed Exp Conn



MIPI CSI



MAIN

seeed The IoT Hardware Enabler	https://www.seeedstudio.com	
	Title: Beagleboard FPGA	
Size: A3	Document Number: 16_Exp Conn	Rev: v0.1
Draw By: Xiangnan	Date: Saturday, September 18, 2021	Sheet: 16 of 17