Schematic: Expansion Accessory

SHEET	SHEET NAME
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08	JTAG/SPI Flash
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Revision History

DATE	REVISION	DESCRIPTION
May. 21 2021	v0.1	1. Initial
Aug. 19 2022	v0.2	1.Change MPU From MPFS250 to MPFS025. 2.Change Ethernet PHY From TI_DP83867CSRGZ to Realtek_RTL8211FS-CG. 3.Change High Speed Connector to QSH-020-01-F-D-DP-A. 4.P8,P9,CSI and High Speed Connector Some Pins Re-assignment. 5.SD Card is connected to the same SPI bus as the ADC. 6.Change User Button and Reset Signals GPIO. 7.Connect eMMC directly to MSS eMMC controller . 8.Change J4 to LPJG0933H11NL. 9.Change LPDDR4 to Samsung_K4F6E3S4HM-MGCJ. 10.Add the GPIO Expander Microchip_MCP23008-E/ML to expand GPIO.
Aug. 26 2022	v0.2	1.Change High Speed Connector signal type to Transceiver Port 4lanes. 2.Move XCVR_RX1/TX1 from M.2 Connector to High Speed Connector. 3.Add the XCVR_0C_REFCLK Signals to High Speed Connector P2C_CLK. 4.Add the HSIO73P/N Signals to High Speed Connector C2P_CLK. 5.Change the R171 vaule from 10K to 49.9K_1%. 6.Remove GPIO Expander and use some HSIO with level shift (U34,U35) to fill the lack pin of P8. 7.Add B0_HSIO76N Signal to P9_PIN9. 8.Configure P9_PIN19,PIN20 as IIC signals, and connect to High Speed Connector. 9.Change M2_W_DISABLE1 to HSIO74P. 10.Remove the PCM from M.2 Connector. 11.The schematic version number does not change, and it is v0.2.
Sep.01 2022	v0.2	1.Page5: Add High Speed Connector VIO Power Circuit and Use HSIO76N to enable the VIO Power. 2.Remove P9_PWR_BUT Signal. 3.The schematic version number does not change, and it is v0.2.
Sep.022 2022	v0.2	1.Page16:Change CSI Connector to 0.5K-DX-22PWB. 2.Page12:Change PCIE REFCLK of M2 connector to Synchronized clock. 3.The schematic version number does not change, and it is v0.2.
Sep.01 2023	Rev A	1.Page5:Add Overvoltage and Reverse polarity protection circuit to J1. 2.Page11:Add Some series resistance 100R to U11_CH0-6. 3.Page17:Change the XCVR1-3 Signals to meet PCIe requirements. 4.PChange PCB color to Red.

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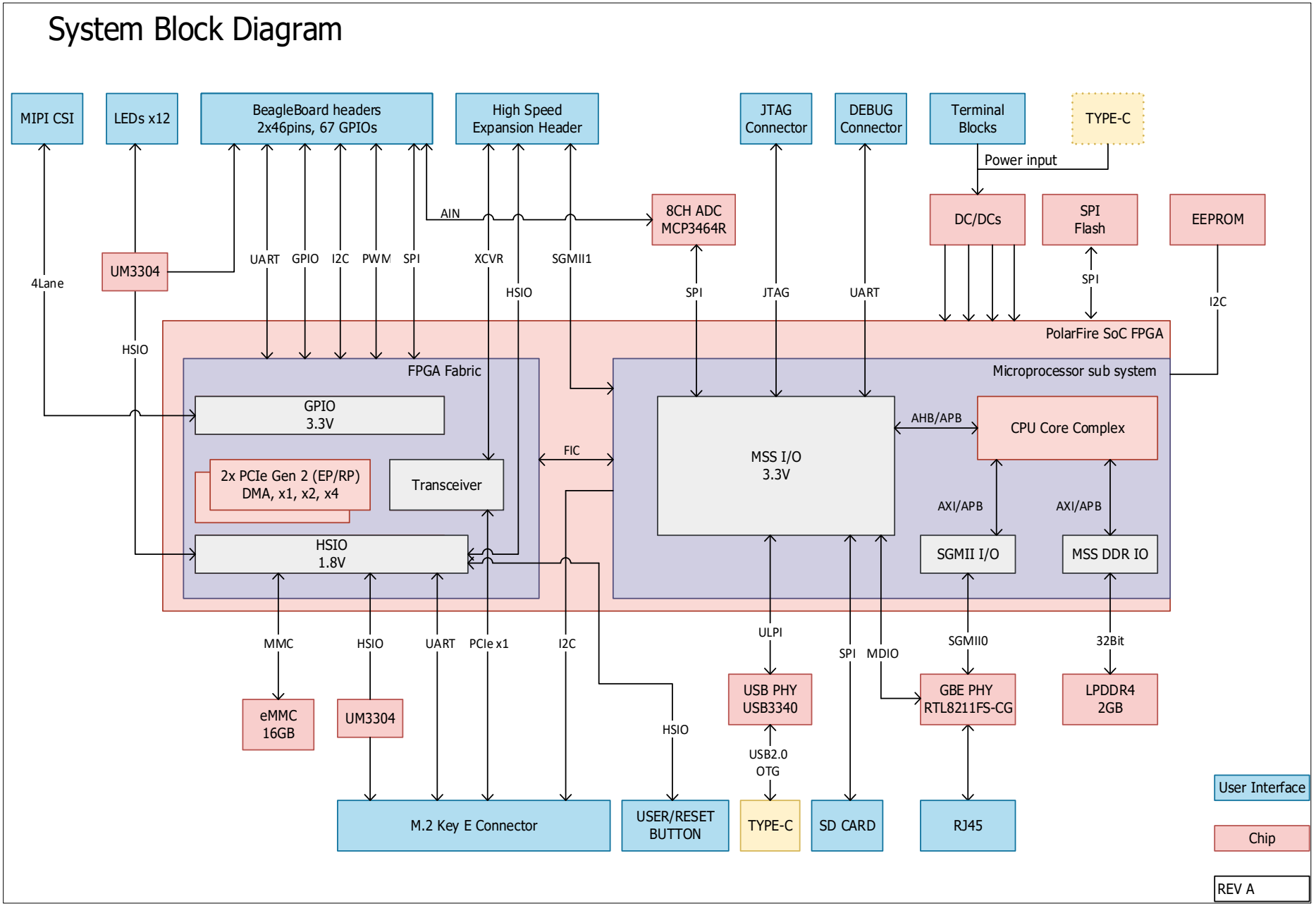
Title: BeagleV-Fire

Size: A3	Document Number: 01_Title/Revision History	Rev: V0.2
Draw By: JN.FUONG	Date: Monday, October 09, 2023	Sheet: 1 of 17

System Block Diagram



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	Title: BeagleV-Fire	
Size: A3	Document Number: 02_System Block Diagram	Rev: V0.2
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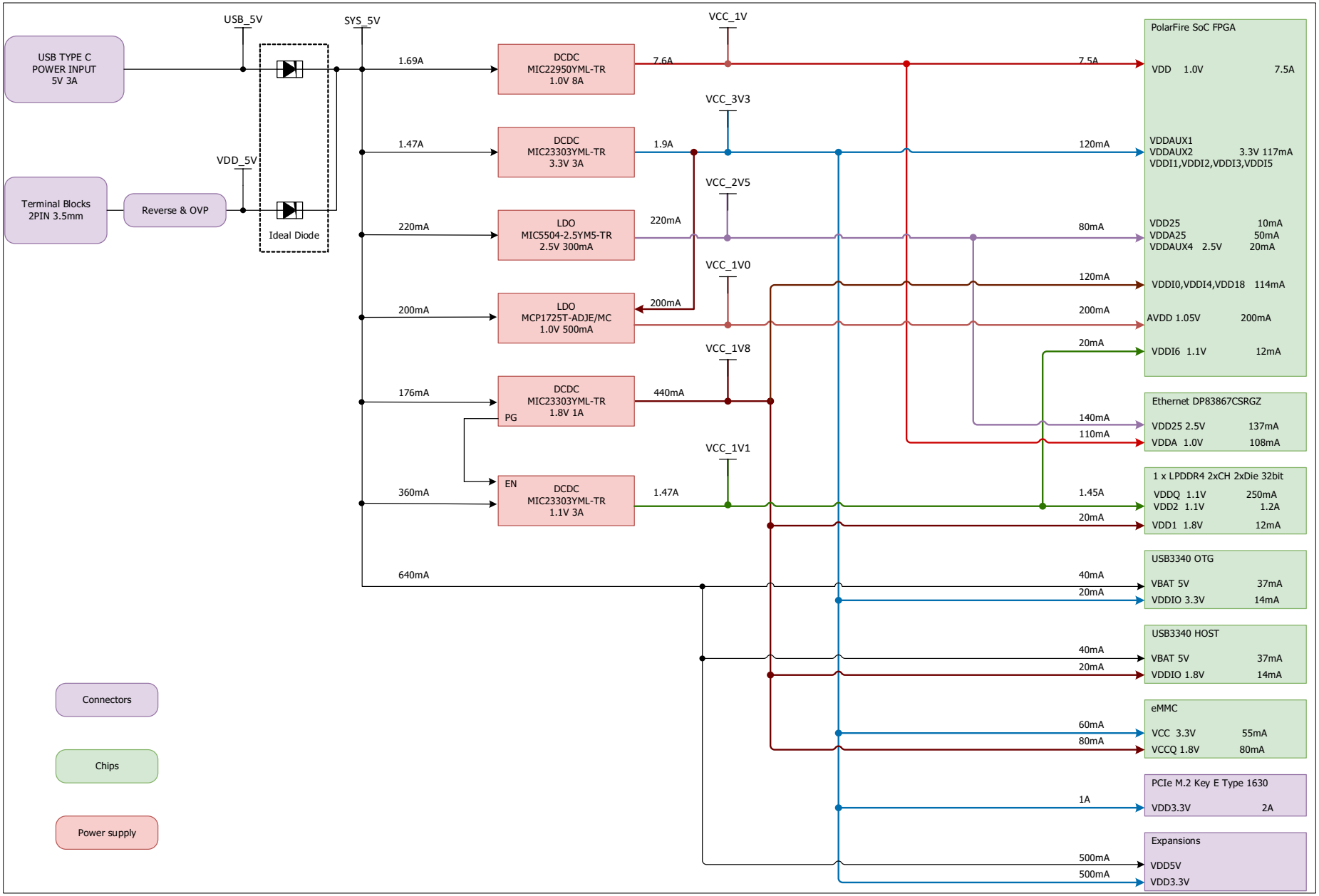
Power Tree Diagram



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	Title: BeagleV-Fire	
Size: A3	Document Number: 03_Power Tree Diagram	Rev: V0.2
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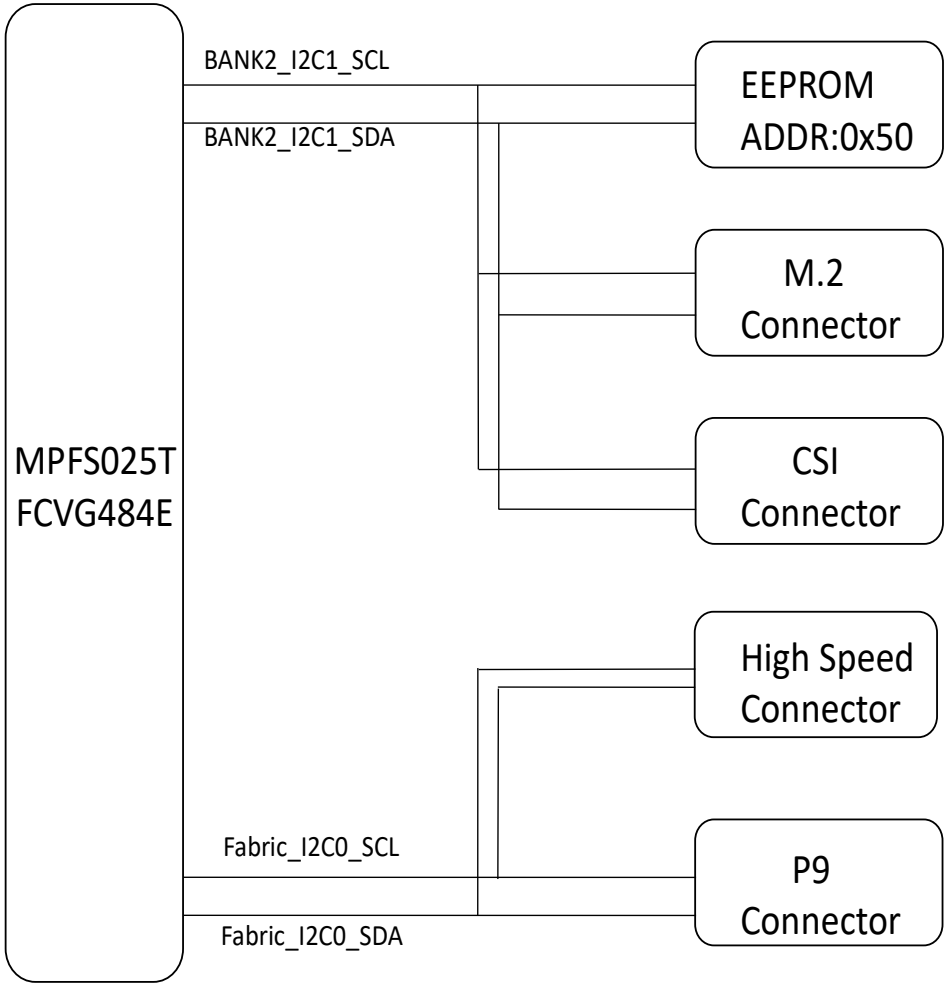
IIC Tree Diagram



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Size: A3	Document Number: 04_IIC Tree	Rev: V0.2
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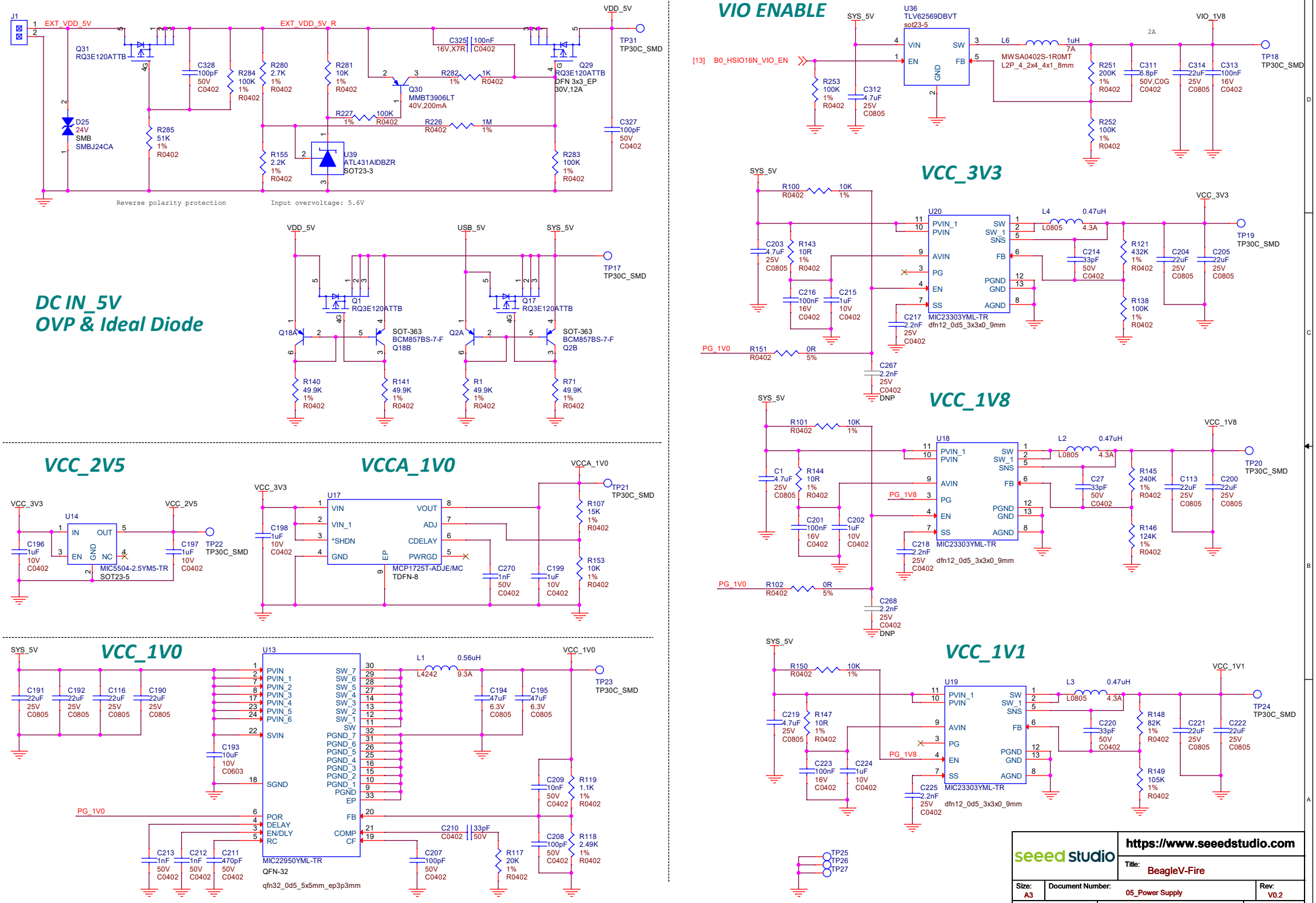
DC IN_5V
OVP & Ideal Diode
VIO ENABLE
VCC_3V3
VCC_2V5
VCCA_1V0
VCC_1V8
VCC_1V0
VCC_1V1
Reverse polarity protection
Input overvoltage: 5.6V
MIC22950YML-TR
QFN-32
qfn32_0d5_5x5mm_ep3p3mm
MIC23303YML-TR
dfn12_0d5_3x3x0_9mm
MCP1725T-ADJE/MC
TDFN-8
MIC5504-2.5YM5-TR
SOT23-5
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Title: BeagleV-Fire
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Document Number: 05_Power Supply
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Date: Monday, October 09, 2023
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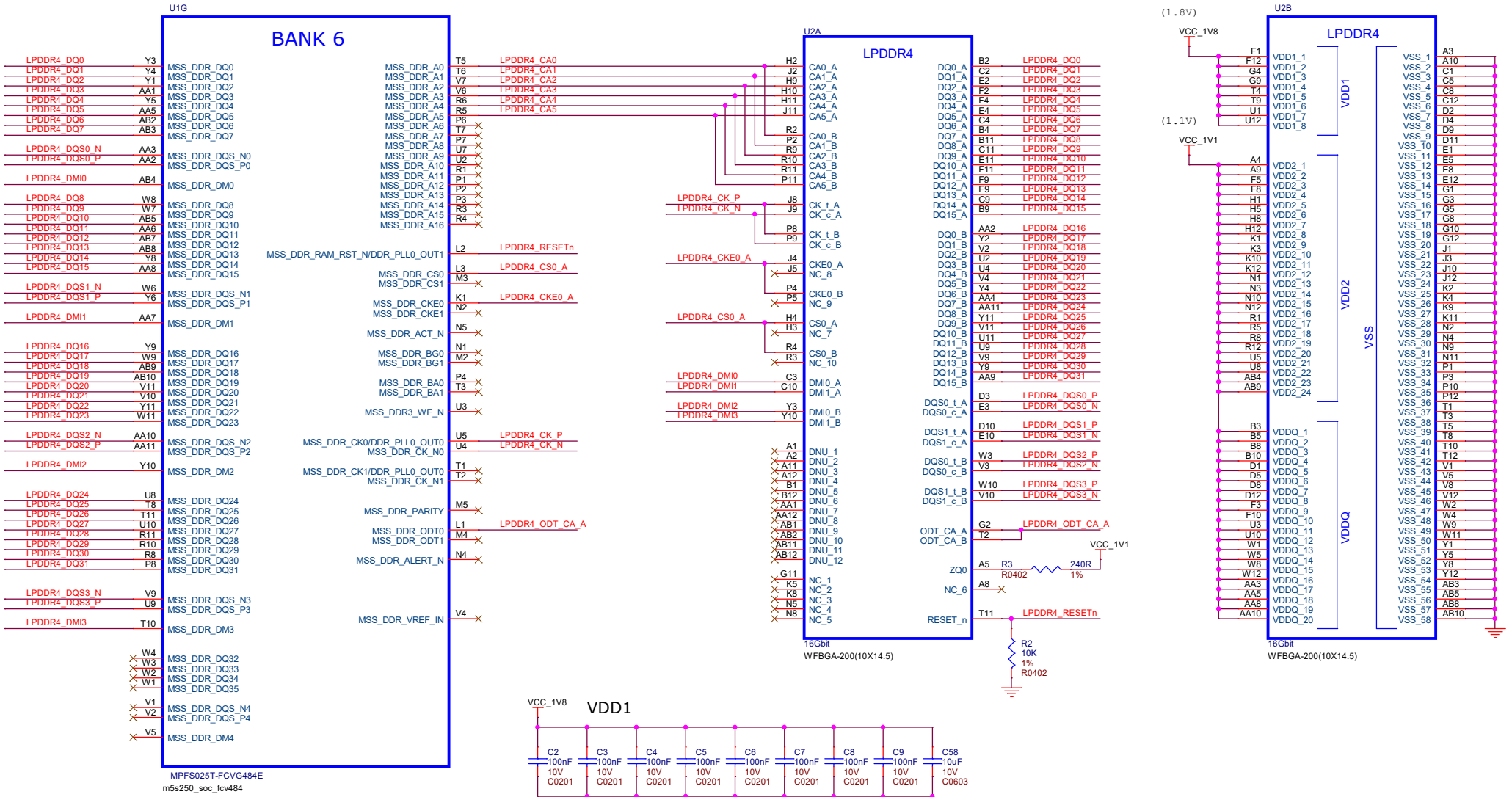
LPDDR4_CONNECTION



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Title: BeagleV-Fire		
Size: A3	Document Number: 06_LPDDR4	Rev: V0.2
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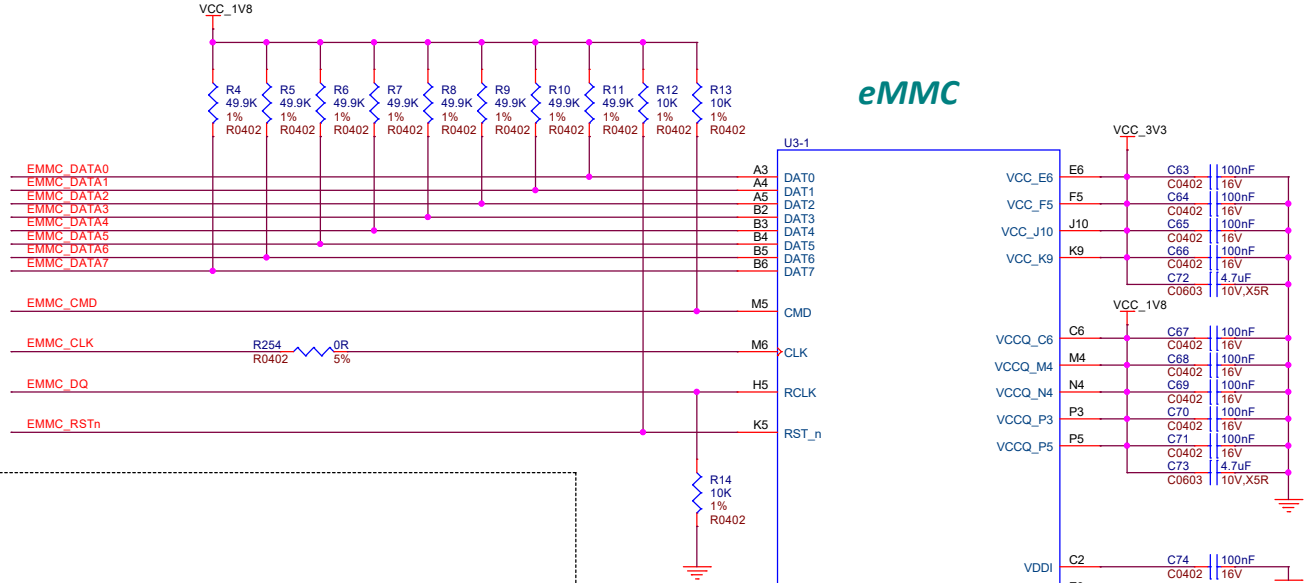
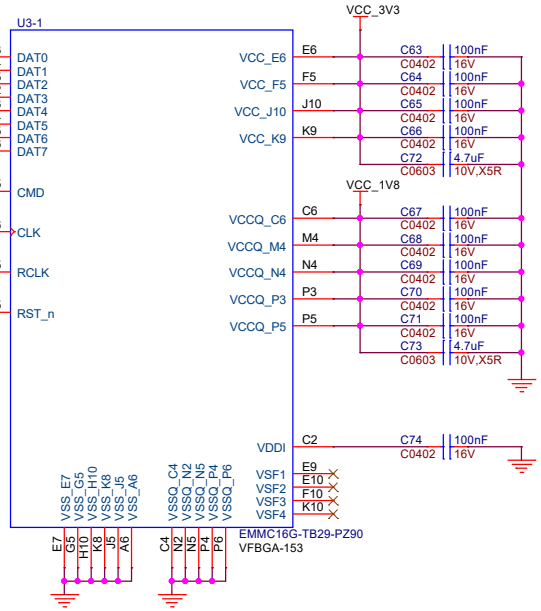
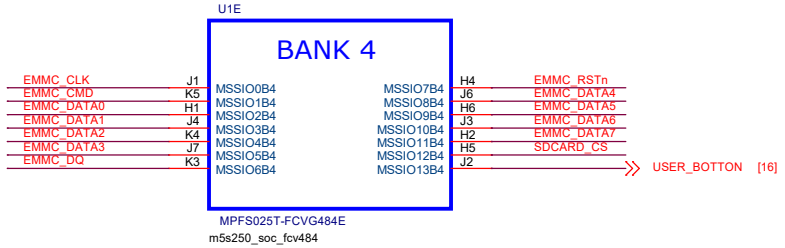
eMMC/SD

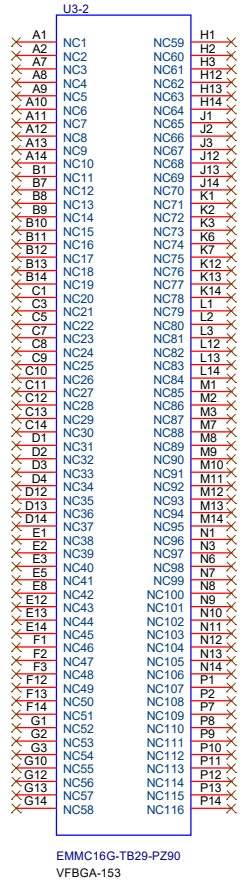


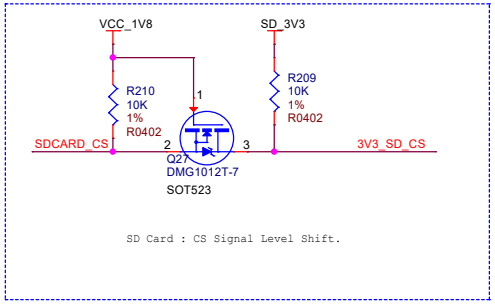
eMMC

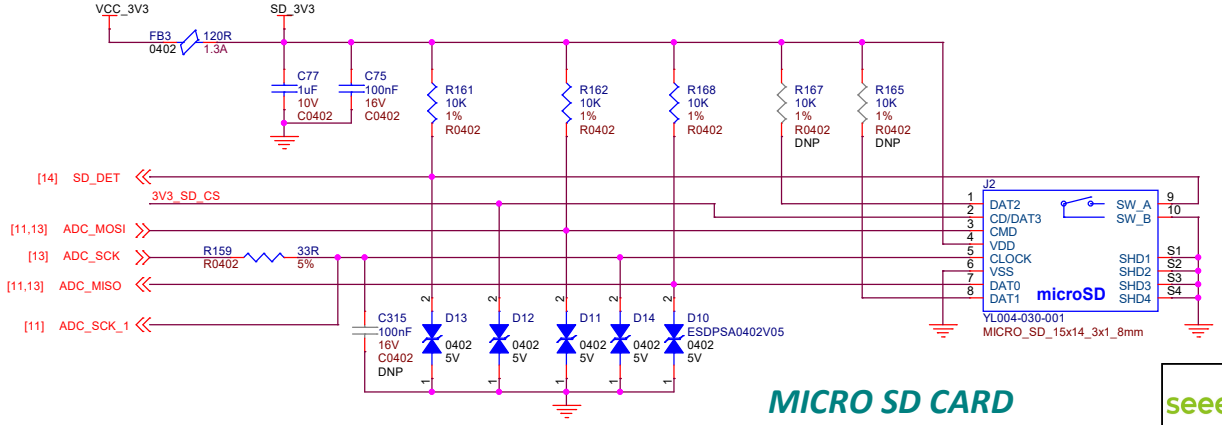


BANK4 1.8V









MICRO SD CARD

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	Title: BeagleV-Fire	
Size: A3	Document Number: 07_eMMC/SD	Rev: V0.2
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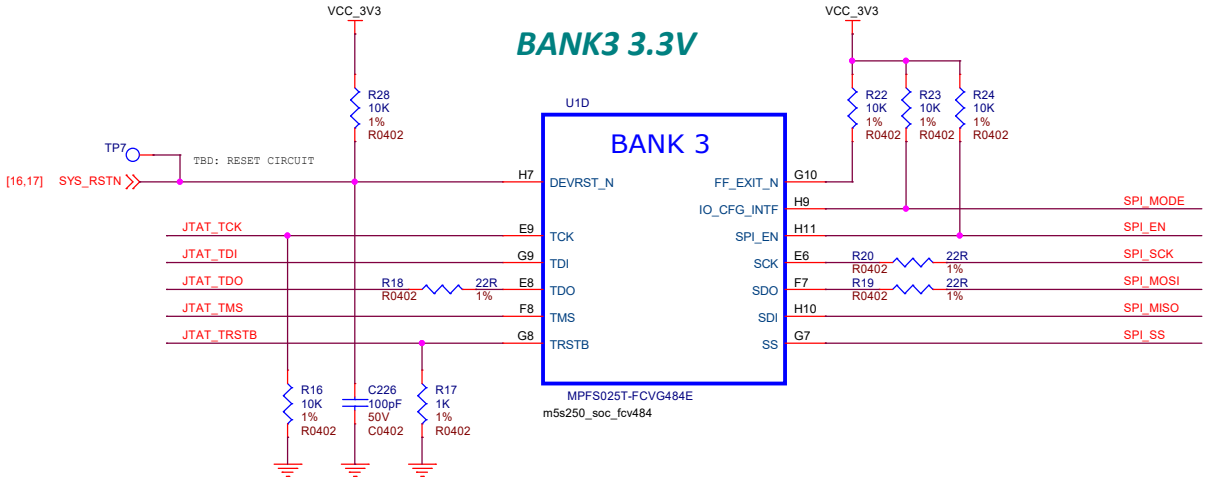
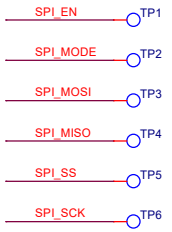
JTAG/SPI Flash

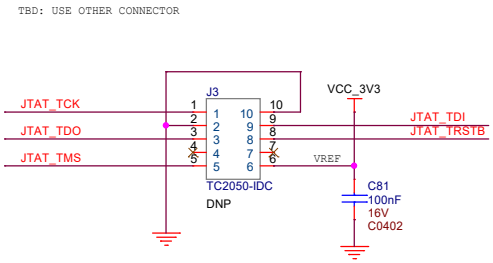
BANK3 3.3V



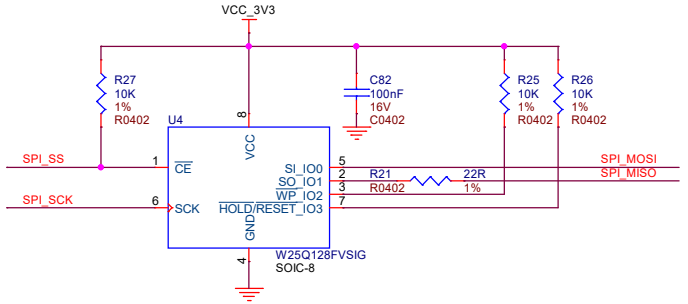
Programming the SPI Flash Using External Master



JTAG for Tag-Connect cable



SPI Flash



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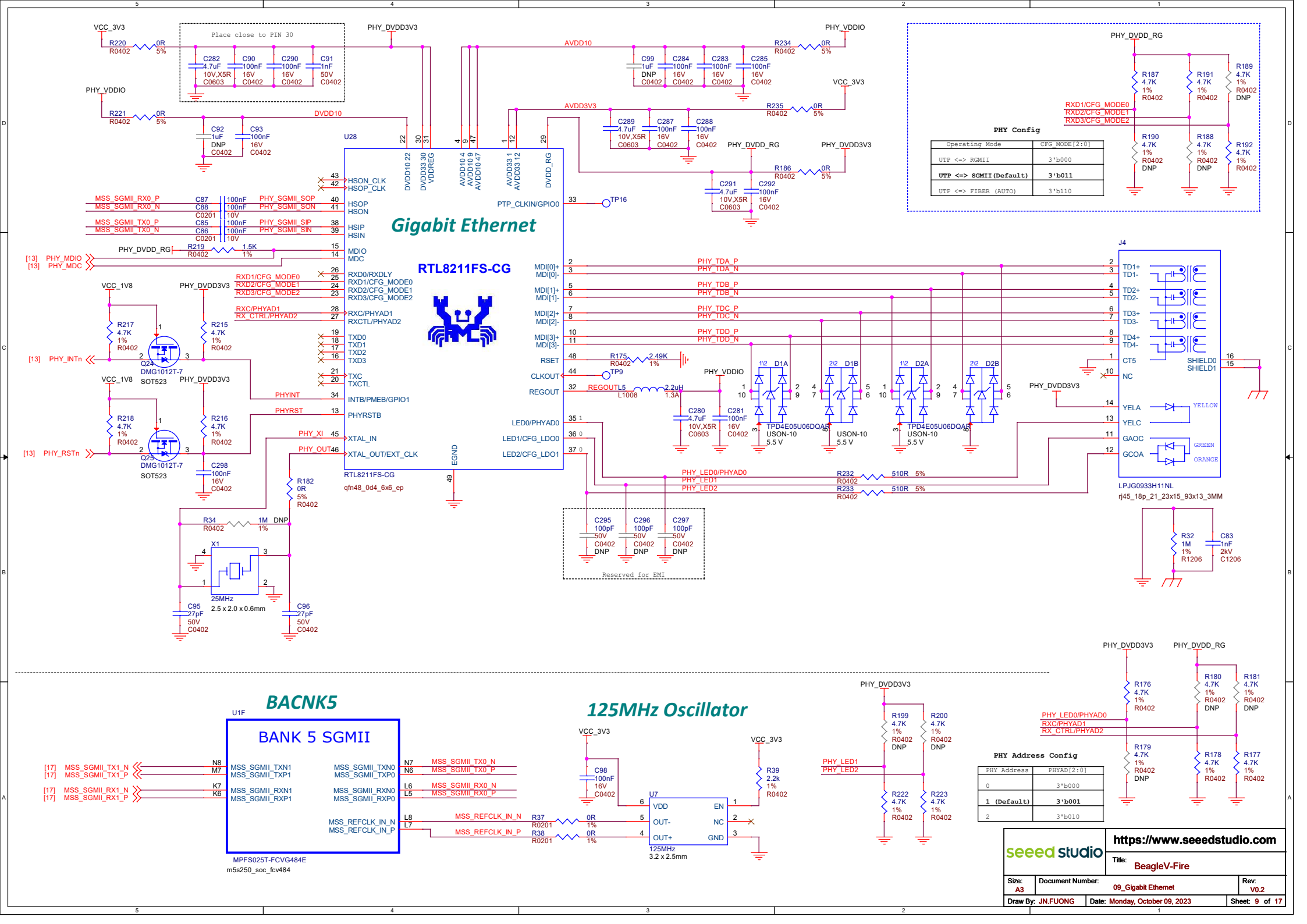
	Title: BeagleV-Fire	
Size: A3	Document Number: 08_JTAG/SPI Flash	Rev: V0.2
Draw By: JN.FUONG	Date: Monday, October 09, 2023	Sheet: 8 of 17


Gigabit Ethernet
RTL8211FS-CG
BACNK5
125MHz Oscillator
PHY Config
PHY Address Config
U28
U1F
U7
J4
BANK 5 SGMII
MPFS025T-FCVG484E
m5s250_soc_fcv484
RTL8211FS-CG
qfn48_0d4_6x6_ep
LPJG0933H11NL
rj45_18p_21_23x15_93x13_3MM
Reserved for EMI
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https://www.seeedstudio.com
Title: BeagleV-Fire
Size: A3
Document Number: 09_Gigabit Ethernet
Rev: V0.2
Draw By: JN.FUONG
Date: Monday, October 09, 2023
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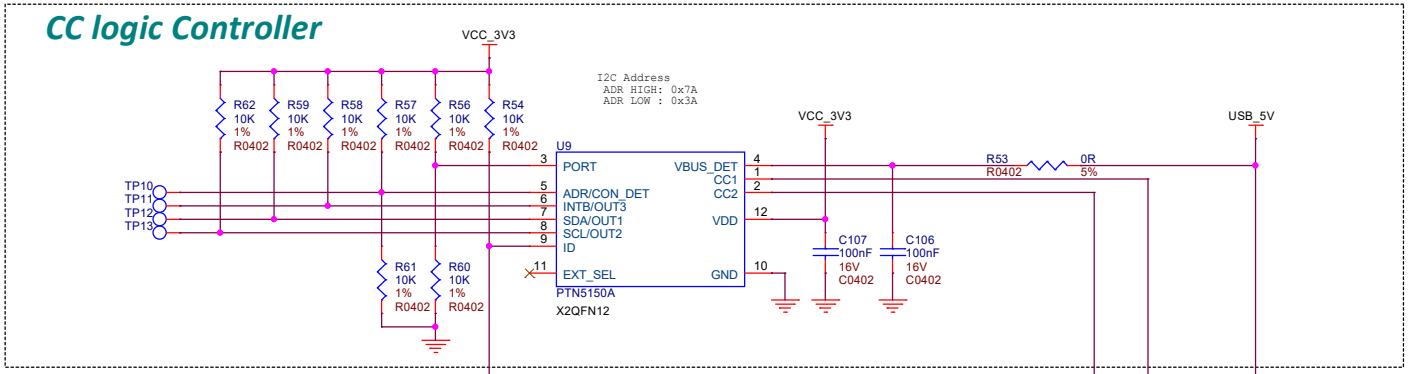
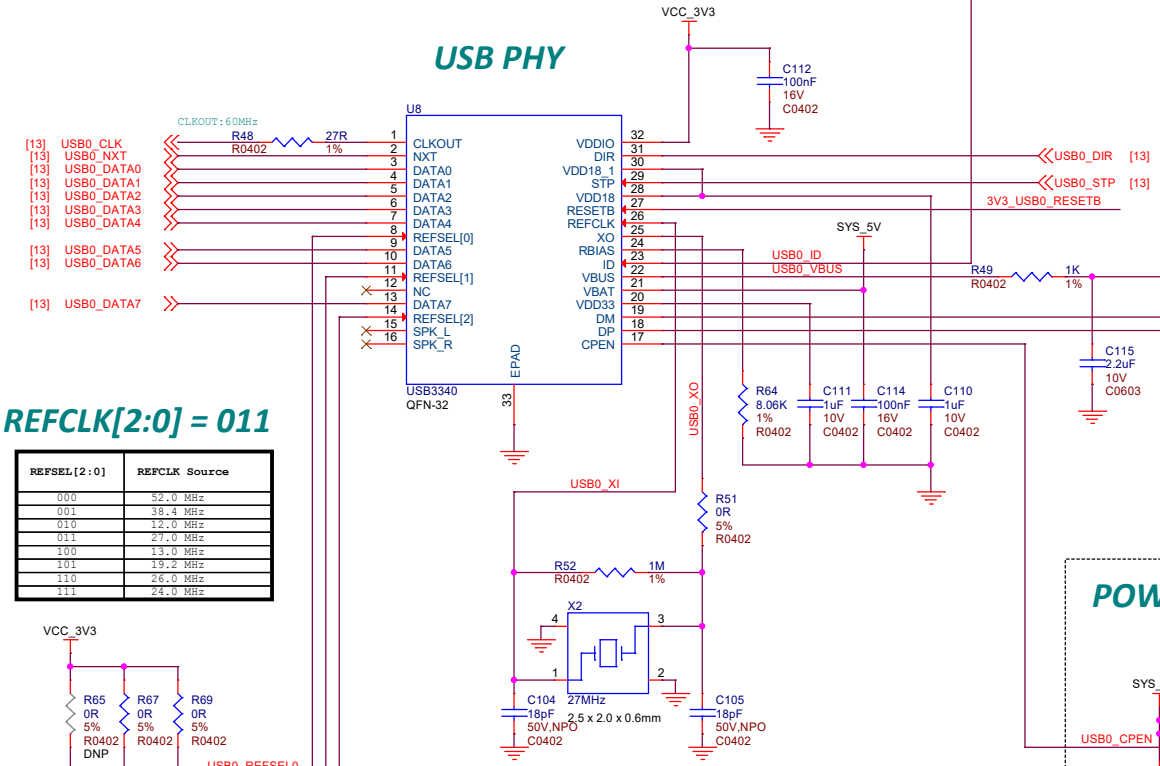
USB OTG

CC logic Controller

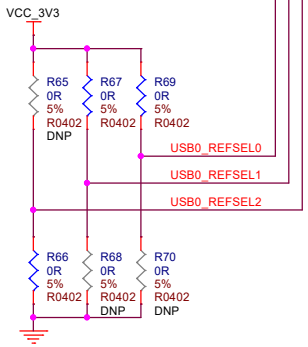


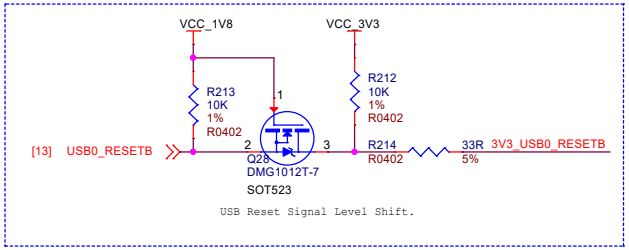
USB PHY



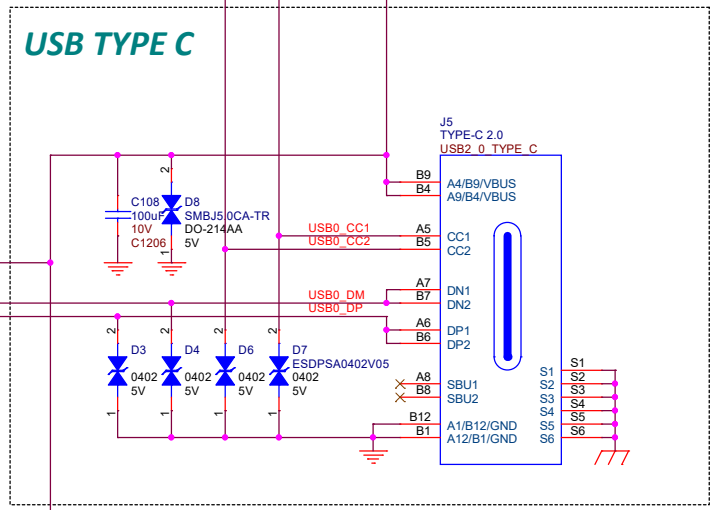
REFCLK[2:0] = 011

REFSEL[2:0]	REFCLK Source
000	52.0 MHz
001	38.4 MHz
010	12.0 MHz
011	27.0 MHz
100	13.0 MHz
101	19.2 MHz
110	26.0 MHz
111	24.0 MHz

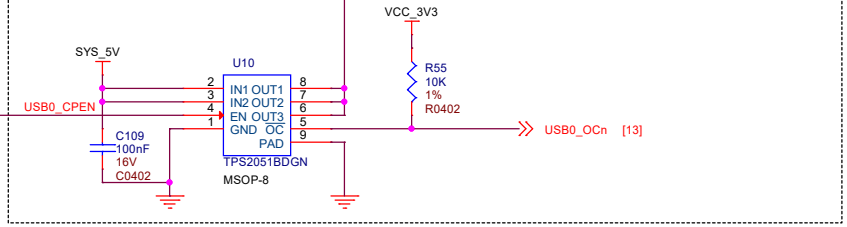




USB TYPE C



POWER SWITCH



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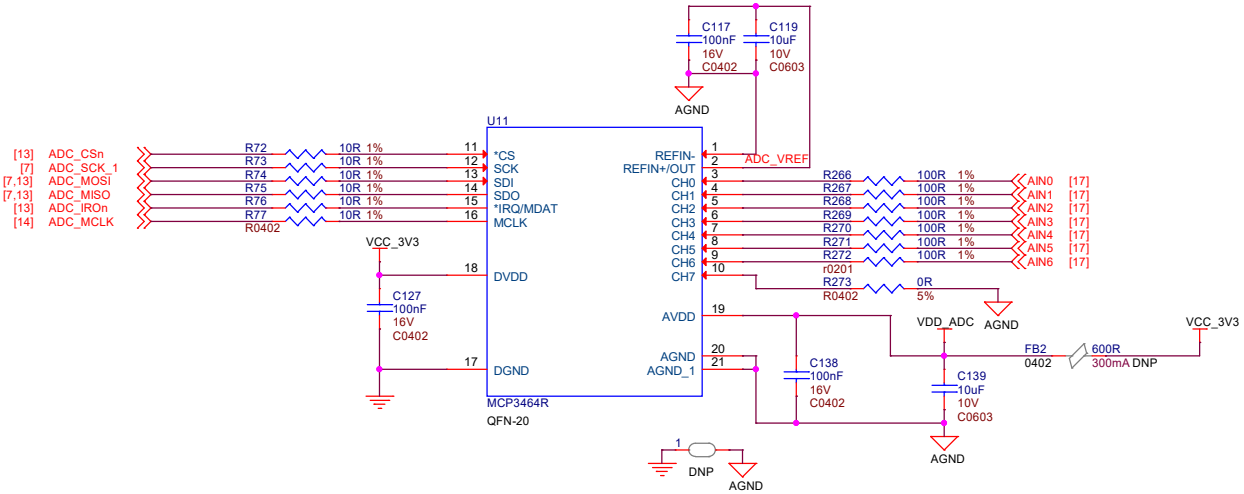
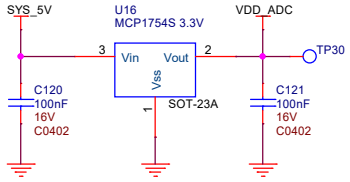
	Title: BeagleV-Fire		
Size: A3	Document Number: 10_USB OTG TYPE C		Rev: V0.2
Draw By: JN.FUONG	Date: Monday, October 09, 2023	Sheet: 10 of 17	

16-bit Delta-Sigma ADC



High PSRR LDO



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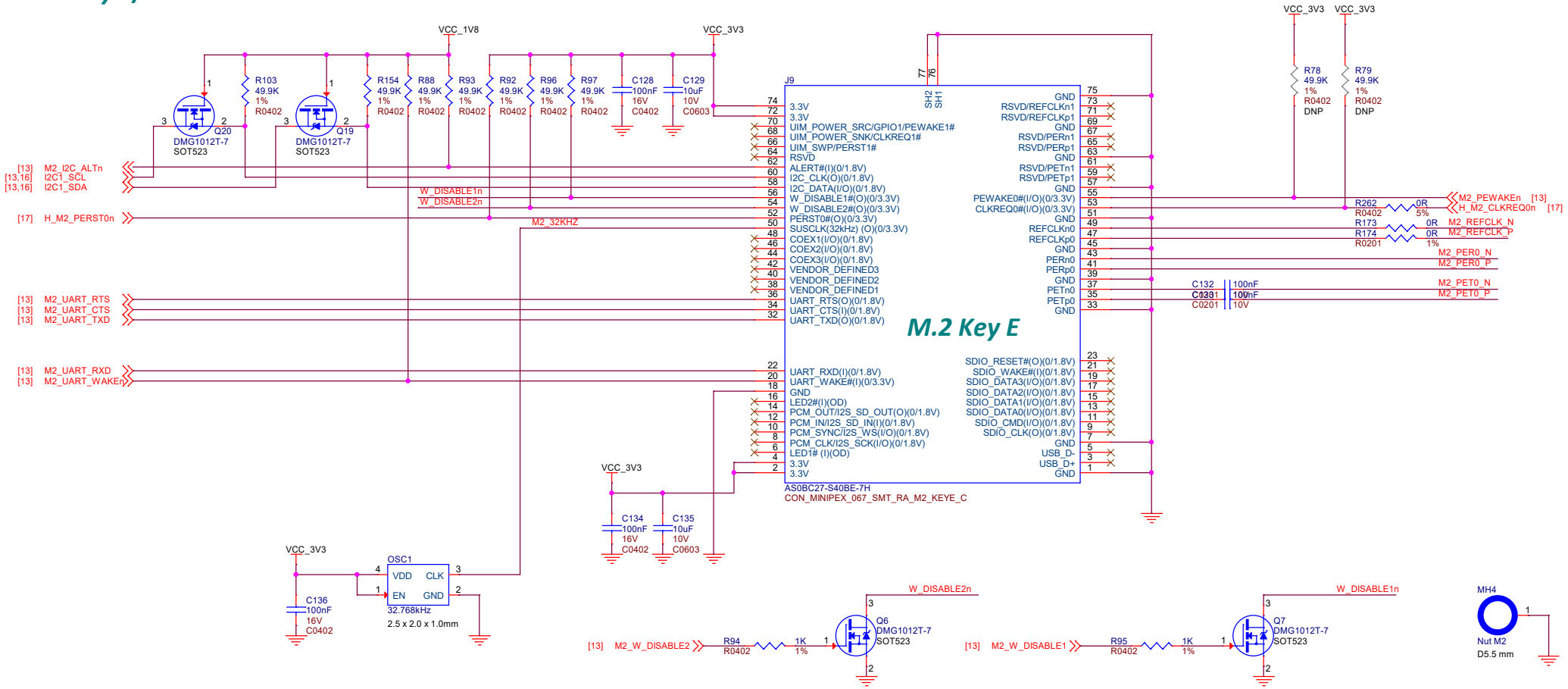
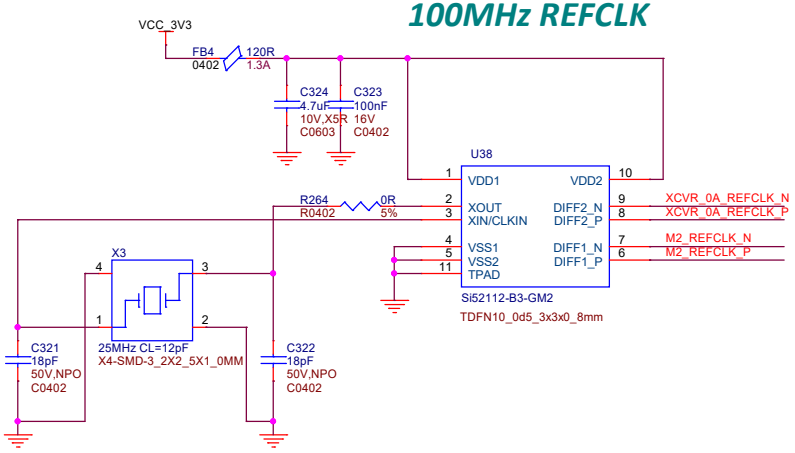
	Title: BeagleV-Fire	
Size: A3	Document Number: 11_ADC	Rev: V0.2
Draw By: JN.FUONG	Date: Monday, October 09, 2023	Sheet: 11 of 17

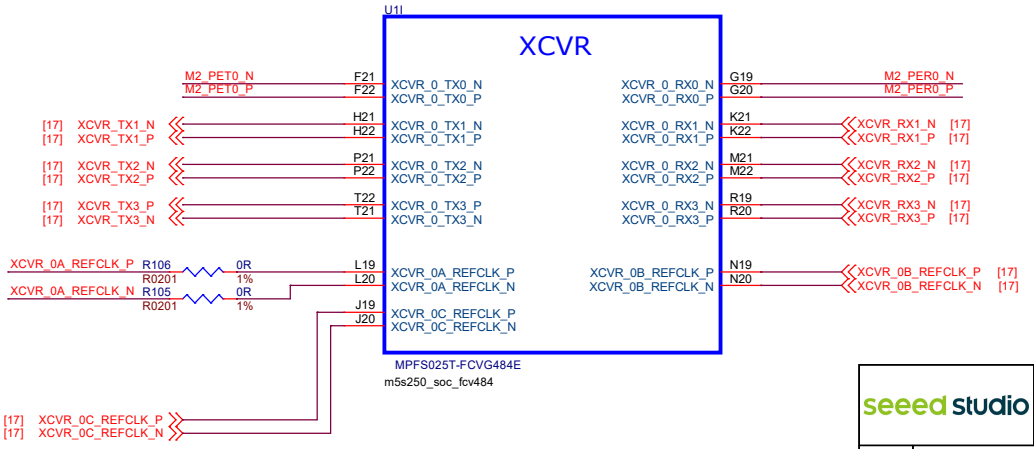
M.2 Key E/XCVR



100MHz REFCLK



XCVR



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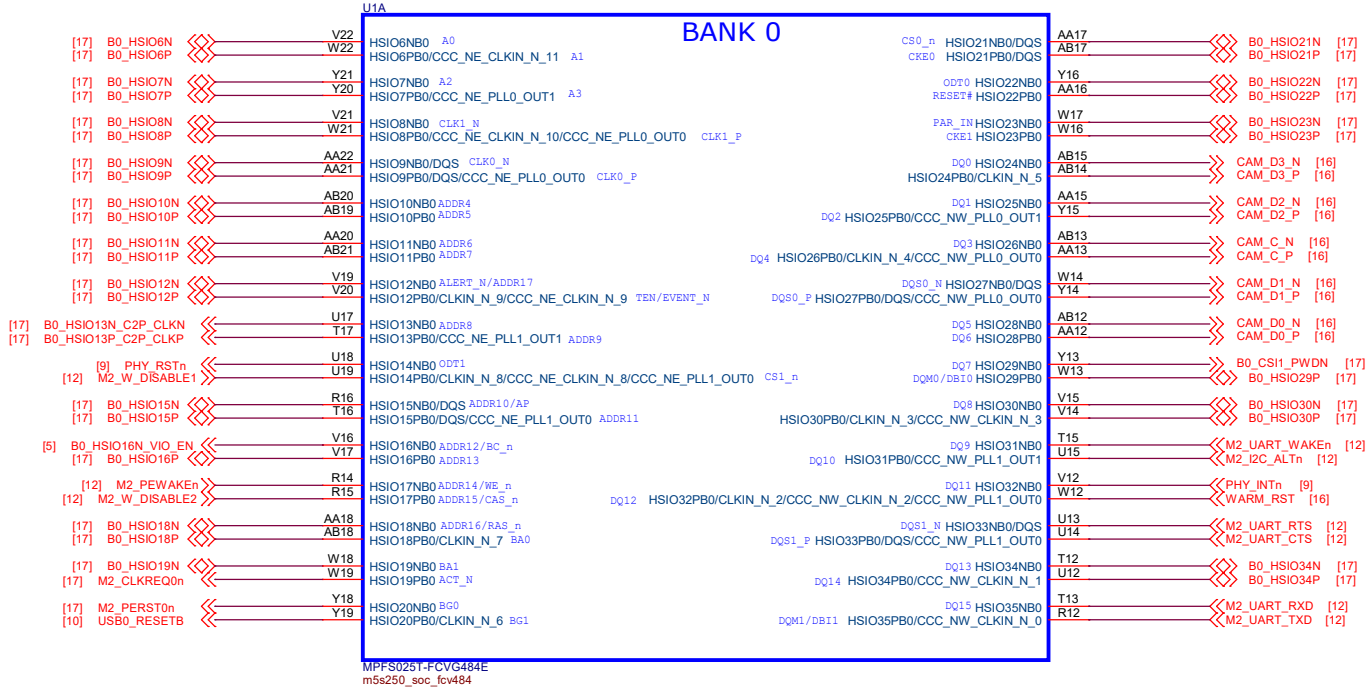
Title: BeagleV-Fire

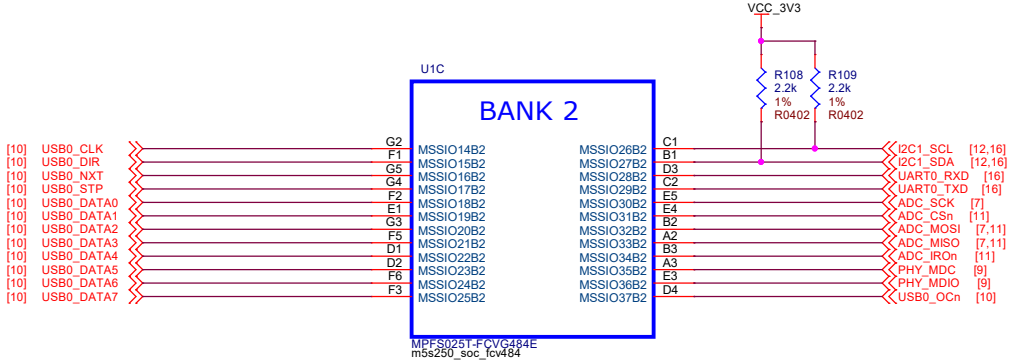
Size: A3	Document Number: 12_M.2 Key E/XCVR	Rev: V0.2
Draw By: JN.FUONG	Date: Monday, October 09, 2023	Sheet: 12 of 17

SoC Back0/Bank2

BANK0 HSIO 1.8V



BANK2 MSSIO 3.3V



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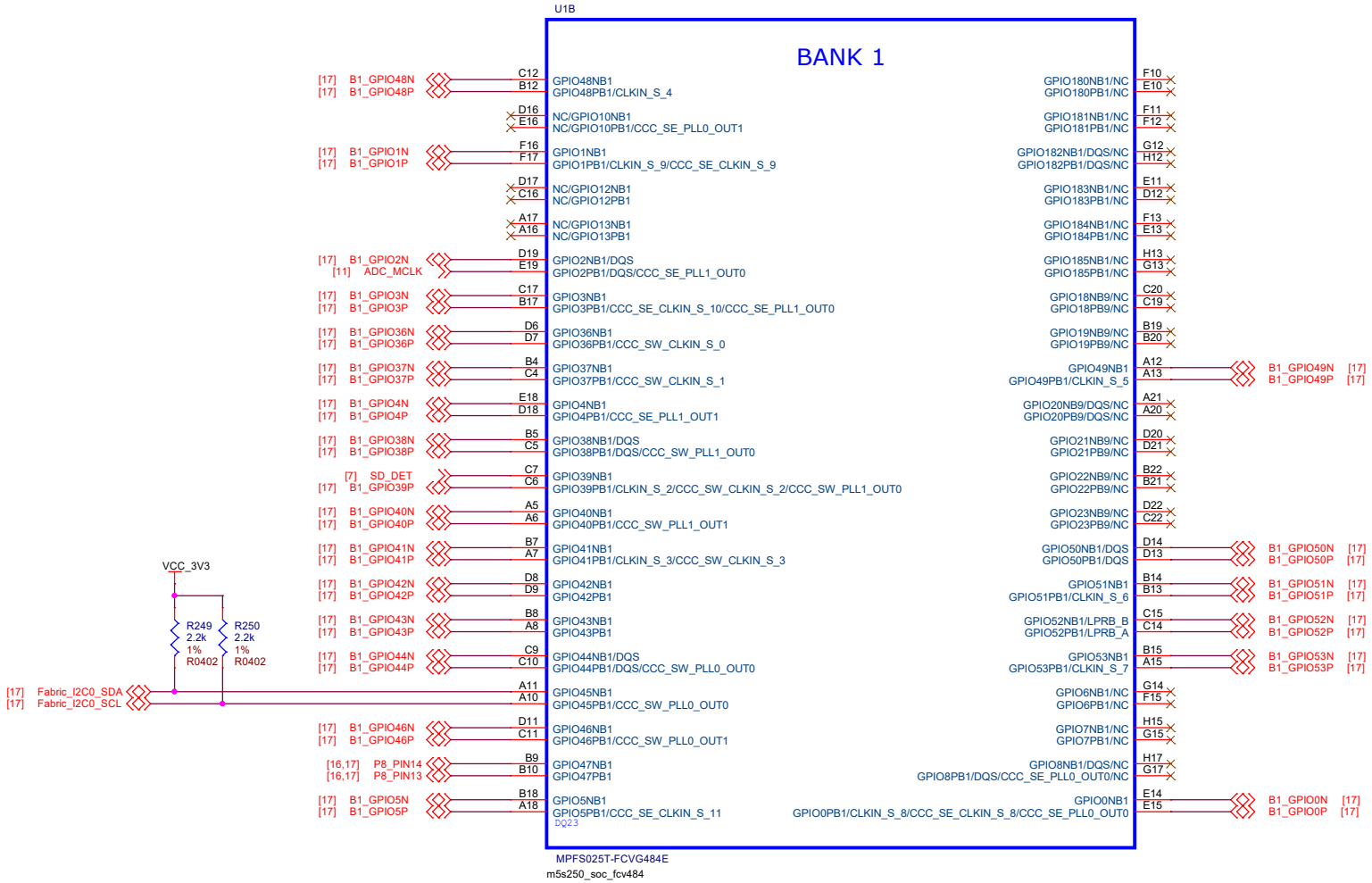
	Title: BeagleV-Fire		
Size: A3	Document Number: 13_SoC BANK0/BANK2		Rev: V0.2
Draw By: JN.FUONG	Date: Monday, October 09, 2023		Sheet: 13 of 17

SoC BANK1



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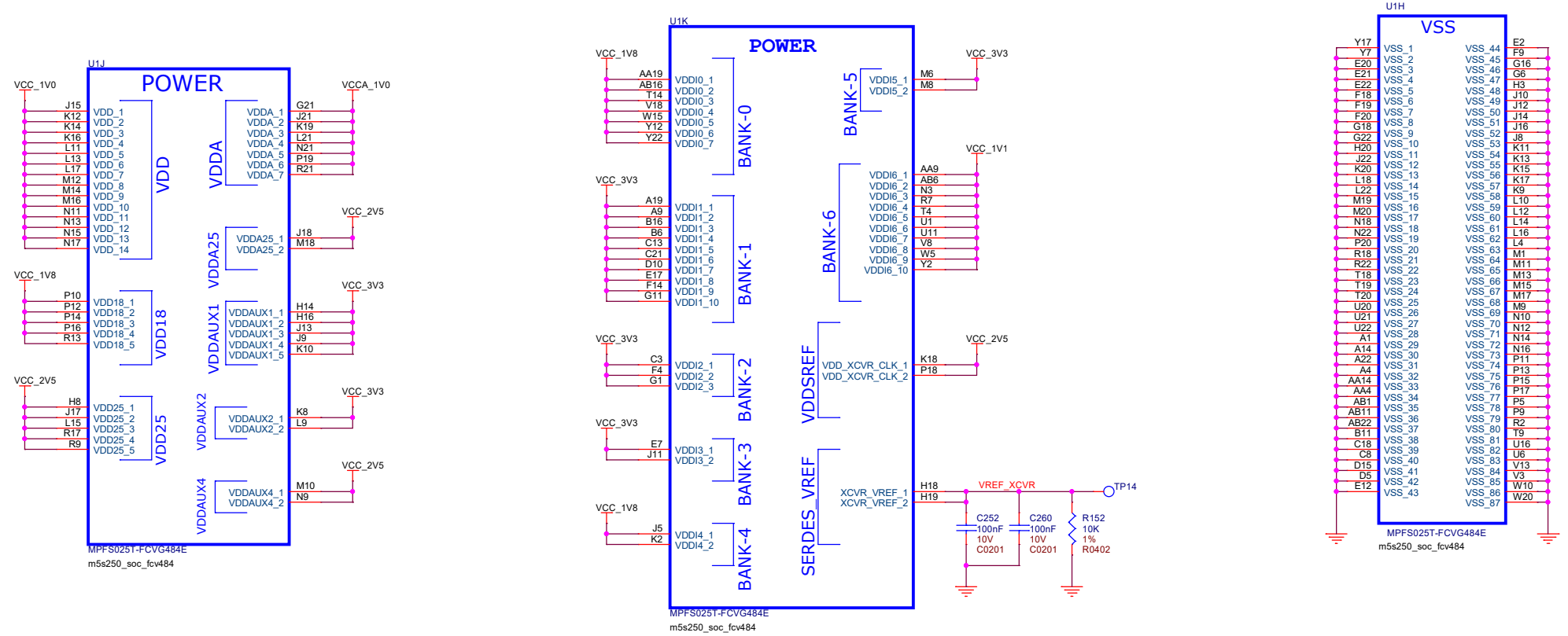
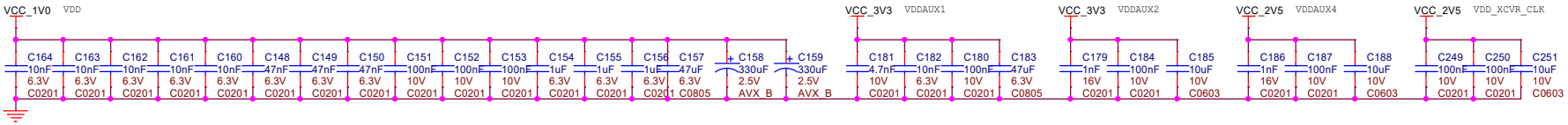
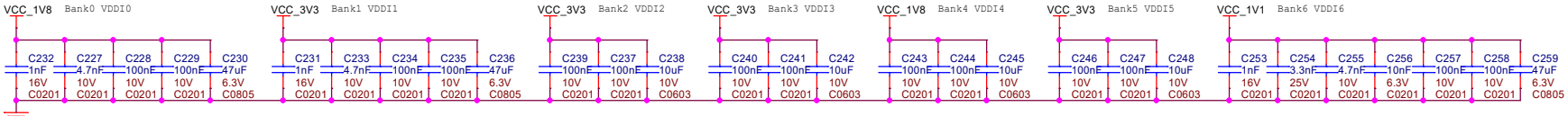
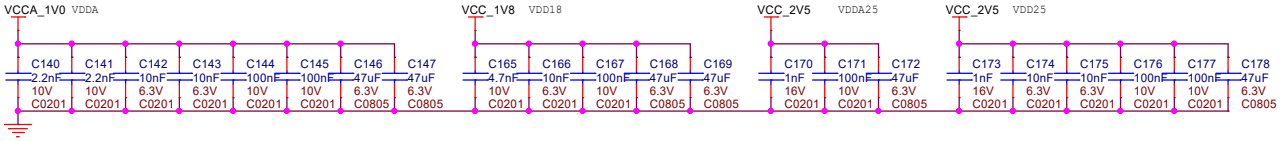
	Title: BeagleV-Fire	
Size: A3	Document Number: 14_SoC BANK1	Rev: V0.2
Draw By: JN.FUONG	Date: Monday, October 09, 2023	Sheet: 14 of 17

SoC Power

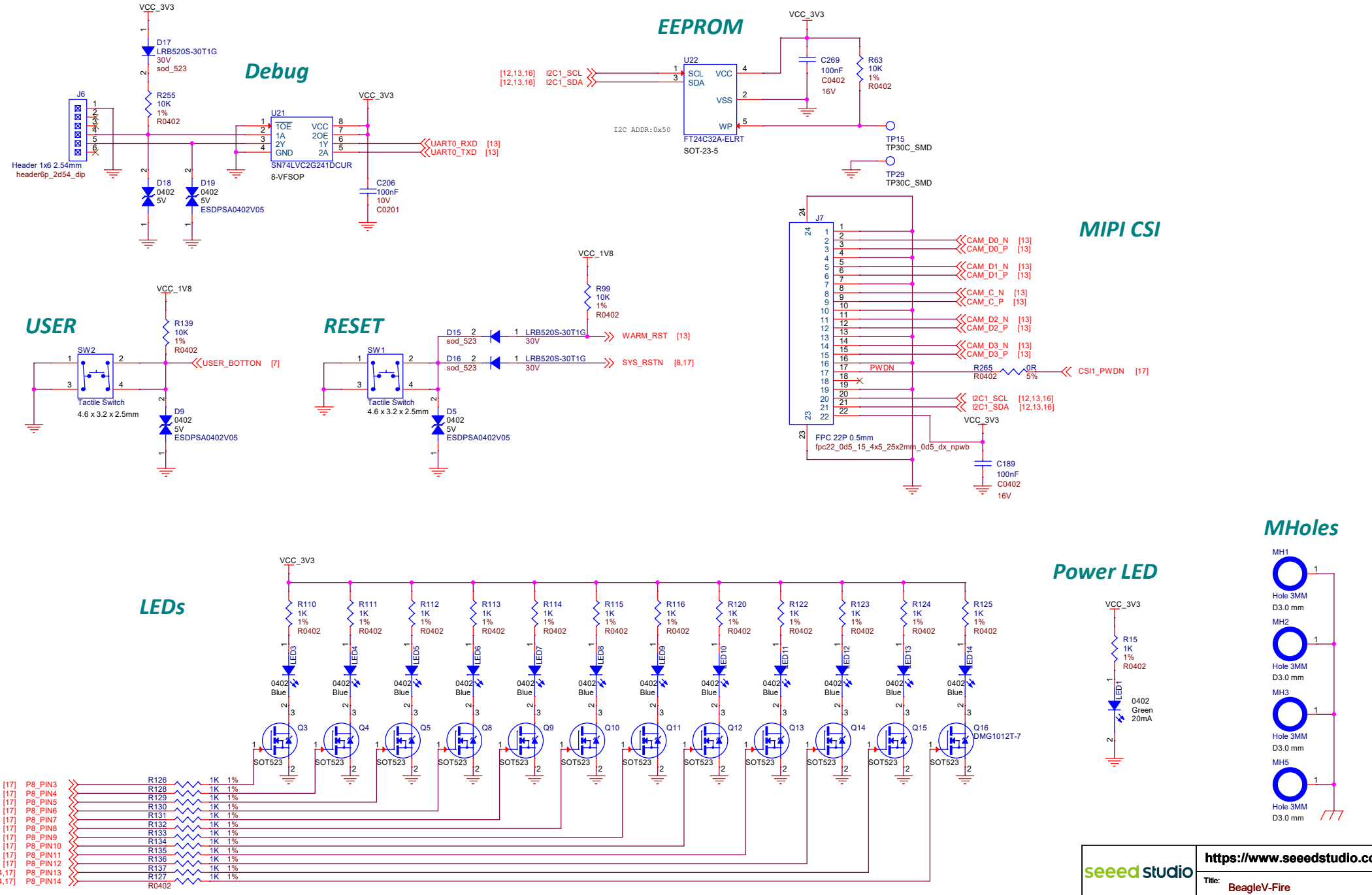








seeed studio	https://www.seeedstudio.com	
	Title: BeagleV-Fire	
Size: A3	Document Number: 15_SoC Power	Rev: V0.2
Draw By: JN.FUONG	Date: Monday, October 09, 2023	Sheet: 15 of 17


Debug
VCC_3V3
D17
LRB520S-30T1G
30V
sod_523
R255
10K
1%
R0402
J6
Header 1x6 2.54mm
header6p_2d54_dip
U21
SN74LVC2G241DCUR
8-VFSOP
D18
0402
5V
D19
0402
5V
ESDPSA0402V05
C206
100nF
10V
C0201
UART0_RXD [13]
UART0_TXD [13]
EEPROM
U22
FT24C32A-ELRT
SOT-23-5
I2C ADDR:0x50
[12,13,16] I2C1_SCL
[12,13,16] I2C1_SDA
C269
100nF
C0402
16V
R63
10K
1%
R0402
TP15
TP30C_SMD
TP29
TP30C_SMD
MIPI CSI
J7
FPC 22P 0.5mm
fpc22_0d5_15_4x5_25x2mm_0d5_dx_npwb
CAM_D0_N [13]
CAM_D0_P [13]
CAM_D1_N [13]
CAM_D1_P [13]
CAM_C_N [13]
CAM_C_P [13]
CAM_D2_N [13]
CAM_D2_P [13]
CAM_D3_N [13]
CAM_D3_P [13]
PWDN
R265
0R
5%
CSI1_PWDN [17]
I2C1_SCL [12,13,16]
I2C1_SDA [12,13,16]
C189
100nF
C0402
16V
USER
SW2
Tactile Switch
4.6 x 3.2 x 2.5mm
R139
10K
1%
R0402
USER_BOTTON [7]
D9
0402
5V
ESDPSA0402V05
RESET
SW1
Tactile Switch
4.6 x 3.2 x 2.5mm
R99
10K
1%
R0402
D15
D16
LRB520S-30T1G
30V
sod_523
WARM_RST [13]
SYS_RSTN [8,17]
D5
0402
5V
ESDPSA0402V05
LEDs
R110 R111 R112 R113 R114 R115 R116 R120 R122 R123 R124 R125
1K 1% R0402
LED3 LED4 LED5 LED6 LED7 LED8 LED9 LED10 LED11 LED12 LED13 LED14
0402 Blue
Q3 Q4 Q5 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15 Q16 DMG1012T-7
SOT523
[17] P8_PIN3
[17] P8_PIN4
[17] P8_PIN5
[17] P8_PIN6
[17] P8_PIN7
[17] P8_PIN8
[17] P8_PIN9
[17] P8_PIN10
[17] P8_PIN11
[17] P8_PIN12
[14,17] P8_PIN13
[14,17] P8_PIN14
R126 R128 R129 R130 R131 R132 R133 R134 R135 R136 R137 R127
1K 1%
R0402
Power LED
R15
1K
1%
R0402
LED1
0402
Green
20mA
MHoles
MH1 MH2 MH3 MH5
Hole 3MM
D3.0 mm
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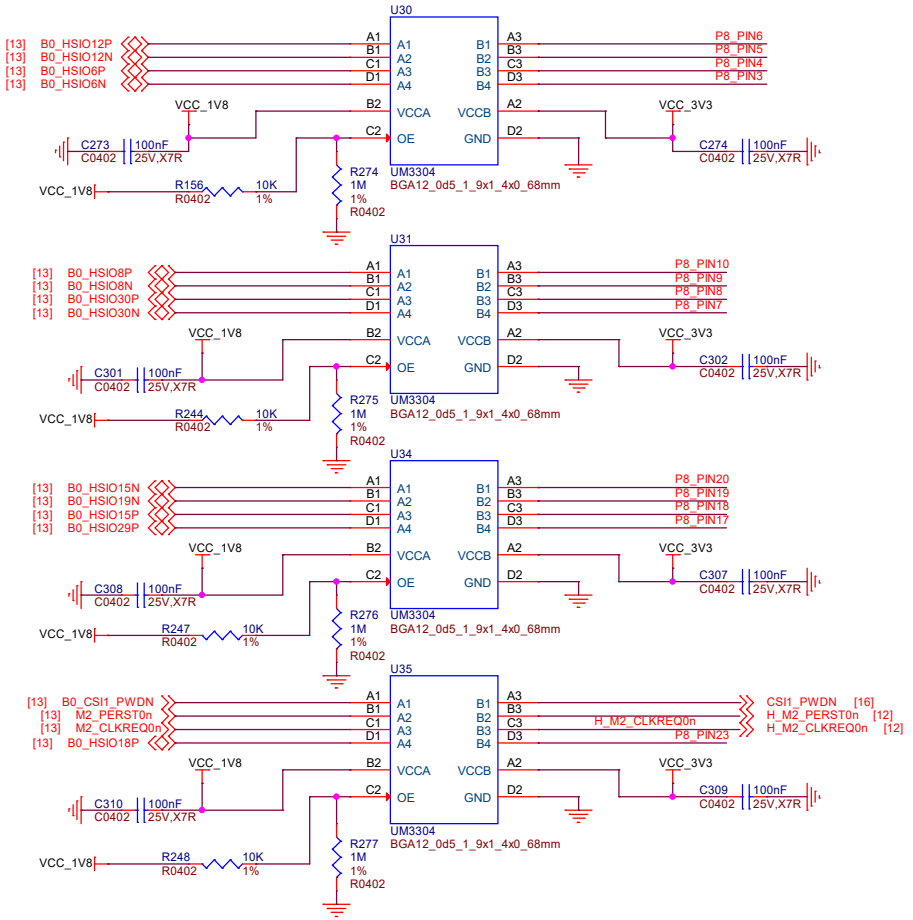
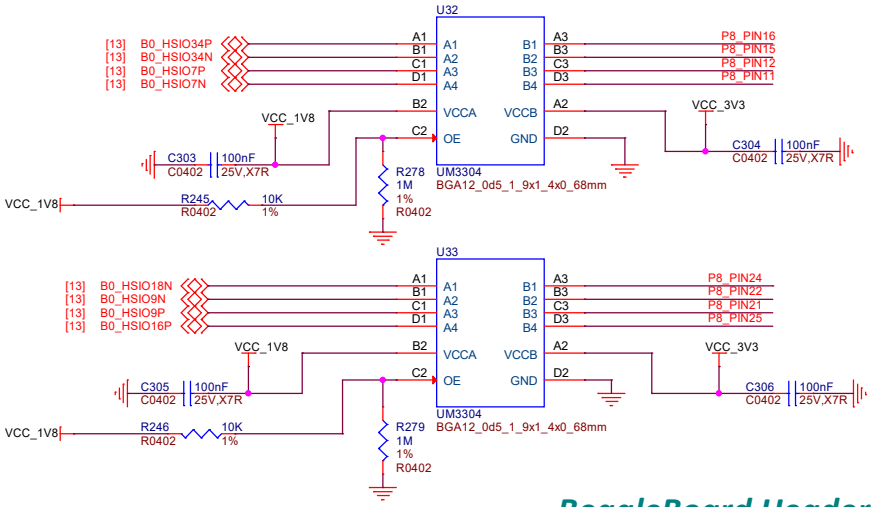
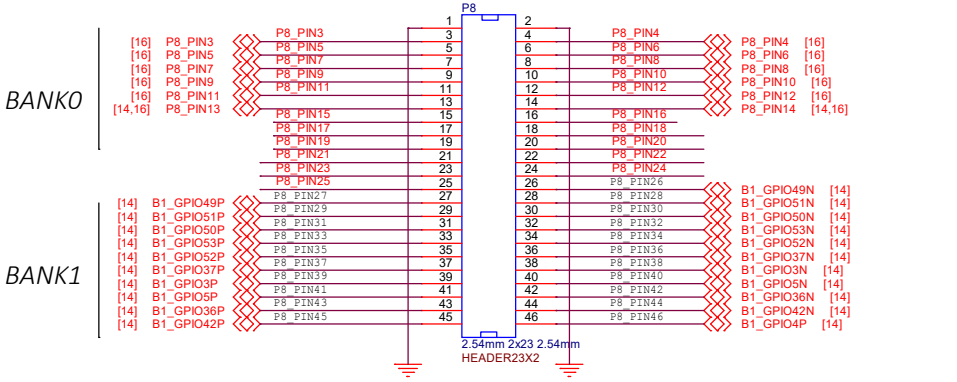
3.3V To 1V8 Level translator



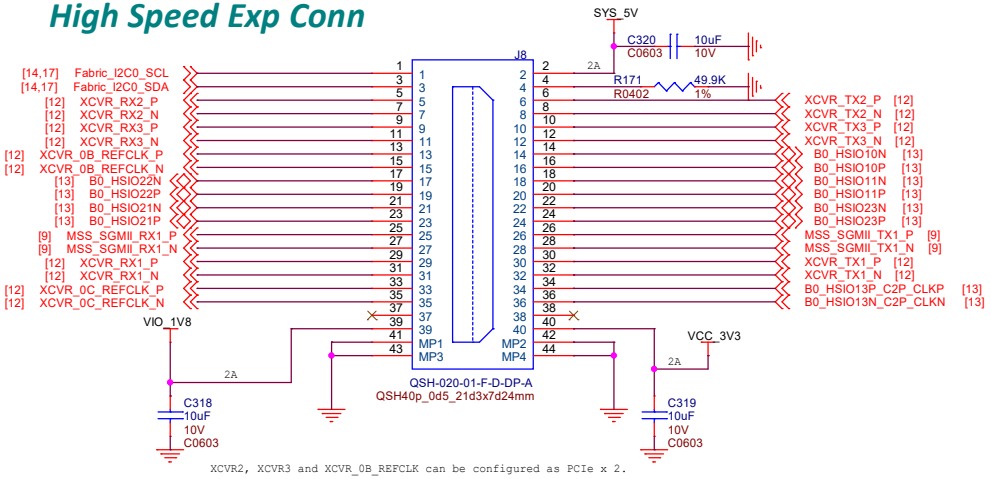
3.3V To 1V8 Level translator



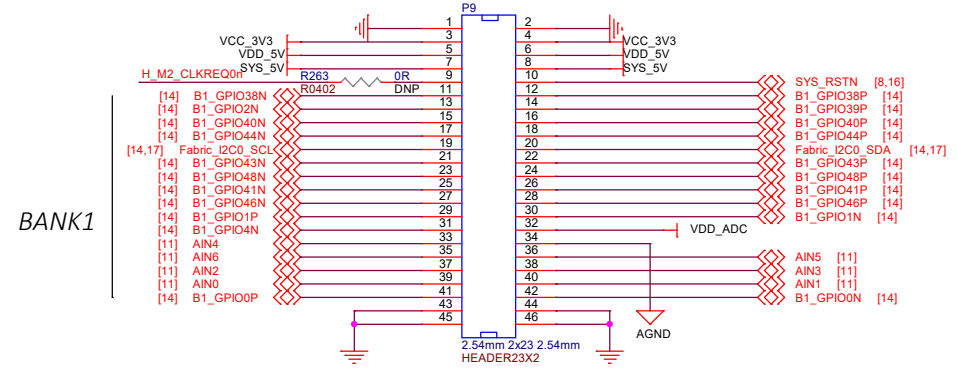
BeagleBoard Header



High Speed Exp Conn



XCVR2, XCVR3 and XCVR_0B_REFCLK can be configured as PCIe x 2.



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