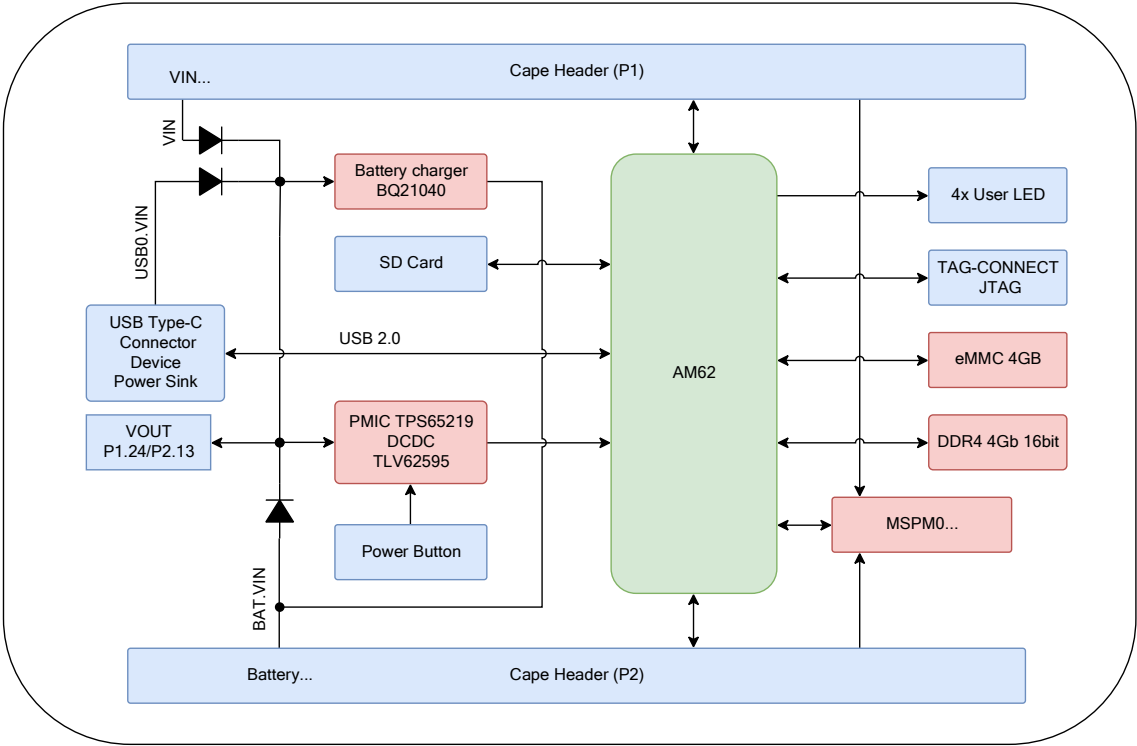


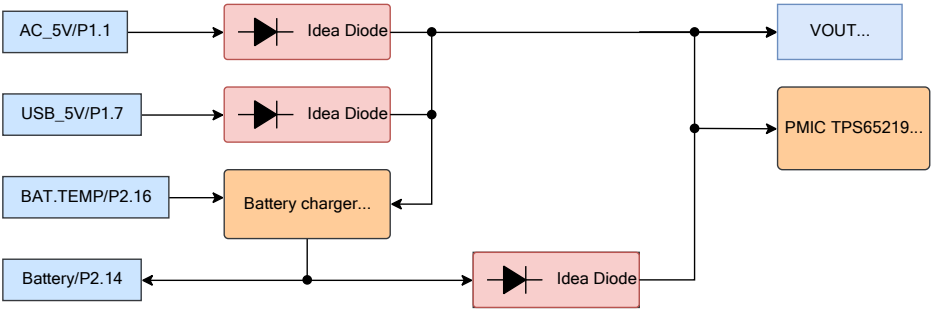
PAGE LIST	
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005	005_PMIC & Charger
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009	009_SoC MMC & eMMC & SD
010	010_SoC WKUP/MCU/System
011	011_SoC Bootstrap
012	012_SoC RGMII/OSPI
013	013_SoC GPIO/MCASP/VOUT
014	014_SoC USB/OLDI/CSI & USB C
015	015_SoC JTAG & MISC
016	016_BP P1 & P2

REVISION HISTORY			
VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR
0.1	28 Oct. 2022	First release	qxn
0.2	1 Nov. 2022	1. Remove unused nets 2. Use WKUP_I2C0 for PMIC 3. Add pull-down to VPP 4. Move eMMC_RSTn to GPIO0_7 5. Add USER button for boot mode seletion 6. Try to add a CSI connector 7. Using processor boall numbers for signal name on P1 and P2 8. Change SoC to AM6232, change eMMC to 4GB, change DDR to 512MB	qxn
0.3	2 Nov. 2022	1. Remove CSI 2. Add SD card, move LDO0 to VDD_SD 3. Power the VPP with VDD_1V8 through a jumper 4. Connect P2.19 to AC20 instead	qxn
0.4	23 Dec.2022	1. Replace the ideal diode with LM73100RPWR 2. Replace EEPROM and ADC with MSPM0 3. Correct the boot settings 4. Connect AD24(MDC) to P2.17 and AB22(MDIO) to P2.20 which is same as pocketbeagle.	qxn
0.5	28 Dec.2022	1. Add B5 (MCU_UART0_RXD) to P2_5. 2. Add A5 (MCU_UART0_TXD) to P2_7. 3. Add A18 (EXT_REFCLK1) to P1_10. 4. Add AD24 (MDIO0_MDC) to P2_1. 5. Add AB22 (MDIO0_MDIO) to P2_3.	qxn
0.6	09 Oct.2022	1. Add a buffer on reset 2. Correct typo - WKUP_I2C0_SDL 3. Add decoupling capacitors for LM73100 4. Change R44 to 100k 0.1% 5. Add pulldown resistors on RESETSTATz and PORZ_OUT 6. Correct the ideal diode control logic 7. Change C17 to 10uF 8. Change the SD card holder to lower profile with insertion detection 9. Move C11 to be in parallel with R260 10. Add pullup resistors to WKUP_I2C0 11. Add voltage divider on USB1_VBUS	qxn

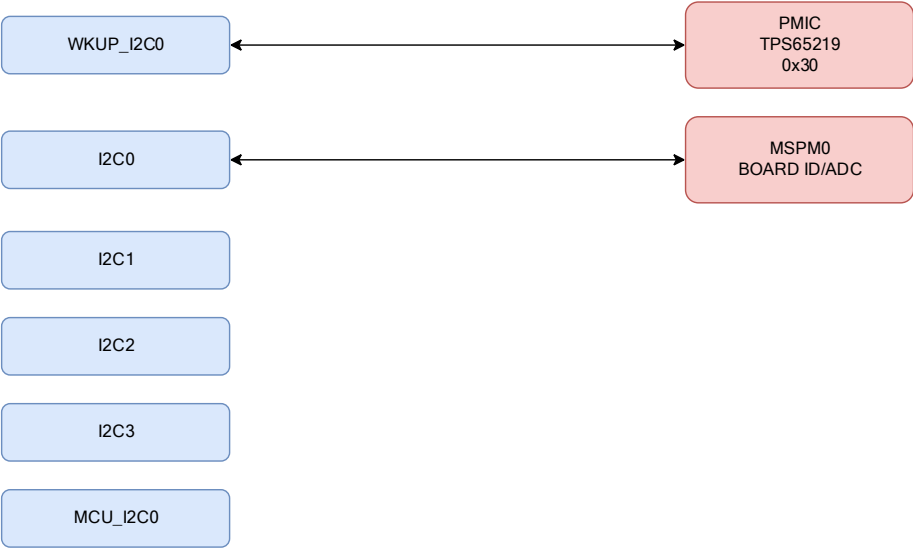
Block Diagram



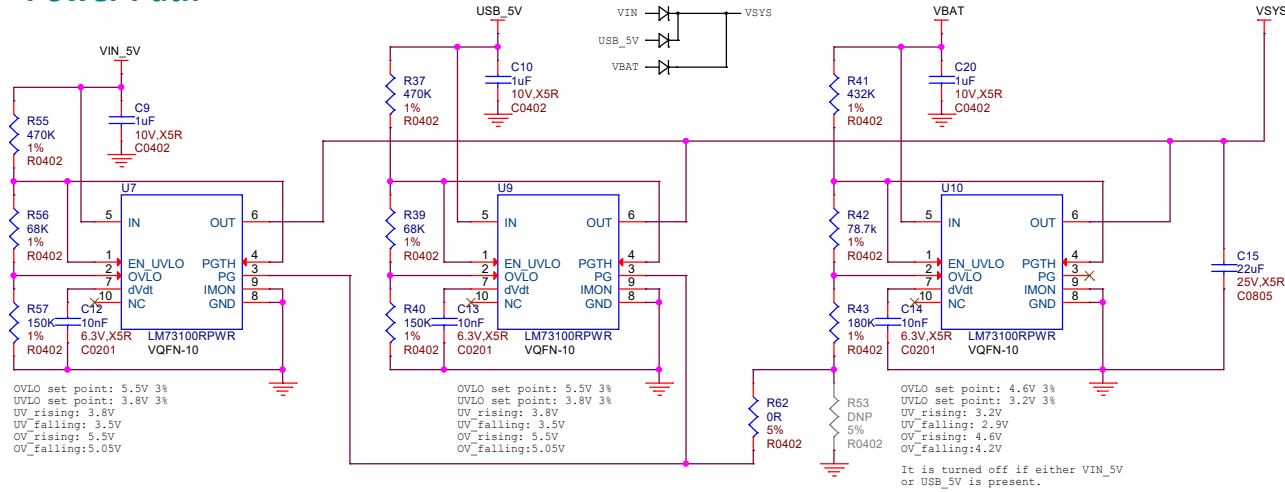
Power tree



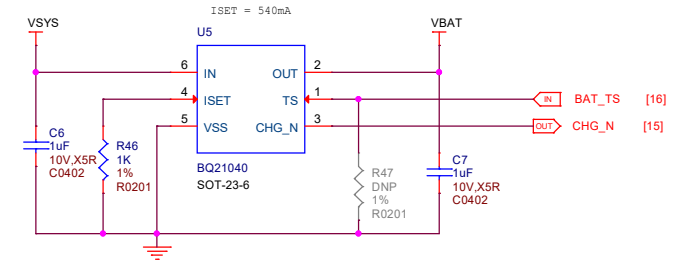
I2C Usage Diagram



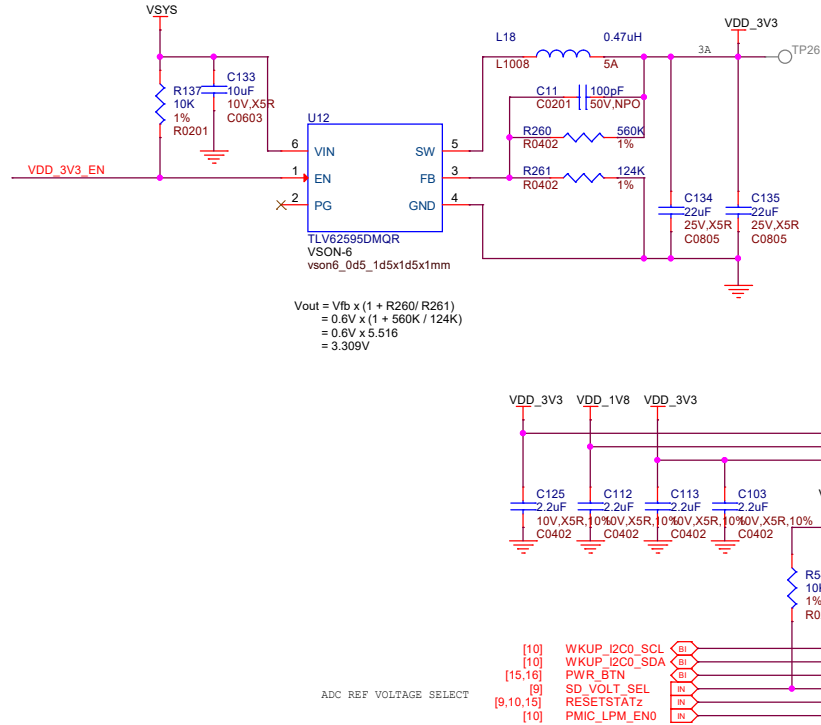
## Power Path



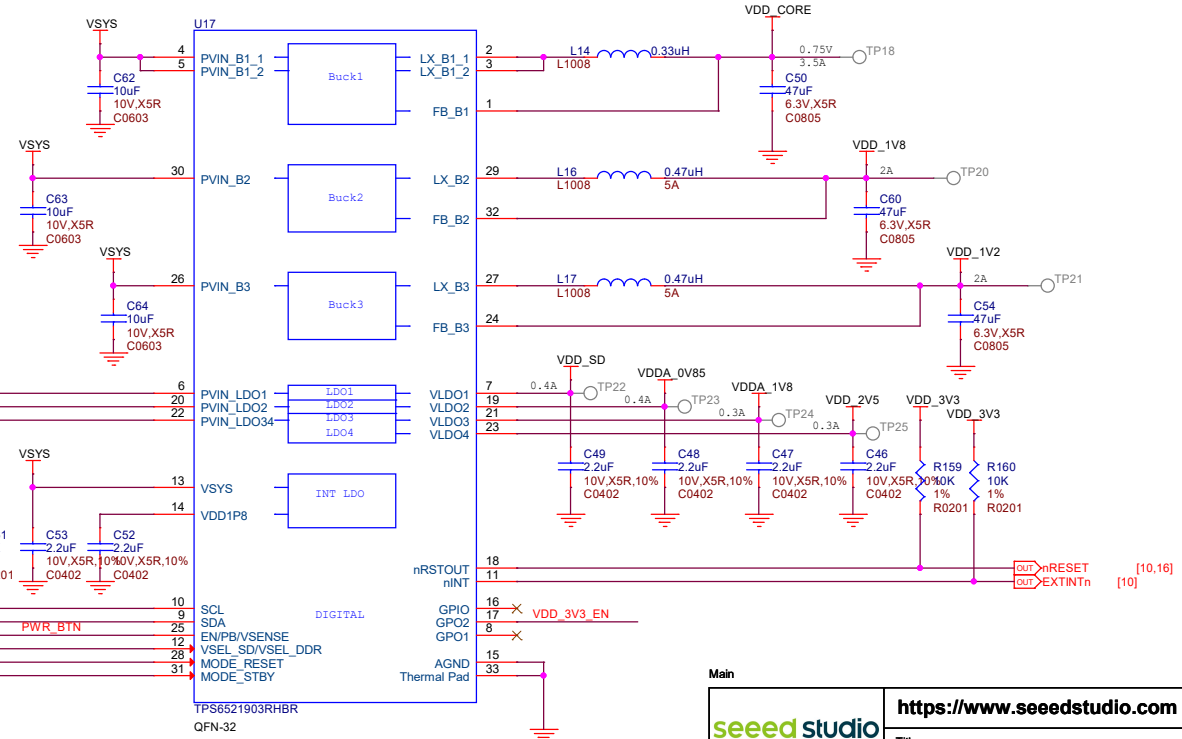
## Battery Charger



## DCDC 3V3

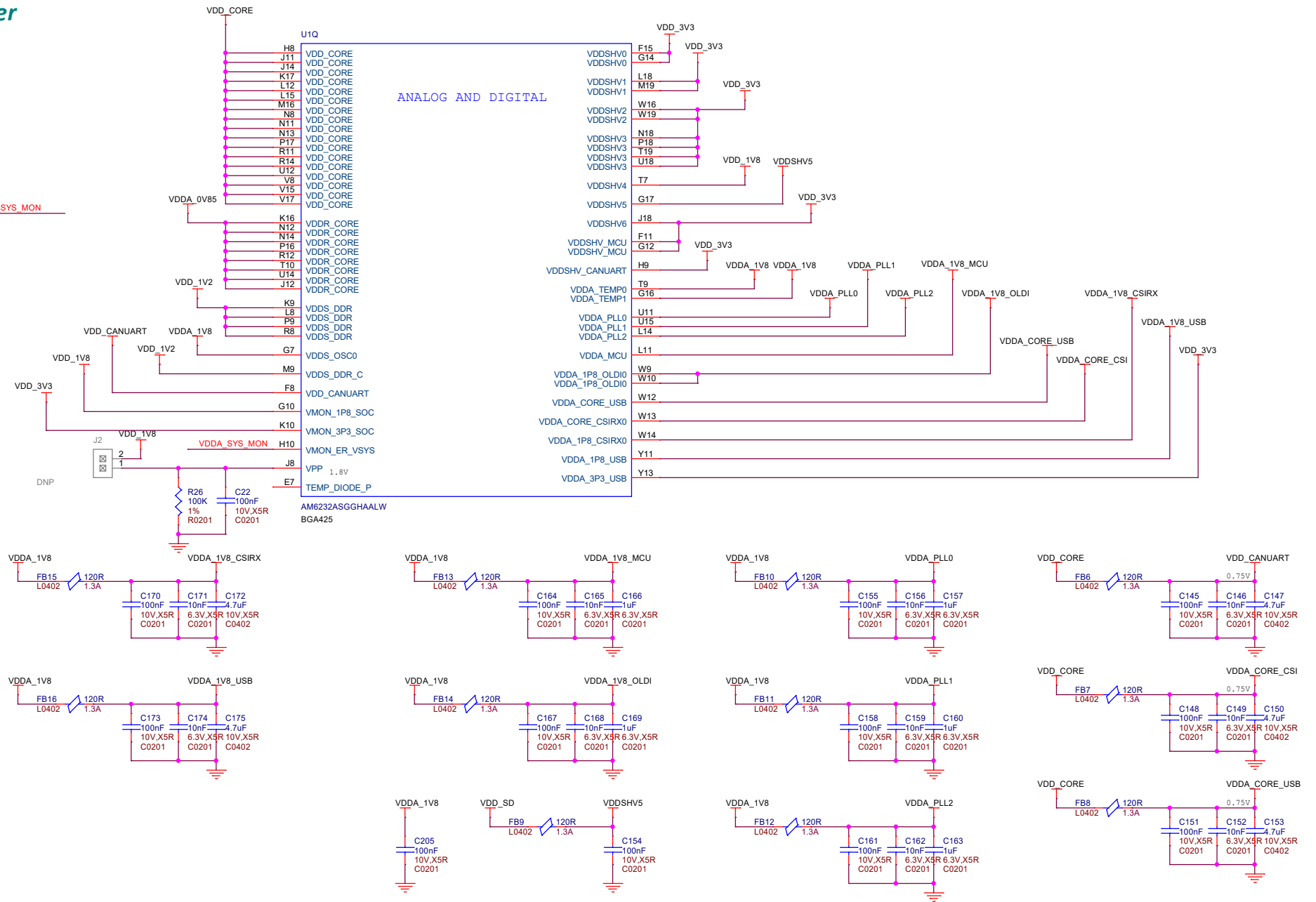


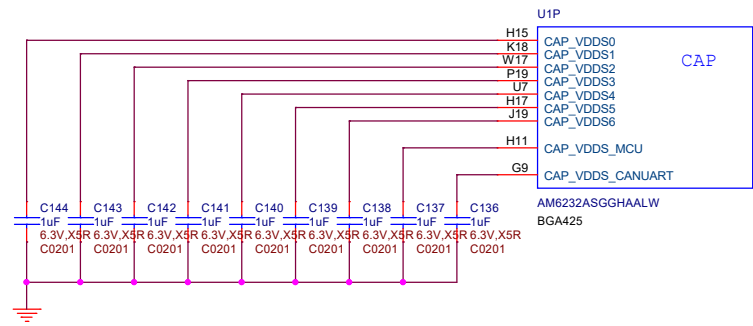
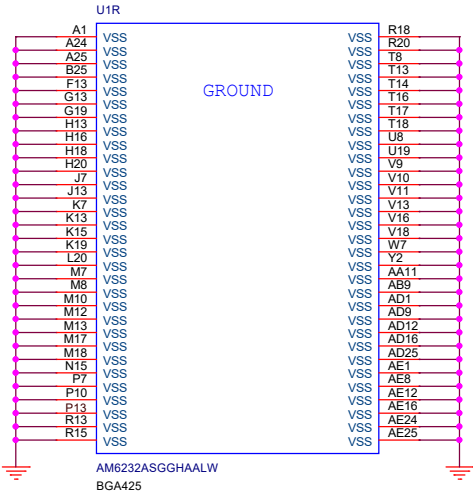
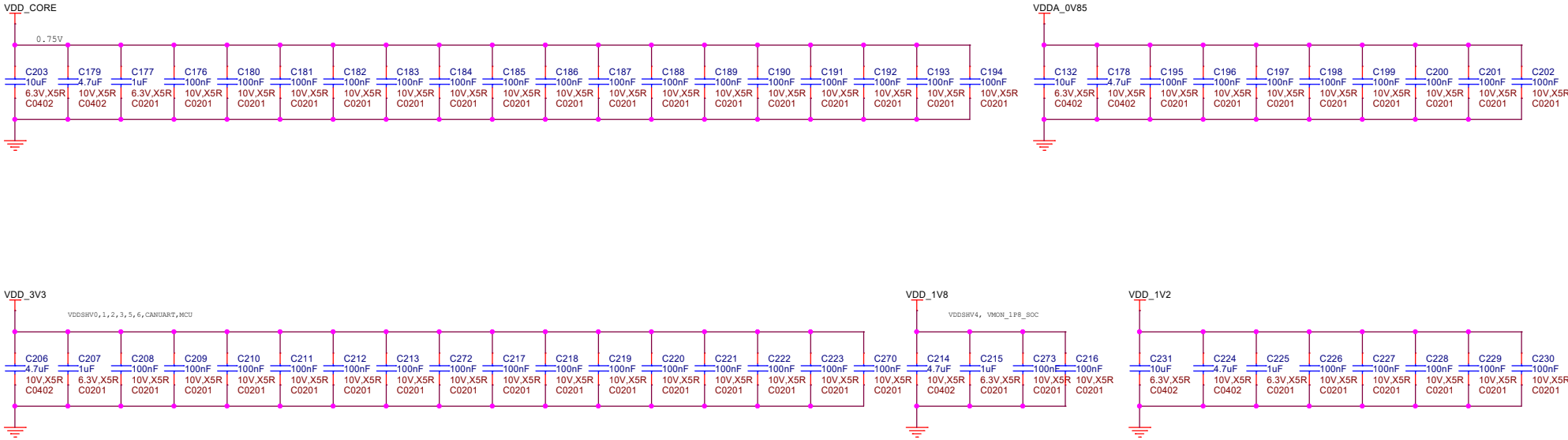
## PMIC



Main

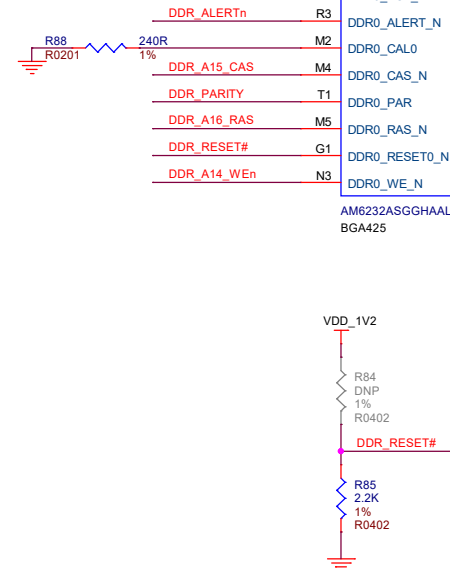
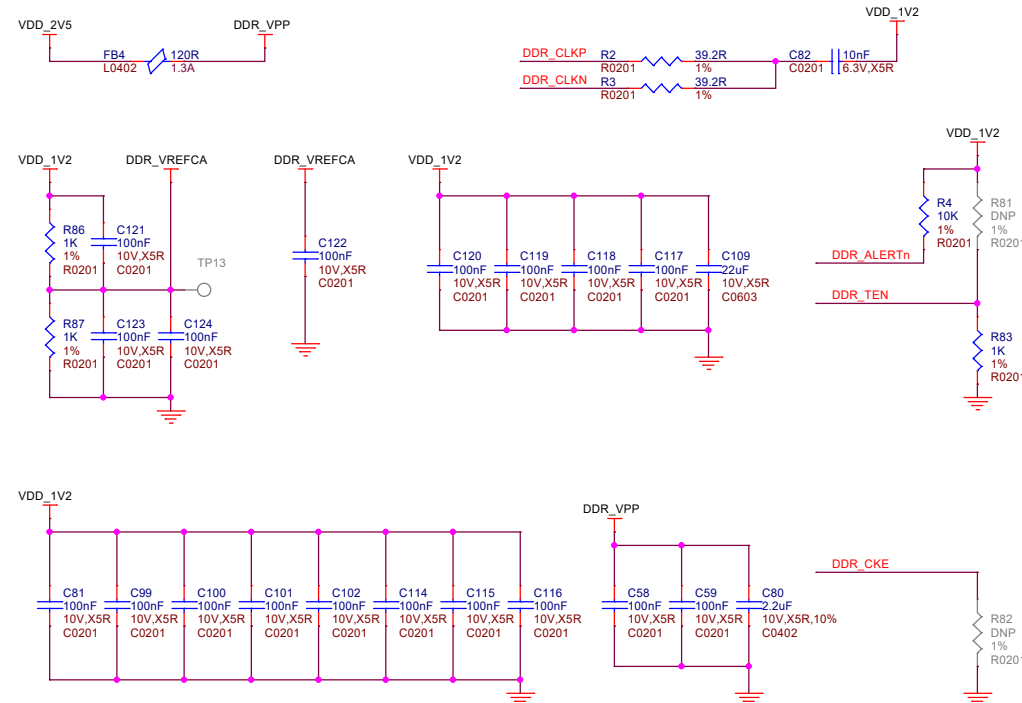
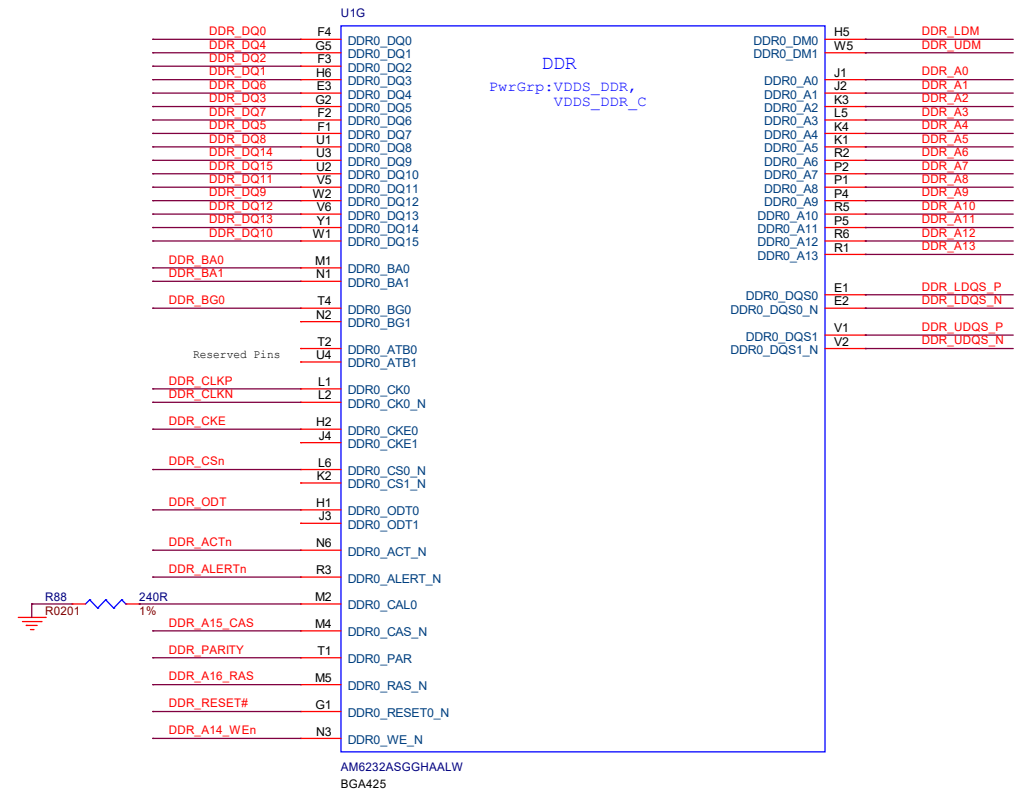
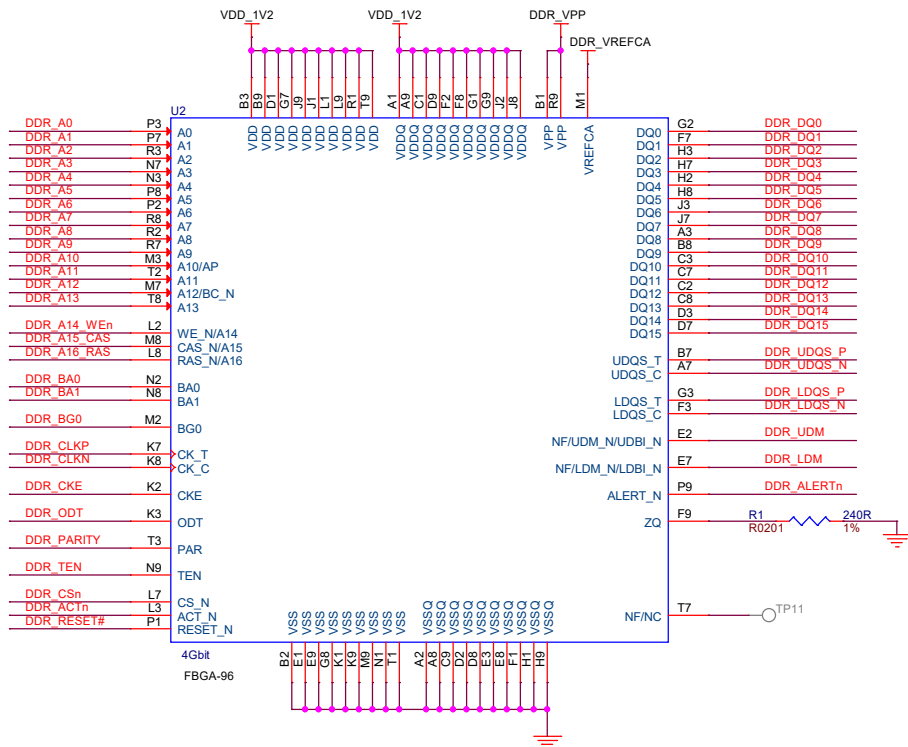
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Size: A3	Document Number:	005_PMIC & Charger	Rev: v0.6
Draw By: qxm	Date: Monday, October 09, 2023	Sheet: 5 of 16	





# DDR4

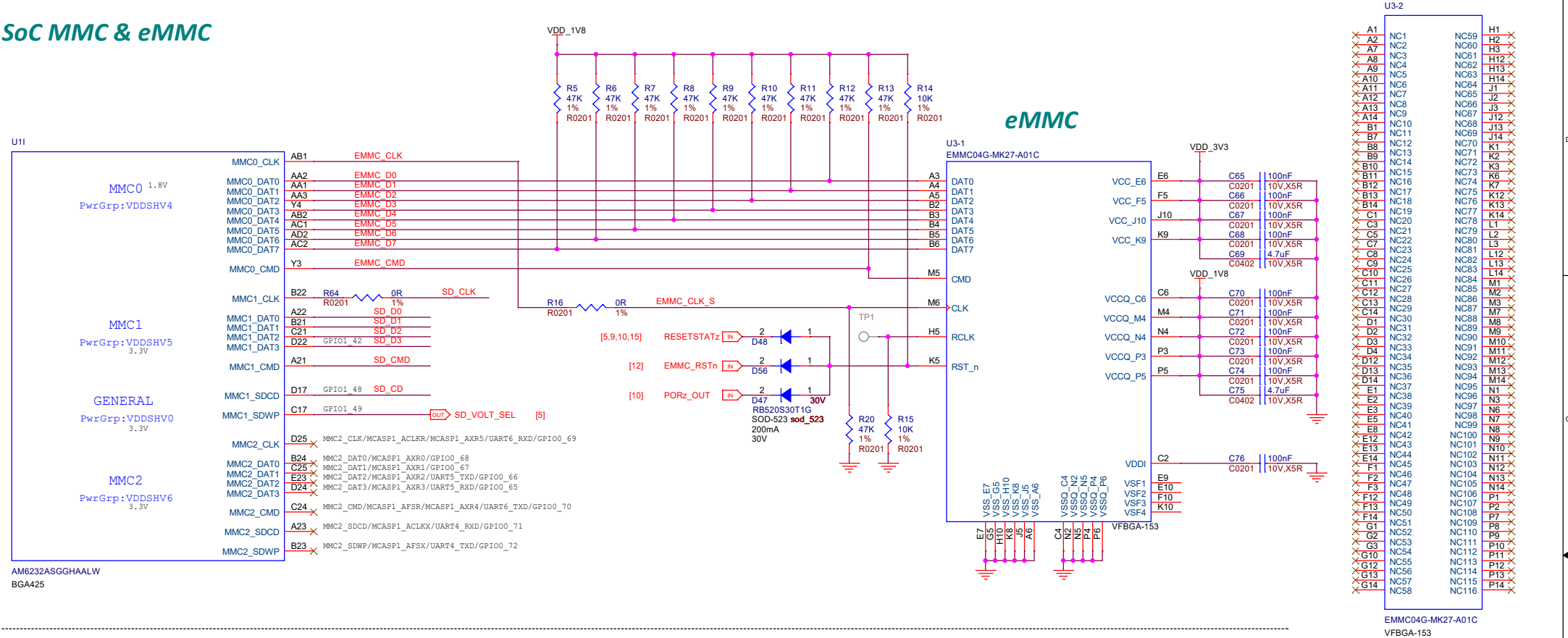
# SoC DDR controller



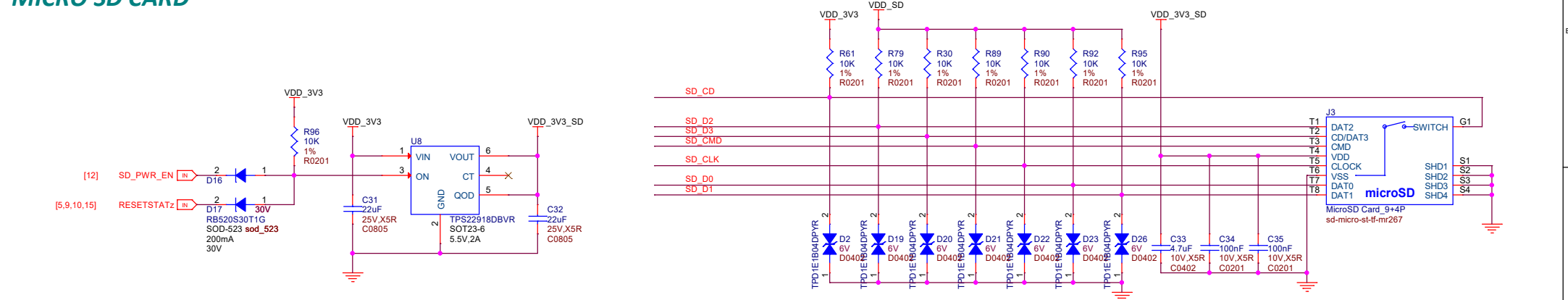
NOTE: DDR DQ Lines Swapped  
Within Data Byte



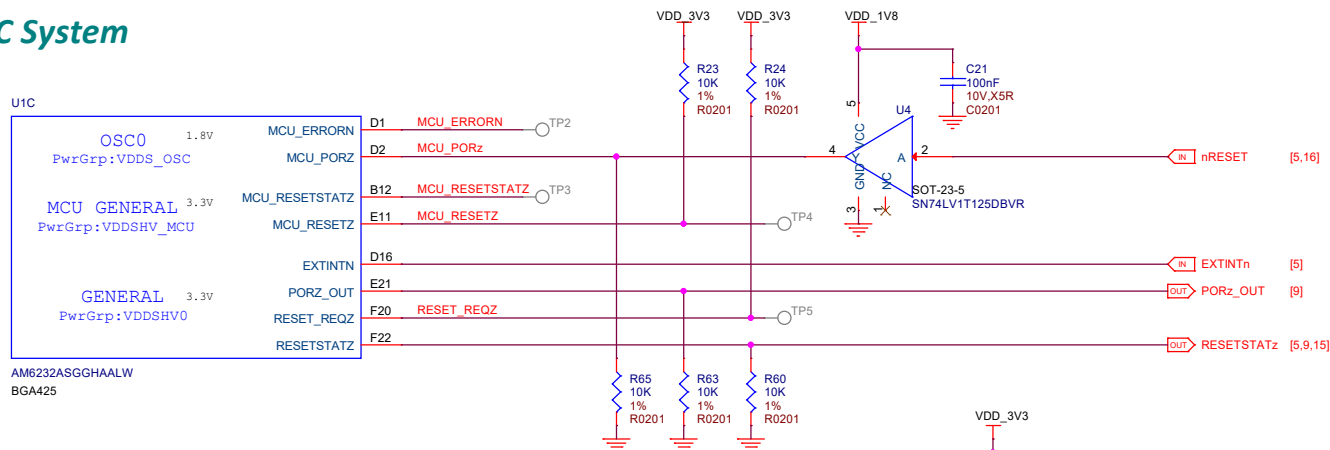
SoC MMC & eMMC



MICRO SD CARD

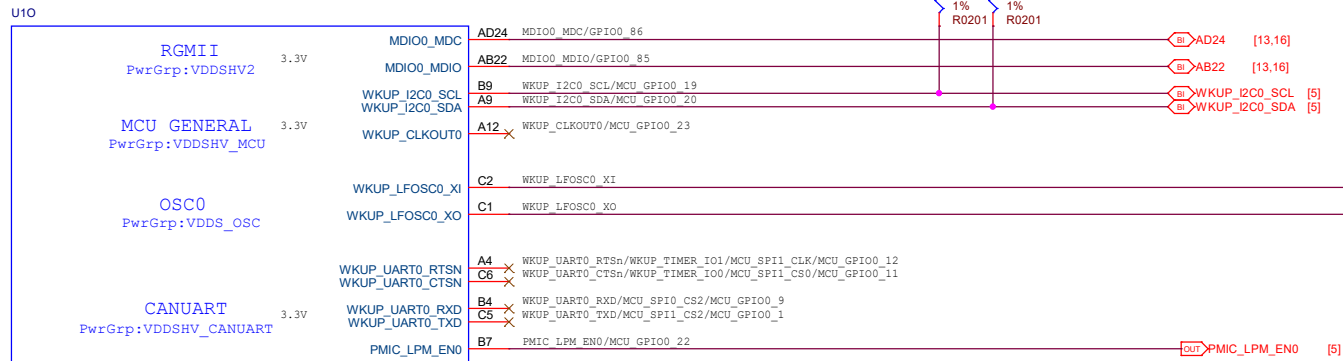


## SoC System



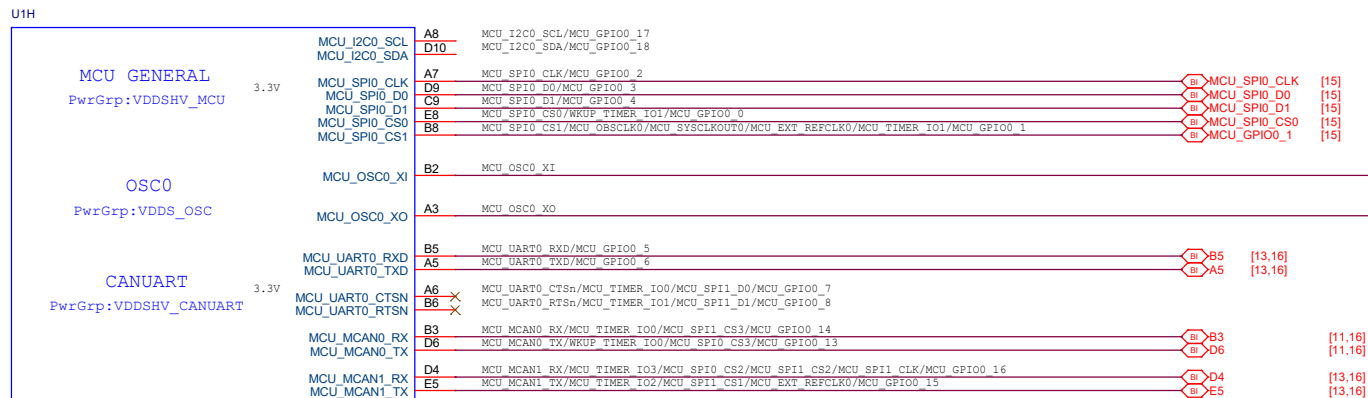
AM6232ASGGHAALW  
BGA425

## WKUP Domain



AM6232ASGGHAALW  
BGA425

## MCU Domain



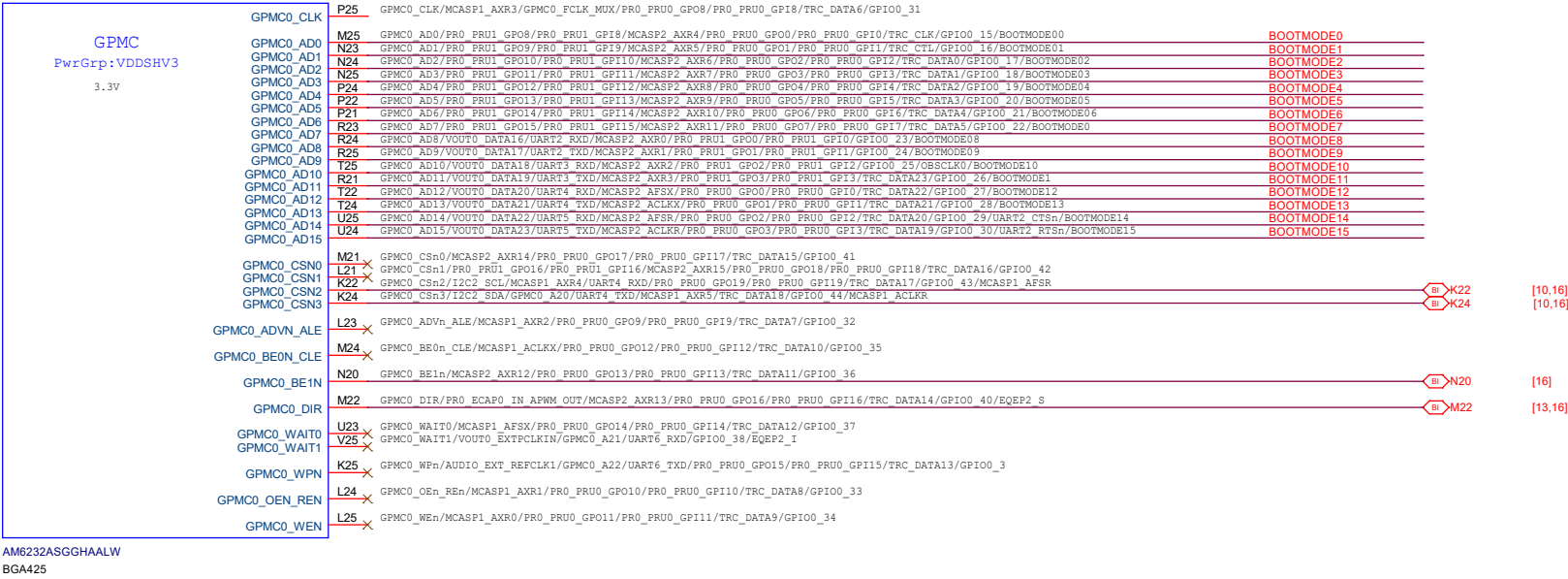
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Main

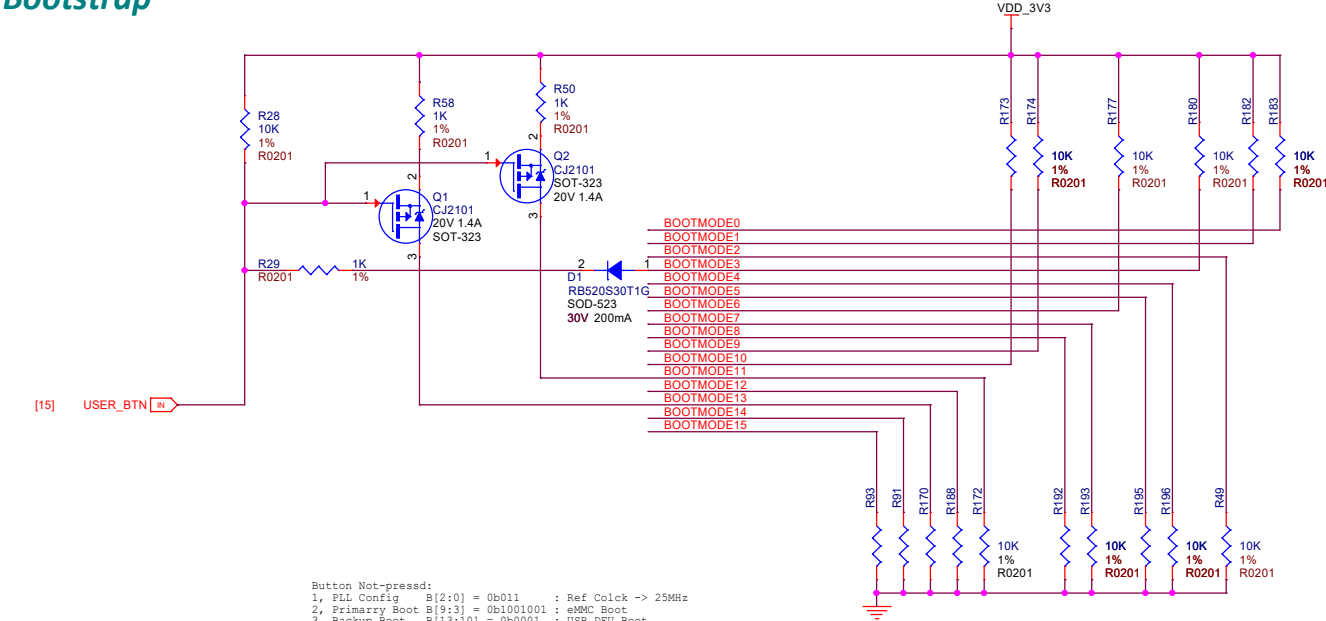
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Document Number:	010_SoC WKUP/MCU/System	Rev:	v0.6
Draw By: qxm	Date: Sunday, October 08, 2023	Sheet:	10 of 16

SoC GPIO 1.8V

U1F



Bootstrap



Button Not-pressed:  
1, PLL Config B[2:0] = 0b011 : Ref Colck -> 25MHz  
2, Primary Boot B[9:3] = 0b1001001 : eMMC Boot  
3, Backup Boot B[13:10] = 0b0001 : USB DPU Boot

Button Pressed:  
1, PLL Config B[2:0] = 0b011 : Ref Colck -> 25MHz  
2, Primary Boot B[9:3] = 0b1001000 : SDCard FS Boot  
3, Backup Boot B[13:10] = 0b1011 : UART Boot

Main

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Size: A3

Document Number: 011\_SoC Bootstrap

Rev: v0.6

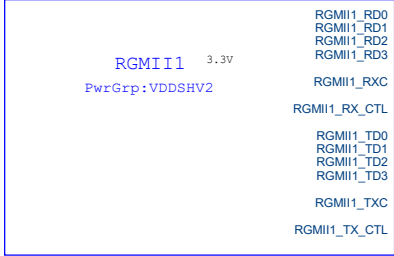
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Date: Monday, October 09, 2023

Sheet: 11 of 16

# RGMII

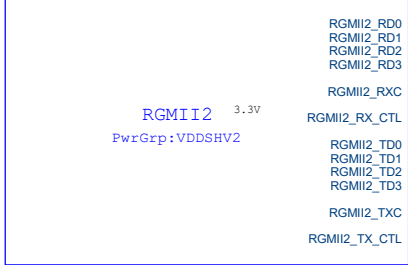
U1M



AM6232ASGGHAALW  
BGA425

AB17	RGMII1_RD0/RMII1_RXD0/GPIO0_81		
AC17	RGMII1_RD1/RMII1_RXD1/GPIO0_82		
AB16	RGMII1_RD2/PR0_UART0_RTSn/GPIO0_83		
AA15	RGMII1_RD3/GPIO0_84		
AD17	RGMII1_RXC/RMII1_REF_CLK/PR0_UART0_CTSn/GPIO0_80		
AE17	RGMII1_RX_CTL/RMII1_RX_ER/GPIO0_79		
AE20	RGMII1_TD0/RMII1_TXD0/GPIO0_75		
AD20	RGMII1_TD1/RMII1_TXD1/GPIO0_76		
AE18	RGMII1_TD2/PR0_UART0_RXD/GPIO0_77		
AD18	RGMII1_TD3/PR0_UART0_TXD/GPIO0_78		
AE19	RGMII1_TXC/RMII1_CRS_DV/GPIO0_74		
AD19	RGMII1_TX_CTL/RMII1_TX_EN/GPIO0_73		

U1S

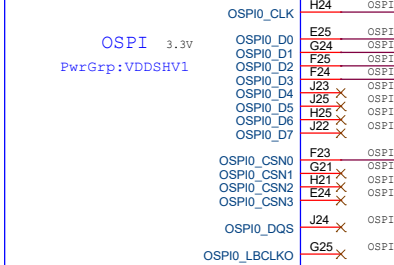


AM6232ASGGHAALW  
BGA425

AE23	RGMII2_RD0/RMII2_RXD0/MCASP2_AXR2/PR0_PRU0_GPO2/PR0_PRU0_GPI2/PR0_UART0_RTSn/GPIO1_3		
AB20	RGMII2_RD1/RMII2_RXD1/MCASP2_AFSR/PR0_PRU0_GPO3/PR0_PRU0_GPI3/MCASP2_AXR7/GPIO1_4		
AC21	RGMII2_RD2/MCASP2_AXR0/PR0_PRU0_GPO4/PR0_PRU0_GPI4/PR0_UART0_RXD/GPIO1_5/EQEP2_A		
AE22	RGMII2_RD3/AUDIO_EXT_REFCLK0/PR0_PRU0_GPO16/PR0_PRU0_GPI16/PR0_UART0_TXD/GPIO1_6/EQEP2_B		
AD23	RGMII2_RXC/RMII2_REF_CLK/MCASP2_AXR1/PR0_PRU0_GPO1/PR0_PRU0_GPI1/PR0_ECAP0_SYNC_IN/GPIO1_2		
AD22	RGMII2_RX_CTL/RMII2_RX_ER/MCASP2_AXR3/PR0_PRU0_GPO0/PR0_PRU0_GPI0/GPIO1_1		
Y18	RGMII2_TD0/RMII2_TXD0/MCASP2_AXR6/PR0_PRU1_GPO2/PR0_PRU1_GPI2/GPIO0_89		
AA18	RGMII2_TD1/RMII2_TXD1/MCASP2_ACLKR/PR0_PRU1_GPO3/PR0_PRU1_GPI3/MCASP2_AXR8/GPIO0_90		
AD21	RGMII2_TD2/MCASP2_AFSX/PR0_PRU1_GPO4/PR0_PRU1_GPI4/PR0_ECAP0_IN_APMW_OUT/GPIO0_91/EQEP2_I		
AC20	RGMII2_TD3/MCASP2_ACLKX/PR0_PRU1_GPO16/PR0_PRU1_GPI16/PR0_ECAP0_SYNC_OUT/PR0_UART0_CTSn/GPIO1_0/EQEP2_S		
AE21	RGMII2_TXC/RMII2_CRS_DV/MCASP2_AXR5/PR0_PRU1_GPO1/PR0_PRU1_GPI1/GPIO0_88		
AA19	RGMII2_TX_CTL/RMII2_TX_EN/MCASP2_AXR4/PR0_PRU1_GPO0/PR0_PRU1_GPI0/GPIO0_87		

# OSPI

U1J



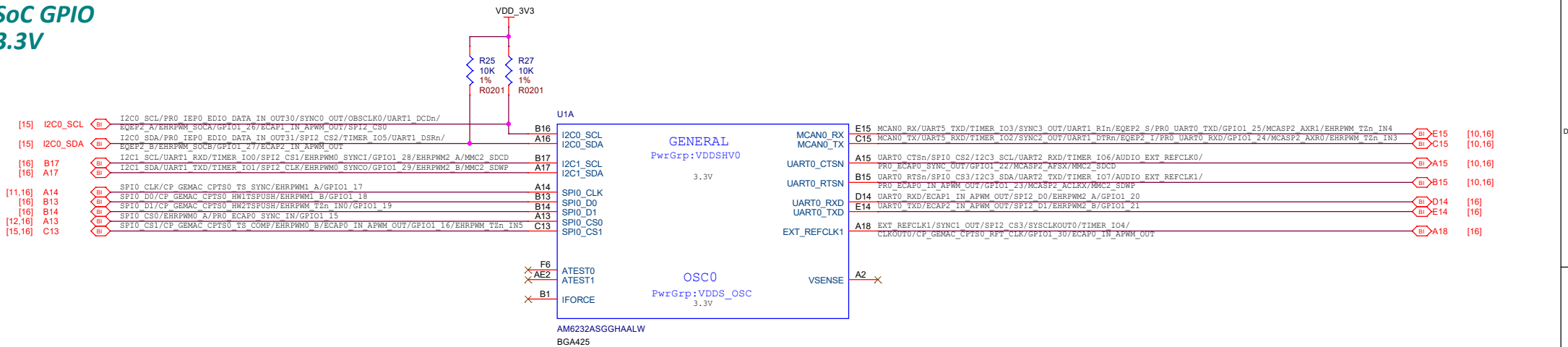
AM6232ASGGHAALW  
BGA425

H24	OSPI0_CLK/GPIO0_0		
E25	OSPI0_D0/GPIO0_3		
G24	OSPI0_D1/GPIO0_4		
F25	OSPI0_D2/GPIO0_5		
F24	OSPI0_D3/GPIO0_6		
J23	OSPI0_D4/SP11_CSN0/MCASP1_AXR1/UART6_RXD/GPIO0_7		
J25	OSPI0_D5/SP11_CLK/MCASP1_AXR0/UART6_TXD/GPIO0_8		
H25	OSPI0_D6/SP11_D0/MCASP1_ACLKX/UART6_RTSn/GPIO0_9		
J22	OSPI0_D7/SP11_D1/MCASP1_AFSX/UART6_CTSn/GPIO0_10		
F23	OSPI0_CSN0/GPIO0_11		
G21	OSPI0_CSN1/GPIO0_12		
H21	OSPI0_CSN2/SP11_CSN1/OSPI0_RESET_OUT1/MCASP1_AFSR/MCASP1_AXR2/UART5_RXD/GPIO0_13		
E24	OSPI0_CSN3/OSPI0_RESET_OUT0/OSPI0_ECC_FAIL/MCASP1_ACLKR/MCASP1_AXR3/UART5_TXD/GPIO0_14		
J24	OSPI0_DQS/UART5_CTSn/GPIO0_2		
G25	OSPI0_LBCLKO/UART5_RTSn/GPIO0_1		

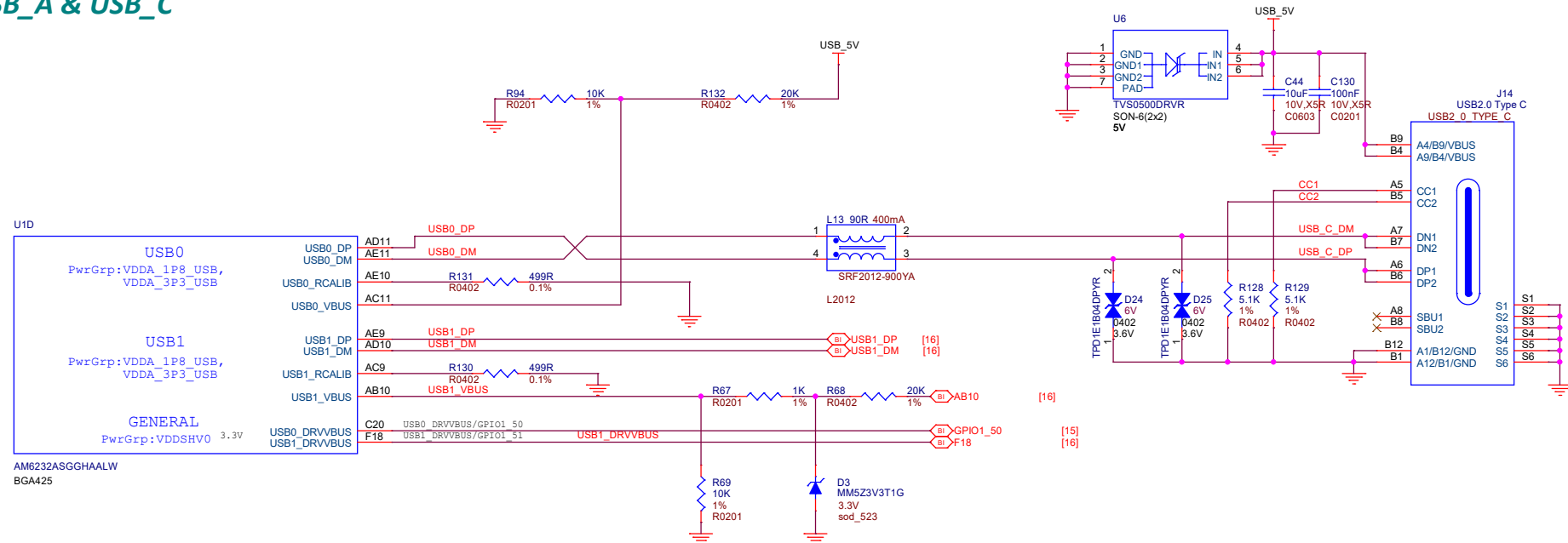
Main

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Document Number:	012_SoC RGMII/OSPI	Rev:	v0.6
Draw By: qm	Date: Saturday, October 07, 2023	Sheet:	12 of 16

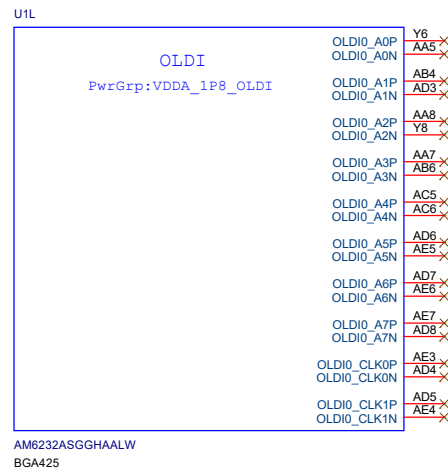
# SoC GPIO 3.3V



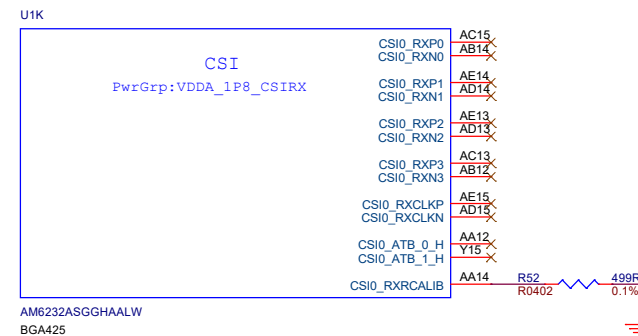
## USB\_A & USB\_C



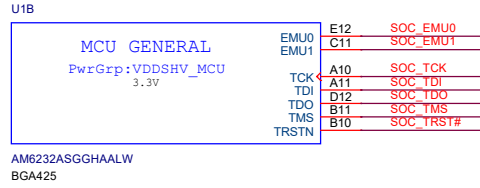
**OLDI**



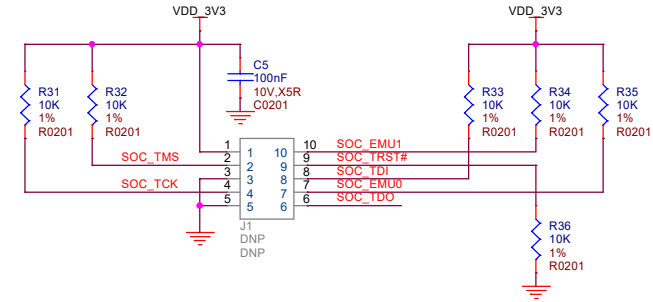
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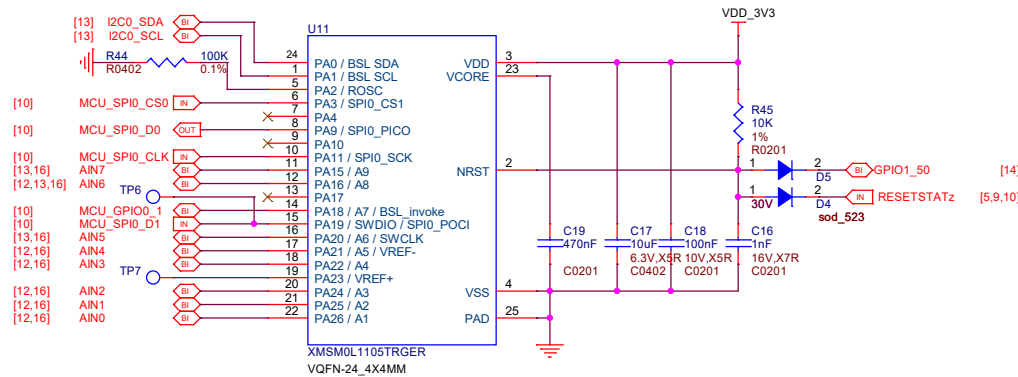
## JTAG



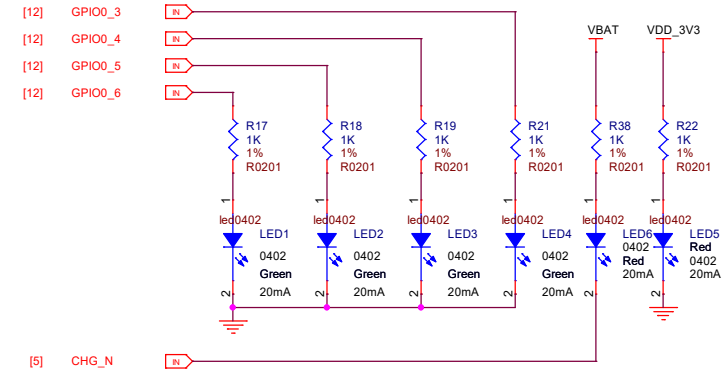
## Tag-Connect



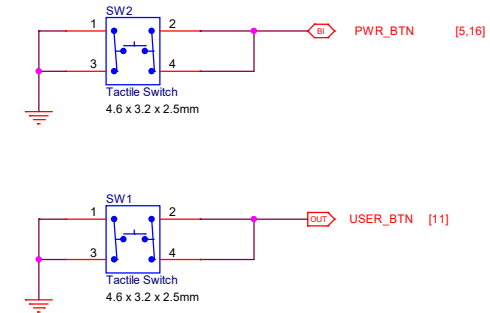
## MCU



## LEDs



## Power Button



Main

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Title:		PocketBeagle2	
Size: A3	Document Number:	015_SoC JTAG & MISC	Rev: v0.6
Draw By: qxm	Date: Monday, October 09, 2023	Sheet: 15 of 16	

