PAGE LIST

REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR
0.1	28 Oct. 2022	First release	qxn
0.2	1 Nov. 2022	1. Remove unused nets 2. Use WKUP_I2C0 for PMIC 3. Add pull-down to VPP 4. Move eEMMC_RSTn to GPIO0_7 5. Add USER button for boot mode seletion 6. Try to add a CSI connector 7. Using processor boall numbers for signal name on P1 and P2 8. Change SoC to AM6232, change eMMC to 4GB, change DDR to 512MB	qxn
0.3	2 Nov. 2022	1. Remove CSI 2. Add SD card, move LDO0 to VDD_SD 3. Power the VPP with VDD_1V8 through a jumper 4. Connect P2.19 to AC20 instead	qxn
0.4	23 Dec.2022	1. Replace the ideal diode with LM73100RPWR 2. Replace EEPROM and ADC with MSPM0 3. Correct the boot settings 4. Connect AD24(MDC) to P2.17 and AB22(MDIO) to P2.20 which is same as pocketbealge.	qxn
0.5	28 Dec.2022	1. Add B5 (MCU_UART0_RXD) to P2_5. 2. Add A5 (MCU_UART0_TXD) to P2_7. 3. Add A18 (EXT_REFCLK1) to P1_10. 4. Add AD24 (MDIO0_MDC) to P2_1. 5. Add AB22 (MDIO0_MDIO) to P2_3.	qxn
0.6	09 Oct.2023	1. Add a buffer on reset 2. Correct typo - WKUP_I2C0_SDL 3. Add decoupling capacitors for LM73100 4. Change R44 to 100k 0.1% 5. Add pulldown resistors on RESETSTATz and PORZ_OUT 6. Correct the ideal diode control logic 7. Change C17 to 10uF 8. Change the SD card holder to lower profile with insertion detection 9. Move C11 to be in parallel with R260 10. Add pullup resistors to WKUP_I2C0 11. Add voltage divider on USB1_VBUS	qxn
0.7	05 Mar.2024	1. Add 3-pin JST connector for UART debug 2. Add buffer to debug UART	qxn
0.8	21 Nov.2024	1. Fix typo of 'debug' in schematic 2. Correct ideal diode control logic.	qxn
0.9	3 Dec.2024	1. Modify the boot order of non-emmc version, add a pull-down resistor on non-emmc version to force SD boot as primary boot	qxn
1.0	20 Dec.2024	1. Change USB_5V to charger input to prevent battery voltage flowing back to the charger input through the ideal diode, causing charger indicator light problems 2. Change the main MPU to AM6232ASGGHAALW which has PRU 3. Change ADC MCU to MSPM0L1105	qxn

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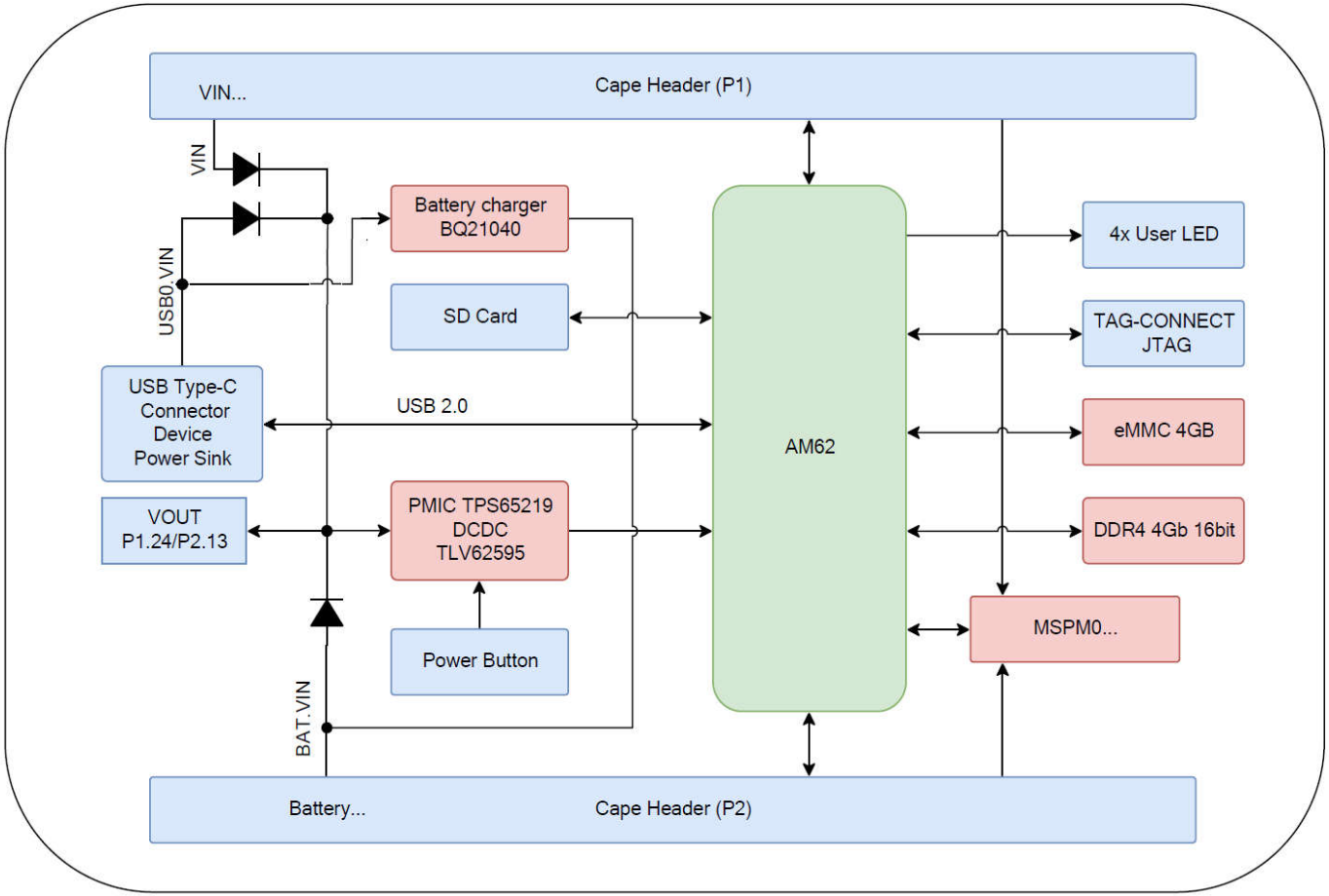
Title: PocketBeagle2

Size:	Document Number:	Rev:
A3	001_Revision History	v1.0

Draw By:	Date:	Sheet:
qxn	Friday, December 20, 2024	1 of 16

Block Diagram



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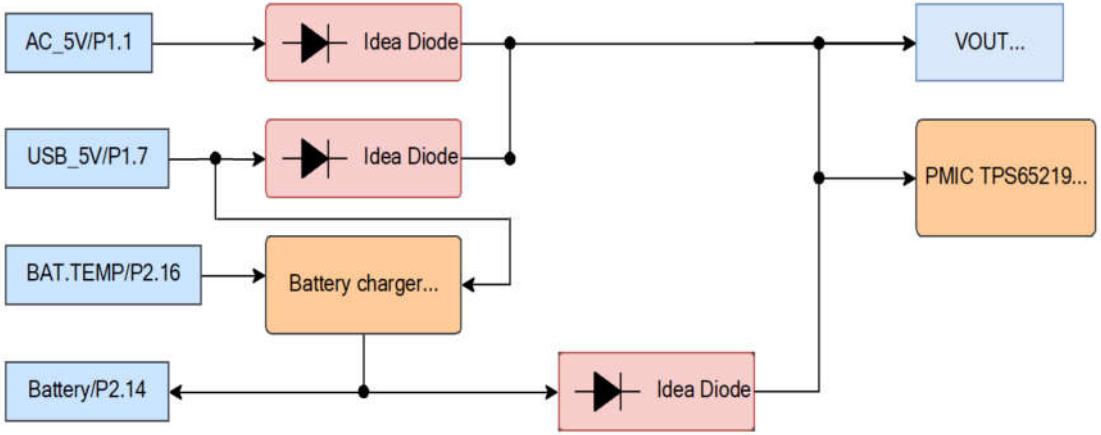
	Title: PocketBeagle2	
Size: A3	Document Number: 002_Block Diagram	Rev: v1.0
Draw By: qxn	Date: Thursday, December 05, 2024	Sheet: 2 of 16

Power tree



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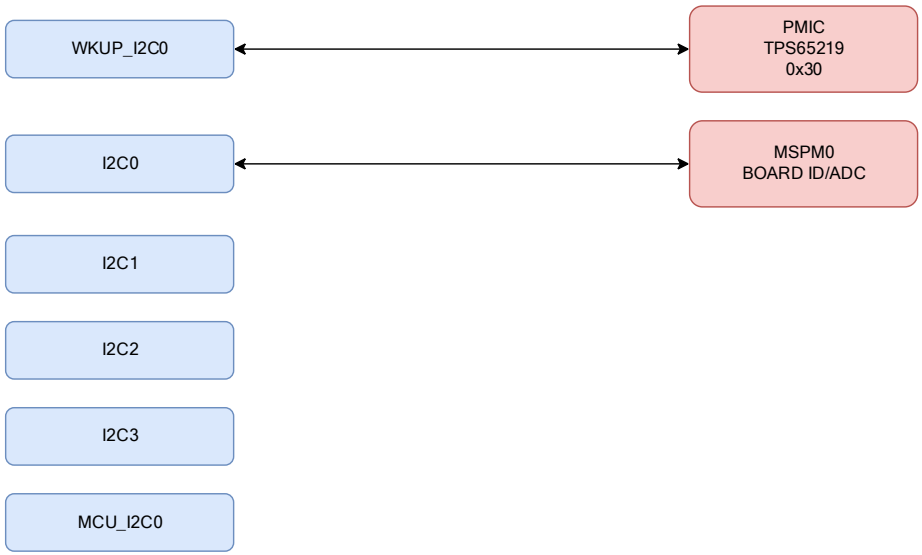
	Title: PocketBeagle2	
Size: A3	Document Number: 003_Power Tree	Rev: v1.0
Draw By: qxn	Date: Thursday, December 05, 2024	Sheet: 3 of 16

I2C Usage Diagram



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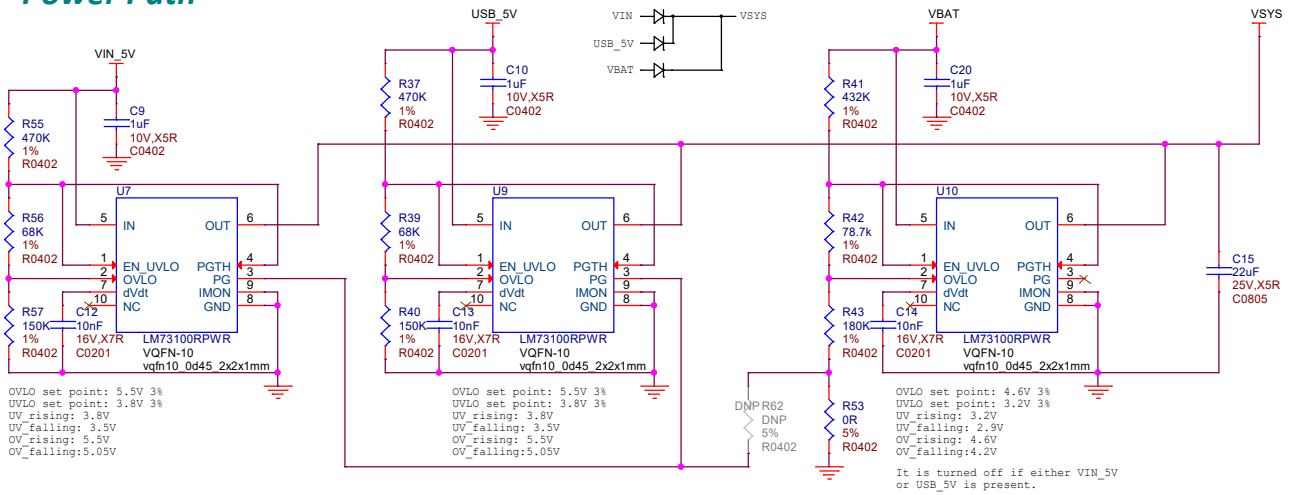
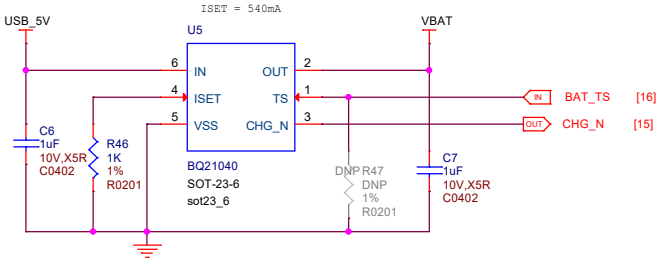
Size: A3	Document Number: 004_I2C Usage Diagram	Rev: v1.0
Draw By: qxn	Date: Wednesday, December 04, 2024	Sheet: 4 of 16

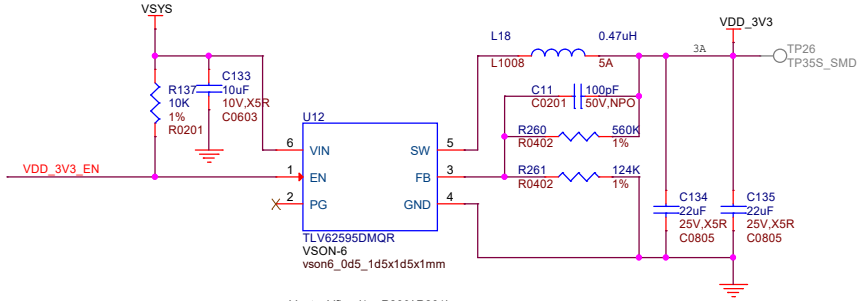
Power Path



Battery Charger



DCDC 3V3



PMIC

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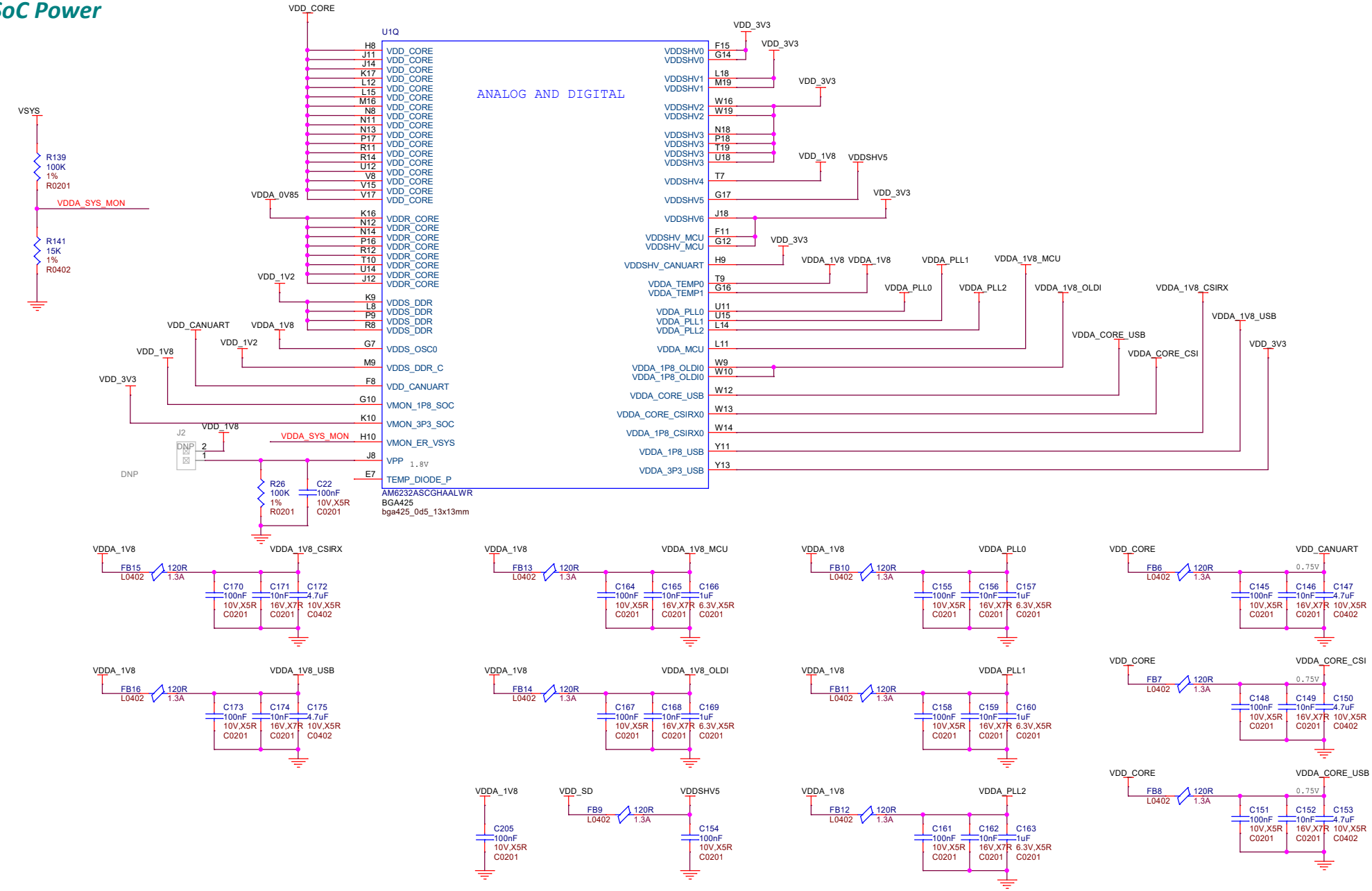
Size: A3	Document Number: 005_PMIC & Charger	Rev: v1.0
Draw By: qxn	Date: Thursday, December 05, 2024	Sheet: 5 of 16

SoC Power



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Rev: v1.0	
Draw By: qxn	Date: Friday, December 20, 2024
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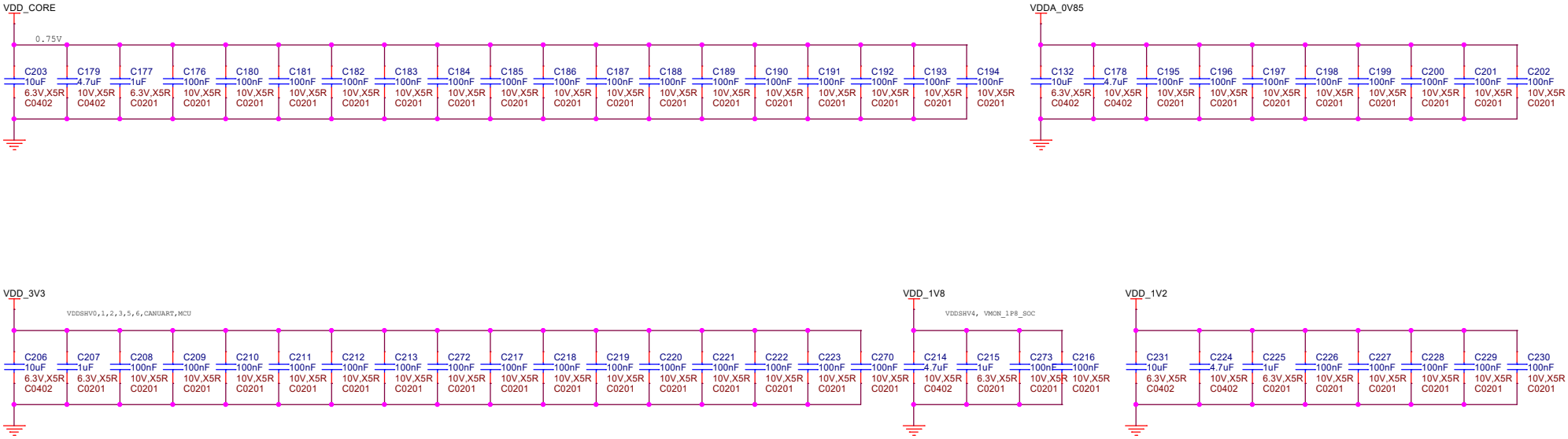
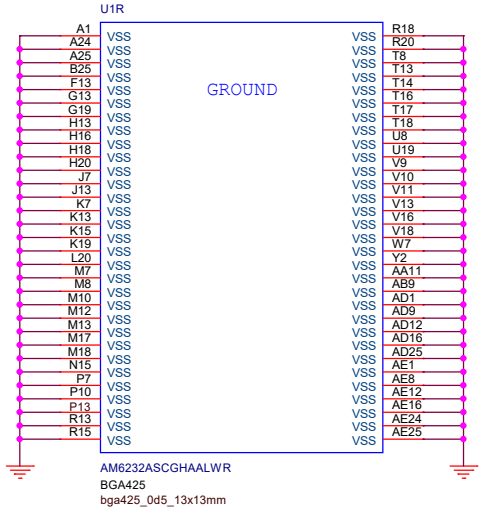
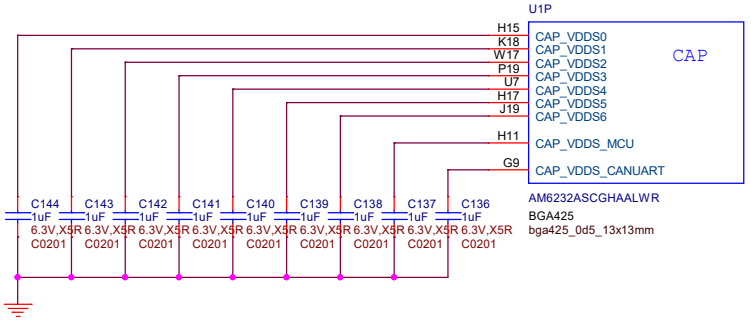
SoC DCAPs







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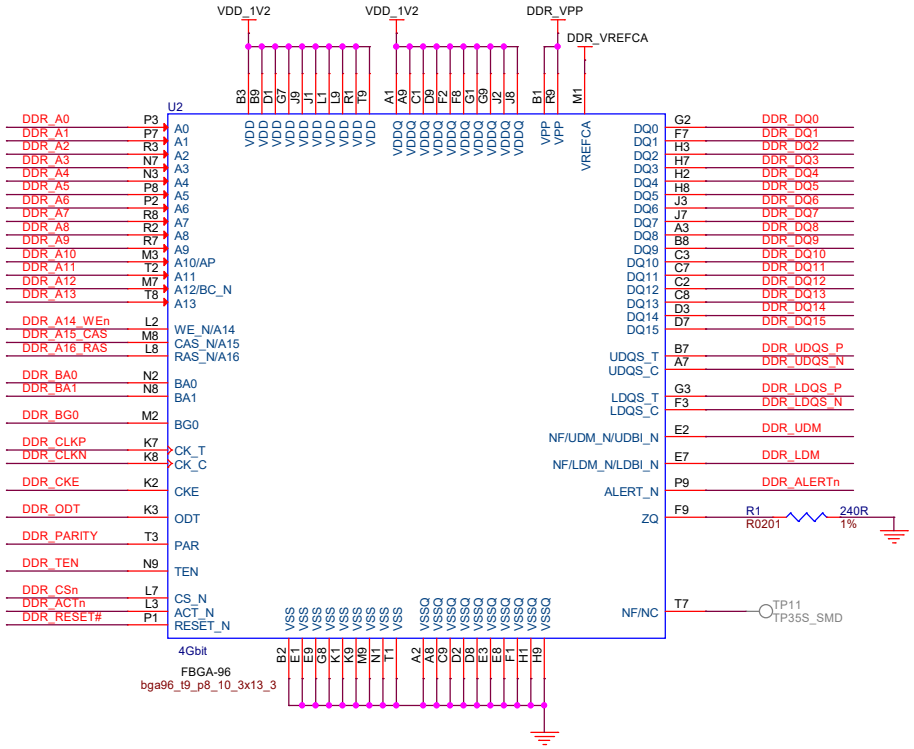
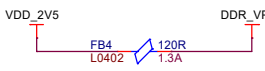
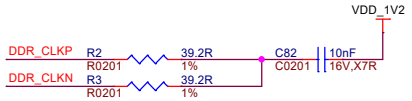
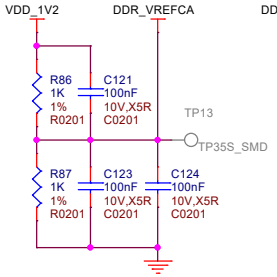
Draw By: qxn	Date: Friday, December 20, 2024	Sheet: 7 of 16

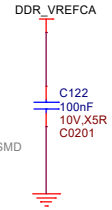
DDR4

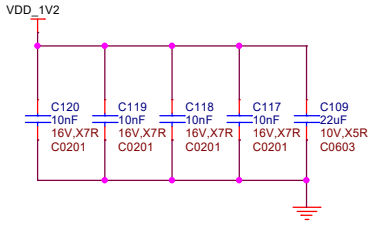


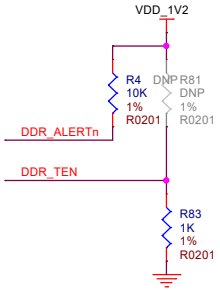


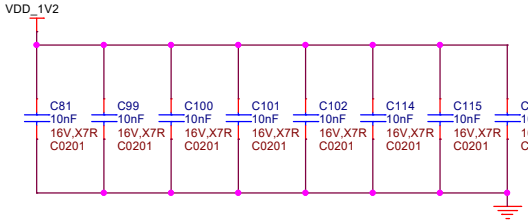


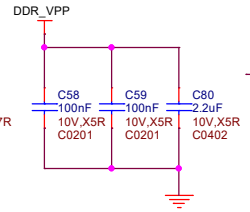


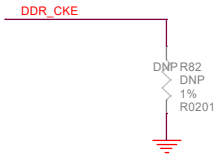




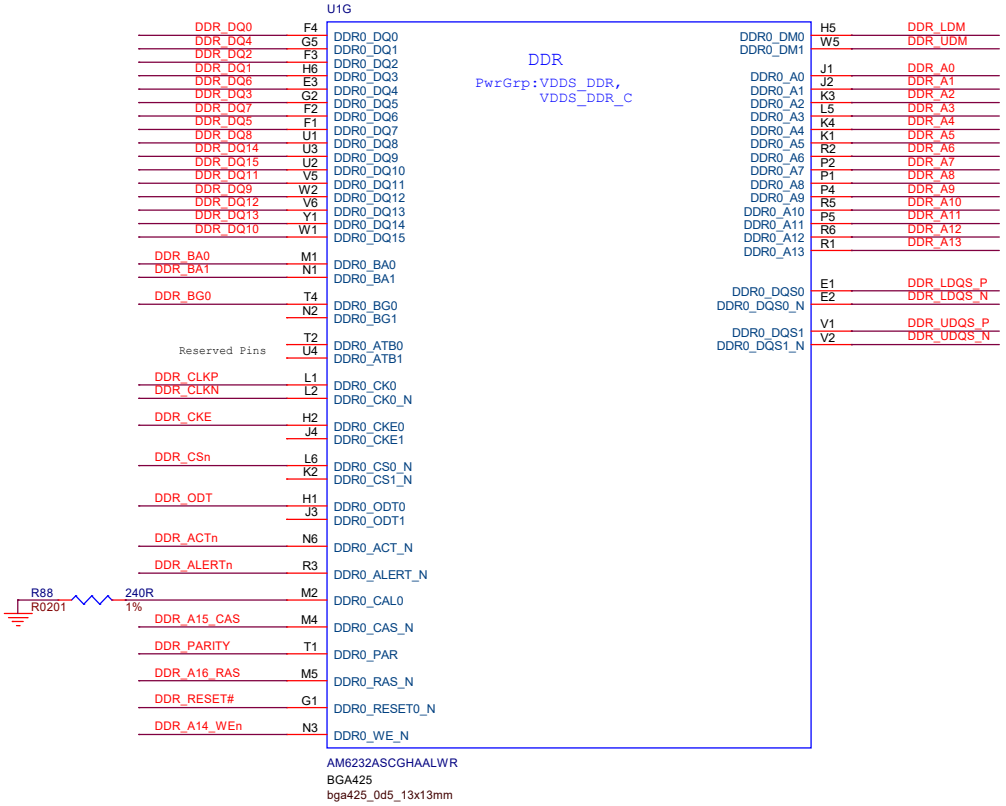


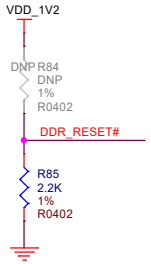






SoC DDR controller





NOTE: DDR DQ Lines Swapped Within Data Byte

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Size: A3	Document Number: 008_SoC DDR & DDR4	Rev: v1.0
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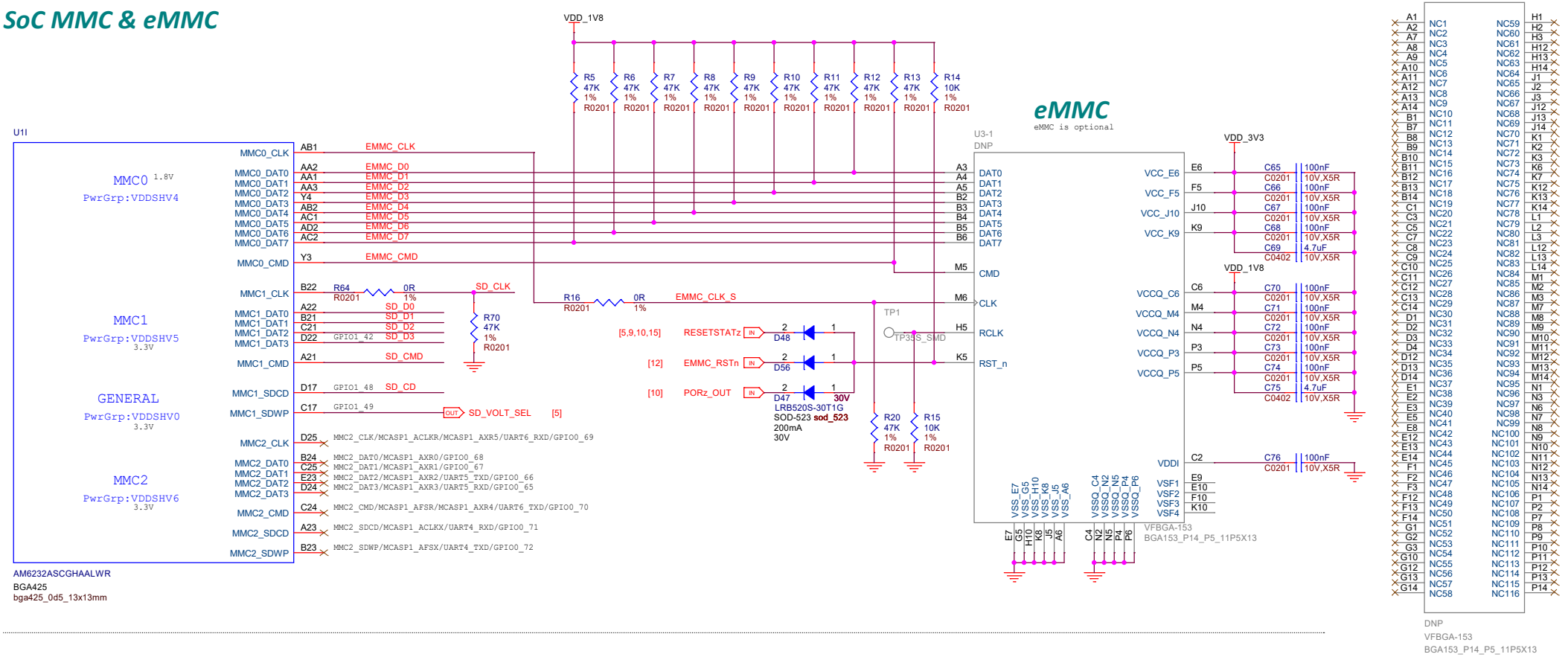
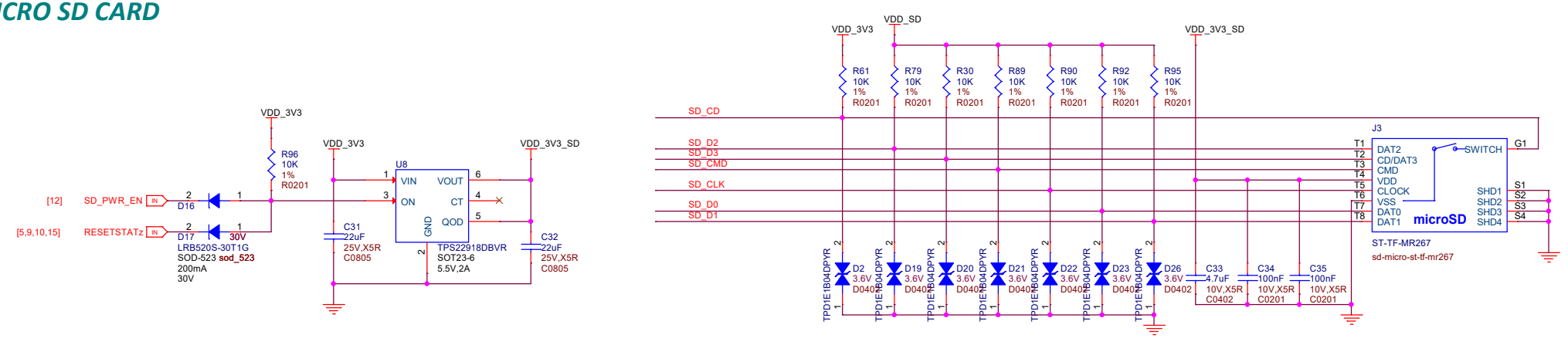
SoC MMC & eMMC



MICRO SD CARD



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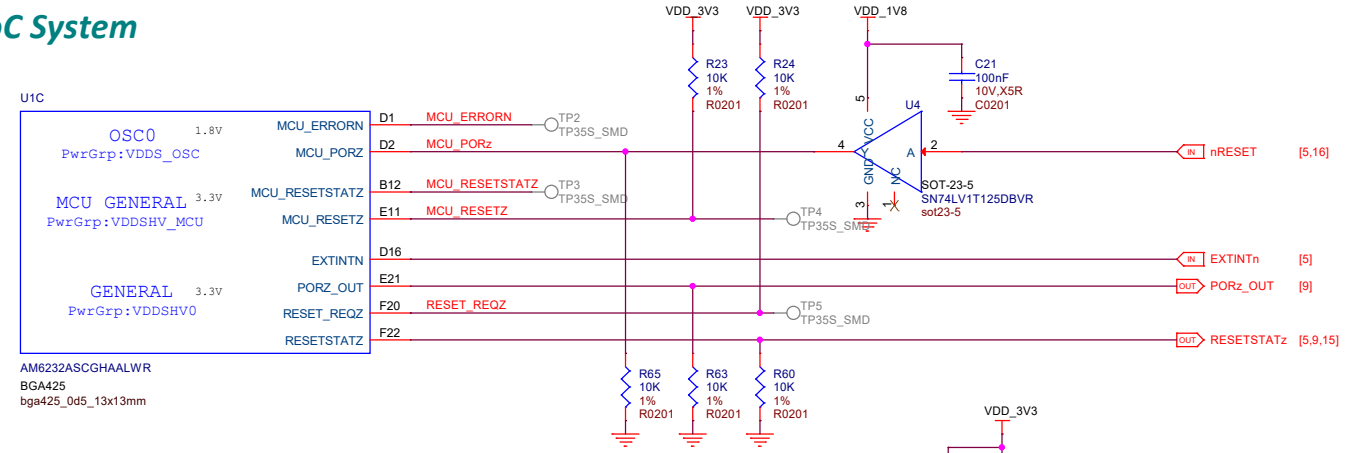
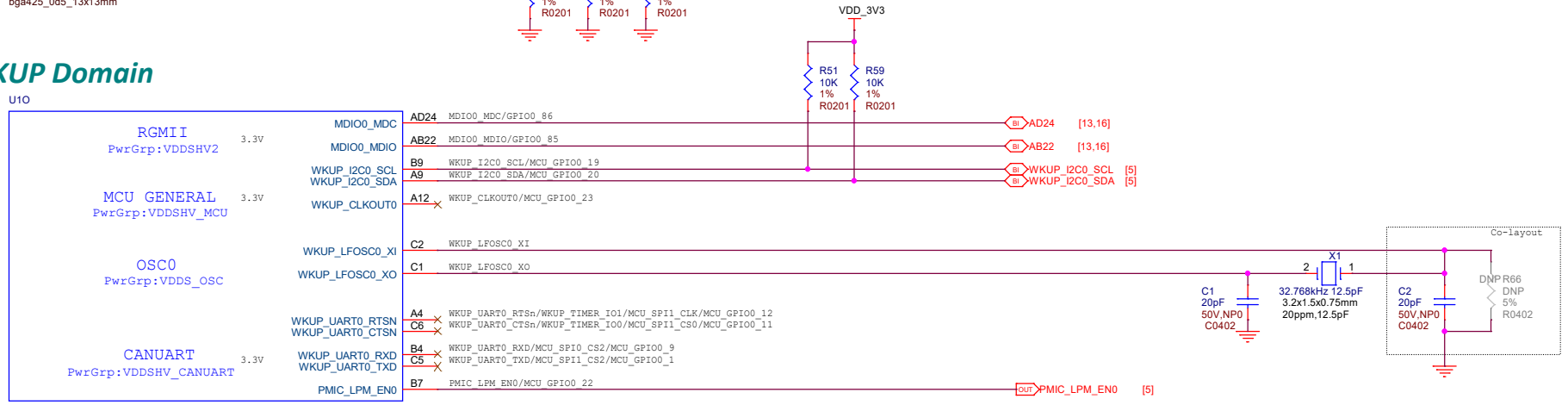
Draw By: qxn	Date: Friday, December 20, 2024	Sheet: 9 of 16

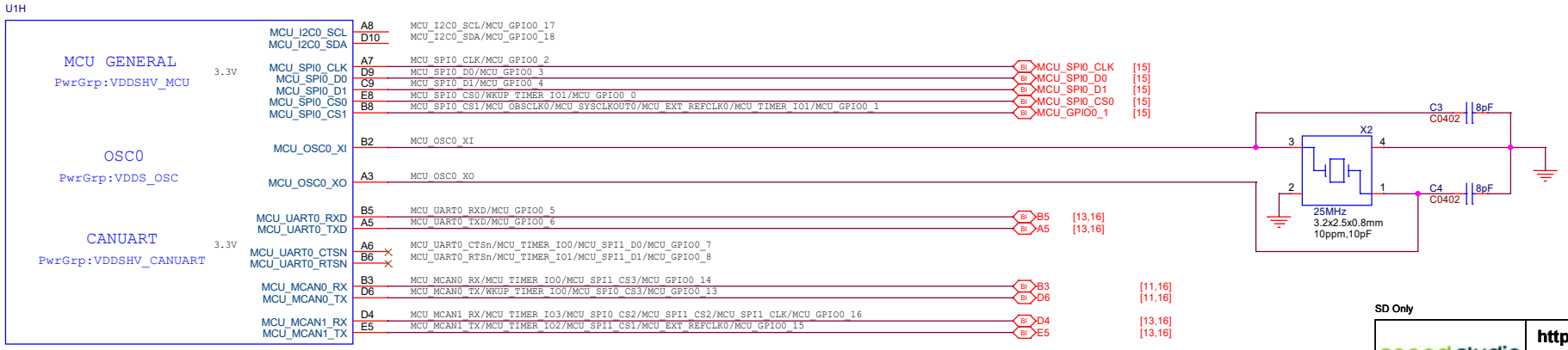
SoC System



WKUP Domain



MCU Domain



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Size: A3	Document Number: 010_SoC WKUP/MCU/System	Rev: v1.0
Draw By: qxn	Date: Friday, December 20, 2024	Sheet: 10 of 16

SoC GPIO

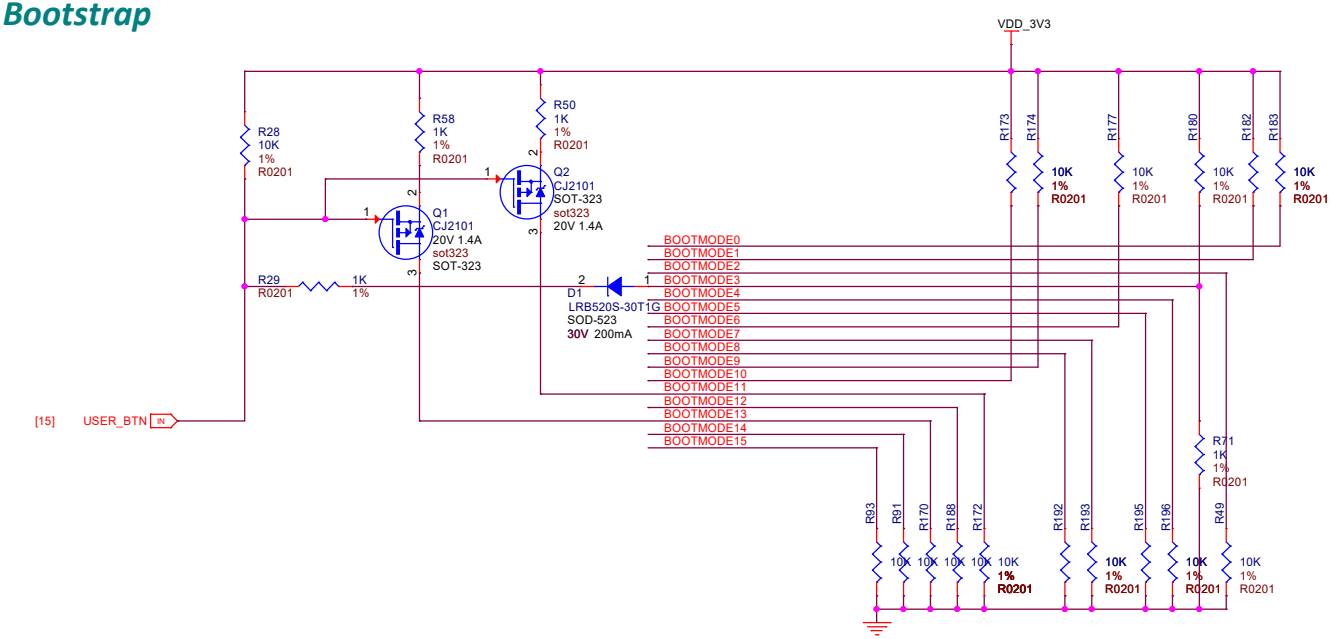
U1F

GPMC
PwrGrp:VDDSHV3
3.3V

GPMC0_CLK	P25	GPMC0_CLK/MCASP1_AXR3/GPMC0_FCLK_MUX/PR0_PRU0_GPO8/PR0_PRU0_GPI8/TRC_DATA6/GPIO0_31		
GPMC0_AD0	M25	GPMC0_AD0/PR0_PRU1_GPO8/PR0_PRU1_GPI8/MCASP2_AXR4/PR0_PRU0_GPO0/PR0_PRU0_GPI0/TRC_CLK/GPIO0_15/BOOTMODE00	BOOTMODE0	
GPMC0_AD1	N23	GPMC0_AD1/PR0_PRU1_GPO9/PR0_PRU1_GPI9/MCASP2_AXR5/PR0_PRU0_GPO1/PR0_PRU0_GPI1/TRC_CTL/GPIO0_16/BOOTMODE01	BOOTMODE1	
GPMC0_AD2	N24	GPMC0_AD2/PR0_PRU1_GPO10/PR0_PRU1_GPI10/MCASP2_AXR6/PR0_PRU0_GPO2/PR0_PRU0_GPI2/TRC_DATA0/GPIO0_17/BOOTMODE02	BOOTMODE2	
GPMC0_AD3	N25	GPMC0_AD3/PR0_PRU1_GPO11/PR0_PRU1_GPI11/MCASP2_AXR7/PR0_PRU0_GPO3/PR0_PRU0_GPI3/TRC_DATA1/GPIO0_18/BOOTMODE03	BOOTMODE3	
GPMC0_AD4	P24	GPMC0_AD4/PR0_PRU1_GPO12/PR0_PRU1_GPI12/MCASP2_AXR8/PR0_PRU0_GPO4/PR0_PRU0_GPI4/TRC_DATA2/GPIO0_19/BOOTMODE04	BOOTMODE4	
GPMC0_AD5	P22	GPMC0_AD5/PR0_PRU1_GPO13/PR0_PRU1_GPI13/MCASP2_AXR9/PR0_PRU0_GPO5/PR0_PRU0_GPI5/TRC_DATA3/GPIO0_20/BOOTMODE05	BOOTMODE5	
GPMC0_AD6	P21	GPMC0_AD6/PR0_PRU1_GPO14/PR0_PRU1_GPI14/MCASP2_AXR10/PR0_PRU0_GPO6/PR0_PRU0_GPI6/TRC_DATA4/GPIO0_21/BOOTMODE06	BOOTMODE6	
GPMC0_AD7	R23	GPMC0_AD7/PR0_PRU1_GPO15/PR0_PRU1_GPI15/MCASP2_AXR11/PR0_PRU0_GPO7/PR0_PRU0_GPI7/TRC_DATA5/GPIO0_22/BOOTMODE0	BOOTMODE7	
GPMC0_AD8	R24	GPMC0_AD8/VOUT0_DATA16/UART2_RXD/MCASP2_AXR0/PR0_PRU1_GPO0/PR0_PRU1_GPI0/GPIO0_23/BOOTMODE08	BOOTMODE8	
GPMC0_AD9	R25	GPMC0_AD9/VOUT0_DATA17/UART2_TXD/MCASP2_AXR1/PR0_PRU1_GPO1/PR0_PRU1_GPI1/GPIO0_24/BOOTMODE09	BOOTMODE9	
GPMC0_AD10	T25	GPMC0_AD10/VOUT0_DATA18/UART3_RXD/MCASP2_AXR2/PR0_PRU1_GPO2/PR0_PRU1_GPI2/GPIO0_25/OBSCLK0/BOOTMODE10	BOOTMODE10	
GPMC0_AD11	R21	GPMC0_AD11/VOUT0_DATA19/UART3_TXD/MCASP2_AXR3/PR0_PRU1_GPO3/PR0_PRU1_GPI3/TRC_DATA23/GPIO0_26/BOOTMODE1	BOOTMODE11	
GPMC0_AD12	T22	GPMC0_AD12/VOUT0_DATA20/UART4_RXD/MCASP2_AFSX/PR0_PRU0_GPO0/PR0_PRU0_GPI0/TRC_DATA22/GPIO0_27/BOOTMODE12	BOOTMODE12	
GPMC0_AD13	T24	GPMC0_AD13/VOUT0_DATA21/UART4_TXD/MCASP2_ACLKX/PR0_PRU0_GPO1/PR0_PRU0_GPI1/TRC_DATA21/GPIO0_28/BOOTMODE13	BOOTMODE13	
GPMC0_AD14	U25	GPMC0_AD14/VOUT0_DATA22/UART5_RXD/MCASP2_AFSR/PR0_PRU0_GPO2/PR0_PRU0_GPI2/TRC_DATA20/GPIO0_29/UART2_CTSn/BOOTMODE14	BOOTMODE14	
GPMC0_AD15	U24	GPMC0_AD15/VOUT0_DATA23/UART5_TXD/MCASP2_ACLKR/PR0_PRU0_GPO3/PR0_PRU0_GPI3/TRC_DATA19/GPIO0_30/UART2_RTSn/BOOTMODE15	BOOTMODE15	
GPMC0_CSN0	M21	GPMC0_CSn0/MCASP2_AXR14/PR0_PRU0_GPO17/PR0_PRU0_GPI17/TRC_DATA15/GPIO0_41		
GPMC0_CSN1	L21	GPMC0_CSn1/PR0_PRU1_GPO16/PR0_PRU1_GPI16/MCASP2_AXR15/PR0_PRU0_GPO18/PR0_PRU0_GPI18/TRC_DATA16/GPIO0_42		
GPMC0_CSN2	K22	GPMC0_CSn2/I2C2_SCL/MCASP1_AXR4/UART4_RXD/PR0_PRU0_GPO19/PR0_PRU0_GPI19/TRC_DATA17/GPIO0_43/MCASP1_AFSR	BI K22	[10,16]
GPMC0_CSN3	K24	GPMC0_CSn3/I2C2_SDA/GPMC0_A20/UART4_TXD/MCASP1_AXR5/TRC_DATA18/GPIO0_44/MCASP1_ACLKR	BI K24	[10,16]
GPMC0_ADVN_ALE	L23	GPMC0_ADVn_ALE/MCASP1_AXR2/PR0_PRU0_GPO9/PR0_PRU0_GPI9/TRC_DATA7/GPIO0_32		
GPMC0_BE0N_CLE	M24	GPMC0_BE0n_CLE/MCASP1_ACLKX/PR0_PRU0_GPO12/PR0_PRU0_GPI12/TRC_DATA10/GPIO0_35		
GPMC0_BE1N	N20	GPMC0_BE1n/MCASP2_AXR12/PR0_PRU0_GPO13/PR0_PRU0_GPI13/TRC_DATA11/GPIO0_36	BI N20	[16]
GPMC0_DIR	M22	GPMC0_DIR/PR0_ECAP0_IN_APWM_OUT/MCASP2_AXR13/PR0_PRU0_GPO16/PR0_PRU0_GPI16/TRC_DATA14/GPIO0_40/EQEP2_S	BI M22	[13,16]
GPMC0_WAIT0	U23	GPMC0_WAIT0/MCASP1_AFSX/PR0_PRU0_GPO14/PR0_PRU0_GPI14/TRC_DATA12/GPIO0_37		
GPMC0_WAIT1	V25	GPMC0_WAIT1/VOUT0_EXTPCLKIN/GPMC0_A21/UART6_RXD/GPIO0_38/EQEP2_I		
GPMC0_WPN	K25	GPMC0_WPn/AUDIO_EXT_REFCLK1/GPMC0_A22/UART6_TXD/PR0_PRU0_GPO15/PR0_PRU0_GPI15/TRC_DATA13/GPIO0_3		
GPMC0_OEN_REN	L24	GPMC0_OEn_REn/MCASP1_AXR1/PR0_PRU0_GPO10/PR0_PRU0_GPI10/TRC_DATA8/GPIO0_33		
GPMC0_WEN	L25	GPMC0_WEn/MCASP1_AXR0/PR0_PRU0_GPO11/PR0_PRU0_GPI11/TRC_DATA9/GPIO0_34		

AM6232ASCGHAALWR
BGA425
bga425_0d5_13x13mm

Bootstrap




```
EMMC Version
Button Not-pressd:
1, PLL Config    B[2:0] = 0b011     : Ref Colck -> 25MHz
2, Primarry Boot B[9:3] = 0b1001001 : eMMC Boot
3, Backup Boot   B[13:10] = 0b0001  : USB DFU Boot

Button Pressd:
1, PLL Config    B[2:0] = 0b011     : Ref Colck -> 25MHz
2, Primarry Boot B[9:3] = 0b1001000 : SDCard FS Boot
3, Backup Boot   B[13:10] = 0b1011  : UART Boot


SD Version
Button Not-pressd:
1, PLL Config    B[2:0] = 0b011     : Ref Colck -> 25MHz
2, Primarry Boot B[9:3] = 0b1001000 : SDCard FS Boot
3, Backup Boot   B[13:10] = 0b0001  : USB DFU Boot

Button Pressd:
1, PLL Config    B[2:0] = 0b011     : Ref Colck -> 25MHz
2, Primarry Boot B[9:3] = 0b1001000 : SDCard FS Boot
3, Backup Boot   B[13:10] = 0b1011  : UART Boot
```

SD Only

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RGMII

U1M

RGMII1 3.3V
PwrGrp:VDDSHV2

RGMII1_RD0	AB17	RGMII1_RD0/RMII1_RXD0/GPIO0_81
RGMII1_RD1	AC17	RGMII1_RD1/RMII1_RXD1/GPIO0_82
RGMII1_RD2	AB16	RGMII1_RD2/PR0_UART0_RTSn/GPIO0_83
RGMII1_RD3	AA15	RGMII1_RD3/GPIO0_84
RGMII1_RXC	AD17	RGMII1_RXC/RMII1_REF_CLK/PR0_UART0_CTSn/GPIO0_80
RGMII1_RX_CTL	AE17	RGMII1_RX_CTL/RMII1_RX_ER/GPIO0_79
RGMII1_TD0	AE20	RGMII1_TD0/RMII1_TXD0/GPIO0_75
RGMII1_TD1	AD20	RGMII1_TD1/RMII1_TXD1/GPIO0_76
RGMII1_TD2	AE18	RGMII1_TD2/PR0_UART0_RXD/GPIO0_77
RGMII1_TD3	AD18	RGMII1_TD3/PR0_UART0_TXD/GPIO0_78
RGMII1_TXC	AE19	RGMII1_TXC/RMII1_CRS_DV/GPIO0_74
RGMII1_TX_CTL	AD19	RGMII1_TX_CTL/RMII1_TX_EN/GPIO0_73

AE18 [13,16]
AD18 [13,16]

AM6232ASCGHAALWR
BGA425
bga425_0d5_13x13mm

U1S

RGMII2 3.3V
PwrGrp:VDDSHV2

RGMII2_RD0	AE23	RGMII2_RD0/RMII2_RXD0/MCASP2_AXR2/PR0_PRU0_GPO2/PR0_PRU0_GPI2/PR0_UART0_RTSn/GPIO1_3
RGMII2_RD1	AB20	RGMII2_RD1/RMII2_RXD1/MCASP2_AFSR/PR0_PRU0_GPO3/PR0_PRU0_GPI3/MCASP2_AXR7/GPIO1_4
RGMII2_RD2	AC21	RGMII2_RD2/MCASP2_AXR0/PR0_PRU0_GPO4/PR0_PRU0_GPI4/PR0_UART0_RXD/GPIO1_5/EQEP2_A
RGMII2_RD3	AE22	RGMII2_RD3/AUDIO_EXT_REFCLK0/PR0_PRU0_GPO16/PR0_PRU0_GPI16/PR0_UART0_TXD/GPIO1_6/EQEP2_B
RGMII2_RXC	AD23	RGMII2_RXC/RMII2_REF_CLK/MCASP2_AXR1/PR0_PRU0_GPO1/PR0_PRU0_GPI1/PR0_ECAP0_SYNC_IN/GPIO1_2
RGMII2_RX_CTL	AD22	RGMII2_RX_CTL/RMII2_RX_ER/MCASP2_AXR3/PR0_PRU0_GPO0/PR0_PRU0_GPI0/GPIO1_1
RGMII2_TD0	Y18	RGMII2_TD0/RMII2_TXD0/MCASP2_AXR6/PR0_PRU1_GPO2/PR0_PRU1_GPI2/GPIO0_89
RGMII2_TD1	AA18	RGMII2_TD1/RMII2_TXD1/MCASP2_ACLKR/PR0_PRU1_GPO3/PR0_PRU1_GPI3/MCASP2_AXR8/GPIO0_90
RGMII2_TD2	AD21	RGMII2_TD2/MCASP2_AFSX/PR0_PRU1_GPO4/PR0_PRU1_GPI4/PR0_ECAP0_IN_APWM_OUT/GPIO0_91/EQEP2_I
RGMII2_TD3	AC20	RGMII2_TD3/MCASP2_ACLKX/PR0_PRU1_GPO16/PR0_PRU1_GPI16/PR0_ECAP0_SYNC_OUT/PR0_UART0_CTSn/GPIO1_0/EQEP2_S
RGMII2_TXC	AE21	RGMII2_TXC/RMII2_CRS_DV/MCASP2_AXR5/PR0_PRU1_GPO1/PR0_PRU1_GPI1/GPIO0_88
RGMII2_TX_CTL	AA19	RGMII2_TX_CTL/RMII2_TX_EN/MCASP2_AXR4/PR0_PRU1_GPO0/PR0_PRU1_GPI0/GPIO0_87

Y18 [13,16]
AA18 [13,16]
AD21 [16]
AC20 [16]
AE21 [16]
AA19 [13,15,16]

AM6232ASCGHAALWR
BGA425
bga425_0d5_13x13mm

OSPI

U1J

OSPI 3.3V
PwrGrp:VDDSHV1

OSPI0_CLK	H24	OSPI0_CLK/GPIO0_0
OSPI0_D0	E25	OSPI0_D0/GPIO0_3
OSPI0_D1	G24	OSPI0_D1/GPIO0_4
OSPI0_D2	F25	OSPI0_D2/GPIO0_5
OSPI0_D3	F24	OSPI0_D3/GPIO0_6
OSPI0_D4	J23	OSPI0_D4/SPI1_CS0/MCASP1_AXR1/UART6_RXD/GPIO0_7
OSPI0_D5	J25	OSPI0_D5/SPI1_CLK/MCASP1_AXR0/UART6_TXD/GPIO0_8
OSPI0_D6	H25	OSPI0_D6/SPI1_D0/MCASP1_ACLKX/UART6_RTSn/GPIO0_9
OSPI0_D7	J22	OSPI0_D7/SPI1_D1/MCASP1_AFSX/UART6_CTSn/GPIO0_10
OSPI0_CSN0	F23	OSPI0_CSn0/GPIO0_11
OSPI0_CSN1	G21	OSPI0_CSn1/GPIO0_12
OSPI0_CSN2	H21	OSPI0_CSn2/SPI1_CS1/OSPI0_RESET_OUT1/MCASP1_AFSR/MCASP1_AXR2/UART5_RXD/GPIO0_13
OSPI0_CSN3	E24	OSPI0_CSn3/OSPI0_RESET_OUT0/OSPI0_ECC_FAIL/MCASP1_ACLKR/MCASP1_AXR3/UART5_TXD/GPIO0_14
OSPI0_DQS	J24	OSPI0_DQS/UART5_CTSn/GPIO0_2
OSPI0_LBCLKO	G25	OSPI0_LBCLKO/UART5_RTSn/GPIO0_1

H24 → OUT SD_PWR_EN [9]
E25 → OUT GPIO0_3 [15]
G24 → OUT GPIO0_4 [15]
F25 → OUT GPIO0_5 [15]
F24 → OUT GPIO0_6 [15]
J23 → IN J23 [15]
J25 → OUT J25 [15]
F23 → OUT EMMC_RSTn [9]

AM6232ASCGHAALWR
BGA425
bga425_0d5_13x13mm

SD Only

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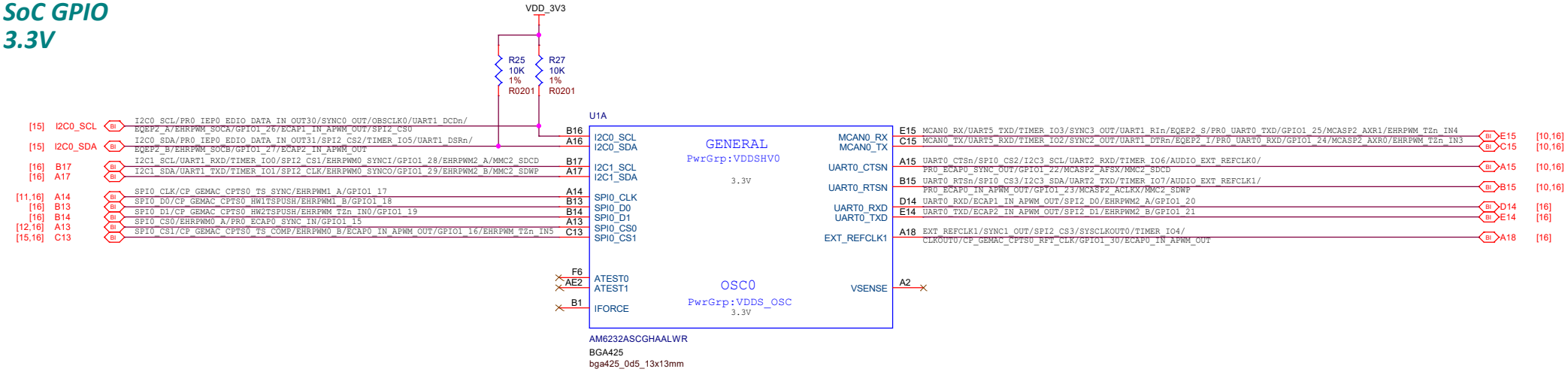
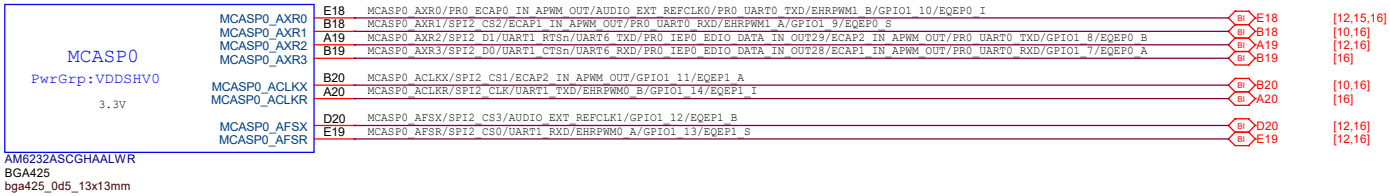
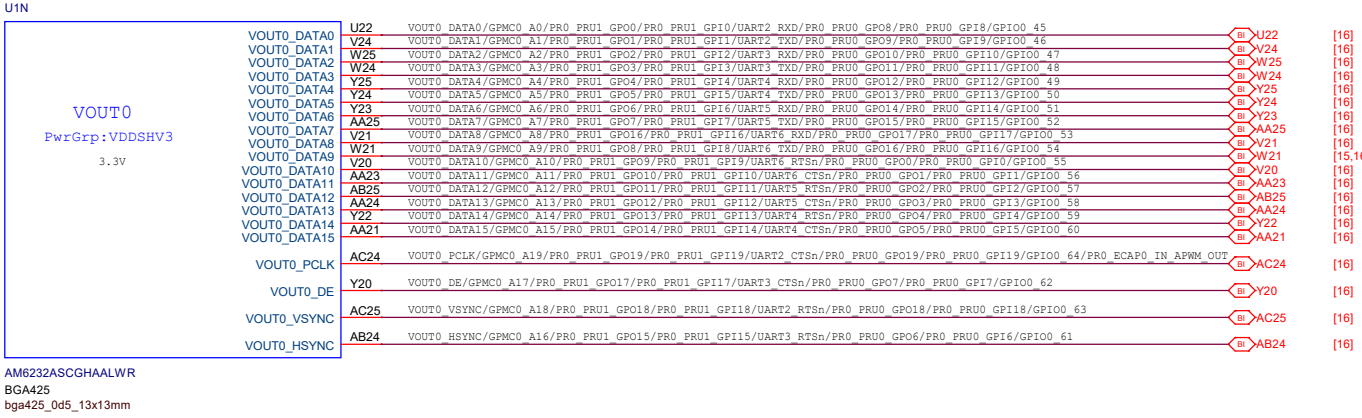
SoC GPIO 3.3V







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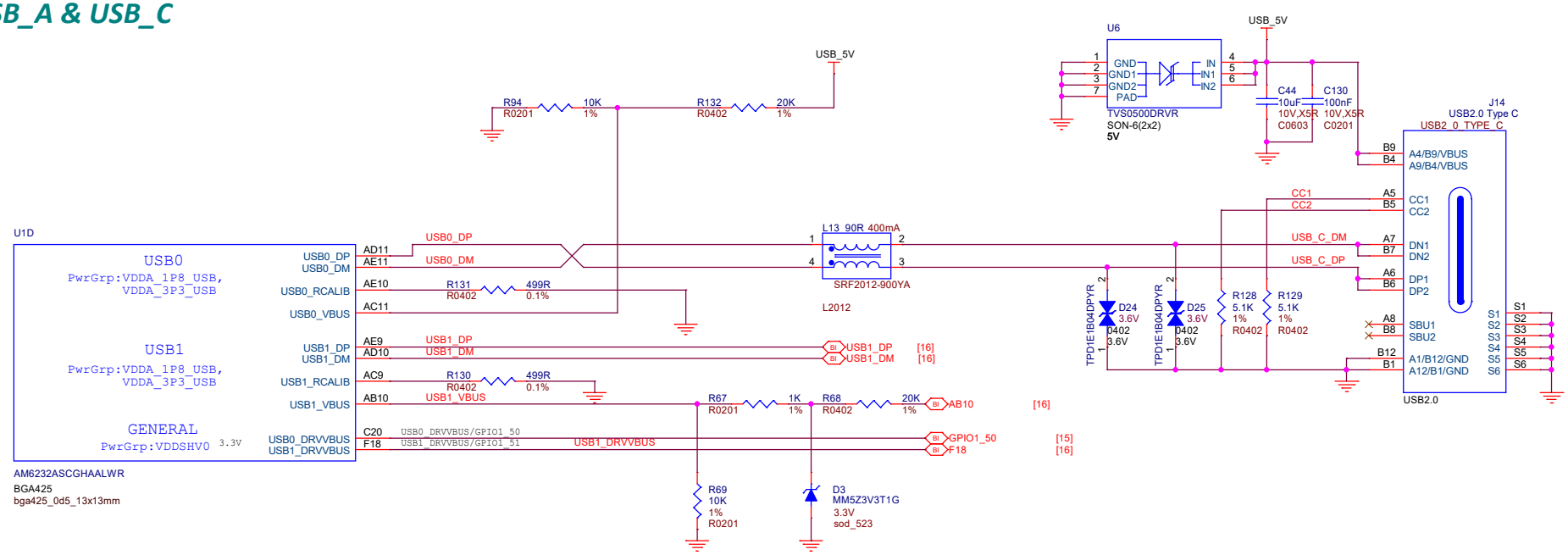
USB_A & USB_C



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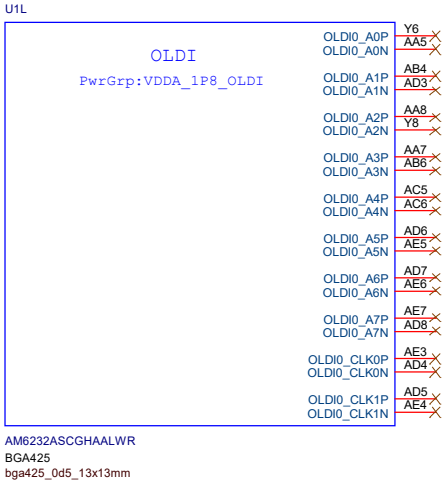

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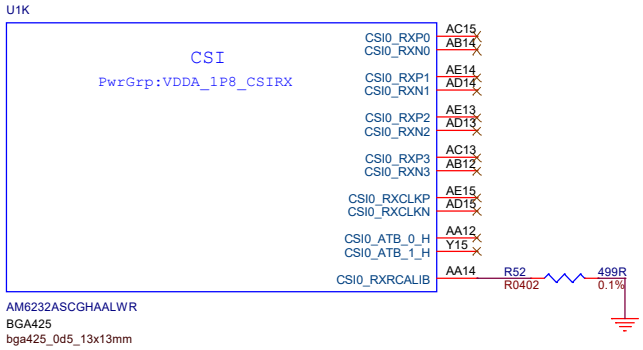

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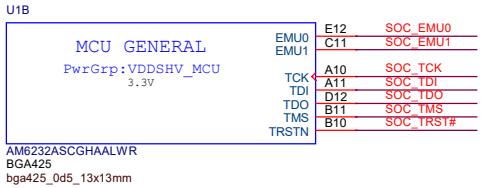
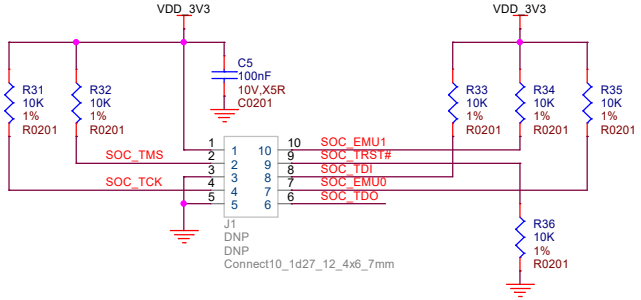
JTAG



Tag-Connect



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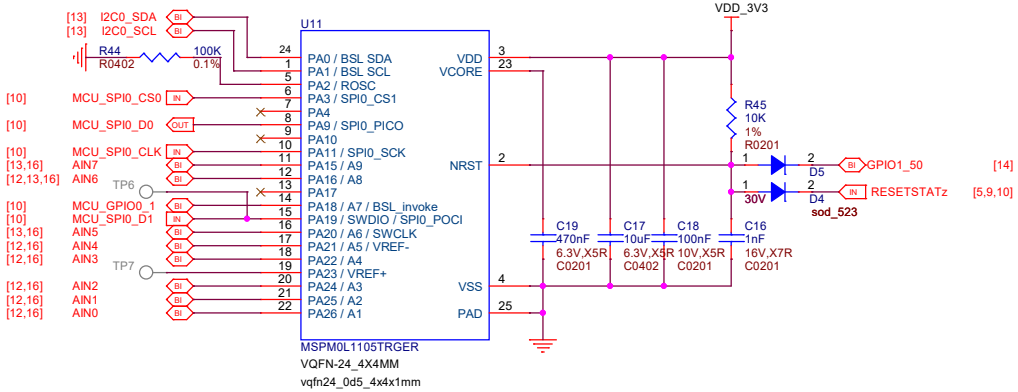
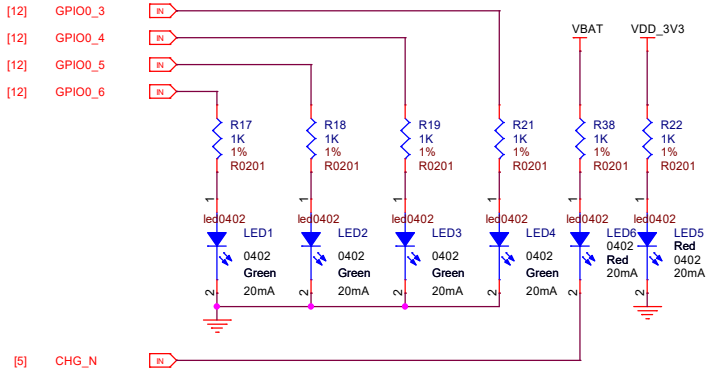
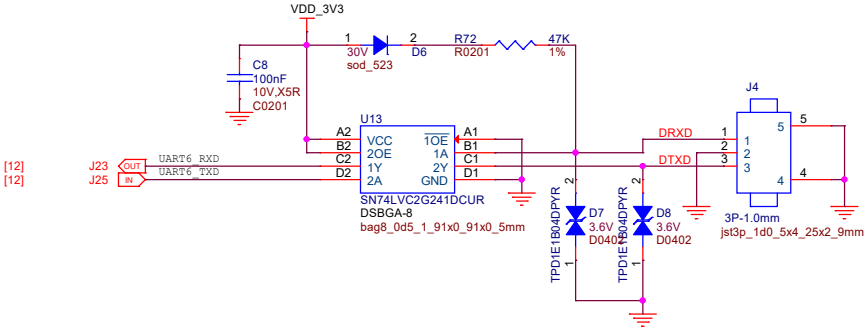


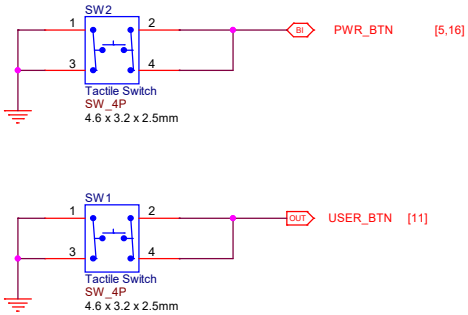
LEDs



Debug



Power Button



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