EPFL

ROW DECODER IMPLEMENTATION

Fundamentals of VLSI 2023

Project Presentation

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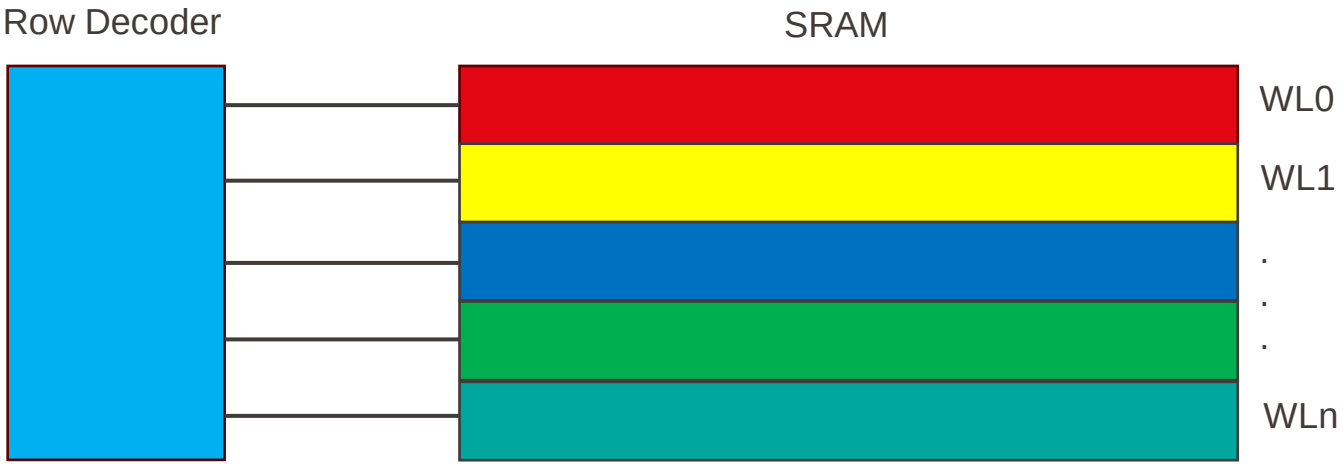
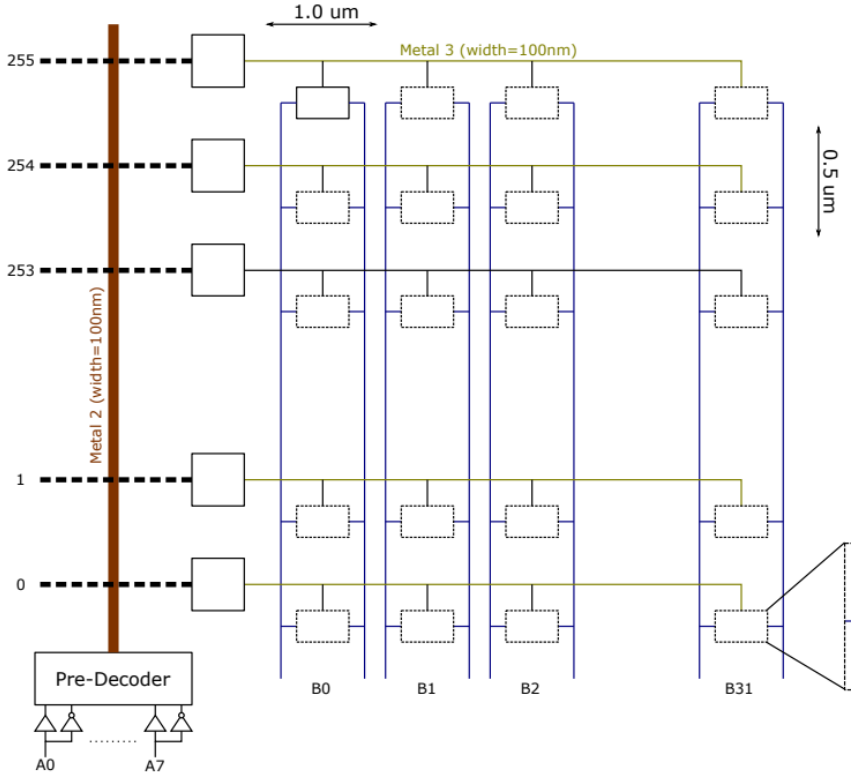
Summary of the Problem: Row Decoder

- Row Decoders are a peripheral of SRAM's that allows to access the right Word Line
- High level structure: Pre-decoder and Post-decoder
- Three architectures are explored: no pre-decoder, 2 bit pre-decoder, 4-bit pre-decoder.



Technology Parameters: Metal Wires



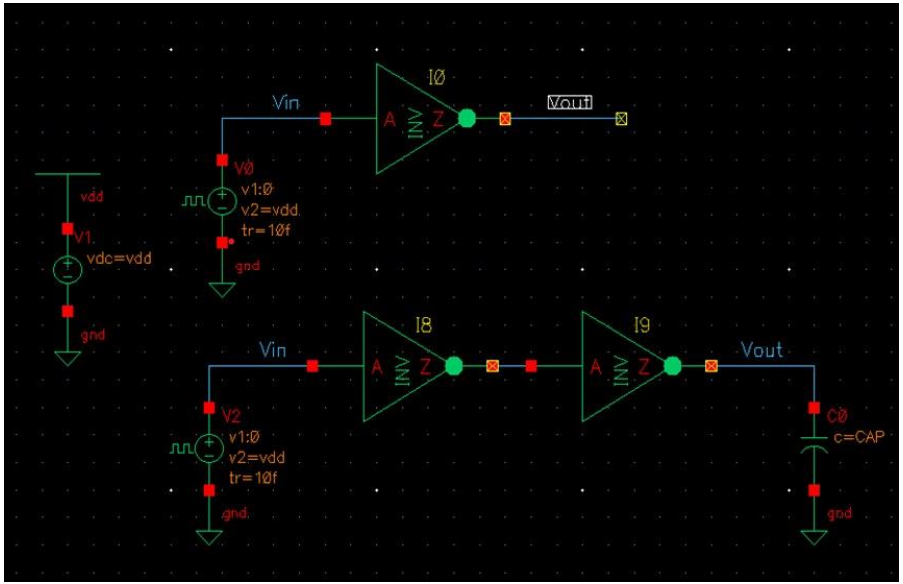
PreDec to PostDec Wire

- Metal 2
- Length = heigth of bit-cell * 256
- Coupling Worst Case: one wire switches and the two adjacent wires switch with opposite polarity → $4 * C_c$

Word Line

- Metal 3
- Length = width of bit-cell * 32
- Coupling Worst Case: the word line being deselected is adjacent to the selected one → $3 * C_c$

Values Extractions



Effrot delay of the inverter:

$$\tau_f = 3.717\text{ps}$$

Intrinsic delay of the inverter:

$$\tau_p = 6.180\ ps$$

Intrinsic capacitance of an inverter:

$$C_{int}^{INV} = 0.5e^{-15}\ F$$

Intrinsic capacitance of a transistor:

$$C_0^{diff} = \frac{C_{int}^{INV}}{(\beta+1)} = 0.14e^{-15}F$$

NOTE:

For advanced node: $C_0 = C_0^{diff}$

β=2.5

Technology Parameters: Values Obtained

Quantity	Formula	Value
C_0	-	0.14 fF
C_0^{diff}	-	0.14 fF
C_{bitcell}	$C_0 * 32 * 2$	8.96 fF
C_{wire}^{M2}	$L_{M2} * (W_{M2} * C_{pp}^{M2} + C_F^{M2})$	1.7664 fF
C_c^{M2}	$4 * C_c^{M2} * \frac{S_0}{S_{M2}} * L_{M2}$	2.0504 fF
R_{M2}	$R_0^{M2} * \frac{L_{M2}}{W_{M2}}$	134.4 Ω
C_{wire}^{M3}	$L_{M3} * (W_{M3} * C_{pp}^{M3} + C_F^{M3})$	0.3648 fF
C_c^{M3}	$4 * C_c^{M3} * \frac{S_0}{S_{M3}} * L_{M3}$	0.4080 fF
R_{M3}	$R_0^{M3} * \frac{L_{M3}}{W_{M3}}$	33.6 Ω

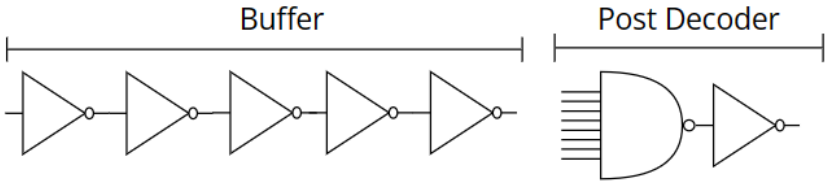
Technology Parameters: Values Obtained

Quantity	Formula	Value
C_{tot}^{M3}	$C_{wire}^{M3} + C_c^{M3}$	1.74 fF
C_{tot}^{M2}	$C_{wire}^{M2} + C_c^{M2}$	38.1 fF
τ_{M3}	$\frac{0.69}{2} * R_{M3} * C_{tot}^{M3}$	0.02 ps
τ_{M2}	$\frac{0.69}{2} * R_{M2} * C_{tot}^{M2}$	1.76 ps

Notation

- Every resistance is expressed in Ohm
- Every delay is expressed in pico seconds
- At first the sizes of the complete circuit are calculated without interconnection delay. Then they are taken into account as additional fanout to the pre-decoder, so it is necessary to resize only the first part of the circuit
- C_{WIRE} represents the total capacitance of the new fanout, so the total input capacitance of the gate after the wire (with possible branches) and the Pre2Post wire capacitance
- $C_{WL} = C_{tot}^{M3} + C_{bitcell}$ → Considers the wire delay and the bit cell

Eight 1-2 pre-decoders: 1st no wire

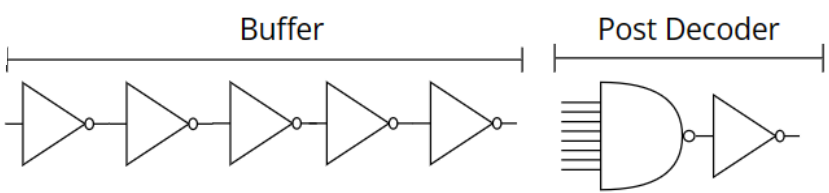


Delay: 1.613 ns

D_{min}: 181.06 ps

	Initial buffer	INV 1	INV 2	INV 3	INV 4	NAND	INV
γ	1	1	1	1	1	1	1
$\hat{f}$	3.634						
C_{load}	500 aF	500 aF	500 aF	500 aF	1.5 fF	500 aF	10.89 fF

Optimized



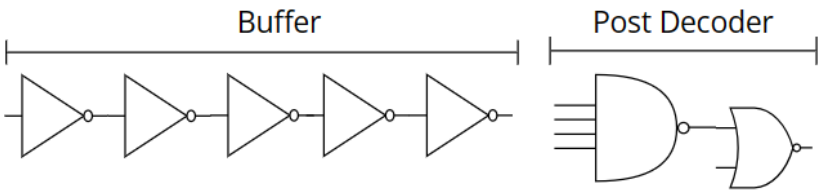
Delay: 181.06 ps

D_{min}: 181.06 ps

	Initial buffer	INV 1	INV 2	INV 3	INV 4	NAND	INV
γ	1	3.63	13.20	47.98	174.32	1.65	5.99
$\hat{f}$	3.634						
C_{load}	1.8 fF	6.6 fF	28.9 fF	87.2 fF	2.5 fF	2.99 fF	10.89 fF

Unfeasible sizes, useless to simulate with wires

Eight 1-2 pre-decoders: 2nd no wire

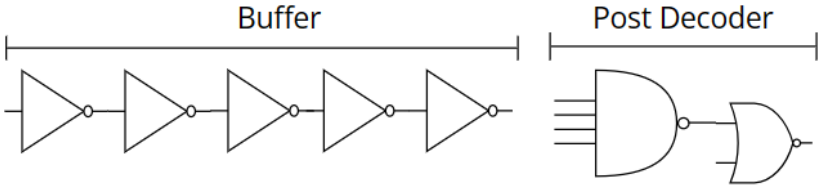


Delay: 1.054 ns

D_{min}: 163.33 ps

	Initial buffer	INV 1	INV 2	INV 3	INV 4	NAND	NOR
γ	1	1	1	1	1	1	1
$\hat{f}$	3.665						
C_{load}	500 aF	500 aF	500 aF	500 aF	928.5 aF	857.1 aF	10.89 fF

Optimized



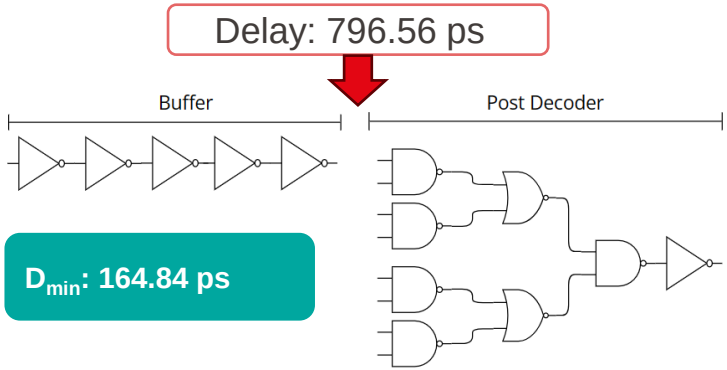
Delay: 163.33 ps

D_{min}: 163.33 ps

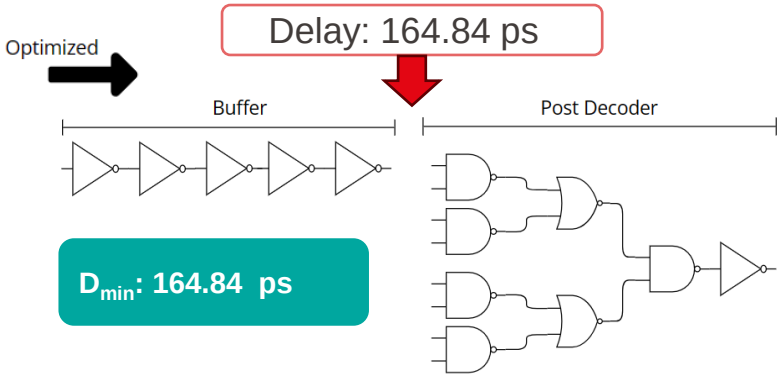
	Initial buffer	INV 1	INV 2	INV 3	INV 4	NAND	NOR
γ	1	3.66	13.43	49.21	180.35	2.78	5.94
$\hat{f}$	3.665						
C_{load}	1.8 fF	6.7 fF	24.6 fF	90.2 fF	2.6 fF	5.1 fF	10.89 fF

Unfeasible sizes, useless to simulate with wires

Eight 1-2 pre-decoders: 3rd no wire

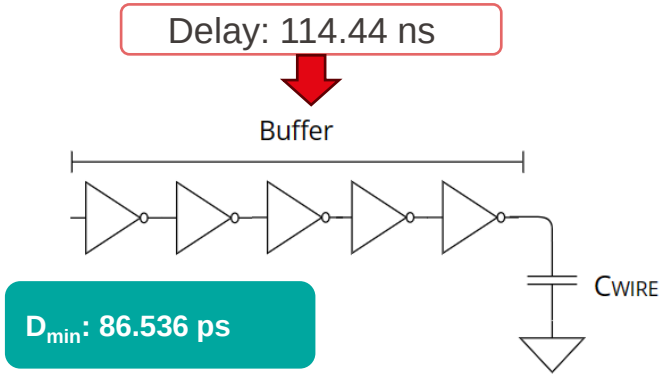


	Input buffer	INV 1	INV 2	INV 3	INV 4	NAND	NOR	NAND	INV
γ	1	1	1	1	1	1	1	1	1
$\hat{f}$	2.711								
C_{load}	500 aF	500 aF	500 aF	500 aF	642 aF	857 aF	642 aF	500 aF	10.89 fF

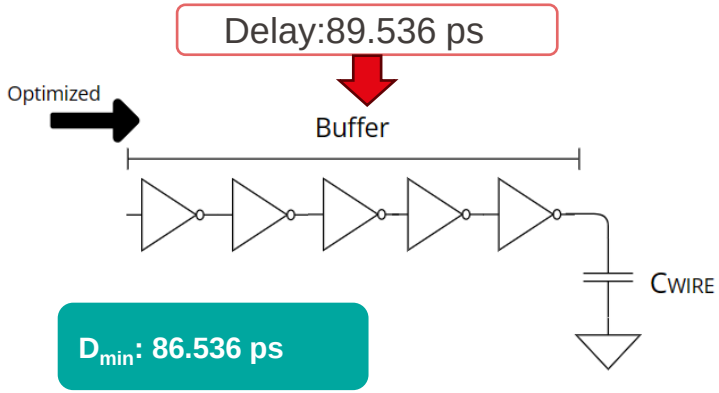


	Input buffer	INV 1	INV 2	INV 3	INV 4	NAND	NOR	NAND	INV
γ	1	2.71	7.35	19.92	53.98	0.89	1.41	2.96	8.04
$\hat{f}$	2.711								
C_{load}	1-3 fF	3.7 fF	9.9 fF	26.9 fF	571 aF	1.2 fF	1.9 fF	4.1 fF	10.89 fF

Eight 1-2 pre-decoders: 3rd with wire

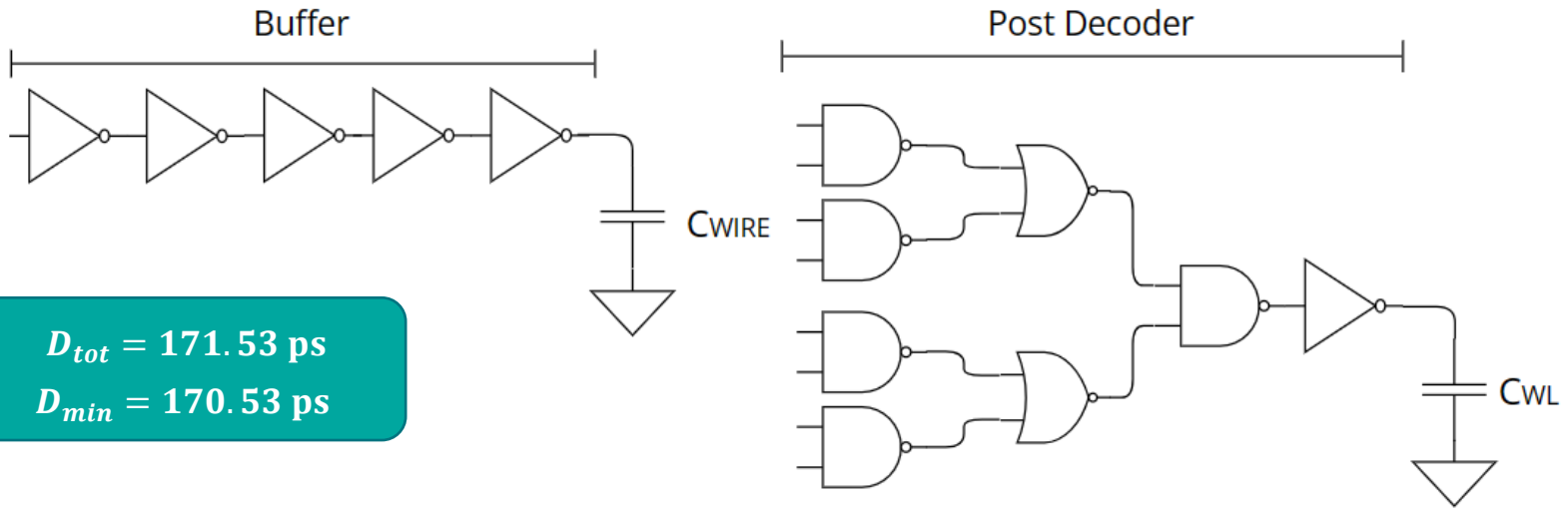


	Input buffer	INV 1	INV 2	INV 3	INV 4
γ	1	1	1	1	1
$\hat{f}$	2.994				
C_{load}	500 aF	500 aF	500 aF	500 aF	120.21 fF



	Input buffer	INV 1	INV 2	INV 3	INV 4
γ	1	2.94	8.96	28.83	80.31
$\hat{f}$	2.994				
C_{load}	1.4 fF	4.5 fF	13.4 fF	40.16 fF	120.21 fF

Final configuration 1x



$D_{tot} = 171.53$ ps

$D_{min} = 170.53$ ps

	Input buffer	INV 1	INV 2	INV 3	INV 4	NAND	NOR	NAND	INV
γ	1	3	9	27	80	1	2	3	8
C_{load}	1.5 fF	4.5 fF	13.5 fF	40 fF	642 aF	1.7 fF	1.9 fF	4 fF	10.89 fF

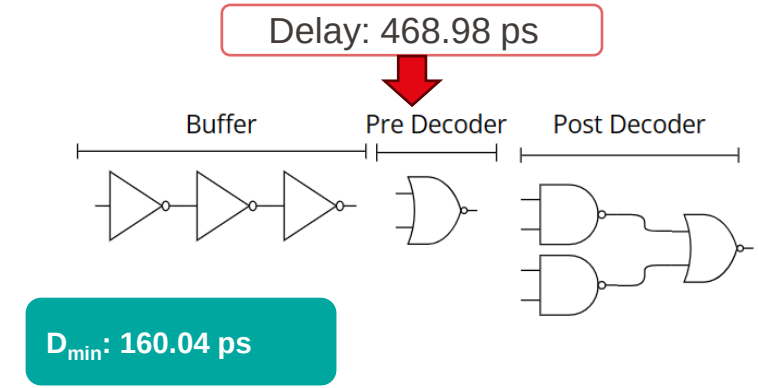
Sum up:

- Configuration involving gates with more input and less stages causes higher delay and are more difficult to optimize due to unfeasible values for gamma and too high number of additional buffer

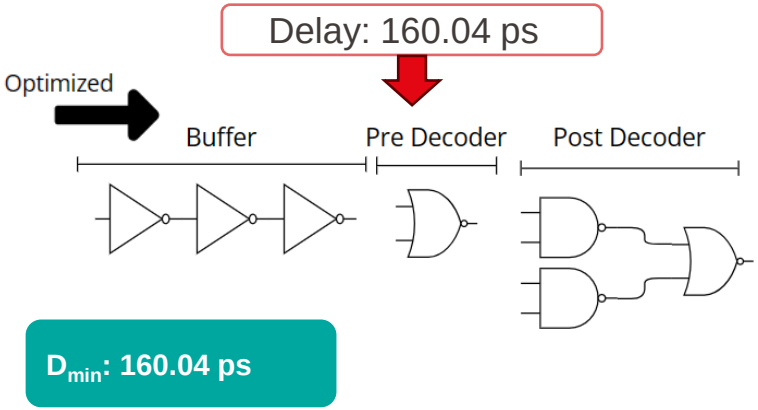
- The last configuration produces an acceptable delay close to the minimum achievable delay but again the upsizing is too high

- From the last configuration layout problem may arise as it is difficult to match the row decoder to the bitcell

Four 2-4 pre-decoders: no wire

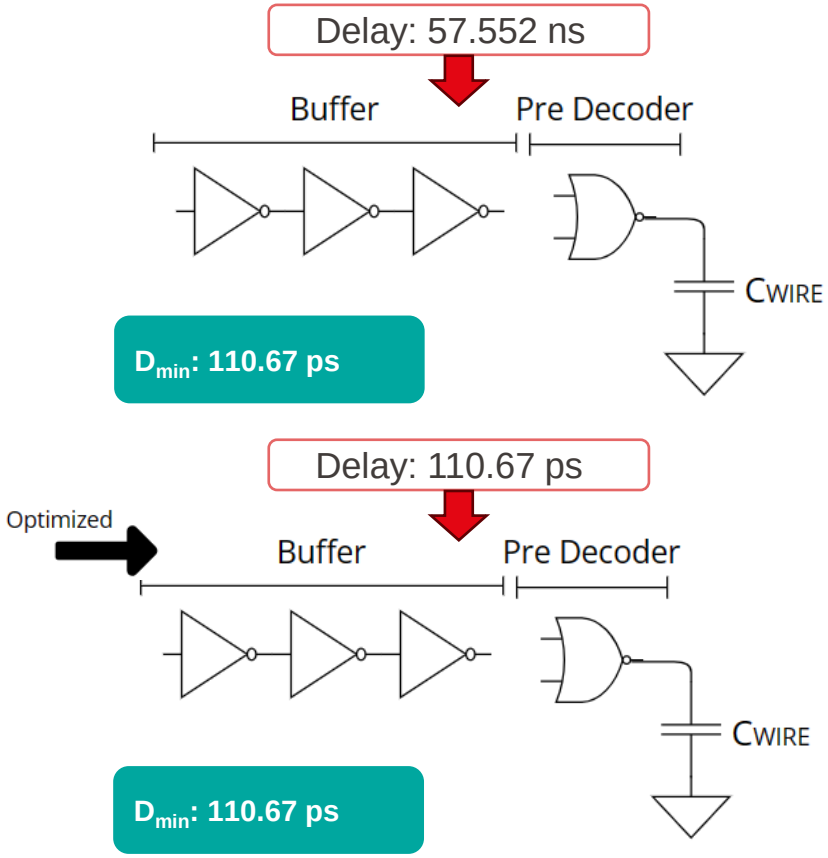


	Input buffer	INV 1	INV 2	NOR	NAND	NOR
γ	1	1	1	1	1	1
$\hat{f}$	4.682					
C_{load}	500 aF	500 aF	857.1 aF	642.9 aF	857.1 aF	10.9 fF



	Input buffer	INV 1	INV 2	NOR	NAND	NOR
γ	1	4.68	21.92	29.93	1.7	4.6
$\hat{f}$	4.682					
C_{load}	2.34 fF	10.96 fF	25.68 fF	1.09 fF	3.99 fF	10.9 fF

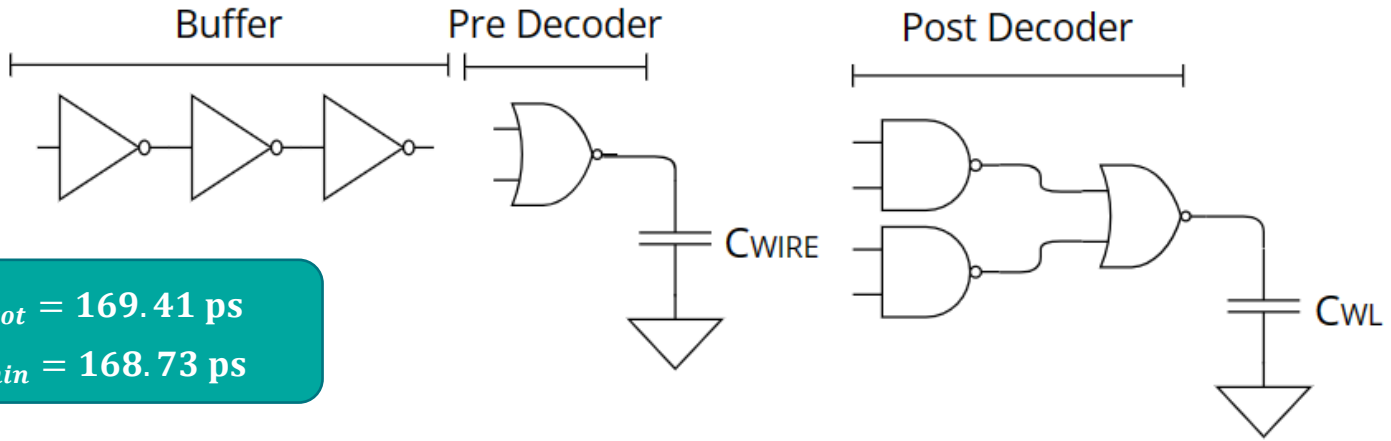
Four 2-4 pre-decoders: with wire



	Initial buffer	INV 1	INV 2	NOR
γ	1	1	1	1
$\hat{f}$	5.365			
C_{load}	500 aF	500 aF	857.1 aF	120.9 fF

	Initial buffer	INV 1	INV 2	NOR
γ	1	5.36	28.79	45.05
$\hat{f}$	5.365			
C_{load}	2.68 fF	14.39 fF	38.61 fF	120.9 fF

Final configuration 2x



$D_{tot} = 169.41$ ps

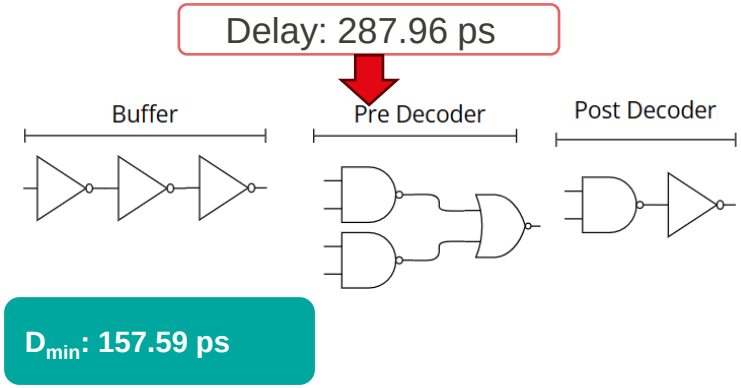
$D_{min} = 168.73$ ps

	Input buffer	INV 1	INV 2	NOR	NAND	NOR
γ	1	5	29	45	2	5
C_{load}	2.5 Ff	14.5 Ff	38.7 fF	1.3 fF	4.2 fF	10.89 fF

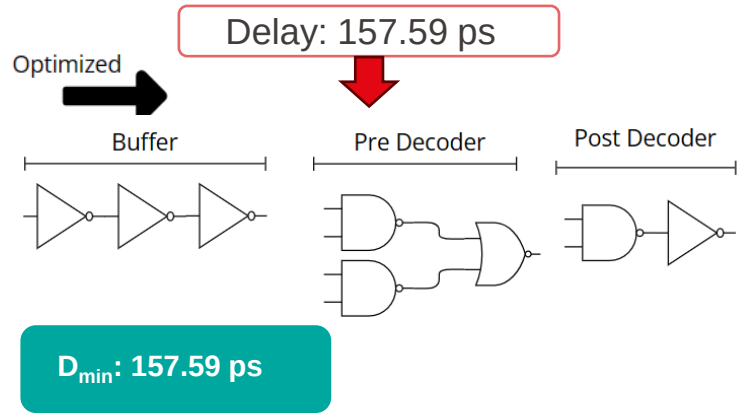
Sum up:

- As it was seen for the 1x case, large fanin gates are far from being optimal so only 2 fanin cells are considered
- The total delay of the analysed configuration is lower than the 1x row decoder and the upsizing are reasonable
- This configuration might cause some matching problem to the bitcell

Two 4-16 pre-decoders: no wires

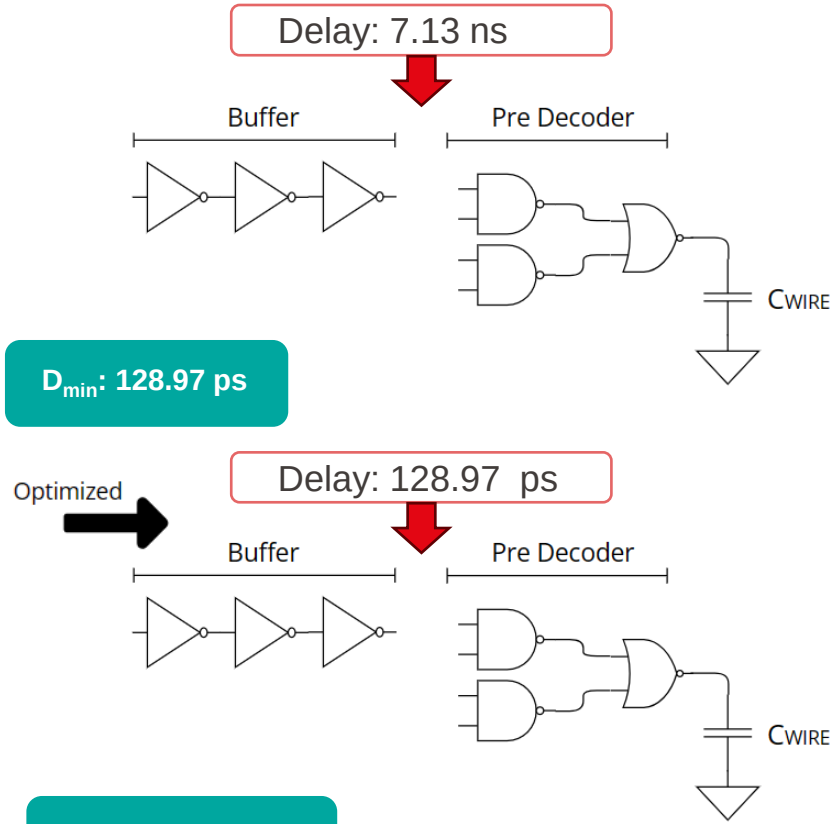


	Input buffer	INV1	INV2	NAND	NOR	NAND	INV
γ	1	1	1	1	1	1	1
$\hat{f}$	3.682						
C_{load}	500 aF	500 aF	642.9 aF	857.1 aF	642.9 aF	500 aF	12.64 fF



	Input buffer	INV1	INV2	NAND	NOR	NAND	INV
γ	1	3.68	13.55	4.85	10.42	1.87	6.87
$\hat{f}$	3.682						
C_{load}	1.84 fF	6.8 fF	3.1 fF	8.9 fF	1.2fF	3.4 fF	12.64 fF

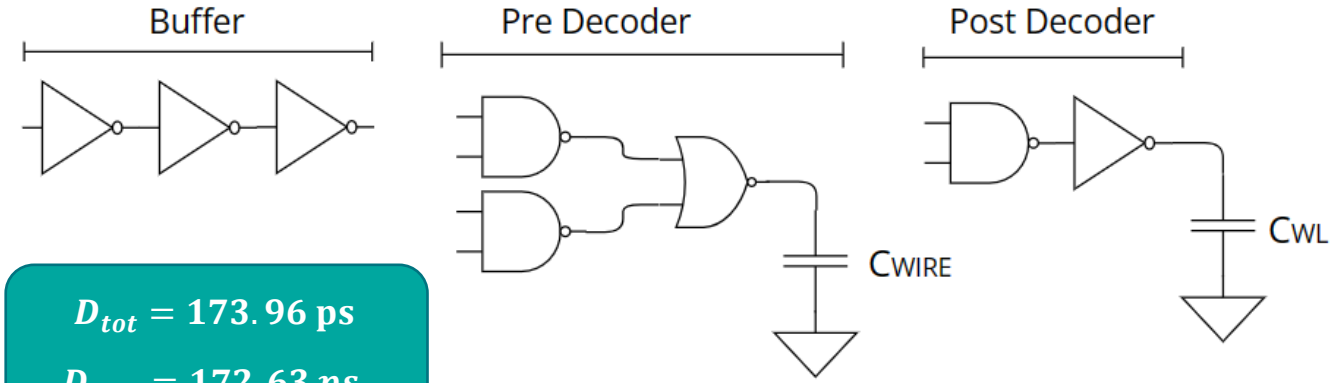
Two 4-16 pre-decoders: with wires



	Input buffer	INV1	INV2	NAND	NOR
γ	1	1	1	1	1
$\hat{f}$	4.612				
C_{load}	500 aF	500 aF	642.9 aF	857.1 aF	59.14 fF

	Input buffer	INV1	INV2	NAND	NOR
γ	1	4.61	21.27	9.56	25.67
$\hat{f}$	4.612				
C_{load}	2.3 fF	10.6 fF	6.1 fF	21.9fF	59.14 fF

Final configuration 4x

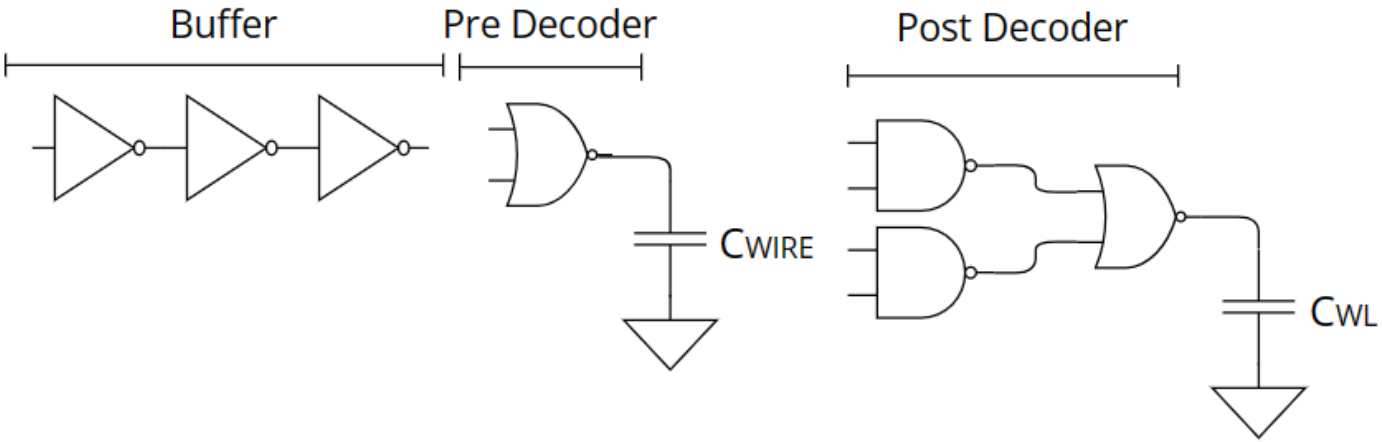


$D_{tot} = 173.96$ ps

$D_{min} = 172.63\ ps$

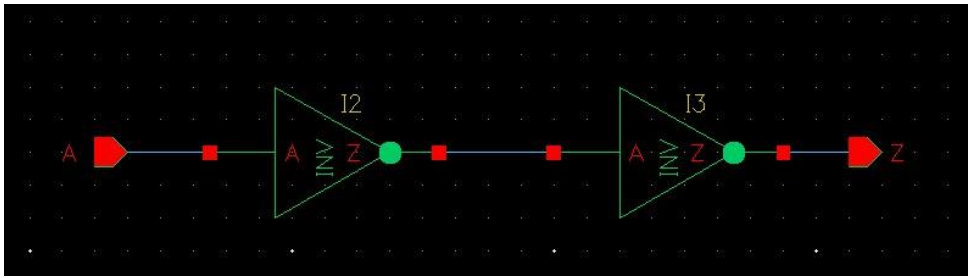
	Input buffer	INV 1	INV 2	NAND	NOR	NAND	INV
γ	1	5	22	10	26	2	7
C_load	2.5 fF	11 fF	6.4 fF	22.3 fF	1.3 fF	3.5 fF	10.9 fF

Final design choice:

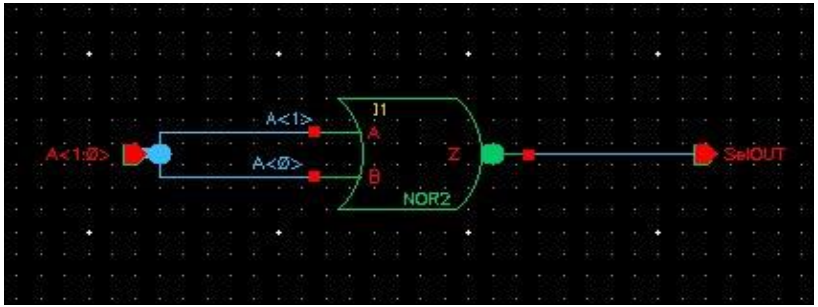


- The 2x row decoder was chosen as it minimizes the total delay
- From the area point of view, it is less optimal compared to the 4x configuration but speed was considered more relevant in this analysis

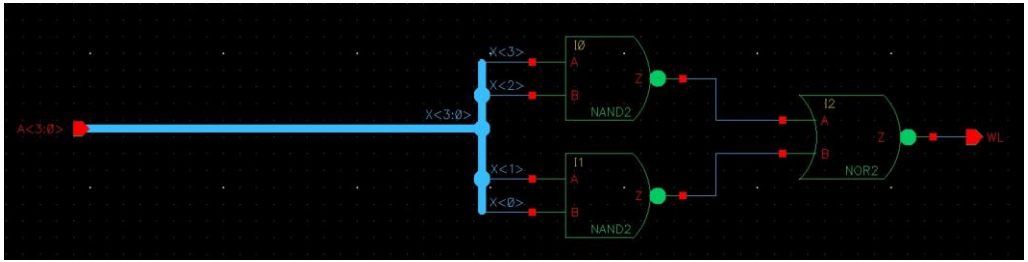
Schematic



Input buffer

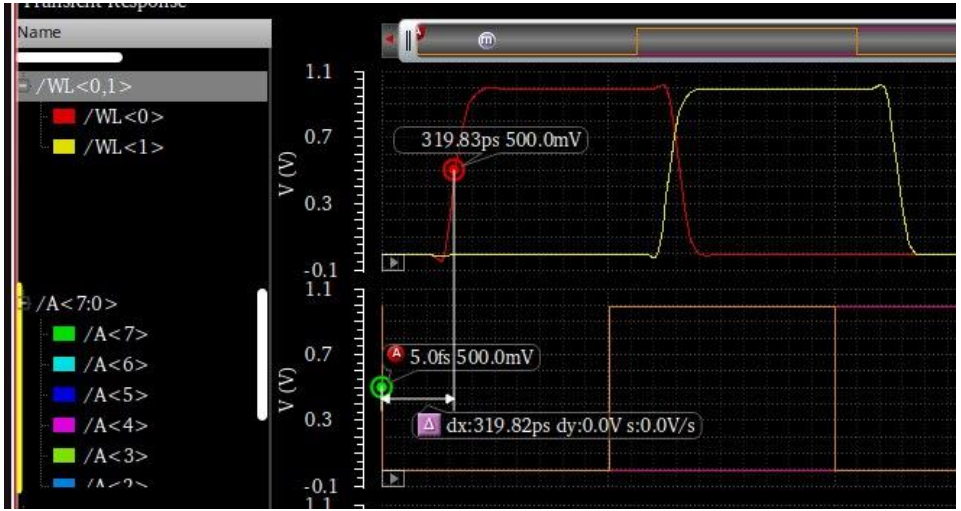


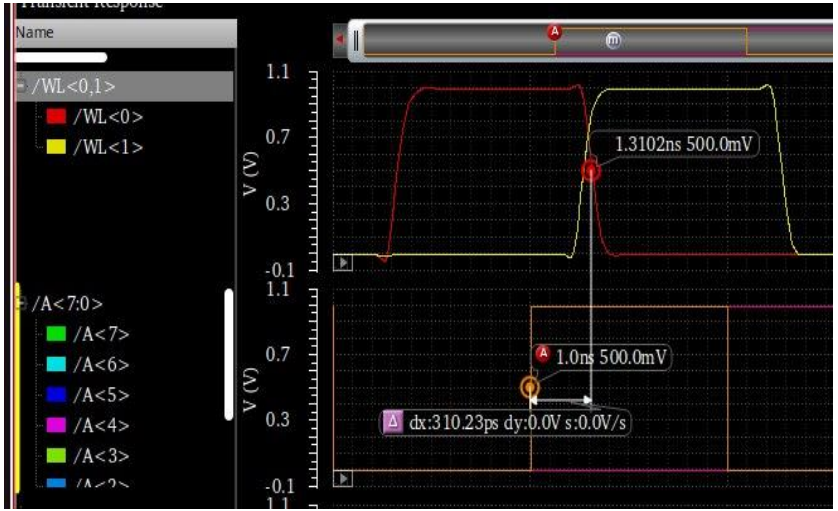
Pre decoder



Post decoder

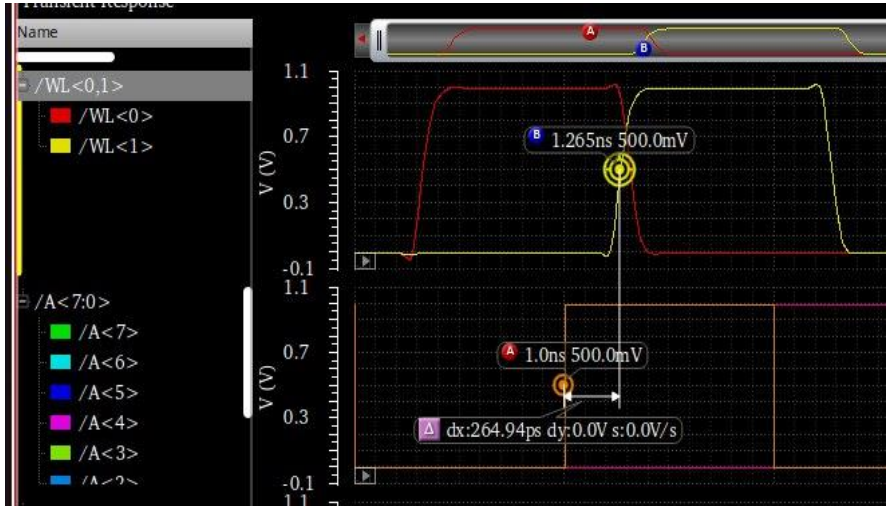
Simulation results without Parasitics

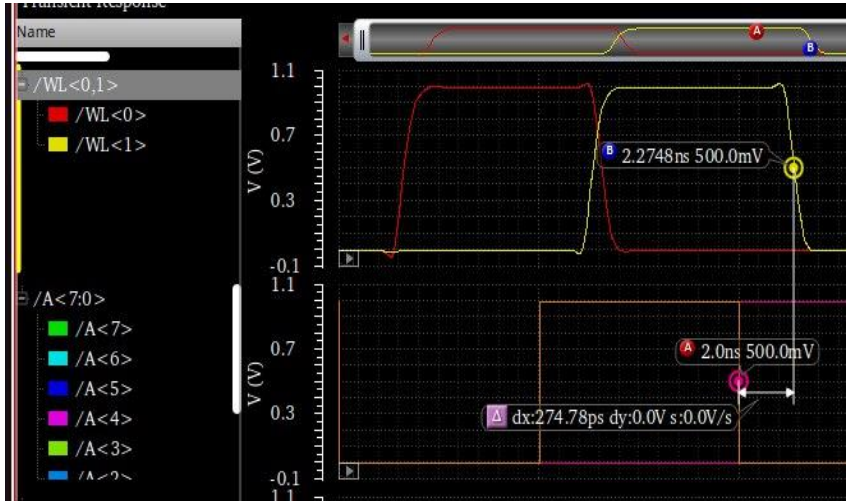




- WL0 Rising and Falling Delay

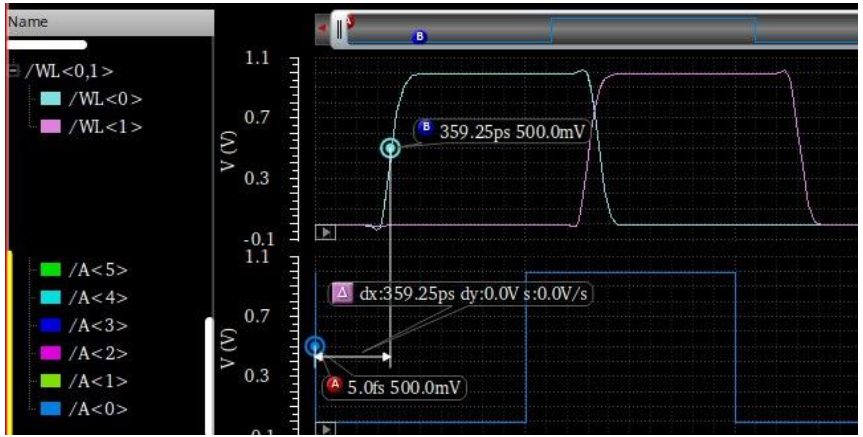
Simulation Results without Parasitics

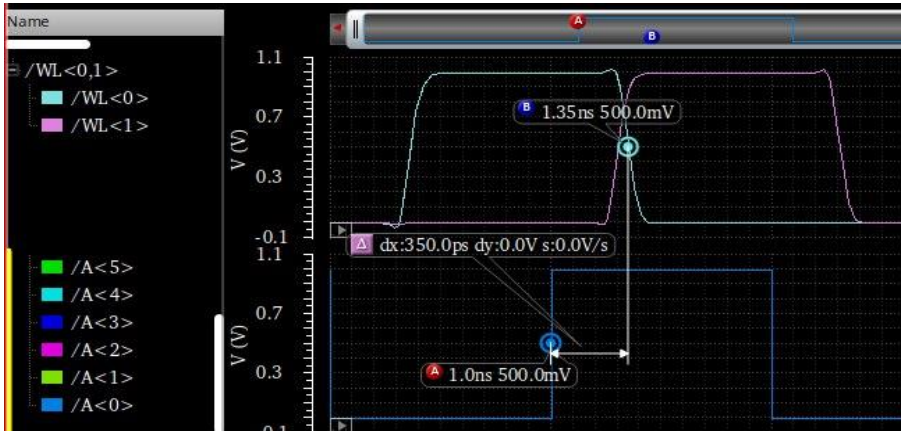




- WL1 Rising and Falling Delay

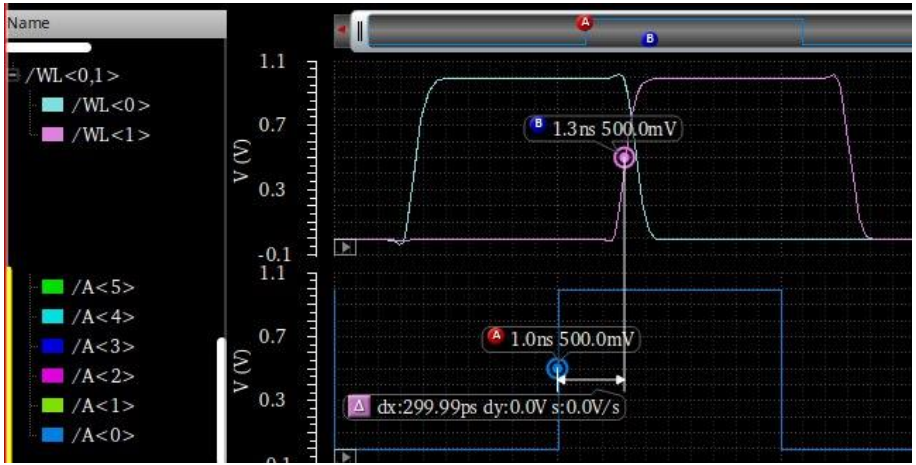
Simulation Results with Calculated Parasitics

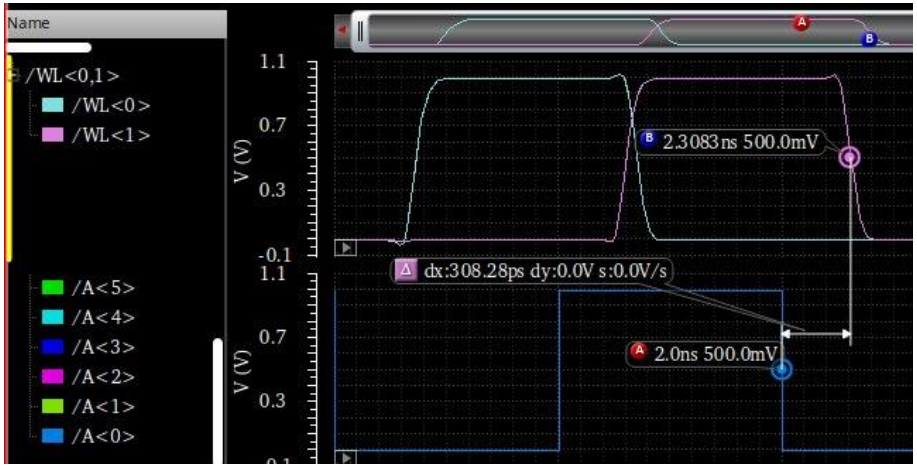




- WL0 Rising and Falling Delay

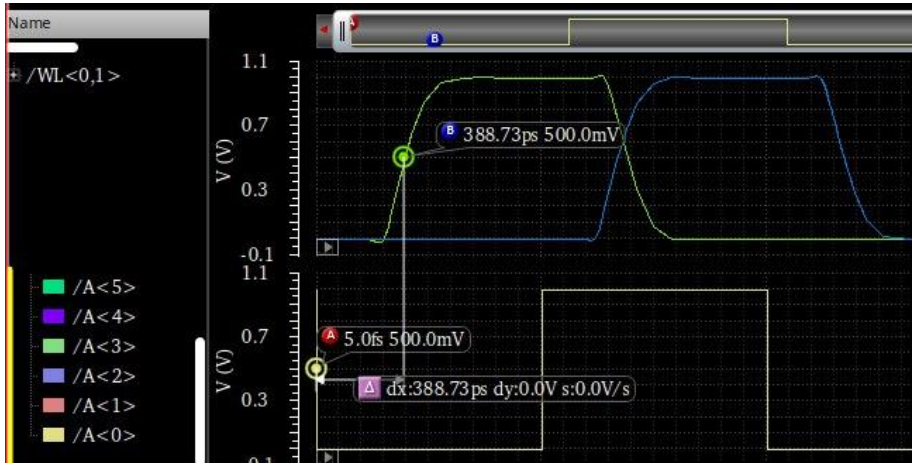
Simulation Results with Calculated Parasitics

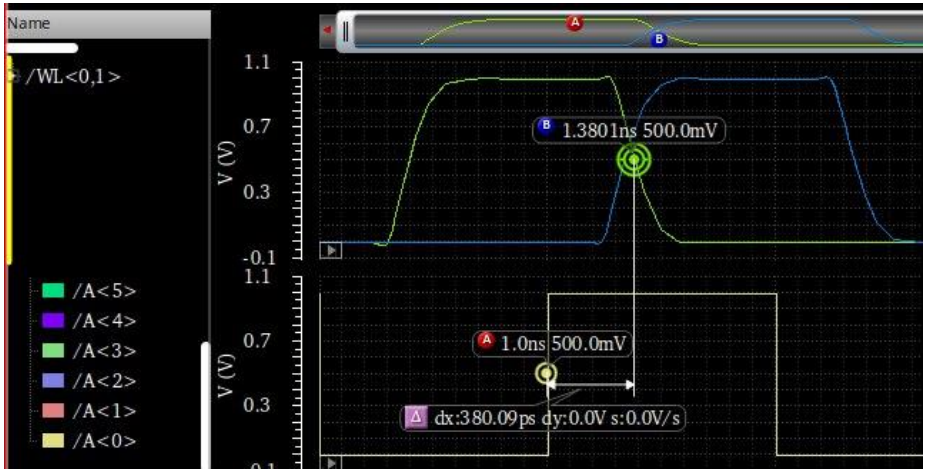




- WL1 Rising and Falling Delay

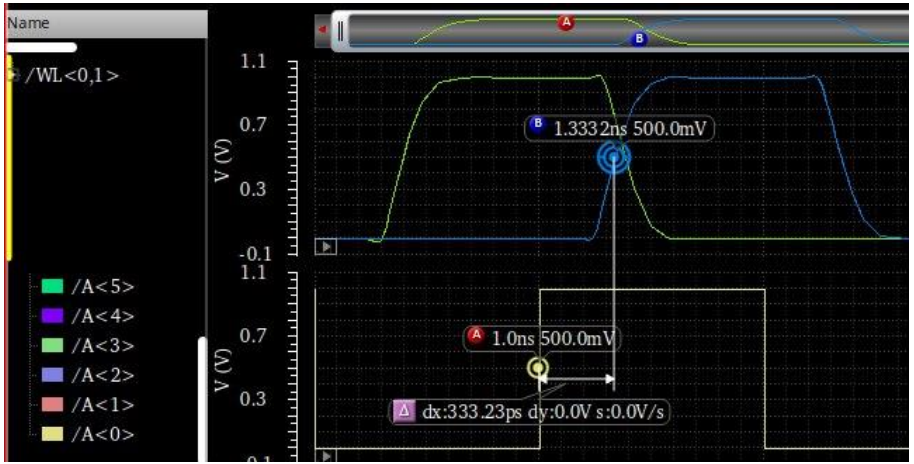
Simulation Dealy Post-PEX

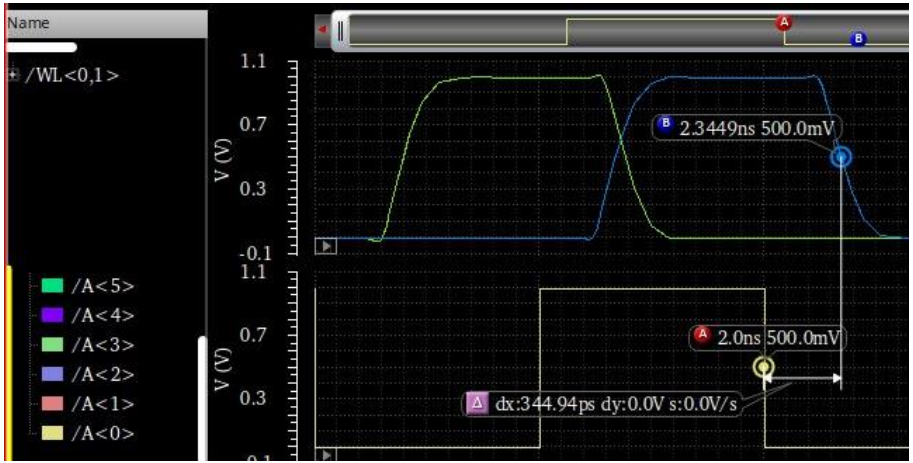




- WL0 Rising and Falling Delay

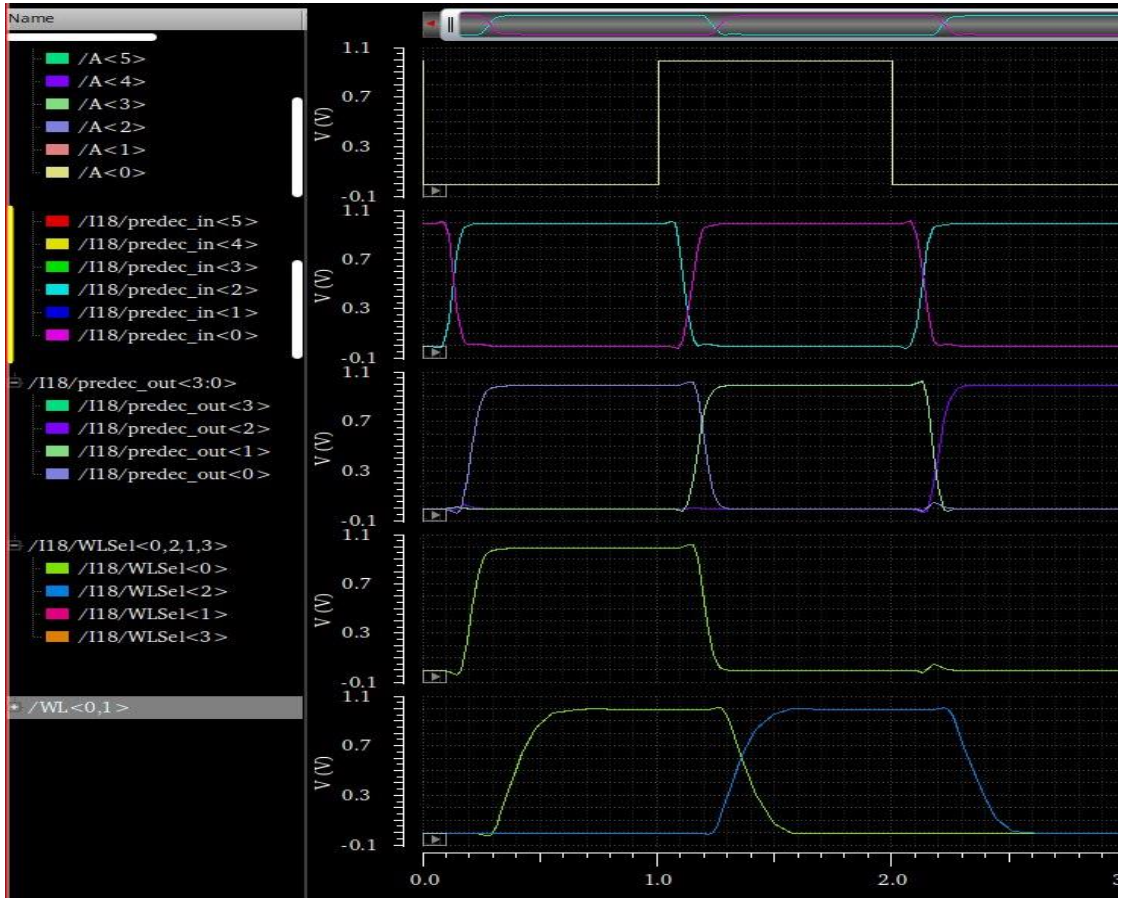
Simulation Dealy Post-PEX





- WL1 Rising and Falling Delay

Simulation Post-PEX waveforms



Sum Up:

	Estimated Delay	Simulated Delay w no Parasitics	Simulated Delay w estimated Parasitics	Simulated Delay w extracted Parasitics
$Total\ delay\ WL_0$	169.41 ps	315.03 ps	354.63 ps	384.41 ps
$Total\ delay\ WL_1$	169-41 ps	269.86 ps	304.14 ps	339.09 ps

- The extracted delays and the estimated delay differs by almost a factor of two
- The critical point of the logical effort are interconnection delay estimations as they could be smaller, comparable or higher than the gates they are driving
- The delays of the two wordline differs of about 50ps

Appendix: Python Program

```
from circuit import *
from optimum_sizing import *
from metal import *

# Library needed to print with the "Engineering Notation" the results
from quantiphy import Quantity
```

Create the final RowDecoder circuit

```
GAMMA_BUFFER_1 = 5
GAMMA_BUFFER_2 = 29
GAMMA_NOR_BRANCH = 45
```

```
buffer1_final = Inverter("buffer1", BETA_OPT, BETA_OPT, GAMMA_BUFFER_1, DUMMY_METAL, C_INT_TRANS, TAU_RATIO)
buffer2_final = Inverter("buffer2", BETA_OPT, BETA_OPT, GAMMA_BUFFER_2, DUMMY_METAL, C_INT_TRANS, TAU_RATIO)

nor_branch_final_list = list()
for i in range(DRIVER_FO):
    nor_2x_preDec = Nor("nor_2x_pre_" + str(i), BETA_OPT, BETA_OPT, GAMMA_NOR_BRANCH, PREDEC_FI, DUMMY_METAL, C_INT_TRANS, TAU_RATIO)
    nor_branch_final_list.append(nor_2x_preDec)

nor_branch_final = Branch("nor_pre", nor_branch_final_list)

rowdec_2x_final_gates = [input_buffer, buffer1_final, buffer2_final, nor_branch_final, nand_branch_wire, nor_final]
rowdec_2x_final = Circuit("RowDecoder 2x - Final Architecture", rowdec_2x_final_gates, TAU_2, TAU_RATIO, (post_WL_metal.Ctot + BITCELL_CAP) / C_GATE_INV)
rowdec_2x_final.info()
```

The program allows to:

- Build the circuit dividing it into buffer, pre and post decoder
- Optimizes sizes
- Calculates optimal number of even buffers
- Table visualization of the circuit

Appendix: Python result for 2x configuration

Circuit name: RowDecoder 2x - Final Architecture

	input_buffer	buffer1	buffer2	nor_pre	nand_post	nor_post
p	1.000	1.000	1.000	2.000	2.000	2.000
g	1.000	1.000	1.000	1.714	1.286	1.714
h	5.000	5.800	2.660	0.033	3.333	2.541
b	1.000	1.000	2.000	94.000	1.000	1.000
gamma	1.000	5.000	29.000	45.000	2.000	5.000
Cin	500 aF	2.5 fF	14.5 fF	38.571 fF	1.2857 fF	4.2857 fF
Cload	2.5 fF	14.5 fF	38.571 fF	1.2857 fF	4.2857 fF	10.89 fF
C_off	0 F	0 F	0 F	38.571 fF	119.57 fF	0 F
gate delay	24.765 ps	27.739 ps	25.955 ps	32.326 ps	28.29 ps	28.551 ps

Delay of the circuit = 167.63 ps
Minimum achievable delay = 166.95 ps
Number of stages = 6
Tau_2 = 3.717 ps
Tau_ratio = 1.663
F_hat = 4.992
Final load = 21.780 * C_in_inv
H = 21.780
G = 3.778
B = 188.000