Beatrice Grassano

Thermal sensing network for power monitoring in integrated cooled electronic systems

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Supervisors:

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Overview:

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1 | Introduction

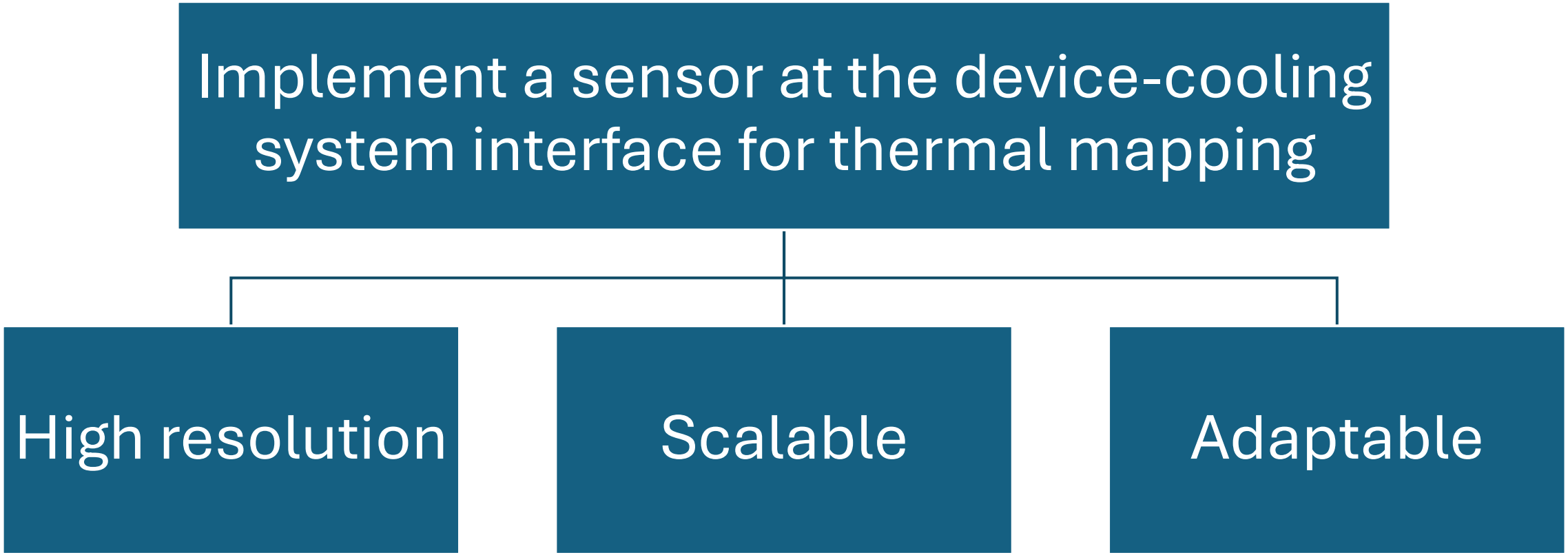
Power density in electronic circuits increased

Performance degradation

Growing need for tailored on-chip cooling with microfluidic channel

Monitoring temperature with thermal cameras not valid

1 | Introduction: Project definition



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1 | Introduction: Importance

Verification of efficacy of cooling systems

Tailoring of cooling systems, avoiding over and under design

Characterization of thermal interfaces and material properties of circuit elements

2 | Exploration phase

Mott Insulator

Materials with conductive properties changing at a critical temperature

Discarded:

- Poor grain refinement and measurement reliability
- Rarity of Mott insulators limits practicality for electronics
- Strong dependence on material purity

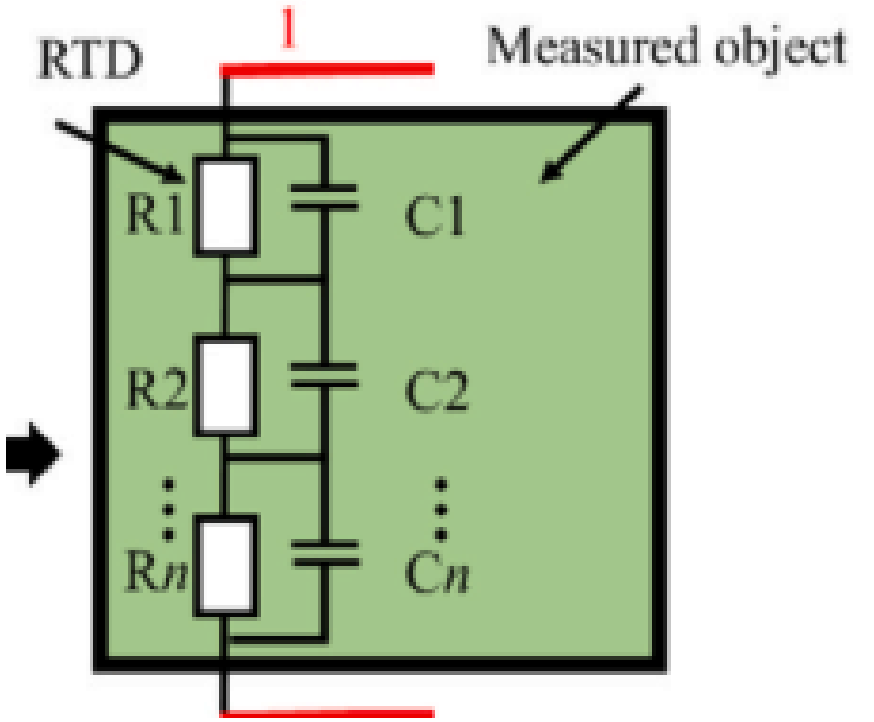
Frequency shift oscillators

Temperature alters circuit component properties, affecting the ring oscillator's frequency

Discarded too many components:

- Circuit implementation is difficult and space-consuming due to counters and voltage shifter
- Continuous calibration is necessary, reducing the device's plug-and-play appeal
- Precision degradation due to internal component drift.

2 | Exploration phase: Integrate Cap



1) Only two cables for network

2) Ready to use

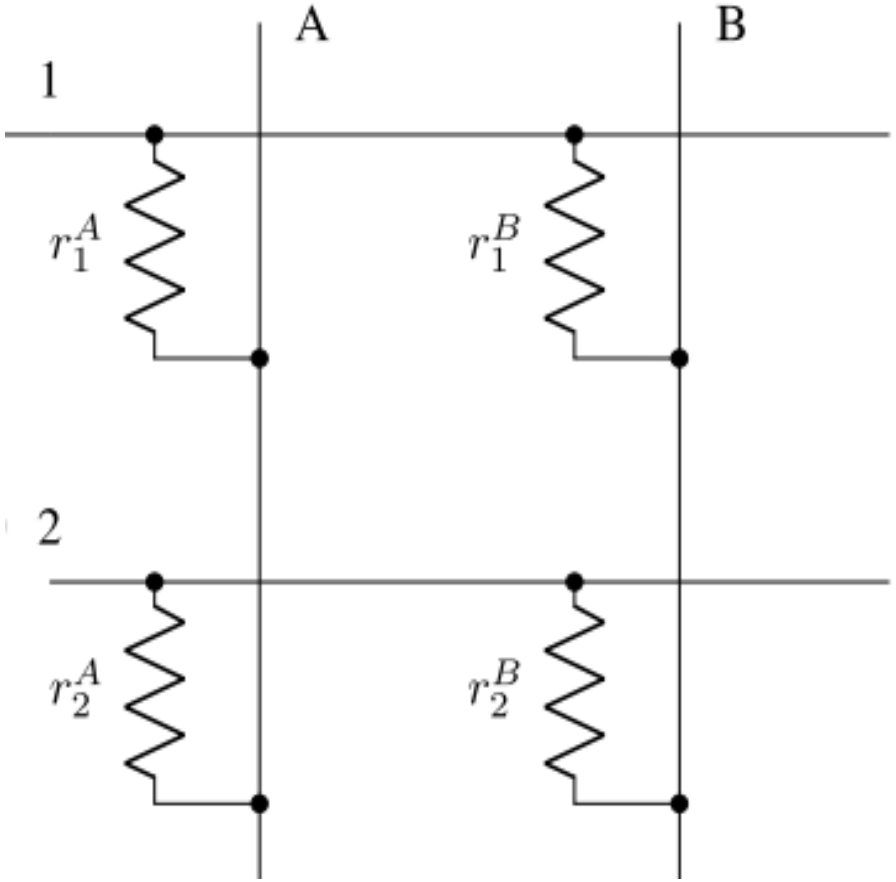
1) Electrolytic capacitor

2) Costly EIR equipment

3) Not scalable

Reference: Temperature prediction in data center combining with deep neural network
Authors: Lele Fang a , Qingshan Xu a,* , Shujuan Li a , Yuanxing Xia a , Quan Chen

3 | Exploration phase: Final configuration



A Fix to ground one of the lines

B Determine R_{ij} by measuring current and voltages between row and column

C Use Python algorithm to extract singular r_{ij}

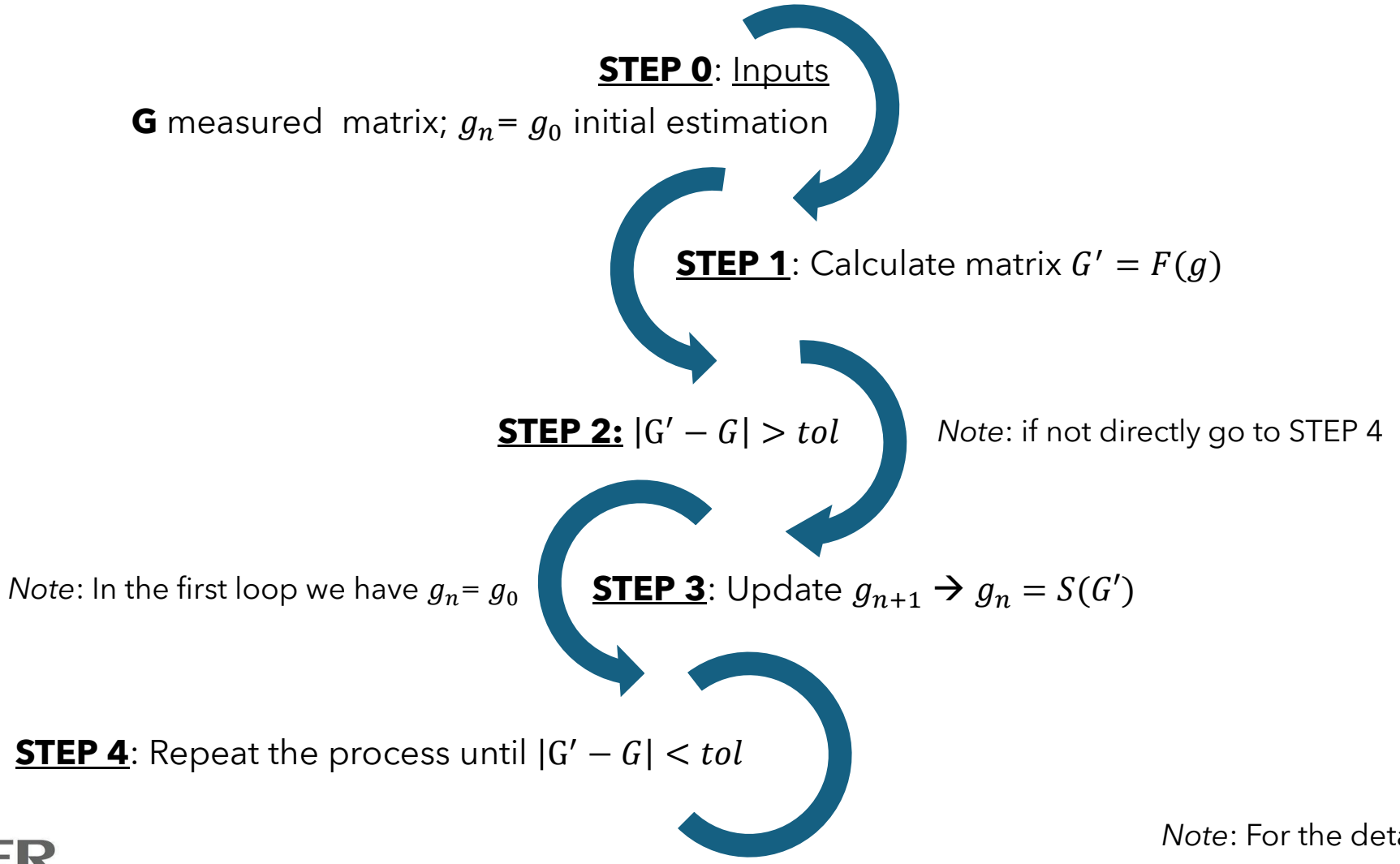
D Use the Callendar-Van Dusen equation to get the point's equivalent temperature

Reference: Circuit Analysis of Matrix-Like Resistor Networks for Eliminating Crosstalk in Pressure Sensitive Mats
Authors: Carlos Medrano-Sánchez , Senior Member, IEEE, Raul Igual-Catalán , Member, IEEE, Victor H. Rodríguez-Ontiveros , and Inmaculada Plaza-García , Senior Member, IEEE

3 | Why this configuration?

- Easy to fabricate and wire out
- Only measure equivalent resistance through N rows and N columns
- No need for machine learning algorithm, exploit numerical solver
- Time and cost-effective
- Possible integration with Si cold plate
- Fine grid and high accuracy can be achieved

4 | Code: Iterative Algotirthm



Note: For the detailed code look at the Appendix

4 | Code: Methods

A Fixed point method

B Leasts squares method

C Newton-Kyrlov method

4 | Code: Methods comparison

	Fixed-point		Least squares		Newton-Krylov	
Matrix size	Errors	Time [s]	Errors	Time [s]	Errors	Time [s]
3x3	8.166×10^{-7}	0.023	5.508×10^{-13}	0.022	5.642×10^{-7}	0.011
4x4	0.018	61.85	2.647×10^{-11}	0.037	1.234×10^{-8}	0.024
6x6	0.041	148.54	9.6622×10^{-10}	0.173	1.263×10^{-8}	0.041
8x8	0.071	328.48	1.140×10^{-11}	1.420	1.112×10^{-7}	0.160
10x10	0.112	880.212	2.259×10^{-9}	3.934	1.509×10^{-6}	0.408
15x15	0.254	3187.43	1.997×10^{-8}	9.962	8.502×10^{-6}	0.487

Comments:

- **Least squares method → most precise**
- **Newton-Kyrlov method → faster**

The code flexibility allows optimal method selection for timing or precision

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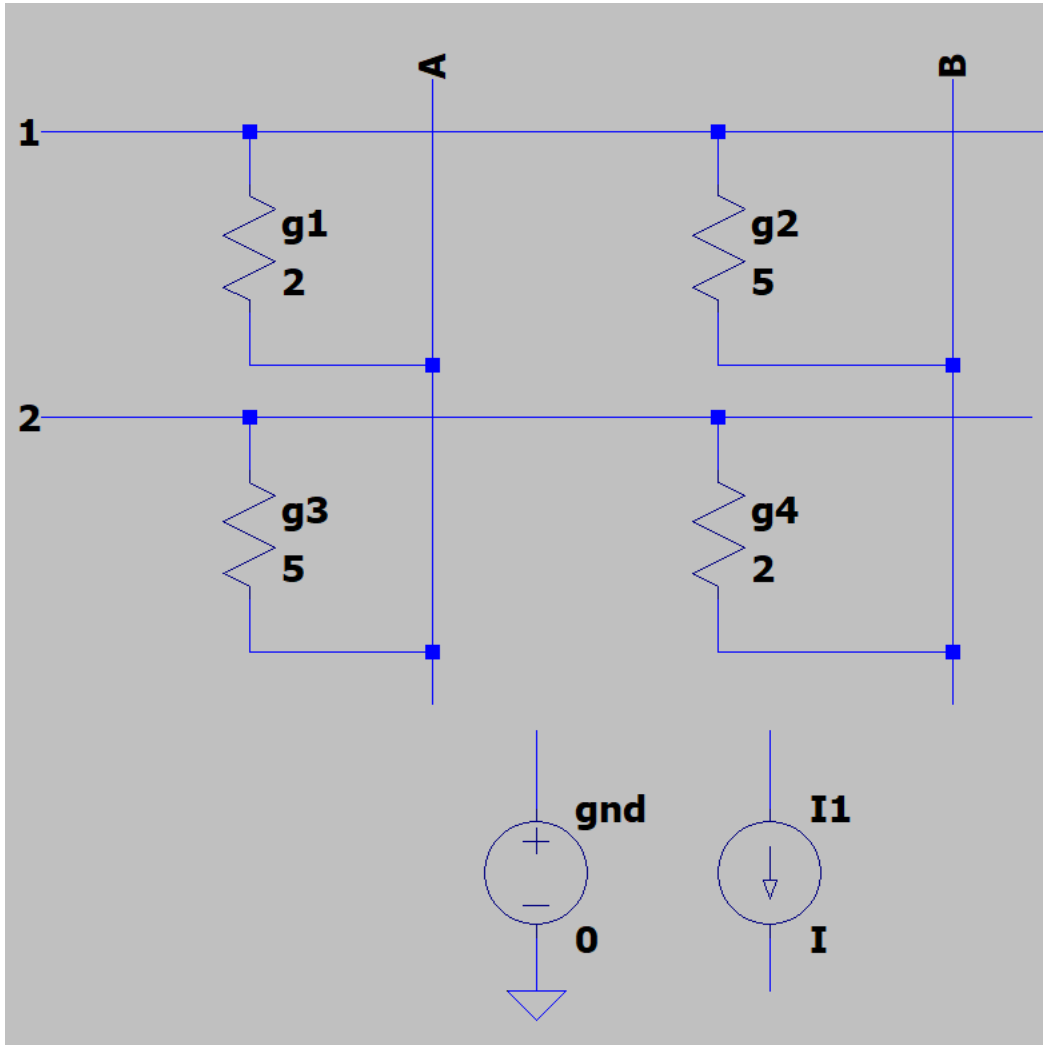
4 | Code: Verification via LTSpice

STEP 0: Inputs
g_n matrix from the code

STEP 1: Extract G_{sim} matrix from .op simulation

STEP 2: $|G_{sim} - G| \cong 0$



Note: For the detailed code look at the Appendix

4 | Results

A
- The code was tested with matrices with sizes 2x2, 3x3, 4x4, 8x8, 10x10 and 15x15

B
- LTSpice simulation showed satisfactory results, with Gsim and G_initial differing at most by 10^{-2}

Caution:

- Non-convergence can occur due to iteration limits and initial guess divergence exceeding two orders of magnitude

5 | Device testing

The goal is to test the device using the following

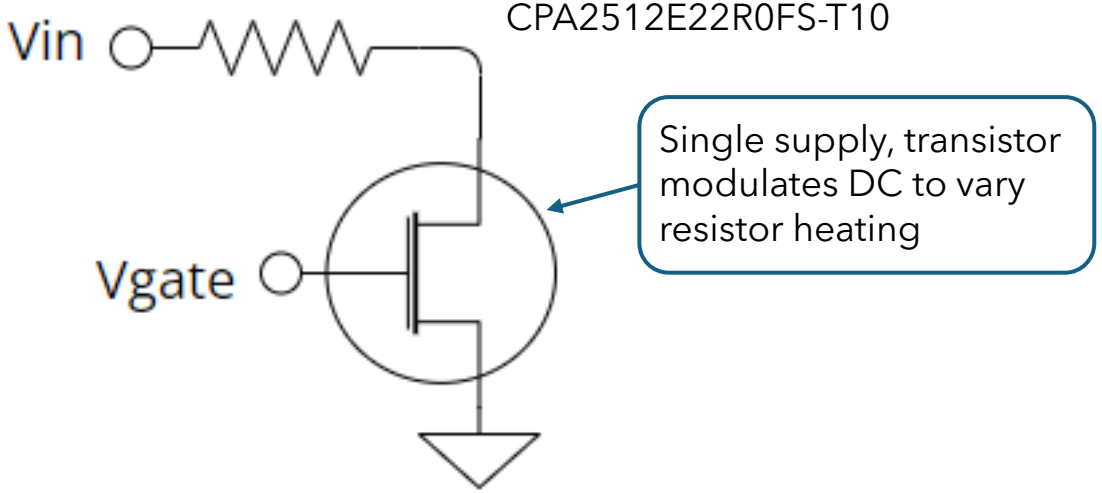
TTV behavior:	Measurement behavior:
• **How:** Through a dissipative element generate an arbitrary thermal map	• **How:** Through the resistance matrix, placed on top of the TTV to detect temperature distribution

Functional check: Resistor matrix monitors power consumption and temperature

5 | PCB Schematic: unit cell

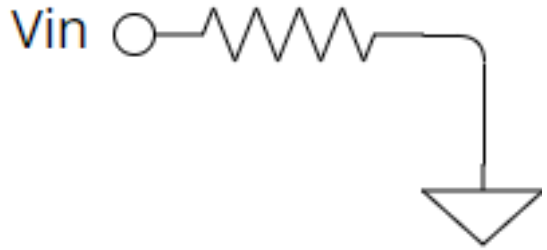
Dissipative element

CPA2512E22R0FS-T10



Verification element

RTD 32207595



Properties of resistance:

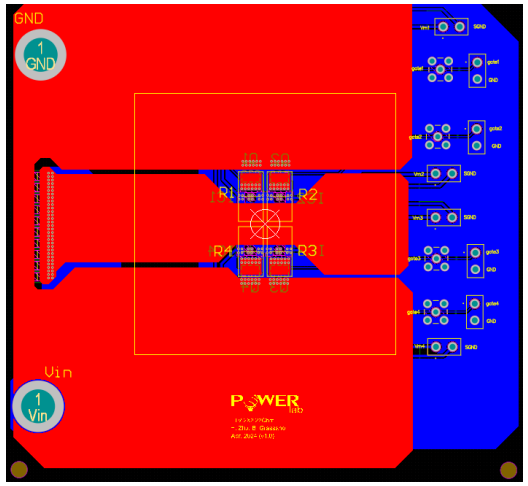
- low temperature coefficient
- sustain high power

Properties of resistance:

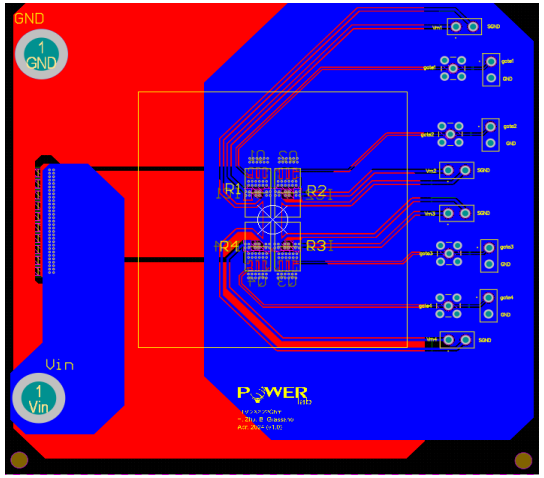
- high temperature coefficient
- low self-heating

5 | PCB Layout: TTV

Top layer

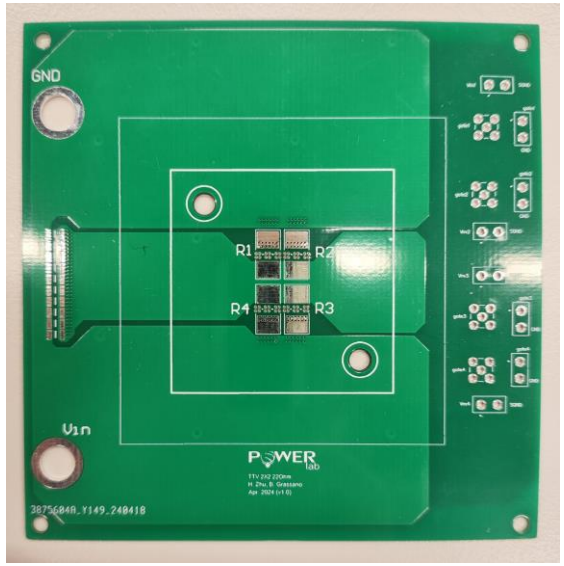


Bottom layer



Device desing

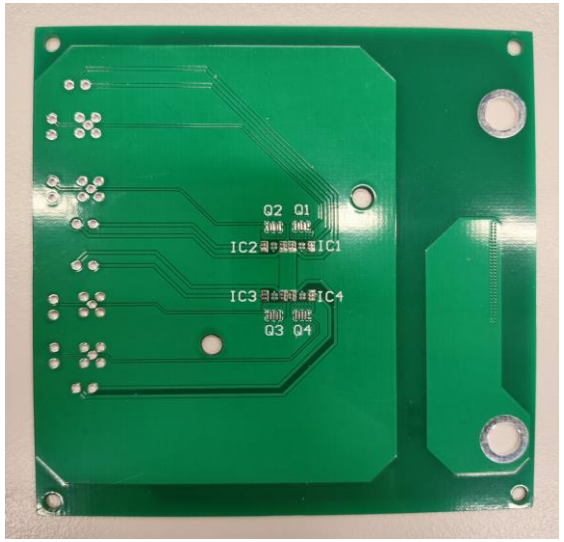
Front



Power Signal

Control Signal

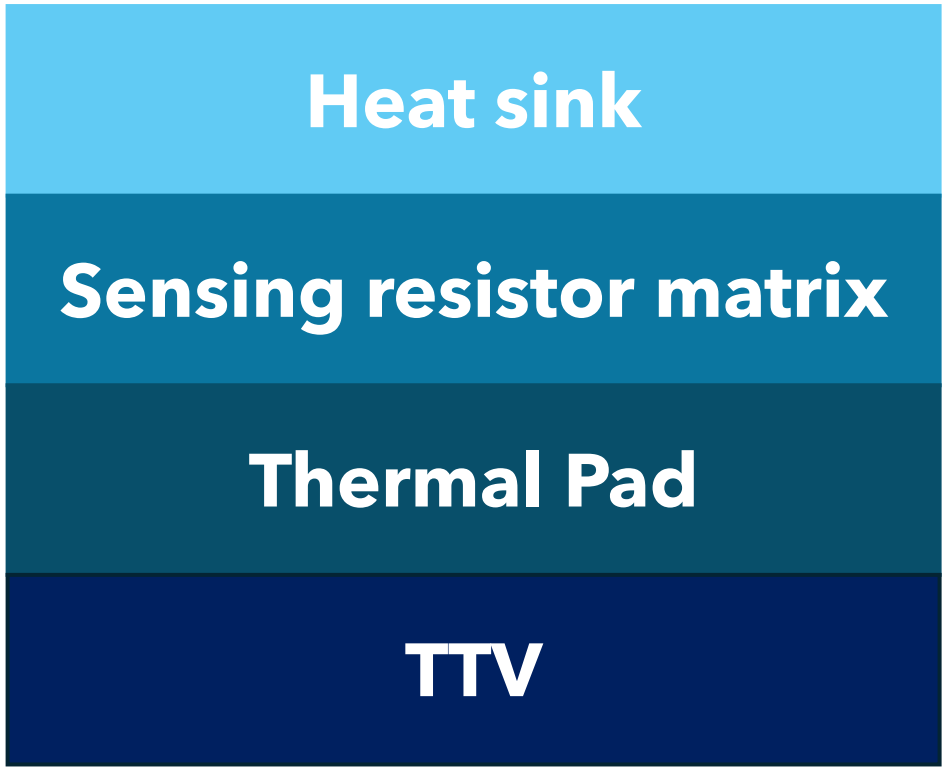
Back



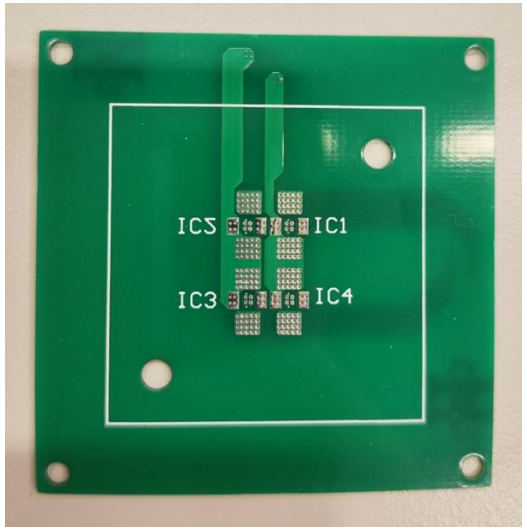
Device produced

5 | Lateral view of complete device

Debug Resistors



RTD 32207595



6 | Device Testing: Set up Measurements

Gate transistors bias:

- V=5V, Variable duty cylce, f = 1kHz

Back resistor bias:

- V=0.240V, I =0.2mA

Power supply to matrix of resistors:

- V= 0.1V

General supply:

- variable, between V= 5V and V=8V

6 | Device Testing: Measurements

Case scenarios: Inhomogeneous thermal maps

Heating one single transistor, no cooling applied	Multiple hotspot, no cooling applied	Experiments with air cooling
• Fixed Duty Cycle • Variable V (between 5V and 8V)	• Variable V • Different Duty Cycle (between 20% and 70% step 10%) for different V	• Repeat the process with a cooling source

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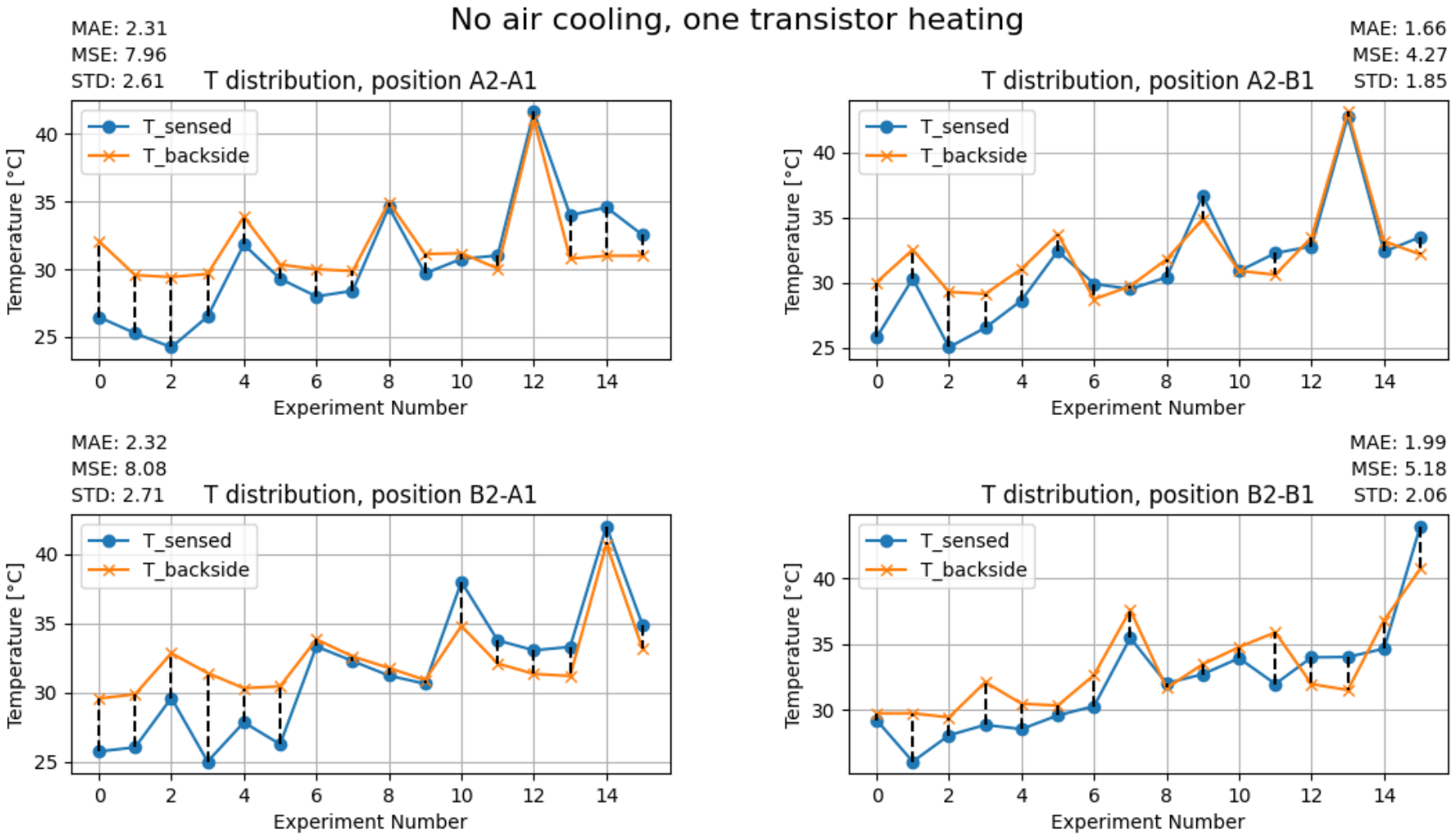
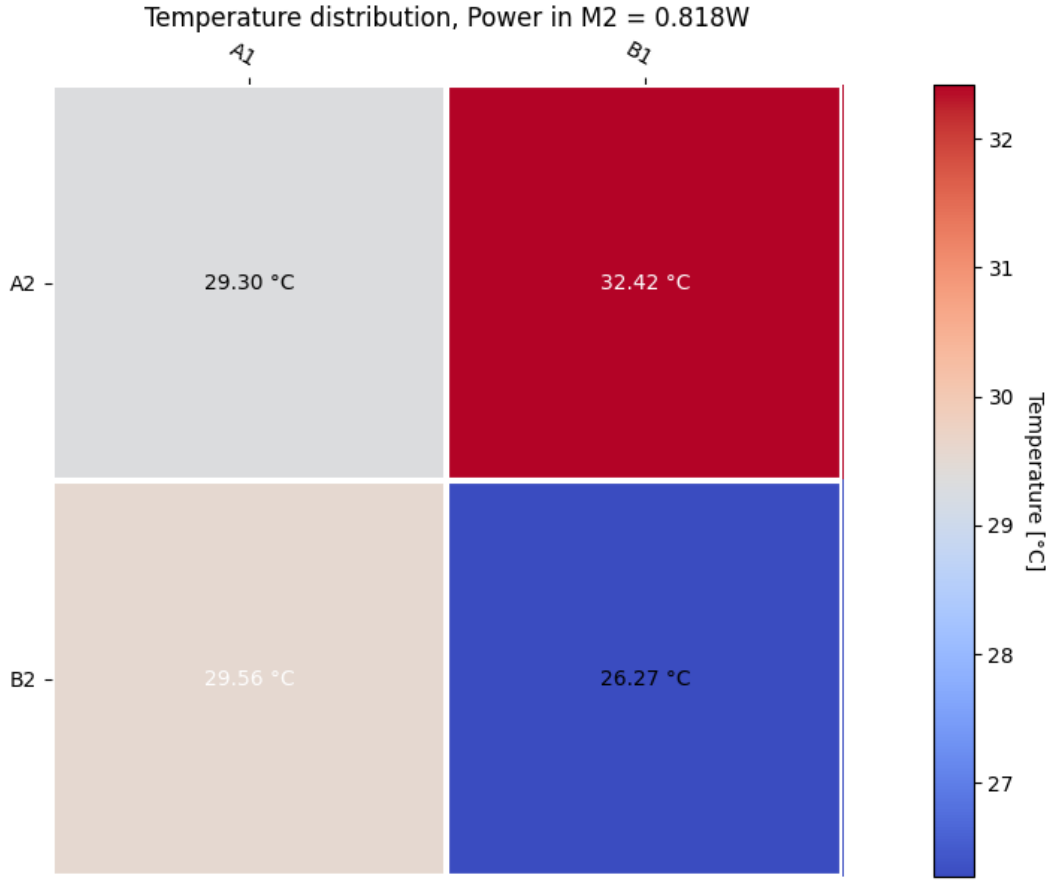
6 | Device Testing: Results



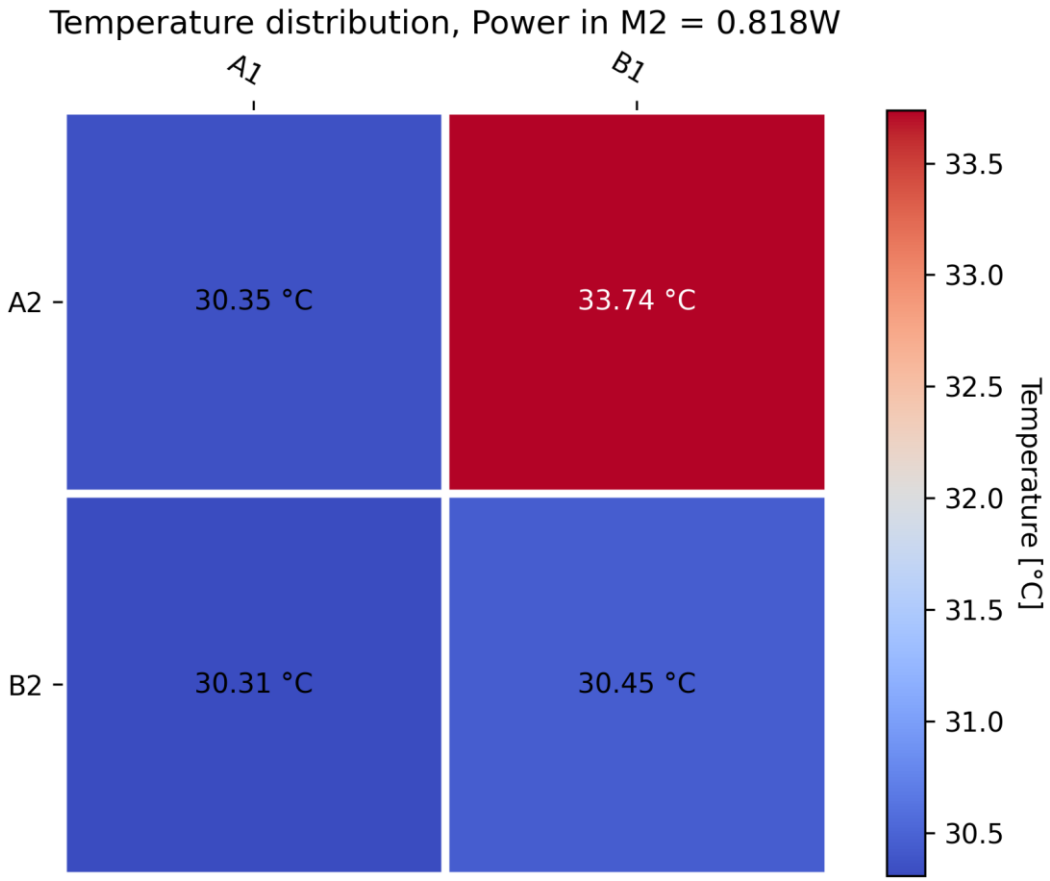
T_sensed follows perfectly the T_backside trend

6 | Device Testing: Example

Experiment 6| Thermal Map Visualization

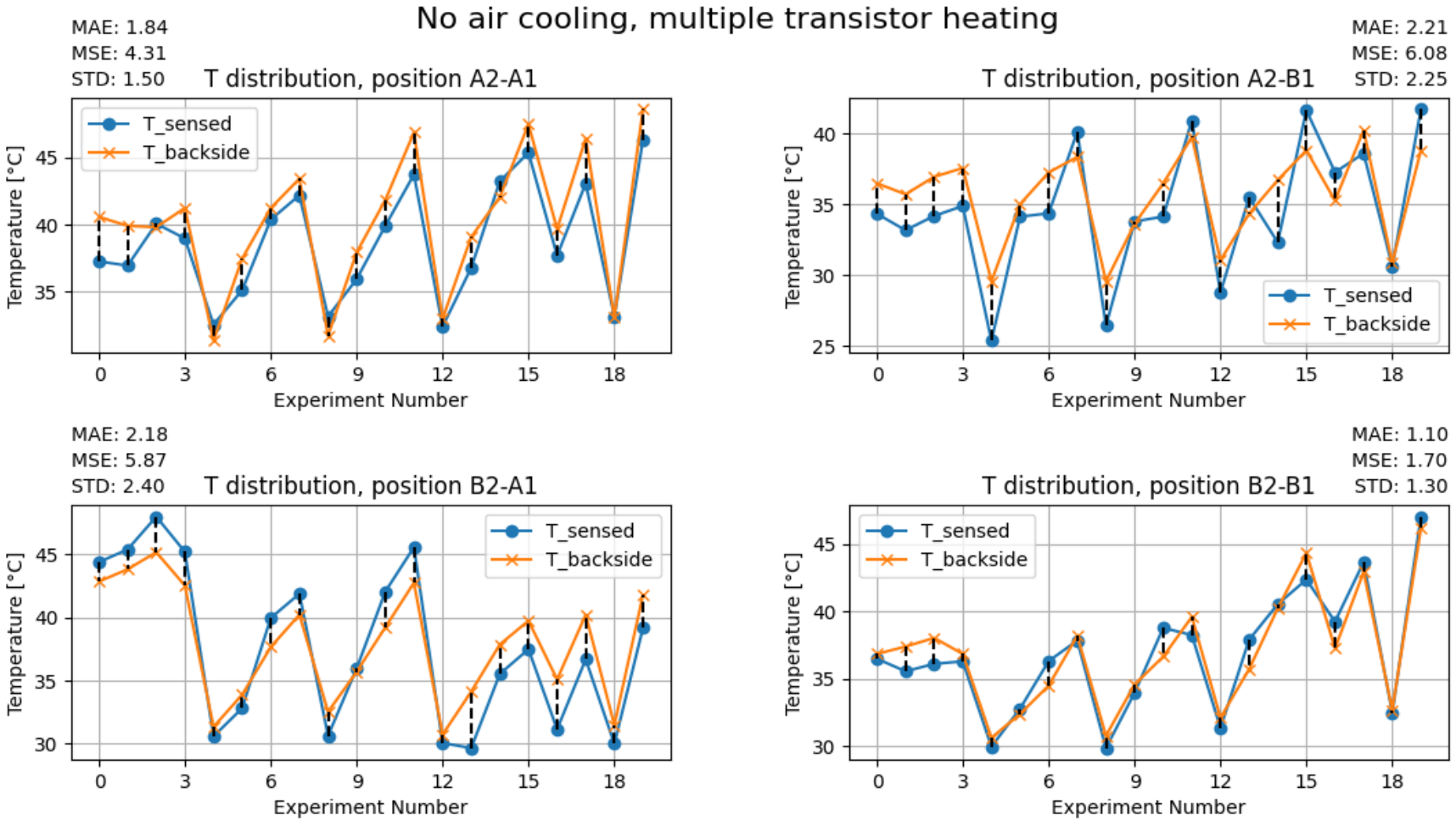


Sensing matrix



Backside resistors

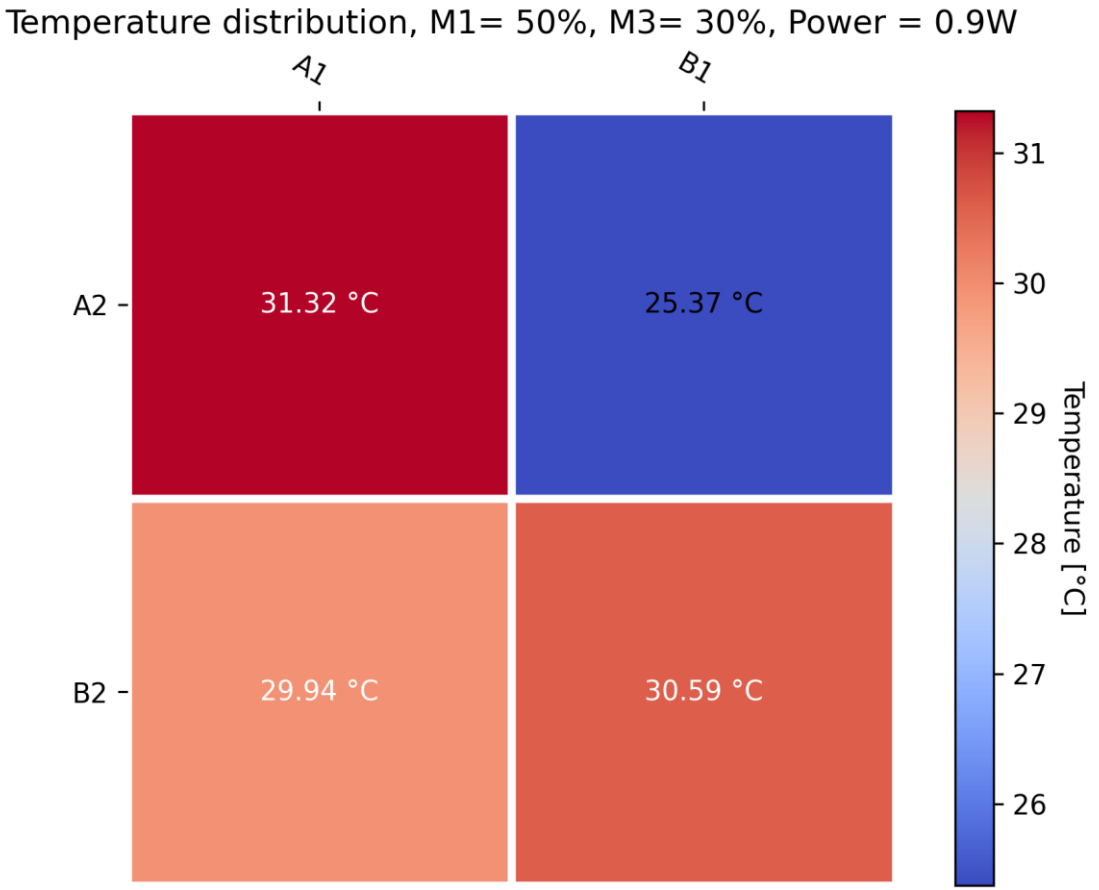
6 | Device Testing: Results



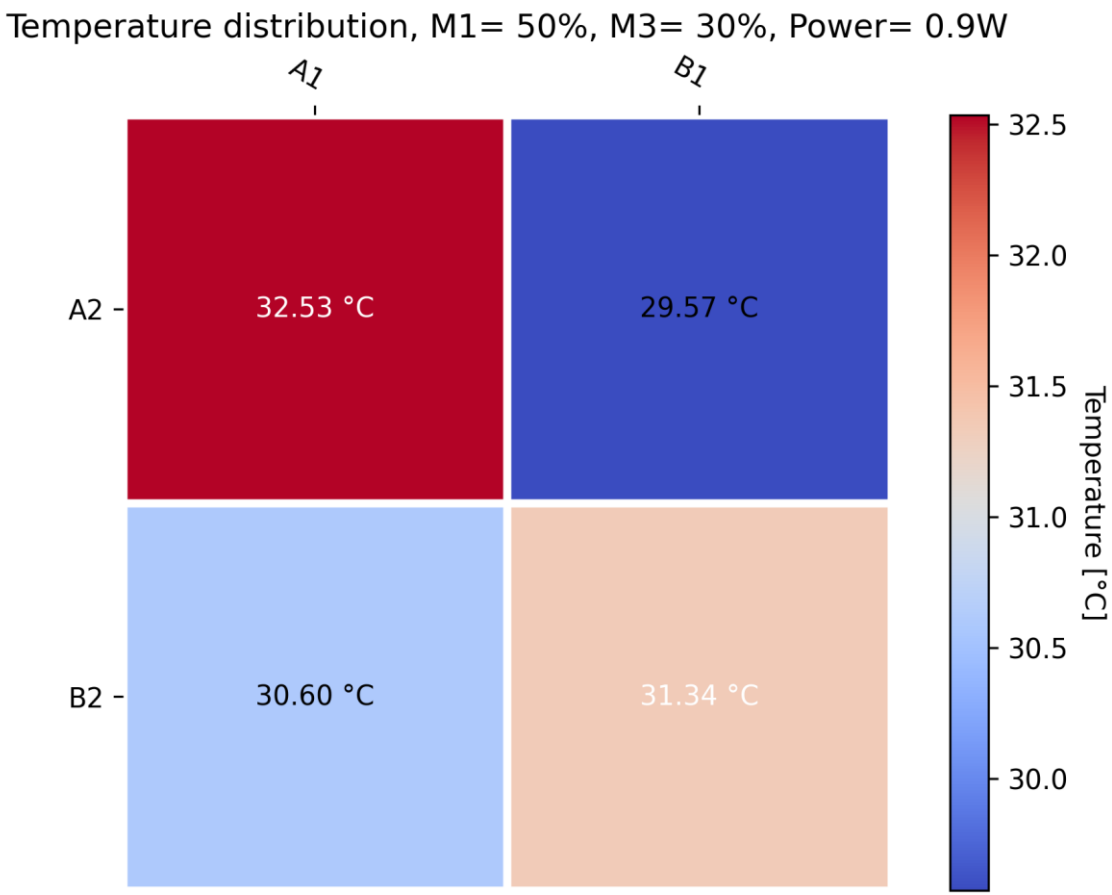
T_sensed follows perfectly the T_backside trend

6 | Device Testing: Example

Experiment 1 |Thermal Map Visualization

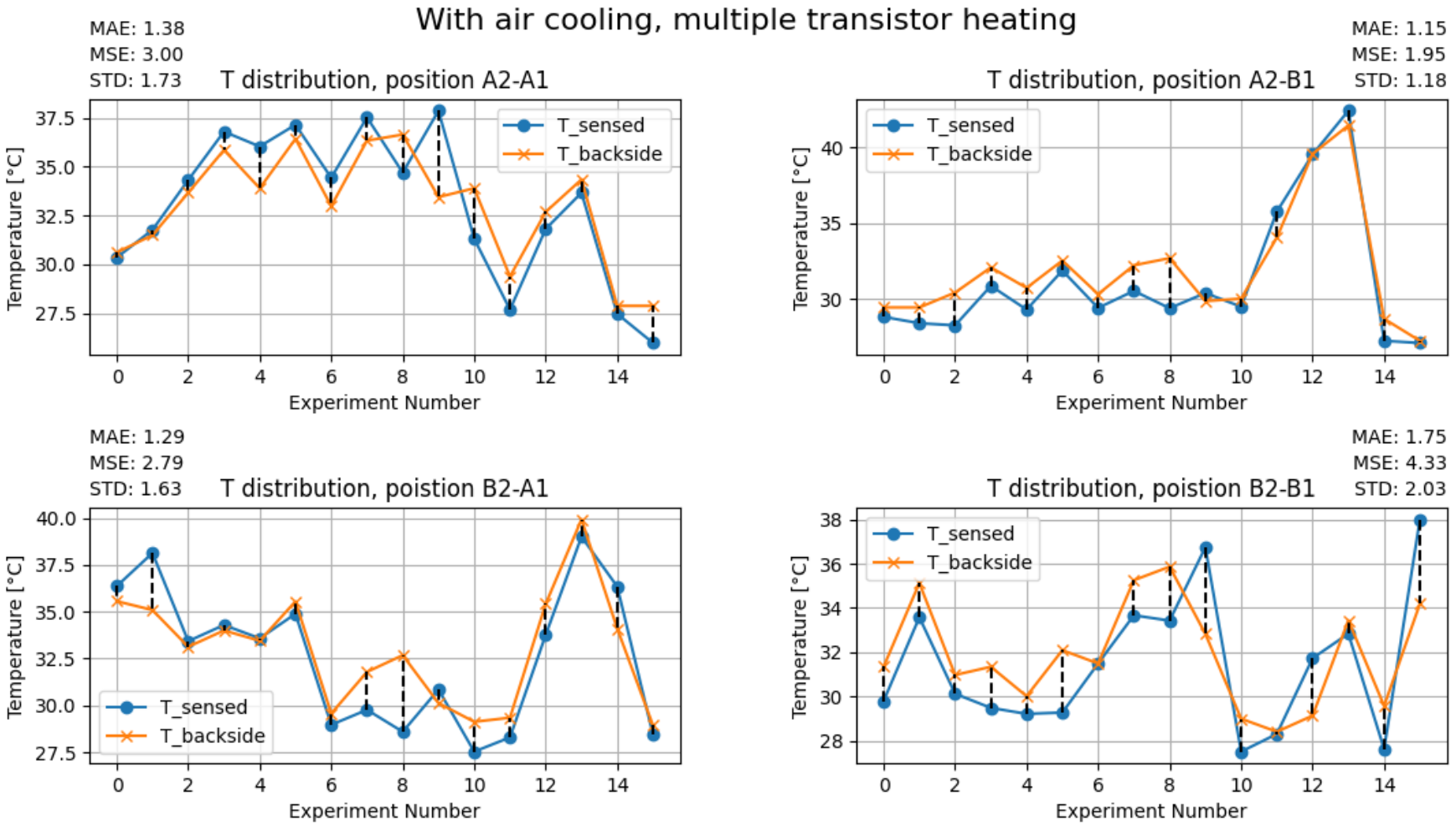


Sensing matrix



Backside resistors

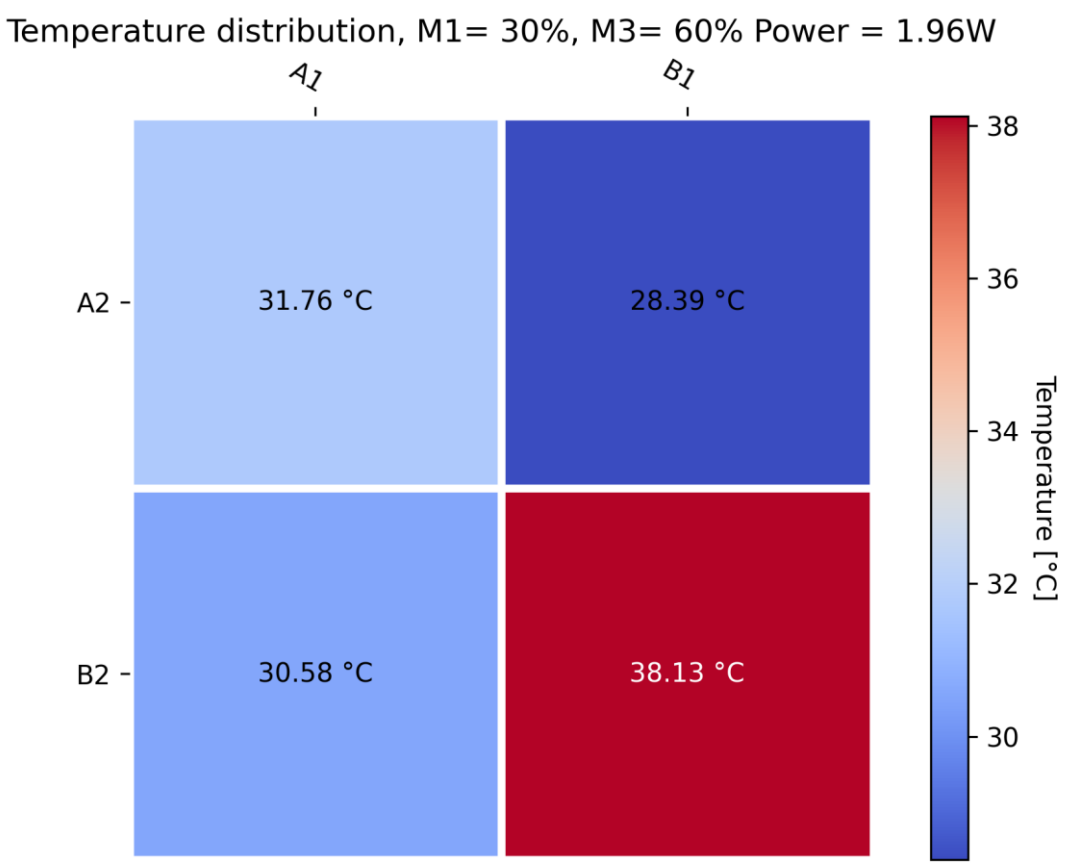
6 | Device Testing: Results



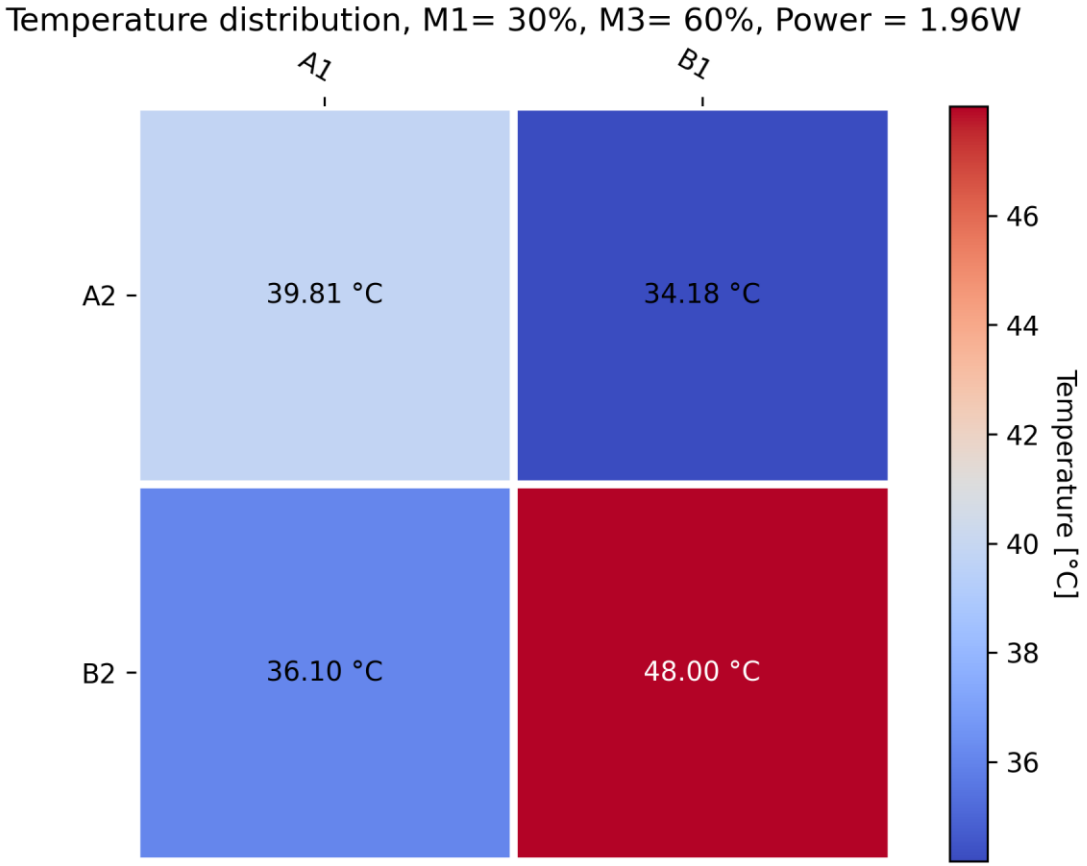
T_sensed follows perfectly the T_backside trend

6 | Device Testing: Example

Experiment 2 |Thermal Map Visualization



Air cooling



No air cooling

6 | Device Testing: Results

Table 4: Temperature[°C] sensed at position B2-A1, no air cooling

	Vin = 5V	Vin = 6V	Vin = 7V	Vin = 8V
DC_M1 = 50%	29.21	28.52	32.00	33.97
DC_M2 = 50%	26.05	29.56	32.69	34.00
DC_M3 = 50%	28.05	30.26	33.91	34.63
DC_M4 = 50%	28.84	35.45	31.95	43.94

Table 8: Temperature[°C] backside at position B2-A1, no air cooling

	Vin = 5V	Vin = 6V	Vin = 7V	Vin = 8V
DC_M1 = 50%	29.72	30.45	31.64	31.94
DC_M2 = 50%	29.72	30.31	31.05	34.00
DC_M3 = 50%	29.41	30.63	30.75	36.79
DC_M4 = 50%	32.09	33.56	35.87	40.70

- Gradual increase of T sensed with increased power consumption
- T sensed comparable to T backside

6 | Device Testing: Results

Table 6: Temperature[°C] sensed at position A2-A1, no air cooling

	Vin = 5V	Vin = 6V	Vin = 7V	Vin = 8V
DC_M1 = 50%, DC_M4 = 30%	32.97	39.07	42.06	47.51
DC_M1 = 50%, DC_M4 = 40%	33.07	39.67	46.44	48.62

Table 12: Temperature[°C] sensed at position A2-B1, no air cooling

	Vin = 5V	Vin = 6V	Vin = 7V	Vin = 8V
DC_M1 = 50%, DC_M4 = 30%	28.77	35.50	32.31	41.63
DC_M1 = 50%, DC_M4 = 40%	30.62	37.26	38.59	41.70

Table 14: Temperature[°C] sensed at position B2-B1, no air cooling

	Vin = 5V	Vin = 6V	Vin = 7V	Vin = 8V
DC_M1 = 50%, DC_M4 = 30%	30.06	29.66	35.54	37.49
DC_M1 = 50%, DC_M4 = 40%	30.00	31.15	36.69	39.18

Table 16: Temperature[°C] sensed at position B2-A1, no air cooling

	Vin = 5V	Vin = 6V	Vin = 7V	Vin = 8V
DC_M1 = 50%, DC_M4 = 30%	31.33	37.9	40.54	42.37
DC_M1 = 50%, DC_M4 = 40%	32.47	39.24	43.67	47.05

The highest temperature is recorded under the most heated element.

The device can detect varying hotspot intensities

6 | Device Testing: Cooling effect

Table 18: Temperature[°C] sensed at position A2-A1, no air cooling

	Vin = 7V	Vin = 8V
DC_M1 = 50%, DC_M4 = 30%	43.25	45.38
DC_M1 = 50%, DC_M4 = 40%	43.08	46.35

Table 19: Temperature[°C] sensed at position A2-A1, air cooling

	Vin = 7V	Vin = 8V
DC_M1 = 50%, DC_M4 = 30%	32.98	36.33
DC_M1 = 50%, DC_M4 = 40%	33.44	36.64

Table 22: Temperature[°C] sensed at position B2-A1, no air cooling

	Vin = 7V	Vin = 8V
DC_M1 = 50%, DC_M4 = 30%	35.54	37.49
DC_M1 = 50%, DC_M4 = 40%	36.69	39.18

Table 23: Temperature[°C] sensed at position B2-A1, air cooling

	Vin = 7V	Vin = 8V
DC_M1 = 50%, DC_M4 = 30%	29.57	31.79
DC_M1 = 50%, DC_M4 = 40%	30.13	32.68

The device can detect the effect of air cooling

6 | Device Testing: Comments

- Results generally aligned with expectation
- Cooling effect observed
- STD between sensed and extracted temperatures never exceeds 2.66°C, which is acceptable given thermal interface presence
- Promising precision within typical temperature ranges for circuits

Note: Still need for larger samples of data for more reliable statistical considerations

7 | Conclusion

- The designed circuit proved to operate correctly for large matrices on software simulation
- A small prototype made of a matrix of resistors 2x2 produced satisfactory results in the real laboratory experiment
- Investing time to address challenges and develop a larger prototypes is worthwhile given the promising results

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8 | Resolution Improvement

Challenge:

- Limited to identifying four temperature regions

Solution:

- Scale up to the resistor matrix
- RTDs on PCB easy integrable
- **Alternative**: Use Pt stripes to save space

Benefits:

- Detailed thermal maps
- Precise cooling based on real-time data

8 | Handling Correlation

Challenge:

- More equations yield higher correlation.
- Ill-posed problems causing non-convergence

Solution:

- Implement Tikhonov regularization

Benefits:

- Stable and accurate matrix computations
- Reliable thermal mapping

8 | Hardware Testing Challenges

Challenge:

- Complex independent control of gate transistors

Solution:

- Use a DEMUX device to simplify control
- Reduces signal requirements from M to log2(M)

Implementation:

- DEMUX controls with pulse squared waves
- Rapid switching creates temporary simultaneous hotspots

Benefit:

- Efficient testing of larger prototypes

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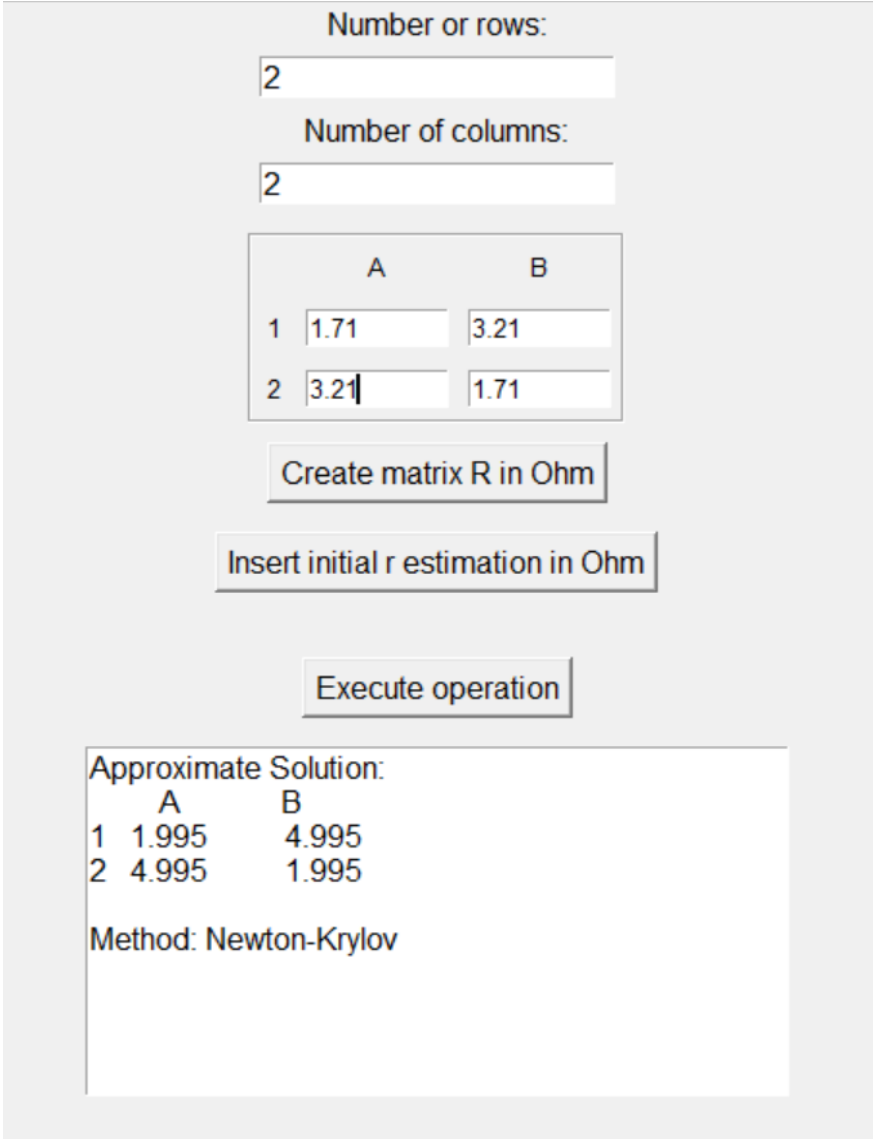
THANK YOU FOR THE ATTENTION

Appendix | Code: GUI

Inputs:	Output:
Number of rows and column in the matrix, matrix of measured R, initial estimation of the singular r	Resistance matrix with calculated values, method with which was calculated and plot of temperature distribution in the quadrants



Appendix | Code: Pseudocode of the two main functions

Calculate G from g

Input: matrix of cell conductances $g_i^j, i = 1, \cdots, N \; j = 1, \cdots, M$
Output: matrix of equivalent conductances $G_i^j, i = 1, \cdots, N \; j = 1, \cdots, M$
for all pairs (i, j) **do**
  Solve equations 3 and 4
  $G_i^j \leftarrow \frac{I_{ref}}{V^j - V_i}$
end for

Iterate

Calcolate g from G

Input: $\mathbf{G}$,β, f_{tol} and n_{max} and initial iterate $(\mathbf{g}_0)$
Output: Approximated solution $\mathbf{g}$
$n \leftarrow 0$
$residual \leftarrow \max(|G_i^j - F_i^j(\mathbf{g}_0)|)$
while $n < n_{max}$ **and** $residual > f_{tol}$ **do**
  $\mathbf{g}_{n+1} \leftarrow \mathbf{g}_n + \beta(\mathbf{G} - \mathbf{F}(\mathbf{g}_n))$
  for all pairs (i, j) **do**
    if $(g_i^j)_{n+1} < 0$ **then**
      $(g_i^j)_{n+1} \leftarrow 0$
    end if
  end for
  $residual \leftarrow \max(|G_i^j - F_i^j(\mathbf{g}_{n+1})|)$
  $n \leftarrow n + 1$
end while
return $\mathbf{g}_n$

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Appendix | Code: Verification via LTSpice Cont

Automatize the process by exploiting the library PyLTSpice

Input: Vector with ground position, vector with current position, r value and the connecting nodes

Output: operating point at every node

```
# Import the netlist
# In this netlist, there is NO current source, NO gnd connection and NO simulation setup
netlist = SpiceEditor("circuit.net")

# Setup all the positions of the current source
gnd_positions = ["1", "1", "1", "1","1","1", "1", "1", "1"]
curr_positions = [("1", "A"),("1", "B"),("1", "C"),("2", "A"),("2", "B"),("2", "C"), ("3", "A"),("3", "B"),("3", "C")]

# Run the simulations
for case in range(len(curr_positions)):
    simulate(netlist, gnd_positions[case], curr_positions[case], runner)
```

```
Running simulation for netlist_1_A
Handling the simulation data of Simulations\circuit_1.raw, log file Simulations\circuit_1.log
Simulation results:
Trace V(1): 0.000000
Trace V(a): 1.320000
Trace V(b): 0.706778
Trace V(c): 0.661233
Trace V(2): 0.855890
Trace V(3): 0.864727
Trace I(I1): 1.000000
Trace I(G9): 0.068066
Trace I(G8): 0.158371
Trace I(G7): -0.226438
Trace I(G6): 0.097472
Trace I(G5): 0.018448
Trace I(G4): -0.115920
Trace I(G2): -0.165539
Trace I(G3): -0.176819
Trace I(G1): -0.657642
Trace I(Gnd): 0.000000
```

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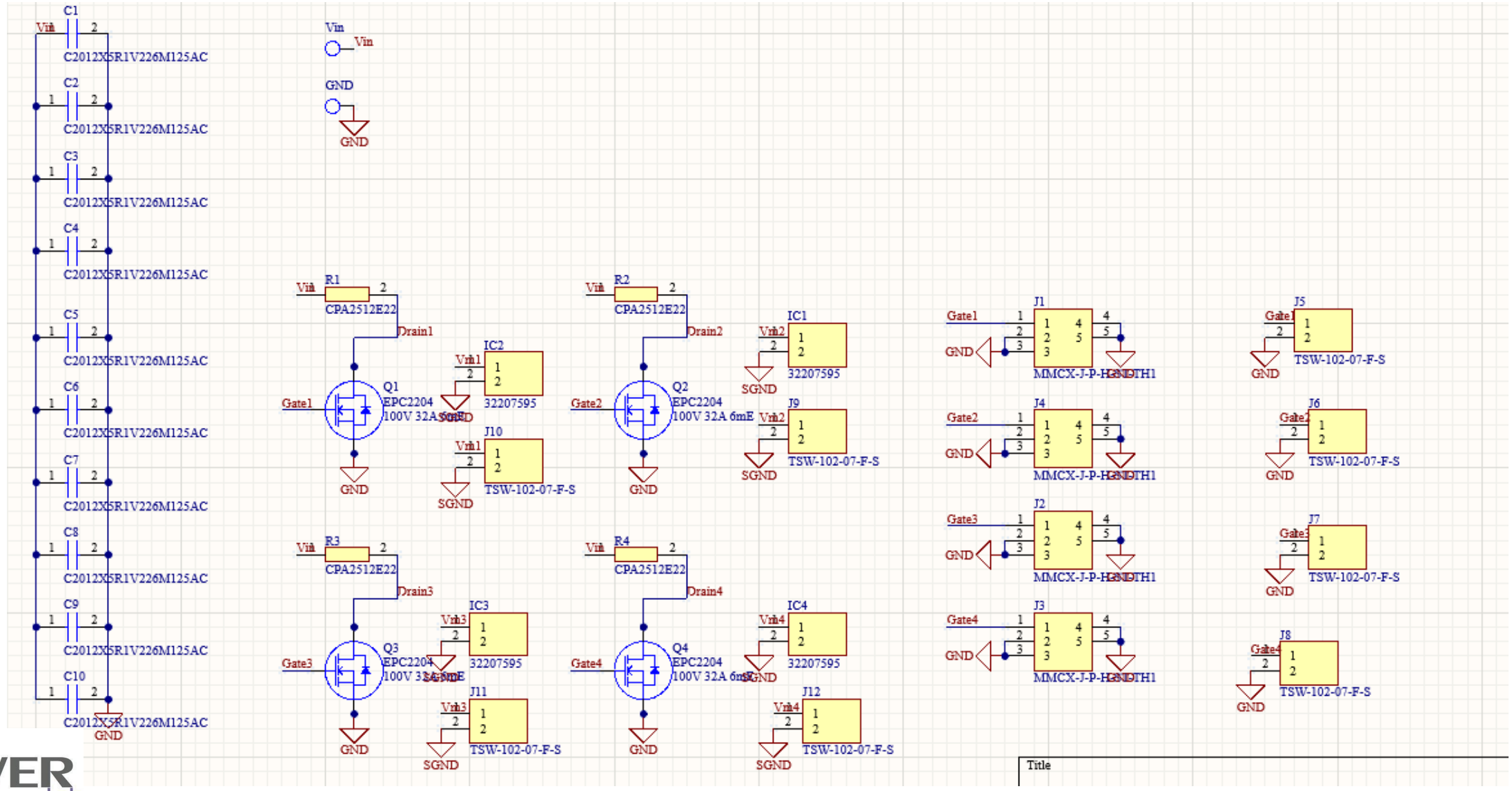
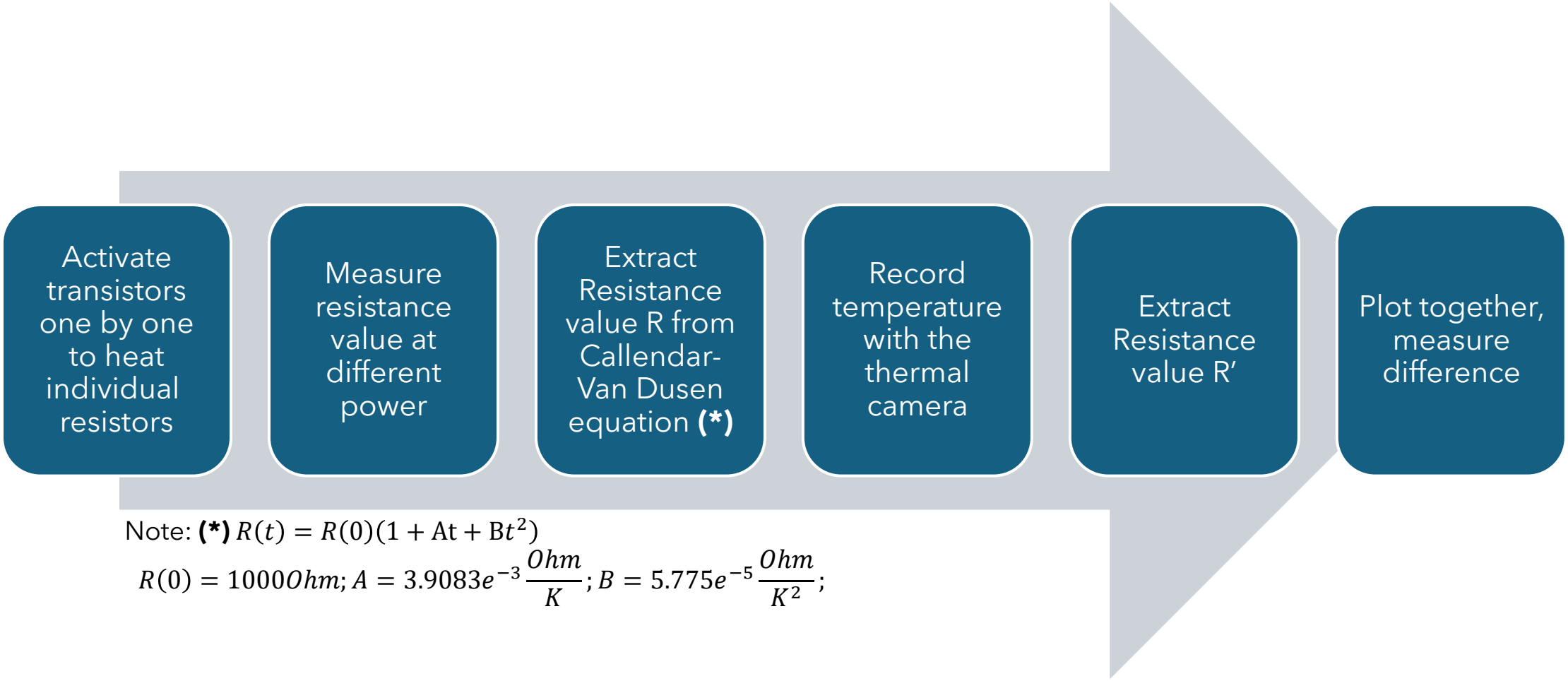
Appendix | Full PCB Schematic



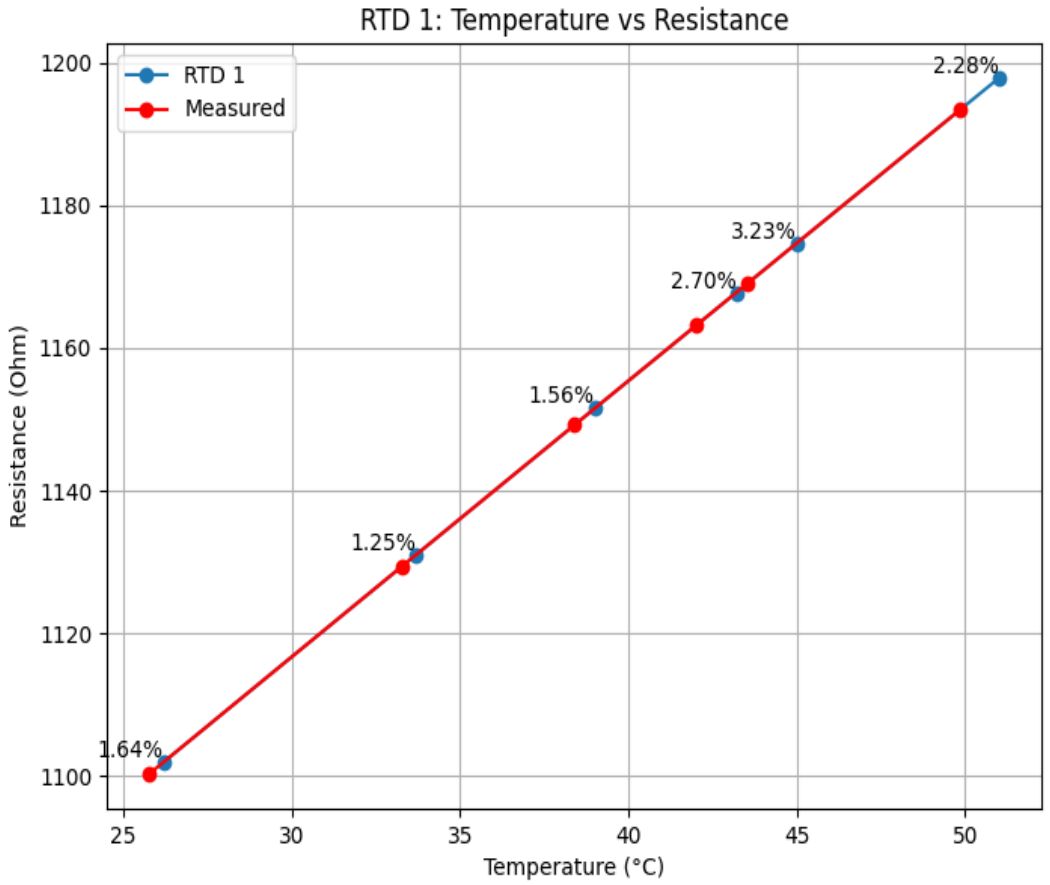
6 | Device Testing: Calibration

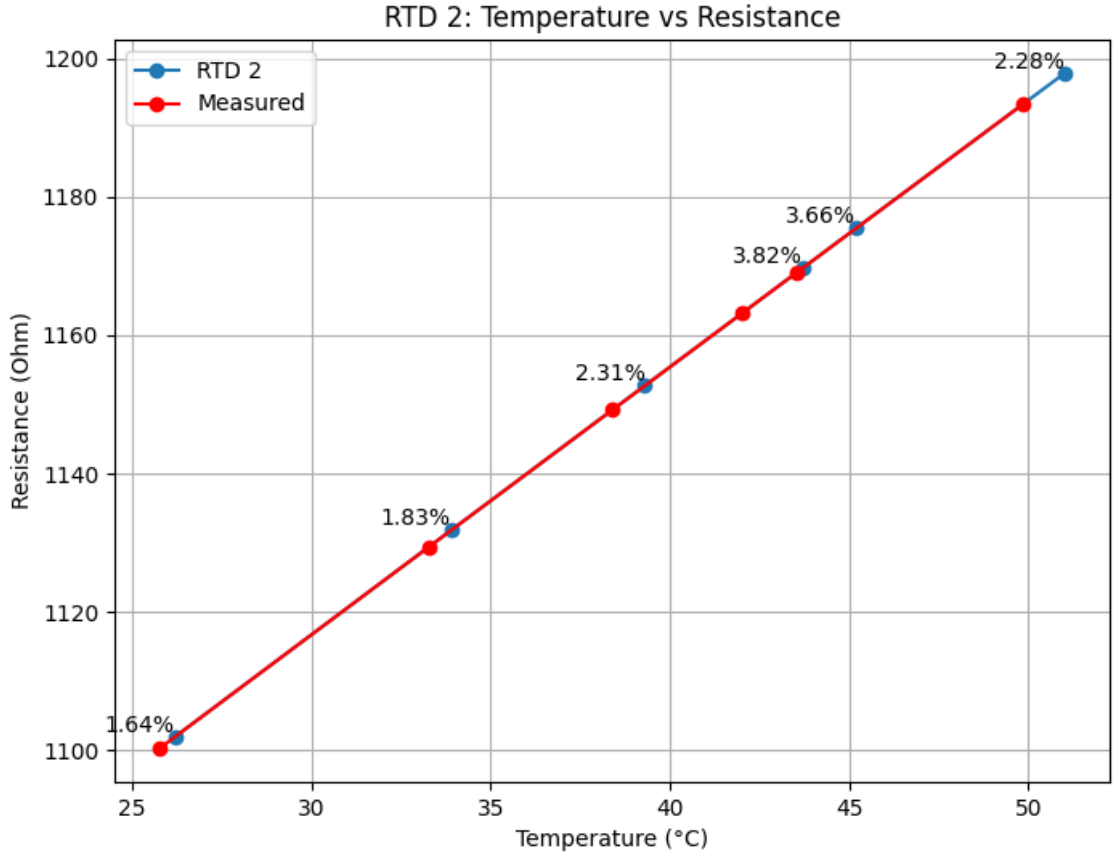


Note: **(*)** $R(t) = R(0)(1 + \mathrm{A}t + \mathrm{B}t^2)$

$R(0) = 1000Ohm; A = 3.9083e^{-3}\frac{Ohm}{K}; B = 5.775e^{-5}\frac{Ohm}{K^2};$

6 | Device Testing: Calibration





6 | Device Testing: Calibration