Voter2-2K
Hardware Reference Manual

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1 INTRODUCTION

This document describes the hardware requirements, design choices, and architecture of the “Voter2-2K” project. This is the first Voter2 with the Voter2-2K specifically designed to fit inside the Motorola MTR-2000 repeaters “Option1” or “Option2” card slot.

The Voter2 is a successor to the original Voter design by Jim Dixon, WB6NIL (SK). At about 10 years old, that design using parts that are becoming obsolete so a new design using current silicon is in order. This newer silicon will also allow significant increases in compute power and memory not economically feasible a decade ago. This added capability will allow additional features, but the baseline feature set must be fully compatible with the Voter protocol, allowing it to fully interoperate with existing Voters and DIAL servers without modification. Where features are significantly different from the original Voter, these will be noted.

A design goal for the Voter2 is to be producible for the long term. In particular for component selection the major parts need to be from reputable suppliers we reasonably expect to be around for the long term. No parts available only from Ebay or Ali Express!

As with the Voter, the Voter2 is a fully open-source hardware and software project.

This revision of the document reflects the feature set of the Rev 1.1 PCB.

2 SCOPE

This document primarily describes the hardware architecture of the device. Its purpose is to introduce the reader to the device’s hardware features and capabilities. A high level overview of the software architecture is included to explain the hardware chosen.

As this is the first Voter2 project, this will describe the entire project. Subsequent Voter2s that target different repeaters (or a stand-alone Voter2) will only need to describe any target-specific differences from this initial design.

The Voter2 hardware platform has a few features not intended for the Voter2 project, but instead for an S-COM project using this same hardware. The Voter2 software will just have code intended to test this hardware. These features are certainly available to the Voter2 project if we come up with a use for them.

3 MCU SELECTION

The choice of MCU was a critical decision and tough given the many good choices available. In order to be as future proof as possible several key requirements narrowed choices. They were:

- Widely accepted architecture to allow a vendor change if needed.
- A vendor with a good track record and promised part production longevity.
- A family of parts reasonably pin-compatible allowing a part upgrade/downgrade if needed.
- As many of the necessary peripherals on-chip as possible.
- Excess CPU horsepower and memory above our initial needs to allow future features
- An instruction set that includes DSP functions for efficient DSP operations
- Free (and good) development tools.
- Alas through-hole packaging cannot be a requirement now. While SMT is the only viable option, it must be parts that can be hand-soldered, not parts that require ovens or IR reflow soldering.

The obvious architecture is the ARM Cortex M series as they dominate the embedded space. The Cortex M7 is the highest performing core in that family allowing processing in the 1000+ DMIPS range, including floating point support and a robust DSP instruction set. A Cortex M4 would be sufficient, but the M7 gives some headroom. Maybe excessive headroom.

There are many good vendors of this architecture. The one I am personally familiar with is ST Microelectronics. They have a rolling 10-year commitment to continue making parts, so there will be a 10-year notice ahead of a part going end-of-life. TI and NXP are also good vendors for these chips with extensive portfolios; ST is just the one I am familiar with. Should there be issues with ST, the code could be ported to chips from one of these vendors.

STs Cortex M7 family is the STM32H7 series. Within that family, there are many options with different internal peripheral/memory options and slightly different CPU capabilities. All include an Ethernet MAC, important for this project. The one chosen is the one with the fastest CPU, most internal RAM and *minimal* internal Flash, the STM32H750VB. It has 1MByte of internal RAM (huge for an MCU) but only 128KBytes of flash. That small amount of internal flash will be supplemented by two external SPI NOR flash parts, a 4Mbyte QSPI NOR part supporting direct execution of code and a 4 or 32Mbyte SPI NOR for offline storage of downloads and data. The external QSPI flash will be slower to access for code execution than internal flash, but is cacheable, much less expensive per byte and also more flexible. That external flash can be easily increased in size.

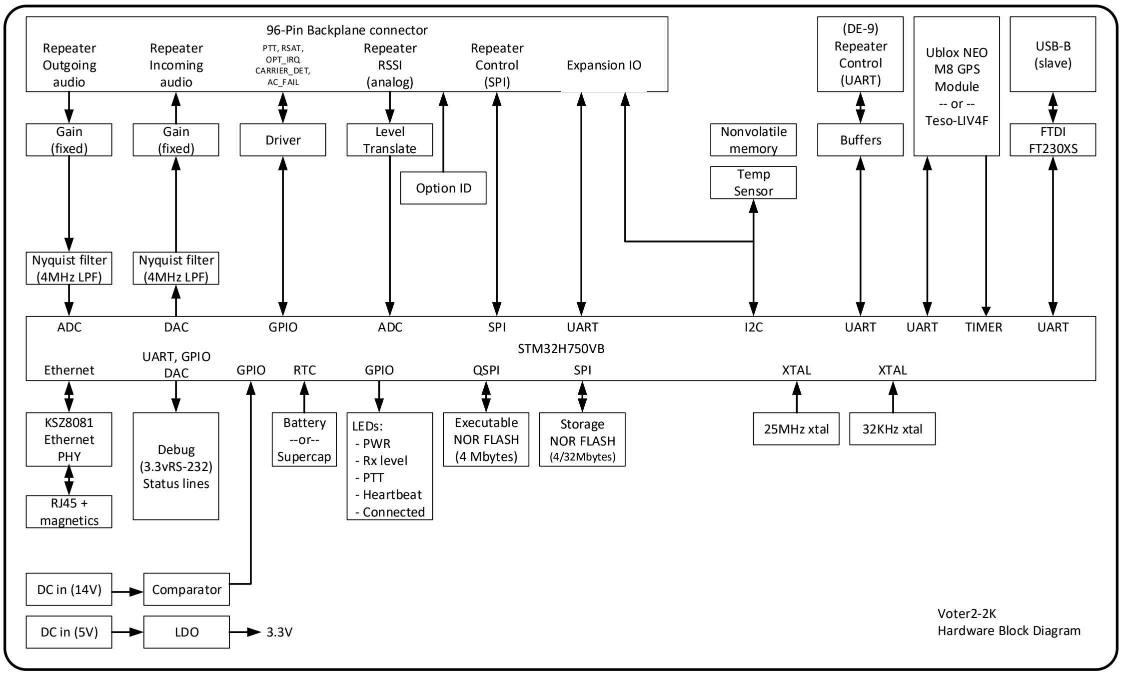
In addition to data and instruction caches, the MCU has two dedicated “tightly coupled” zero-wait-state memories for time critical code and data. These will be used for compute-heavy DSP routines and any other time-critical code like ISRs. The majority of the code will be the RTOS and TCP/IP stack which are less time critical and suitable for the external QSPI NOR flash.

The STM32H750 is available in several package types. The one chosen is the 100 pin PQFP package. As features were added during the initial design, the available GPIO has dwindled from 20 to 7 pins, but there are still available GPIO.

Below is a table comparing major specifications of the Voter2 versus the original Voter:

Feature	Voter	Voter2
MCU	dsPIC33FJ128GP	STM32H750VB
Data Bus Width	16-bit	32-bit
Compute Speed	40 DMIPS	1,027 DMIPS
Flash (bytes)	128K	128K + 4 or 32M
RAM (bytes)	16K	1024K
Audio Filtering	Hardware	Software
Package	28 pin PDIP	100 pin PQFP

4 HARDWARE BLOCK DIAGRAM



Compared to the Voter, there are a few notable hardware differences:

4.1 REDUCED HARDWARE SIGNAL FILTERING AND LEVEL CONTROL

The Voter has analog filters for emphasis/de-emphasis, above-band noise detection, and CTCSS filtering. For the Voter2, these filters are implemented using DSP. The only analog filters are the necessary Nyquist filters for A/D and D/A operation. For an 8KHz audio sample rate, the analog filter cutoff frequency is 4KHz using 4th order filters.

As this board is specifically for the Motorola MTR-2000, we do not need extremely flexible audio level control, the audio levels for Tx and Rx are be fixed levels optimized for the MTR-2000.

4.2 ANALOG RSSI INPUT

A new feature request is an analog RSSI input that could be used instead of the above-band noise detection method used by the Voter. This signal is available on the backplane connector and routed to an A2D input on the MCU. This analog RSSI may not change as fast as the per-packet calculations using the "above band" method, so this input is experimental.

4.3 REPEATER CONTROL PORT

A new feature request to provide an RS-232 interface to communicate with the repeater through the Voter2 over Ethernet. The protocol implemented is the UART-over-Telnet RFC2217 Standard. This has been verified with the Motorola RSS control software. Setting up the drivers on the host computer is a bit clunky, but does work.

4.4 POWER VOLTAGE MONITOR

Initially this was an easy extra feature allowing the Voter2 to monitor the repeaters power supply outputs, but as analog IO got scarce, this feature has been omitted. Currently there is only a comparator that triggers around 12V monitoring +14.2V.

4.5 EXTERNAL REFERENCE CLOCK INPUT

A hoped-for significant new feature of the Voter2 is improved support for synchronized same-frequency transmissions or simulcasting. This is a stretch goal. Simulcasting requires the transmitters be extremely closely synchronized. In the Voter1 each Voter had its own crystal driving the A/D and D/A converter timing and these crystals naturally varied not just between crystals, but even over time and temperature. At the project start, the solution envisioned was an external 10MHz GPS-stabilized clock input to keep the audio sampling in phase. As project development progressed, we developed a "digital PLL" that yields the same result using the main GPS's 1PPS. It is therefore highly likely this input will be omitted in future PCBs once we see simulcasting working with the digital PLL.

4.6 CONSOLE INTERFACE

RS-232 ports on computers are now practically non-existent. Instead of an RS-232 port for the console interface it will be a USB slave interface using an FTDI FT230XS USB-UART bridge chip. The MCU has a USB OTG interface, but it requires its own OS driver. The FTDI chips are ubiquitous and drivers part of most OS's, so using it over the native USB controllers is for convenience on the laptop side. The connector is a USB-B mini connector. The FTDI chip is locally powered (vs bus powered) and supplies a "plugged in" state to the MCU via a GPIO. It should be noted, however that the most likely console interface used will be Telnet, not this USB/UART interface.

4.7 EXTERNAL QSPI FLASH

This is flash external to the MCU that is directly executable by the CPU called XIP (eXecute In Place). With it, the CPUs total executable code space is the 128KB internal flash plus this 4Mbyte QSPI flash. MCUs even in the H7 series exist with more on-board flash, but at a notable cost premium. This is true for MCUs from any vendor. An external flash is considerably cheaper per-bit and can be updated to bigger flash quite easily. As an example, an MCU similar to the STM32H750 but with 1Mbyte of flash is approximately $4 more. The external 4Mbyte flash is $0.90. The MCU can support an external flash up to 256Mbytes!

4.8 EXTERNAL SPI FLASH

In addition to the XIP flash, this flash is for offline storage, it is not directly executable by the CPU. Its primary purpose is to store a complete software update image locally and fully verify its integrity before initiating a software update. It is a separate flash from the main XIP flash as it is very difficult to program the same flash that you are also executing code from. This allows the full IP stack running from the XIP flash to continue running while storing the downloaded image into this secondary flash. It will also be the place to store the few "OTP" (One Time Programmable) settings such as MAC address and serial number.

For the S-COM project, this offline flash needs to be much larger, 32Mbytes. It will still be used for software update images, but other data as well. At this time, most SPI NOR flash above 16Mbytes require a larger footprint. The PCB therefore has two footprints for this flash, the smaller one for Voter2 and the larger footprint for the S-COM project. They share the same signals, so only one can be loaded.

4.9 REAL TIME CLOCK

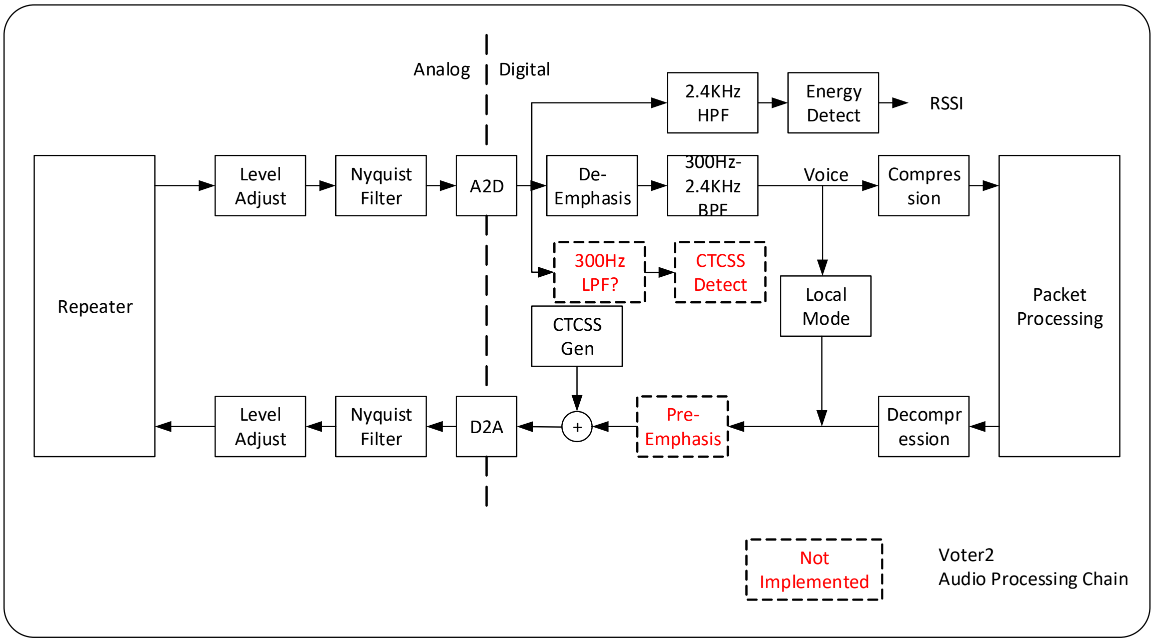
There are some rare but possible circumstances where a local real-time clock could be handy. These mainly have to do with accurate diagnostics logging in situations where network time is not (or not yet) available. The MCU has full RTC support, so "all" that is needed is a battery and 32KHz crystal. A battery is also handy for faster GPS acquisition time, so this optional battery has two possible users. A jumper to allows the battery to be omitted and the crystal can be omitted as well if not desired.

4.10 UNUSED BUT AVAILABLE FEATURES

The STM32H750 has several other interfaces available that are currently not being used, these could be opportunistically included in the future if there are no pin conflicts with existing features, however spare GPIO is getting scarce. They are 1) more I2C, SPI and UART interfaces, 2) an SDIO/MMC SD card interface, 3) CAN interfaces, 4) 2 USB OTG interface, 5) and a digital camera interface.

5 DSP FLOW DIAGRAM

Below is the proposed DSP flow diagram for audio functions—including showing the split between hardware filtering and software filtering.



As mentioned in the hardware section, the only analog filtering for audio in and out is Nyquist filtering. For incoming audio, after digitizing, the samples will go to a first order De-emphasis filter, a 2.4KHz high-pass filter and (maybe) a 300Hz low-pass filter. The high pass filter is for detecting energy above 2.4KHz for RSSI, second is a bandpass filter for voice data, and finally maybe a low pass filter for CTCSS detection.

The output of the high pass filter will go to an energy detect function to derive an RSSI value. This function is performed in the analog domain in the Voter, so suspect considerable tweaking will be necessary to come up with similar RSSI numbers to match the Voter1 results for a similar signal. One concern is that the Voter filter is able to (and does) use frequencies higher than 4KHz. That is not possible with the way our audio sampling is set up with the Nyquist filters. Options are covered later.

The output of the voice bandpass filter goes to the MuLawADPCM compressor and finally into packets with timestamps for Ethernet packet processing.

If there is a need for the Voter2 to perform CTCSS detection, the low pass filter may not be necessary as the CTCSS detector may be able to just look at the signal out of the A/D's. This will be a single filter function with access to different table entries depending on the desired CTCSS tone. As the MTR-2000 has its own CTCSS detection, this function is not planned for the Voter2-2K.

For audio packets from the packet processor to be transmitted, the samples will get decompressed using MuLaw/ADPCM, then (optionally) run through a first order Pre-emphasis filter. After that filter a CTCSS tone can be optionally added before being sent to the D/A.

In the absence of a connection to a DIAL server, the Voter2 will revert to local mode, implementing a reduced local repeater feature set similar to the local mode of the Voter1.

Of course, the nice thing about using DSP is changes—even radical changes—are entirely possible as it is "just software"! :)

6 SOFTWARE STRUCTURE

With additional memory and compute power, it is possible to use a more structured (and admittedly less space efficient) approach to the software architecture than was possible with the Voter. The limited memory available on the Voter forced a very low-level approach to packet processing. The Voter2 uses two open-source software packages. The first is the RTOS package called FreeRTOS. This is a well-supported and vetted RTOS for embedded systems allowing multiple threads, pre-emptive task swapping and inter-process comms. The second is the Ethernet stack called LwIP. It is also a well supported and vetted Ethernet stack for embedded systems supporting basic UDP and TCP traffic as well as many higher layer protocols such as DHCP and DNS. Utilizing these packages over “rolling our own” will give a big head start on code reliability. Both are open source and royalty free. If, over time these packages prove to be too burdensome, we can migrate away from either in favor of “roll our own” code. It’s “just software” :).

7 HARDWARE INTERFACES

Listed below are the external physical interfaces for the Voter2-2K.

7.1 REPEATER INTERFACE

As this is a plug-in card for Motorola MTR-2000 repeater, this is the connector available on the backplane. It is a 96-pin "Eurocard" connector. This card will plug into the Option1 or Option2 slot. Signals used from this connector are:

7.1.1 POWER AND GROUND

+5V (Pins A3, B3, C3): 5V at 1.5A max is available. There are 13 ground pins, all will be tied to a common ground.

7.1.2 TRANSMIT AUDIO

AUX_TX_AUDIO (Pin C16): Page 35 of the MTR-2000 manual calls out -20dBm to 0dBm (variable). No impedance is listed. Assuming a 600 ohm load, and a high-ish target of -6dBm, this comes to 1.1V p-p.

7.1.3 RECEIVE AUDIO

DISC_RX_AUDIO (Pin A16): Page 36 of the MTR-2000 manual calls out -20dBm to +7dBm for 100% RSD. No impedance is listed. Assuming a 600 ohm load and a high-ish target of 0dBm, this comes to 2.2Vp-p.

7.1.4 PTT

EXT_PTT (Pin A23): TTL input, Active low. While there is no mention of a pull-up on the repeater side, the pin can be left un-connected so this is implied. 5V is mentioned as the high level. It will be an open collector output from Voter2 to repeater.

7.1.5 ANALOG RSSI

Pin A22: Analog RSSI signal from repeater to Voter2. 0.5V for -120dBm to 3.5V for -40dBm. As the top voltage is above 3.3V, it needs a voltage divider before going to an MCU ADC. The open question is if this RSSI signal is responsive enough to use for voting.

7.1.6 CARRIER DETECT and RDSTAT

CARRIER_DETECT_SWITCH (Pin B29): TTL Output, active high. Output from repeater to Voter2 indicating a carrier is present. RDSTAT (Pin A31): Output, active high. Output from the repeater to the Voter2 indicating a valid CTCSS tone. The Voter2 is user-programmable to react to either, both, or neither of these inputs.

7.1.7 SPI BUS

MOSI (Pin A7), MISO (Pin B8), SCK (Pin C8), OPx_CS1 (Pin B11), OPx_CS2 (Pin A10). Signals are OP1_xxx for Option slot 1, OP2_xxx for Option Slot 2. The MTR-2000 is the bus master and Voter2 the slave. If the MTR-2000 asserts CS1, that is a write to the Voter2. If the MTR-2000 asserts CS2, that is a read from the Voter2. Reads and writes are 16-bits. The MCU has only one chip select and since the two Chip selects by the MTR-2000 are mutually exclusive, the two chip selects are combined and logic (an RS-flip-flop) notes which chip select was asserted which is read by the MCU.

7.1.8 OPTION_ID

This is an analog voltage to the MTR-2000 to know a board is plugged in and what class board is plugged in. To the MTR-2000 the Voter2 shows up as a CLN6698 Aux IO card. The voltage supplied by the Voter2 is approximately 0.38V. Editor's note: The schematic I copied had both pull-down resistors on OPTION_ID, no idea why. I put both in the layout but not loading the larger resistor.

7.2 GPS INTERFACE:

The Voter2-2K supports two on-board modules. The first is a daughter card, the NEO M8 module. This module uses a "sub-module" from Ublox which is a good long-term supplier, but the module itself is likely a short-term company. The second is a direct on-PCB GPS module from ST Micro, the Teso LIV4F, a more costly module, but that is a much more reliable long-term source.

7.3 ETHERNET INTERFACE:

RJ45 connector with LEDs for speed and activity. The interface supports up to 100Mbps full duplex. While the MCU has an Ethernet MAC, an external PHY is necessary. The one chosen was for its low cost, wide availability from a reputable supplier and being hand-solderable.

7.4 EXTERNAL CLOCK:

SMA connector. The incoming clock is DC isolated with a P-P voltage of 1V (approx) to 5V. Expected frequency is 10MHz. If this circuit is not needed, install R52 to ensure no floating inputs into the MCU.

7.5 LEDS

The six LEDs are:

7.5.1 POWER:

Green. Lit if there is power, no SW dependency.

7.5.2 HEARTBEAT

Green. 1 blink/sec if the RTOS is running. Also blinks 5 times rapidly on boot-up if NVM is blank/corrupted and factory defaults loaded into volatile memory only.

7.5.3 CONNECTED

Yellow. On if Voter2 is authenticated to a DIAL server. Blinks if communicating with the DIAL sever, but not authorized.

7.5.4 AUDIO LEVEL

Red/Green. Off for no audio, yellow for low audio, green for good levels, and red for overdriven audio.

7.5.5 TRANSMITTING

Red. On for transmitting (PTT active).

7.5.6 GPS

Yellow. On if getting valid GPS data and 1PPS. Blinks if getting GPS but not (yet) 1PPS.

7.6 DEBUGGING CONNECTORS

To support debugging, the following connections are included. These certainly will be installed on initial units, but may be optional once the project is being produced.

7.6.1 ST DEBUG INTERFACES

The first is a standard 0.05” pitch 14-pin connector supporting full debug, tracing, and a UART interface for debugging messages from the application. The second is the simpler 6-pin 0.1” header compatible with the lower cost ST Nucleo boards.

7.7 REAL TIME STATUS

These are simply GPIO pins on the CPU. They get updated by software at the start and end of critical real-time routines. Their intended use is to be able to observe with an oscilloscope in real time when (and how long) critical code is running. Three signals are defined for the Timer ISR, Audio ISR, and DSP ISR. As they are GPIO though, they could be repurposed for anything. A fourth signal is a DAC output to show the audio signal at intermediate stages of the audio DSP chain, very handy for DSP debugging.

7.8 RESET BUTTON

Calling this a debug feature!

8 INTERNAL HARDWARE

Besides hardware associated with external connections, there is additional internal hardware of note:

8.1 SOURCE VOLTAGE MONITOR

This was a feature of convenience, but alas in working through the IO “Tetris”, this feature fell victim to IO constraints. The pins available as A/D inputs overlapped considerably with the Ethernet interface, so a feature I hoped would be almost-free wasn’t possible. Monitoring for 14V is a comparator triggering at about 12V and there is no monitoring of 5V as its value would be limited to a failure that was less than 5V but more than 3.5V as below that voltage the MCU would reset. The value of the 14V monitor is questionable.

8.2 EEPROM

This is a standard 24LCxx EEPROM. It is currently in a not-quite-so-standard TSOT-5 package The size selected is a 24LC64 (64kbit/8Kbyte).

8.3 TEMPERATURE SENSOR

A P3T1755 I2C temperature sensor from NXP. This looks to be a good, cheap sensor from a reputable vendor. It will share the same I2C bus as the EEPROM. The I2C bus is also routed to the backplane connector where other devices can be detected and communicated with.

8.4 POWER CONDITIONING

Only +5V is used for powering the Voter2. 14V is only monitored. A filtered +5V is used for +5VA (analog) and an LDO regulator is used to derive +3.3V (digital) and additionally filtered for +3.3VA (analog). The power condition block also generates a low impedance 1.65V (1/2 off 3.3V) for the op-amp virtual grounds.

8.5 BATTERY/SUPERCAP

The battery/supercap supports two optional features and is therefore optional itself. The footprint can fit either a CR2032 battery holder or a specific 1F supercap. While the Ublox GPS module has its own battery, the Teso GPS module does not. Battery/supercap support for the GPS module allows quicker recovery after a short power failure. The battery can also support the MCUs Real Time Clock circuit if it is desired. If neither function is desired, install J10 to provide “regular” power instead. Resistor R56 is to support current measurements during development and may be omitted in the future. No software support is require for the battery, but software is required to enable charging the supercap if used. This software isn’t planned at this point.

8.6 TEST POINTS

Of the seven unused GPIO, three are routed to test points for convenience.

9 PRINTED CIRCUIT BOARD

The dimensions of the PCB are fixed by the size of the card cage in the MTR-2000. The design fits easily on a 2-layer board with plenty of ground plane. SMT is unavoidable. My goal is for all parts to be hand solderable, even if SMT. This practically limits pin pitch to around 0.5mm and discrete parts to the 0805 form factor. Through hole parts are still allowed and indeed encouraged for connectors for robustness.

10 DUT (DEVICE UNDER TEST) BOARD

If there are any developers interested in significant software development, a DUT board exists that allows considerable software development without needing an entire repeater. The Voter2 plugs into this board and allows connecting to a microphone, powered speaker, or BNC connectors for signal generators and scopes. It provides power and several useful control signals such as RSSI, AC_FAIL, and RESET. It also allows testing of the external I2C and UART lines. Finally, it supports interfacing to the Digilent AD2/AD3 IO boards which is intended for some form of automated testing.