**FE-I4 code for emulator, release V0.0**

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**Disclaimer**

The version of the FE-I4 blocks used in this release is not the most up to date one. However, for the functionality that this release implements, the version used works fine.
The register definition is done according to the table in the document "FEI4_FINAL_REGISTERS-v9.xls".

**Note**

Keep in mind that every release of the FEI4 code for the emulator implements some functionality of FE-I4, and thus behaves as FE-I4. For a better and deeper understanding of what it does, I recommend to get familiar with FE-I4 before/instead of looking at the emulator code. Plenty of literature on FE-I4 can be found on the indico.

**Functionalities**

This second release of the FE-I4 code for the emulator board allows to write global registers, and to read the configuration back. It expects a **40MHz** clock and the following **slow commands: write register, read register**. The output data format can be **8b10b** or **raw**. The data sent back can be **address record + value record**, or simply **value record**. The output speed is **40Mbps**. For a description of the FE-I4 data output protocol for IBL please refer to the specific document.

**Target applications**

- USBPix firmware/software development

**Implementation**

The main components of the code are

- A **DCM** for clock buffering and multiplication
- The command decoder block (**CMD**)
- A configuration memory written according to the specs of the one in FE-I4 (**CONFIGMEM**)
- The End Of Chip Logic block (**EOCHL**)
- The Data Output block (**DOB**)

The CMD, EOCHL and DOB block syntax has not been modified at all. These blocks stayed exactly as they have been written for FE-I4.
The connections between the blocks are minimal, and basically they are only those needed for the above mentioned task of writing and reading configuration. In particular following the table mentioned above:

- Reg 2, bit [8:1]: EmptyRecordConfig
- Reg 2, bit 9: clk2OutConfig
- Reg 2, bit 10: no8b10b (1 = raw data, 0 = 8b10b encoded data)
- Reg 2, bit 11: Conf_AddrEnable (1 = address read back, 0 = no address read back)

**Instruction of use**

- Download the firmware **FEI4emu_V10** on the module emulator FPGA board
- Connect emulator FPGA board and add-on board

- Power this unit with 5V using the dedicated connector on the add-on board
- Connect the unit via type 0 cable to the USBPix test setup
- Send 40MHz clock to the unit and a write or read slow command using the USBPix firmware usbpixi4.bit