FE-I4 code for emulator, release V0.0

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Note

Keep in mind that every release of the FEI4 code for the emulator implements some functionality of FE-I4, and thus behaves as FE-I4. For a better and deeper understanding of what it does, I recommend to get familiar with FE-I4 before/instead of looking at the emulator code. Plenty of literature on FE-I4 can be found on the indico.

Functionalities

This first release of the FE-I4 code for the emulator board implements only one functionality: it receives the 40MHz clock and sends out **8b10b encoded** data in **FE-I4 format**. Only data records are sent (no service messages, no configuration read back).
For a description of the FE-I4 data output protocol for IBL please refer to the specific document.

Target applications

- USBPix firmware/software development

Implementation

The main components of the code are

- A **ROM** 24 bits wide and 4 bits deep storing a very simple **data file** (see below)
- An early version of the **FE-I4 data output block (DOB)** code from Tomasz Hemperek.
  Some modifications have been made for better synthesis in the FPGA, but the behavior remains the same. For a description of the functionality of the Data Output Block of FE-I4 please refer to the specific literature.

The code also contains some Digital Clock Manager (DCM) for clock multiplication, division, buffering.

The way the code works is the following (simplified explanation):
When the "emptyfifo" signal is 0, the DOB fetches data from the memory. This block then adds Start-Of-Frame (SOF) and End-Of-Frame (EOF), does the 8b10b encoding, and sends the data out via a serializer. When the "emptyfifo" signal is 1, no data is fetched from the memory and only IDLE states are sent out.

Data Output

The data coming out has the following format
N x IDLE, SOF, Data, EOF, N x IDLE, SOF, Data, EOF, N x IDLE, SOF, Data, EOF, etc…
where "Data" can be:

- E90000
- 123456
- 789ABD (this is not a mistake: BC is the decoded EOF so I decided to not use it as data)
- CEF123

Instruction of use

- Download the firmware **FEI4emu_V00** on the module emulator FPGA board
- Connect emulator FPGA board and add-on board
- Power this unit with 5V using the dedicated connector on the add-on board
- Connect the unit via type 0 cable to the USBPix test setup
- Send 40MHz clock to the unit

Note: You need to have the USBPix release for FEI4. **THE USBPix FOR FEI3 WILL NOT WORK!!!**