Demorgans Law

$$\neg[p \wedge q] \equiv \neg p \vee \neg q,$$
$$\neg[p \vee q] \equiv \neg p \wedge \neg q.$$

Rise/Fall time

$$t_r = R_p C, t_f = R_n C$$
$$R_n \propto \frac{L_n}{W_n \mu_{0_n}}, R_p \propto \frac{L_p}{W_p \mu_{0_p}}$$

Elmore's delay

$$\tau_{Di} = \sum_{k=1}^{N} R_k \sum_{j=k}^{N} C_j$$
$$EstimatedDelay = \tau_p = 0.69 * \tau_{Di}$$
$$TotalExpectedEnergy = C_L * f * {V_{dd}}^2$$

Power Probability

$$P_{n\_nand}(0) = P_A(1)P_B(1)$$
$$P_{p\_nand}(1) = 1 - P_A(1)P_B(1)$$
$$P_{n\_nor}(0) = 1 - P_A(0)P_B(0)$$
$$P_{p\_nor}(1) = P_A(0)P_B(0)$$

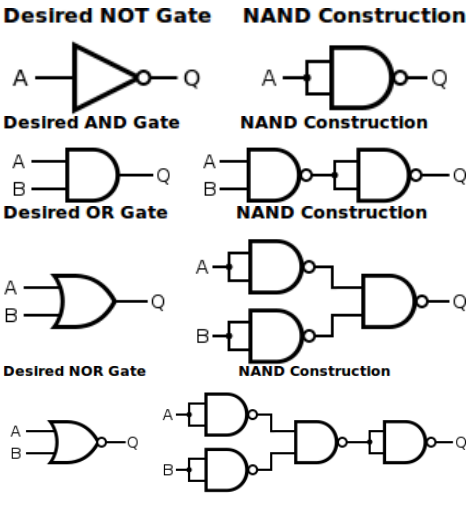
Buffer Chain

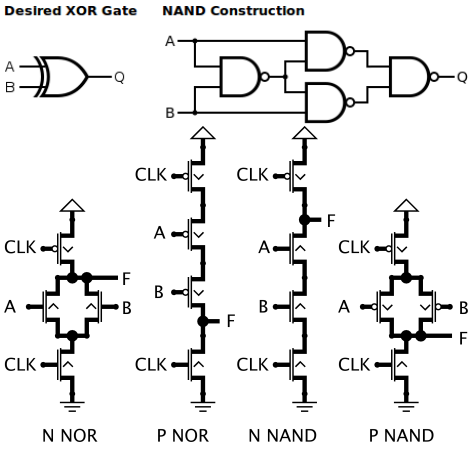
First buffer is of size 1

$$N = Total\ numbers\ of\ buffers$$
$$Size\ of\ buffer\ i = \frac{C_L}{C_1}^{\frac{i}{N}}$$
$$f = \sqrt[N]{\frac{C_L}{C_1}}$$

Min Path Delay

$$t_p = N * t_{po} * (1 + f)$$





Inertial Delay - Time it takes for signal to change value

Transport Delay - Time it takes for signal to travel down wire

Delta Cycle - Is used to order events in VHDL simulation and refers to a zero-physical time. The kernel takes an additional cycle (of delta advancement) to update the evaluated 'future value' into the 'current value' registers, during which the clock doesn't advance.

Channel Length Modulation - Shorting of the length of the inverted channel region with increase in drain bias for large drain biases

Velocity Saturation - Carrier velocity reaches maximum value in presence of electric field.

Latch up - A short circuit in which a low impedance path is created resulting in a parasitic subcircuit that disrupts proper function.

Velocity Saturation - when a strong enough electric field is applied, the carrier velocity in the semiconductor reaches a maximum value. As the applied electric field increases from that point, the carrier velocity no longer increases because the carriers lose energy through increased levels of interaction with the lattice, by emitting phonons and even photons as soon as the carrier energy is large enough to do so.

Hot Carrier - Either holes or electrons that have gained very high kinetic energy after being accelerated by a strong electric field in areas of high field intensities within a semiconductor . Because of high kinetic energy they can get injected and trapped in areas of the device where they shouldn't be.

Scan Chain - Is a technique used for testing digital circuits. The flip flops are all connected together as a shift register into a single (or multiple) scan chains. It increases observability and controllability in the design and also helps to reduce the size of the test-set vector.

Process gain factor -

$$K = \frac{\mu \epsilon_{iO_2}}{t_{ox}}$$

Intrinsic Capacitance - refers to the internal capacitance of a static gate generated dude to diffusion layers, metal contacts, poly-wires. The parasitic capacitance is proportional to the dimensions of the gate (i.e. W and L of transistor). As we increase the size of the gate, the intrinsic capacitance increases, in turn increasing the delay of the gate. We aim to reduce intrinsic capacitances, but it can never be made '0'.

TSPCR - True Single Phase Clock Register performs the flip-flop operation with little power and at high speeds. Stores output using capacitance. Will typically not work at static or low clock speeds: given enough time, leakage paths may discharge the parasitic capacitance enough to cause the flip-flop to enter invalid states.

Master Slave FF - Is edge trigged. Two gated D latches in series and and inverting the enable input to one of them.

Inverter Threshold - When the inverter switches value. NMOS pulls the output low, PMOS pulls output high. To increase the threshold, increase the strength of NMOS and/or reduce strength of PMOS. Strengh of MOSFET is W/L (width/length) ratio. Bigger radio = stronger MOSFET.

Method to overcome leakage - Install keepers at the output of circuit. This uses pos feedback to reduce leakage. Keeper = inverter in series with output with output of inverter connected to input of inverter.

Clock Skew - Spatial variation in temporally equivalent clock edges; deterministic + random, t_sk.

Clock Jitter - Temporal variations in consecutive edges of the clock signal; modulation + random noise. Cycle to Cycle (short-term) t_js.