Demorgans Law

$$\neg[p \wedge q] \equiv \neg p \vee \neg q,$$
$$\neg[p \vee q] \equiv \neg p \wedge \neg q.$$

Rise/Fall time

$$t_r = R_p C, t_f = R_n C$$
$$R_n \propto \frac{L_n}{W_n \mu_{0_n}}, R_p \propto \frac{L_p}{W_p \mu_{0_p}}$$

Elmore's delay

$$\tau_{Di} = \sum_{k=1}^{N} R_k \sum_{j=k}^{N} C_j$$
$$EstimatedDelay = \tau_p = 0.69 * \tau_{Di}$$
$$TotalExpectedEnergy = C_L * f * {V_{dd}}^2$$

Power Probability

$$P_{n\_nand}(0) = P_A(1)P_B(1)$$
$$P_{p\_nand}(1) = 1 - P_A(1)P_B(1)$$
$$P_{n\_nor}(0) = 1 - P_A(0)P_B(0)$$
$$P_{p\_nor}(1) = P_A(0)P_B(0)$$

Buffer Chain

First buffer is of size 1

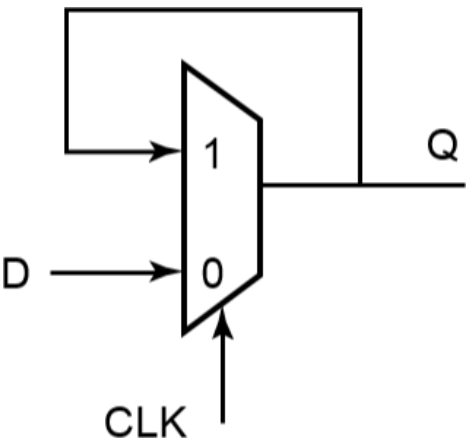
$$N = Total\ numbers\ of\ buffers$$
$$Size\ of\ buffer\ i = \frac{C_L}{C_1}^{\frac{i}{N}}$$
$$f = \sqrt[N]{\frac{C_L}{C_1}}$$

Min Path Delay

$$t_p = N * t_{po} * (1 + f)$$

Mux-Based Latch

$$Q = ClkQ + \ ClkD$$



Inversion Property Inverting all the inputs and ouputs

$$S(A, B, C) = S(\ A,\ B,\ C)$$

Minimize critical path by reducing inverting stages **Binary Adder**

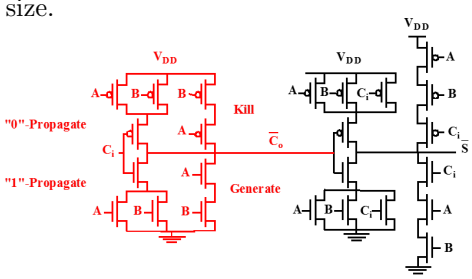
$$S = (A\ B\ C_i) + (\ AB\ C_i) + (\ A\ B\ \ )$$

$$C_o = AB + BC_i + AC_i$$
$$P = A^B$$
$$G = AB$$
$$C_o(G, P) = G + PC_i$$
$$S(G, P) = P_i^C$$

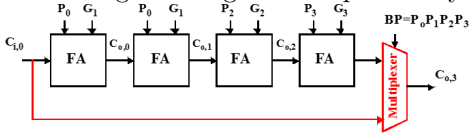
Ripple-Carry Adder Worst case delay linear with number of bits

$$t_d = O(N)t_{adder} = (N-1)t_{carry} + t_{sum}$$

Mirror Adder Maximum of 2 transistions in carry gen circuit
Node Co has a lot of capacitance
Only transistors in carry chain have to be optimized for size.
Transistors in sum stage can be minimal size.



Carry-Bypass Adder In worst case carry generatored at the first bitpositon skips around the bypass stages and is consumed in the last bit position without generating an output carry.



$$t_{adder} = t_{setup} + M_{carry} + (N/M - 1)t_{bypass} + (M-1)t_{carry} + t_{sum}$$

Sqrt Adder

$$t_{adder} = t_{setup} + M * t_{carry} + \sqrt{2N} * t_{max} + t_{sum}$$

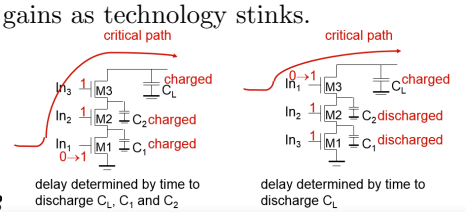
Linear Carry Select

$$t_{adder} = t_{setup} + M * t_{carry} + (N/M) * t_{mux} + t_{sum}$$

Log Look Ahead Adder

$$t_p\ log_2(N)$$

Fast Complex Gate Design Techniques - - Progressive sizing. - Distributed RC line. Can Reduce Delay by more than 20 percent. decreasing gains as technology stinks.

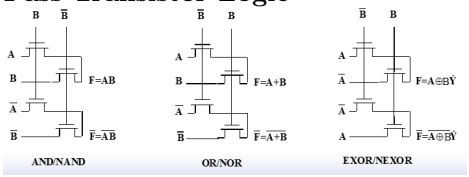


-Alternative logic structures -Isolating fan-in from fan-out using buffer insertion

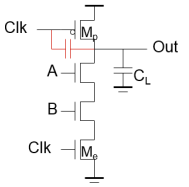
Ratioed Logic - Reduce the number of devices over complementary CMOS

$$V_{OH} = V_{DD}$$
$$V_{OL} = R_{PN}/(P_{PN} + R_L)$$

Pass Transistor Logic

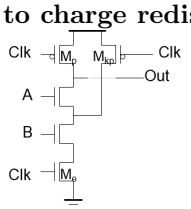


Clock Feed Through

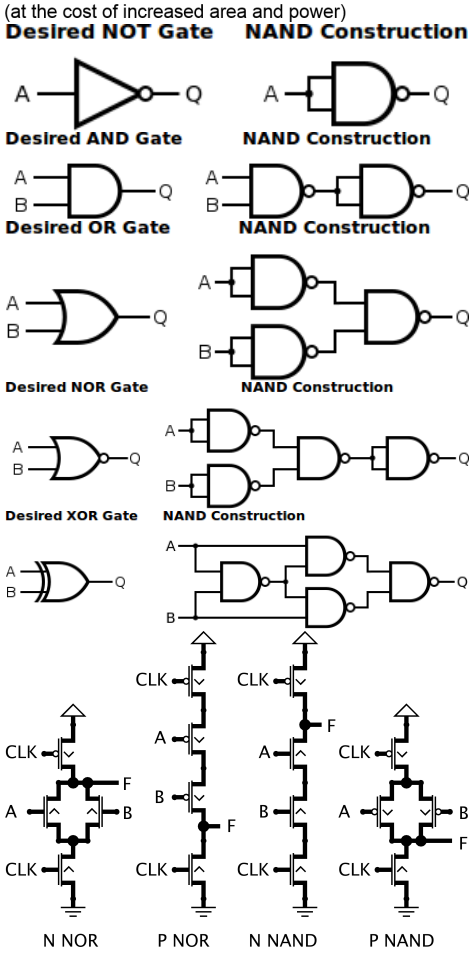


Coupling between Out and Clk input of the precharge device due to the gate to drain capacitance. So voltage of Out can rise above V_{DD}. The fast rising (and falling edges) of the clock couple to Out.

Solution to charge redistribution



Precharge internal nodes using a clock-driven transistor (at the cost of increased area and power)



Inertial Delay - Time it takes for signal to change value

Transport Delay - Time it takes for signal to travel down wire

Delta Cycle - Is used to order events in VHDL simulation and refers to a zero-physical time. The kernel takes an additional cycle (of delta advancement) to update the evaluated 'future value' into the 'current value' registers, during which the clock doesn't advance.

Channel Length Modulation - Shorting of the length of the inverted channel region with increase in drain bias for large drain biases

Velocity Saturation - Carrier velocity reaches maximum value in presence of electric field.

Latch up - A short circuit in which a low impedance path is created resulting in a parasitic subcircuit that disrupts proper function.

Velocity Saturation - when a strong enough electric field is applied, the carrier velocity in the semiconductor reaches a maximum value. As the applied electric field increases from that point, the carrier velocity no longer increases because the carriers lose energy through increased levels of interaction with the lattice, by emitting phonons and even photons as soon as the carrier energy is large enough to do so.

Hot Carrier - Either holes or electrons that have gained very high kinetic energy after being accelerated by a strong electric field in areas of high field intensities within a semiconductor . Because of high kinetic energy they can get injected and trapped in areas of the device where they shouldn't be.

Scan Chain - Is a technique used for testing digital circuits. The flip flops are all connected together as a shift register into a single (or multiple) scan chains. It increases observability and controllability in the design and also helps to reduce the size of the test-set vector.

Process gain factor -

$$K = \frac{\mu \epsilon_{iO_2}}{t_{ox}}$$

Intrinsic Capacitance - refers to the internal capacitance of a static gate generated dude to diffusion layers, metal contacts, poly-wires. The parasitic capacitance is proportional to the dimensions of the gate (i.e. W and L of transistor). As we increase the size of the gate, the intrinsic capacitance increases, in turn increasing the delay of the gate. We aim to reduce intrinsic capacitances, but it can never be made '0'.

TSPCR - True Single Phase Clock Register performs the flip-flop operation with little power and at high speeds. Stores output using capacitance. Will typically not work at static or low clock speeds: given enough time, leakage paths may discharge the parasitic capacitance enough to cause the flip-flop to enter invalid states.

Master Slave FF - Is edge trigged. Two gated D latches in series and and inverting the enable input to one of them.

Inverter Threshold - When the inverter switches value. NMOS pulls the output low, PMOS pulls output high. To increase the threshold, increase the strength of NMOS and/or reduce strength of PMOS. Strengh of MOSFET is W/L (width/length) ratio. Bigger radio = stronger MOSFET.

Method to overcome leakage - Install keepers at the output of circuit. This uses pos feedback to reduce leakage. Keeper = inverter in series with output with output of inverter connected to input of inverter.

Clock Skew - Spatial variation in temporally equivalent clock edges; deterministic + random, t_sk.

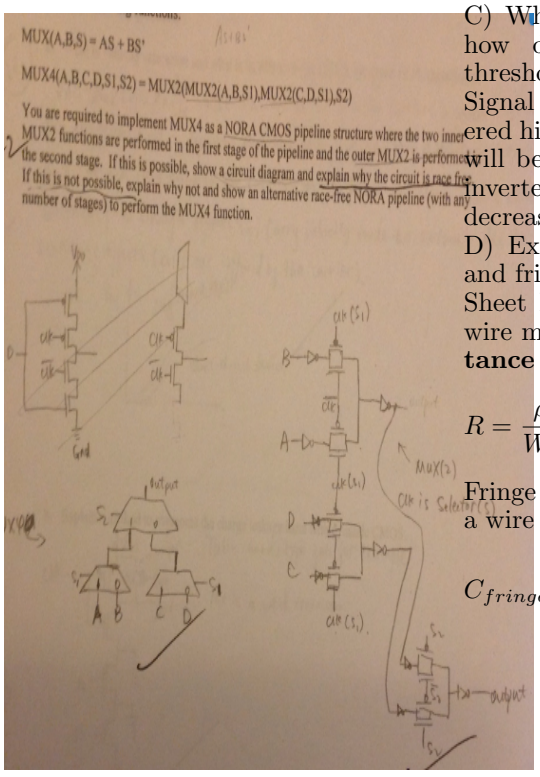
Clock Jitter - Temporal variations in consecutive edges of the clock signal; modulation + random noise. Cycle to Cycle (short-term) t_js.

Dealing with Capacitive Cross Talk - Avoid floating node. Protect sensitive nodes. Make rise fall times large. Do not run wires together for long dist. Use shielding for wires and layers.

C2MOS Pipeline - Racefree as long as even number of inverters.

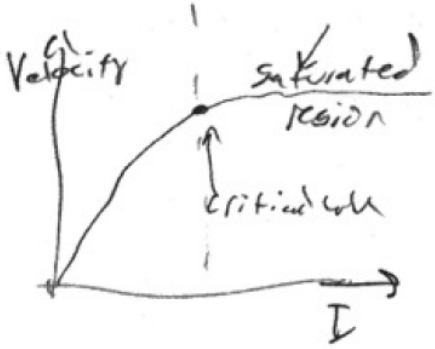
TSPCL - True Single Phase Clock Logic, simplification of NORA so single clock phase is sufficient.

4)



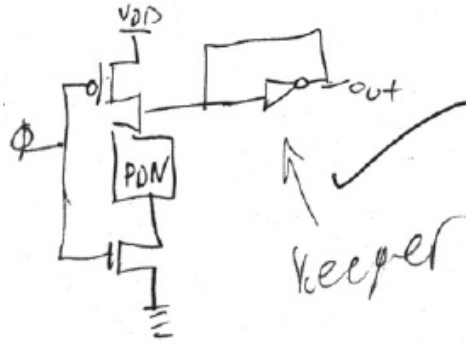
5) A) What is velocity saturation and what is the effect on the CMOS transistor IV characteristics?

"Carrier velocity is proportional to the electric field" does not hold at high electric fields above a critical value and the velocity saturates and remains constant due to scattering effects.



B) Explain a method to overcome the charge leakage issue with dynamic CMOS.

One method is to add keepers at the output of the circuit. This uses positive feedback to reduce leakage.



C) What is the inverter threshold and how does sizing effect the inverter threshold?

Signal bigger than V_IH will be considered high while signal is lower than V_IL will be considered low. V_IH/V_IL are inverter thresholds. Increasing size will decrease V_IH, increase V_IL.

D) Explain the terms sheet resistance and fringe capacitance.

Sheet Resistance is the resistance of a wire modeled as a sheet. **Sheet Resistance**

$$R = \frac{\rho * L}{W * H}$$

Fringe capacitance is the capacitance of a wire due to the fringing electric fields.

$$C_{fringe} = \frac{2\pi * \epsilon_{di}}{log\frac{\epsilon_{di}}{4}}$$