INTRANEX

INTRANEX is a **programmable interconnect network** that accepts a N bit input W and produces a N bit output Z. The interconnect can be programmed to realize any mapping from W to Z.

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Max Thrun
973 919 6593
max.thrun@gmail.com
(Coordinator)

Xiaohu Qi
513 652 2075
qixiaohuihaha@gmail.com

Task Allocation

Task	Person	Milestone	Date
Pinout Diagram	Thrun		10-15-2013
Functional description	Thrun		10-15-2013
Explanation of test mode	Qi		10-15-2013
Description of design decisions	Thrun		10-16-2013
Top-level block diagram	Qi		10-16-2013
Hierarchical logic level design	Thrun	Initial Design Done	10-16-2013
Behavioral model of each gate	Qi		10-17-2013
Behavioral model of slice	Qi		10-17-2013
Behavioral model of entire chip	Qi	VHDL Models Done	10-18-2013
Testbench for each	Thrun		10-19-2013
Simulation results	Thrun	VHDL Slice/Chip Tested	10-19-2013
Slice interconnect description	Qi	1st Progress Report	10-21-2013
Slice circuit diagram	Thrun		10-22-2013
Slice layout	Thrun	Slice Implemented	10-22-2013
Slice IRSIM CMD file	Thrun		10-23-2013
Slice IRSIM result	Qi		10-23-2013
Slice Spice simulation file	Qi		10-24-2013
Slice Spice result	Qi		10-24-2013
Slice Layout Timings	Qi	Slice Layout Tested	10-24-2013
Add gate leaf timings to models	Thrun		10-25-2013
Simulate full chip with new models	Thrun	VHDL Chip With Timings Tested	10-25-2013
Predict overall timing, clock speed, and throughput	Thrun		10-26-2013
Compare simulation results to 1st progress report	Thrun		10-27-2013
Floor plan showing placement of major modules including interslice routing and control and test logic	Qi		10-28-2013
Updated 1st progress report	Thrun		10-29-2013
Description of major design decisions and design revisions	Qi	2nd Progress Report	10-30-2013
Chip level layout in form of color plot	Thrun	Chip Implemented	11-1-2013
Chip Spice simulation file	Qi		11-2-2013
Chip Spice result	Qi		11-3-2013
Chip IRSIM CMD file	Qi		11-3-2013
Chip IRSIM results	Qi		11-3-2013
Chip Layout Timings for normal and test mode	Qi	Chip Layout Tested	11-4-2013
Detailed users guide	Thrun		11-5-2013
Test strategy for test engineer	Qi		11-5-2013
Description of chip architecture, design decisions and the rationale for them. Address revisions.	Thrun		11-6-2013
Updated 1st and 2nd progress reports	Qi		11-7-2013
Final VHDL simulation results and explanation	Thrun	Final Report	11-8-2013

Table 1: Task Breakdown and Allocation

Task Dependencies

The diagram below illustrates the dependencies between the major tasks of our project. Nodes colored in blue are assigned to Thrun and nodes colored red are assigned to Qi. Note that this diagram does not cover every task so work load distribution should not be based soley off this diagram.

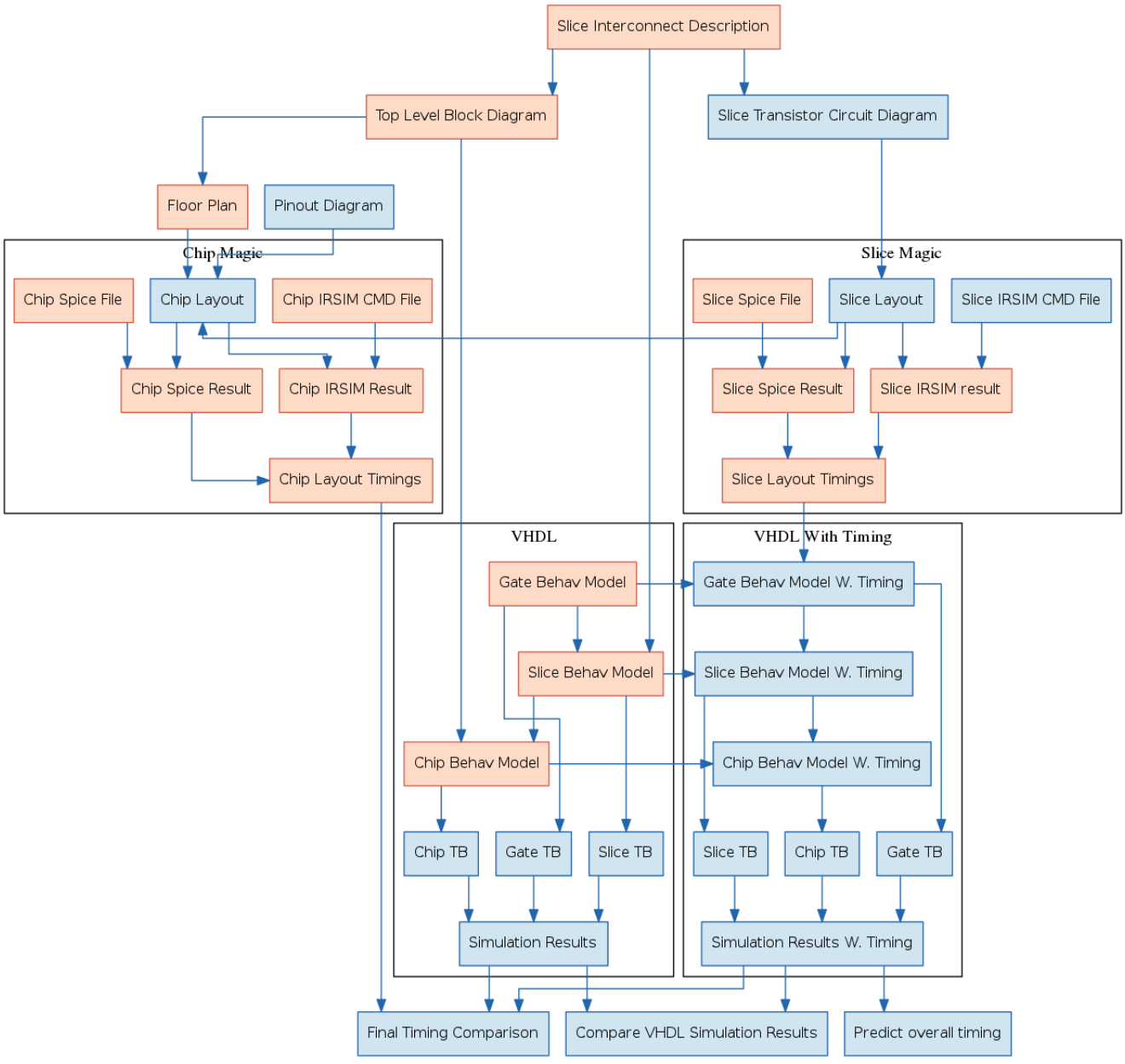

Figure 1: Task Dependencies