Introduction to VLSI Design (EECE 6080)

Fall 2013; Ranga Vemuri

Miniprojects

Propose Own Project (Optional): October 6, 2013
(will receive accept/reject feedback by Oct 10, 2013)

Task Allocation Statement: October 14, 2013
First Progress Report: October 21, 2013
Second Progress Report: October 30, 2012
Final Report: November 8, 2013
Demo and Tape-Out: November 11-13, 2013
(Demo and tape-out sign-up for half-hour time slots. Signup sheet to be posted later.)

The mini-project is to design a VLSI circuit to go on a tinychip. There are several mini-project problems one of which will be assigned to your group.

- The problem descriptions are kept short and simple. You should approach me and/or the TA if you desire additional clarifications as you start un-derstanding and solving the problem.
- The following are inviolable design constraints:
  - Technology: You should use the AMI C5 0.5 n-well CMOS process. Use MOSIS SCMOS SUBM (sub-micron) design rules with lambda set to 0.3 (feature size 0.6 microns). Corresponding Spice/IRSIM model files will be made available to you via the Blackboard system.
  - Area and I/O: Design should fit in the MOSIS TinyChip. This is about 1.5 mm x 1.5 mm area (5000 x 5000 lambda) including a stuffed pad frame. The pad frame will be available via the Blackboard system. The frame has 38 bidirectional pads, one Vdd pad and one ground pad.
  - Design Time: Project must be completed by the due date.
- The Tinychip pad-frames are available for download from the Blackboard system. You will notice that the area and the number of pins are two inviolable constraints. You should simulate your design

before you connect it to the pad-frame. After setting it in the pad-frame you should simulate it again, this time including the pads. Don't forget to connect all the Vdd (GND) wires physically together and to the Vdd (GND) pins; using the same labels is of course not good enough.

- Be reasonable in expecting any control signals coming from outside into the chip. In the normal mode of operation, the only input signals to your circuit are the data bits, power, clock (single phase), and VERY limited number of other unavoidable control signals such as a global reset, data ready etc. All other internal control signals should be generated on chip.

  The exception to this is the test mode where you can use all the I/O pins if you like and supply the control signals for internal logic from the outside.

- You may find the number of primary I/O signals needed by your circuit is much less than the 38 usable pins available. Use the remaining pins to improve the testability of the chip. To improve testability, you should ba-sically provide means to directly observe and control the various registers in the system. For example, you can bring out all the register bits so that the state of the system can be observed at any time. You may provide at the input pins control signals to individual registers so that their state can be controlled in the test mode. How you would test the chip and detect the existence and location of faults should be considered carefully at the time of design. You will find the availability of a lot of pins handy in increasing the testability (especially, observability of internal signals) of the chip. Additional test considerations will be discussed in the class and must be followed.

- Read your email regularly. We may be posting additional instructions and information as we go.

- As usual, start early... Think the design and layout through carefully so you don't run into unanticipated problems.

Each project requires you to design a (mostly) bit-sliced VLSI chip. These problems for the mini-project are so selected that in each case you will design a few basic blocks and repeat them many times to get the overall design. (In addition, you may have to generate and route the control signals to each cell.) The more basic blocks you can put into the chip, the larger is the size of the problem solved by the chip. One of your primary design goals is to design the basic blocks such that you can squeeze in as many blocks as possible in the available area (ie. make N as large as possible.) Among the groups doing the same project, the one that successfully designs the chip with the largest N wins. Parameter N is explicitly identified in each project description.

1. Following are the optimization goals:
    - Maximize N .
    - Maximize the throughput rate.
    - Clock speed must be at least 50 MHz. You should aim for a clock-speed above 100 MHz.
2. If possible, design your chips such that it is possible to build a VLSI system, which caters to a much larger problem size than a single chip can, by interconnecting several of your chips. That is, your bit-slicing scheme should be extensible beyond the chip boundary if possible.

3. You are strongly advised to use standard-cells unless you have a good reason not to. A set of standard-cells are available to you through the Blackboard system.

4. You will notice that the control logic required in your chip is minimal, if any. If you can migrate all the control logic into the basic blocks, your life at the time of layout will be easier.