Introduction to VLSI Design (EECE 6080C)
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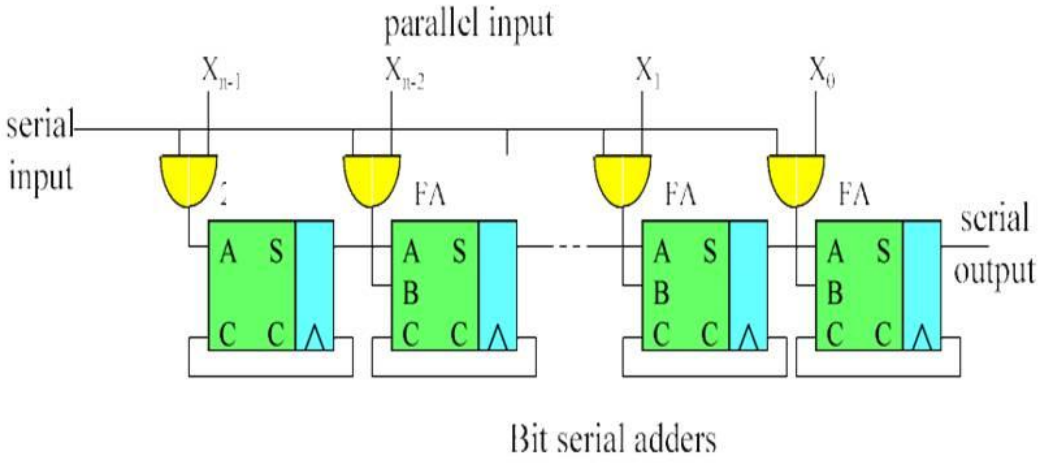
List of Mini Projects

1. Serial by Parallel Multiplier

The serial by parallel Booth multiplier multiplies two N-bit binary numbers A and B and produces a binary number C. It is well suited for computations in which one of the numbers, A, changes relatively infrequently and the other number, B, changes more frequently. The number A will be input serially into a shift register and held in position to provide the parallel input to the multiplier. Then, the number B be input serially over successive clock cycles as the output C is produced over successive clock cycles.

The carry flops associated with the serials adders share the clock and the reset signals. These flops will form a shift register in the test mode.

The following figure is adopted from
http://www.andraka.com/multipli.htm#Serial%20by%20Parallel%20Booth%20Multipliers

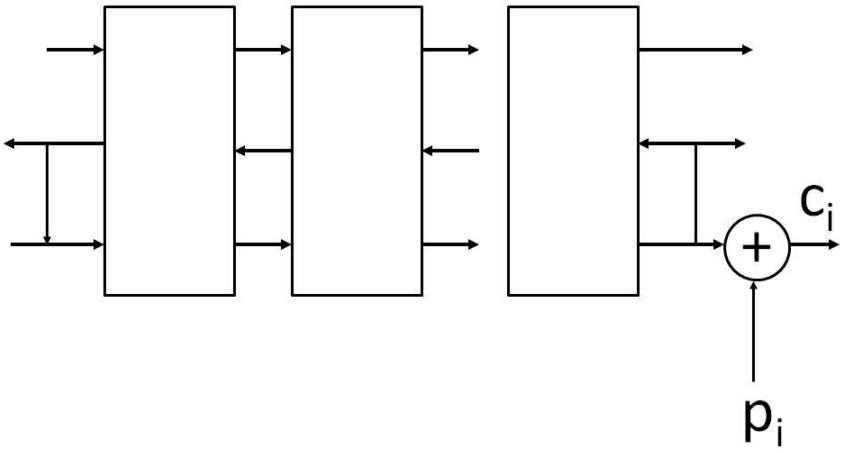


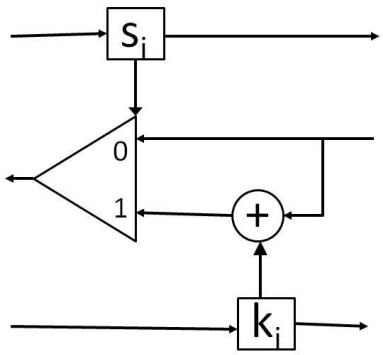
Bit serial adders

2. Simple Stream Cipher

The simple stream cipher encrypts a serial plain text p and generates the serial cipher text c. It uses a programmable linear feedback shift register to generate a pseudo-random key stream which is ex-ored with p as illustrated. The key stream is produced using a N-bit key K and a N-bit LFSR which is programmed using a N-bit feedback select word S. Both S and K are input serially and held in shift registers.

Note that the same cipher can also be used to decrypt the cipher text to recover the original plain text.

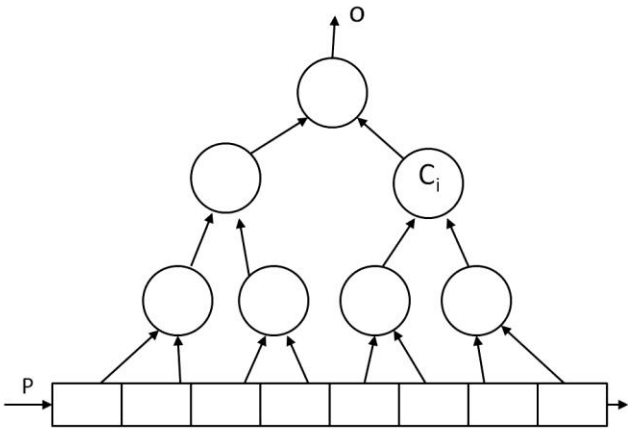


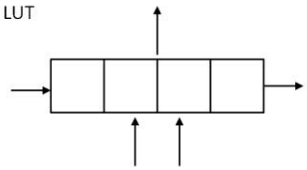


3. Programmable Binary Tree Computation

Each node in the binary tree is a programmable combinational function of two inputs. Each node contains a 4-bit lookup table (LUT) which represents the truth table of the combinational function realized by that node. The lookup tables of all of the nodes together constitute the "program" which denotes the logic function implemented by the binary tree. Once programmed the binary tree accepts the input P and produces a single bit output O. P is a N-bit input where N is twice the number of leaf nodes in the binary tree. P is a serial input, shifted into position using a shift register.

The "program" itself should be shifted into position. All the 4-bit lookup tables should form a long shift register in the program mode. After programming, each LUT will be used as a 1-bit, 4-word ROM during the compute mode. The two input bits to the node are used as the address bits to determine which word of the ROM should be the output.

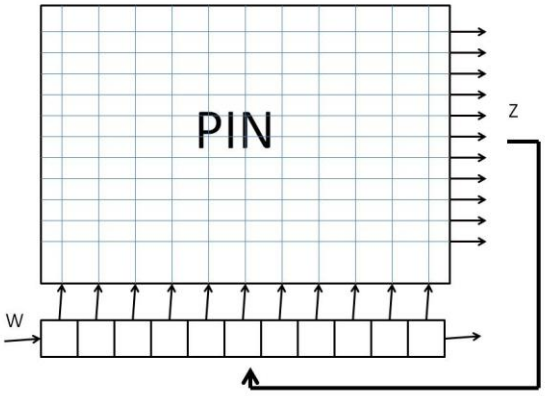


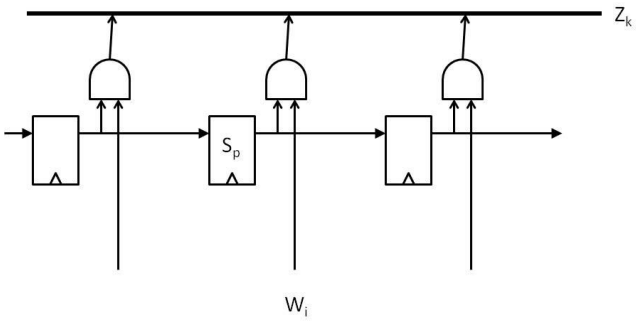


4. Programmable Interconnect Network

The programmable interconnect network accepts a N bit input W and produces a N bit output Z. Every output bit Z_i is mapped from some input bit W_j where the mapping is determined by the interconnect network. The interconnect network can be programmed to realize any mapping from W to Z. W is input serially and shifted into position using a shift register. Z is stored back into the same shift register and shifted out to obtain the output serially.

Each output bit Z_i is obtained from a bus which can be driven by any one of the input bits selected based on a "program" bit. There are N identical and independent buses in the network. Each bus has N program bits corresponding to the N input bits. Care must be taken to ensure that only one of the input bits is selected to drive the bus. Altogether there will be N*N program bits in the network. These program bits together form a configuration shift register. A configuration must be shifted into position during the programming phase of the network.





5. Propose your own project within the TinyChip pad frame constraints. Your project should be a scalable design with the goal of maximizing some defined N. You must identify the speed and/or throughput goals for the project. If you choose this option, please submit the idea at the same level of detail as the projects in this handout by the specified due date. You will receive feedback about it's acceptability. If found unacceptable, you will have to work on the project assigned to you.