Arquiteturas de Alto Desempenho

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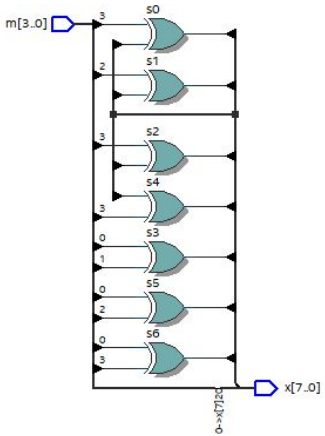
Encoder Paralelo

Utilizando sinais foi possível reduzir o número de operações xor para 7.

```
ARCHITECTURE structure OF Parallel4BitEncoder IS
SIGNAL s0, s1, s2, s3, s4, s5, s6, s7: STD_LOGIC;
BEGIN
    s7 <= m(0);
    s6 <= m(0) xor m(3);
    s5 <= m(0) xor m(2);
    s4 <= s5 xor m(3);
    s3 <= m(0) xor m(1);
    s2 <= s3 xor m(3);
    s1 <= s3 xor m(2);
    s0 <= s1 xor m(3);
    x <= s7 & s6 & s5 & s4 & s3 & s2 & s1 & s0;
END structure;
```



$$\|0\,0\,0\,0\| \times G = \|0\,0\,0\,0\,0\,0\,0\,0\|$$
$$\|0\,0\,0\,1\| \times G = \|1\,1\,1\,1\,1\,1\,1\,1\|$$
$$\|0\,0\,1\,0\| \times G = \|0\,0\,0\,0\,1\,1\,1\,1\|$$
$$\|0\,0\,1\,1\| \times G = \|1\,1\,1\,1\,0\,0\,0\,0\|$$
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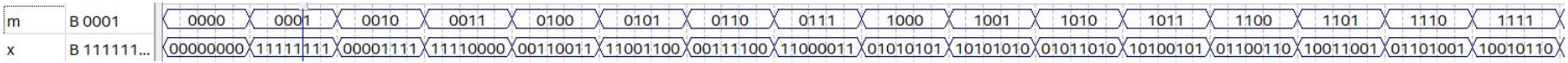


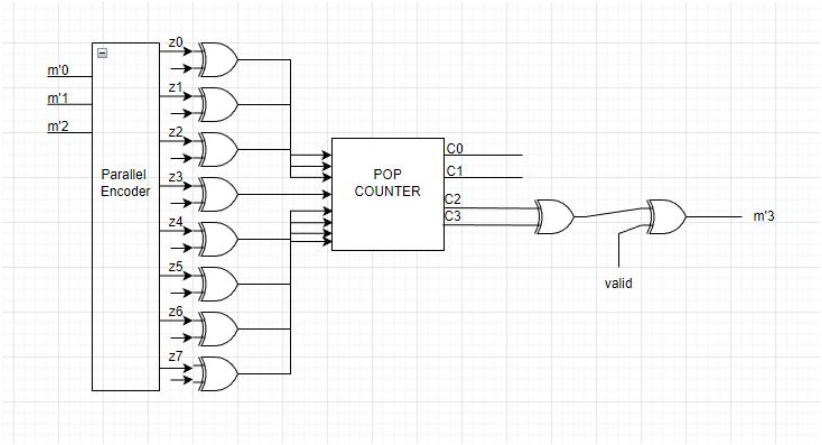
Decoder Paralelo

$mOne = C_3\ C_2\ (C_1 + C_0) + C_1 C_0\ (C_2 + C_3)$

$mZero = \sim C_3\ \sim C_2\ (\sim C_1 + \sim C_0) + \sim C_1\ \sim C_0\ (\sim C_2 + \sim C_3)$«

$MError = \sim (m_{one} + m_{zero})$

$valid = \sim m_{0Error} + \sim m_{1Error} + \sim m_{2Error}$



Custo: 22 Gates Xor
18 Gates And
14 Gates Or
3 Gates NOr