

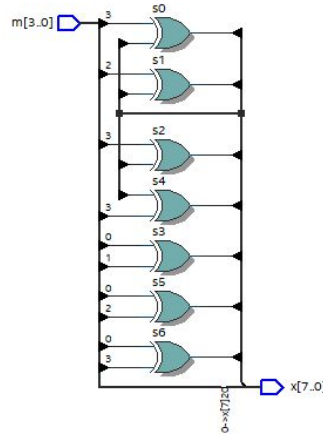
Arquiteturas de Alto Desempenho

Gil Teixeira, 88194
Pedro Rodrigues, 92338

Encoder Paralelo

Utilizando sinais foi possível reduzir o número de operações xor para 7.

```
ARCHITECTURE structure OF Parallel4BitEncoder IS
SIGNAL s0, s1, s2, s3, s4, s5, s6, s7: STD_LOGIC;
BEGIN
    s7 <= m(0);
    s6 <= m(0) xor m(3);
    s5 <= m(0) xor m(2);
    s4 <= s5 xor m(3);
    s3 <= m(0) xor m(1);
    s2 <= s3 xor m(3);
    s1 <= s3 xor m(2);
    s0 <= s1 xor m(3);
    x <= s7 & s6 & s5 & s4 & s3 & s2 & s1 & s0;
END structure;
```



$$\begin{aligned} \begin{bmatrix} 0 & 0 & 0 & 0 \end{bmatrix} \times G &= \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \\ \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \times G &= \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix} \\ \begin{bmatrix} 0 & 0 & 1 & 0 \end{bmatrix} \times G &= \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 \end{bmatrix} \\ \begin{bmatrix} 0 & 0 & 1 & 1 \end{bmatrix} \times G &= \begin{bmatrix} 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \end{bmatrix} \\ \begin{bmatrix} 0 & 1 & 0 & 0 \end{bmatrix} \times G &= \begin{bmatrix} 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \end{bmatrix} \end{aligned}$$

m	B 0001	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
x	B 111111...	00000000	11111111	00001111	11110000	00110011	11001100	00111100	11000011	01010101	10101010	01011010	10100101	01100110	10011001	01101001	10010110

Decoder Paralelo

$$\text{mOne} = C_3 C_2 (C_1 + C_0) + C_1 C_0 (C_2 + C_3)$$

$$\text{mZero} = \sim C_3 \sim C_2 (\sim C_1 + \sim C_0) + \sim C_1 \sim C_0 (\sim C_2 + \sim C_3) \ll$$

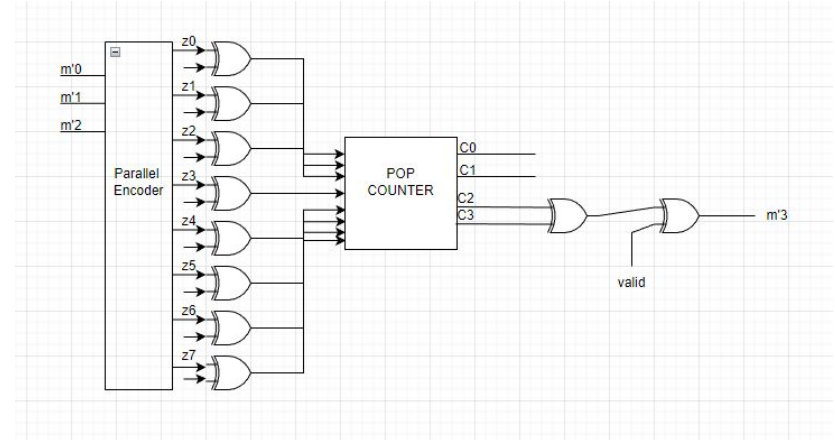
$$\text{MError} = \sim (m_{\text{one}} + m_{\text{zero}})$$

$$\text{valid} = \sim m_{0\text{Error}} + \sim m_{1\text{Error}} + \sim m_{2\text{Error}}$$

Custo: 22 Gates Xor

18 Gates And

14 Gates Or

3 Gates NO_r

x	B 000000...	00000000	01010101	00110011	01100110	00001111	01011010	00111100	00111101	00111111
m	B 0000	0000	1000	0100	1100	0010	1010	0110	0001	
v	B 1									