"Assignment - 2"

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Section: 3C

Course: Digital Logic Design (DLD)

"Question: 1"

$(1281)_{10} \rightarrow$ BCD

$\Rightarrow$ Conversion to 4-bit binary representation

1	2	8	1
8421	8421	8421	8421
0001	0010	1000	0001

BCD = (0001 0010 1000 0001)

"Question : 2"

=> Converting BCD to Decimal using 4-bits

1001	0001	0111	0011
8421	8421	8421	8421
9	1	7	3

Decimal = $(9173)_{10}$

"Question : 3"

a) 1001 + 0011

$$\begin{array}{r} 1001 \\ +\ 0011 \\ \hline 1100 \end{array} \qquad \begin{array}{r} 9 \\ +\ 3 \\ \hline 12 \end{array}$$

Adding 0110 to the invalid BCD number

$$\begin{array}{r} 1100 \\ +\ 0110 \\ \hline 0010 \end{array}$$

1 is carry, so

```
  1001
+ 0011
------
  1100
+ 0110
------
0001 0010
```

1001 + 0011 = 0001 0010
9 + 3 = 1 2

b) 00011001 + 00010011

```
 0001 1001     19
+0001 0011    +13
---------    ----
 0010 1100    32
+ 0110
-------
 0011 0010
```

00011001 + 00010011 = 0011 0010
19 + 13 = 3 2

"Question 14"

$(115)_8 \rightarrow (?)_2$

1	1	5
421	421	421
001	001	101

$(115)_8 = (001\ 001\ 101)_2$

"Question 5"

$(11010)_2 \rightarrow$ Gray Code

1	+	1	+	0	+	1	+	0	Binary
↓		↓		↓		↓		↓	
1		0		1		1		1	Gray

Gray Code = 10111

"Question 6"

Gray Code (01010) to $(?)_2$

0		1		0		1		0	Gray
↓	+/	↓	+/	↓	+/	↓	+/	↓	
0		1		1		0		0	

Binary = 01100

"Question 7"

a) Sign-magnitude form

⇒ +27 = 128 64 32 16 8 4 2 1
0 0 0 1 1 0 1 1

(00011011)

⇒ +127 = 128 64 32 16 8 4 2 1
0 1 1 1 1 1 1 1

Now, we change the sign bit

-127 = 11111111

b) 1's Complement

⇒ +27 = 00011011

1's compliment = 11100100

⇒ +127 = 01111111

1's compliment = 10000000
2's compliment = +1
-127 = 10000001

-127 = 10000001

1's Compliment = 01111110

⇒ -127 - 11111111

1's Compliment = 0000 0000

c) 2's Compliment

⇒ +27 = 00011011

1's Compliment = 11100100
2's Compliment = +1
11100101

⇒ +127 = 0111 1111

1's Compliment = 0000 0000
2's Compliment = +1
01111111

$\Rightarrow$ $-127 = 1000\ 0001$

1's Complement = 0111 1110

2's Complement = $\dfrac{+1}{0111\ 1111}$

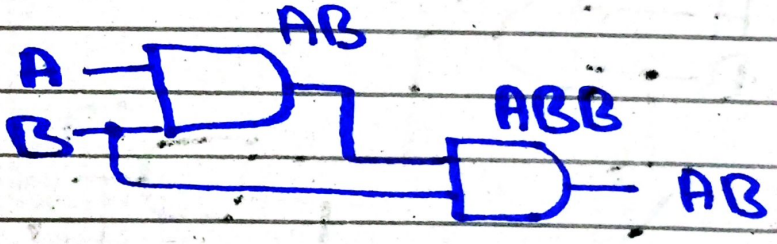
"QUESTION # 8"

a) $X = A' + A'B + AC$

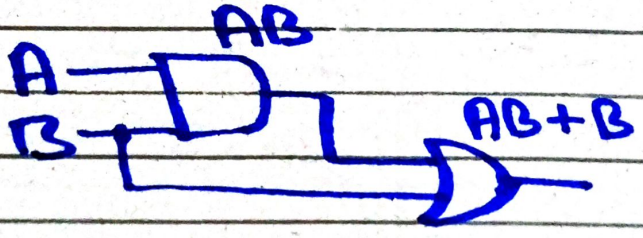
b) $X = \overline{A'B + A'CD + BDD'}$

$X = \overline{A'B + A'CD}$

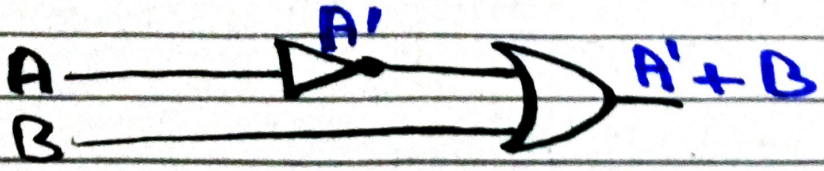
2. a)



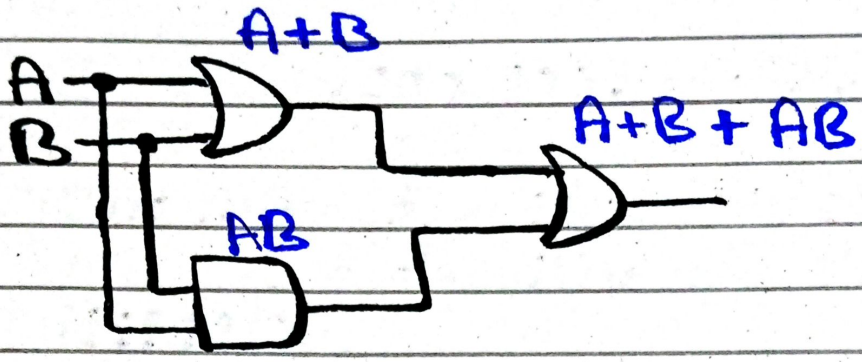
b)



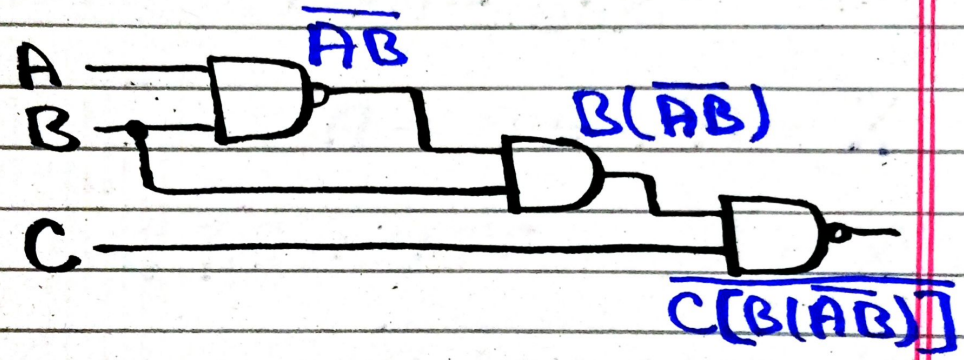
c)



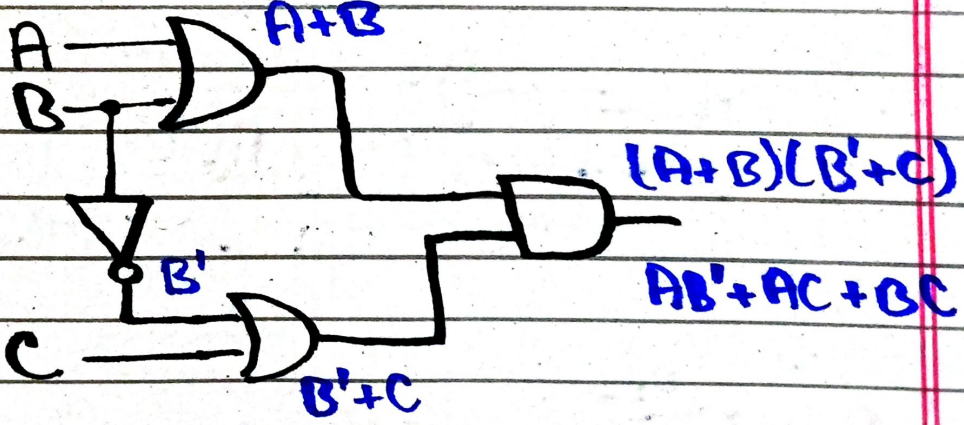
d)


A+B
A
B
A+B+AB
AB

e)


$\overline{AB}$
A
B
B($\overline{AB}$)
C
C[B($\overline{AB}$)]

f)


A+B
A
B
(A+B)(B'+C)
B'
AB'+AC+BC
C
B'+C

"Question 9"

Given:

=> Ignition switch => High = ON, Low = OFF

=> Light Switch => High = ON, Low = OFF

=> Headlights => High = ON, Low = OFF

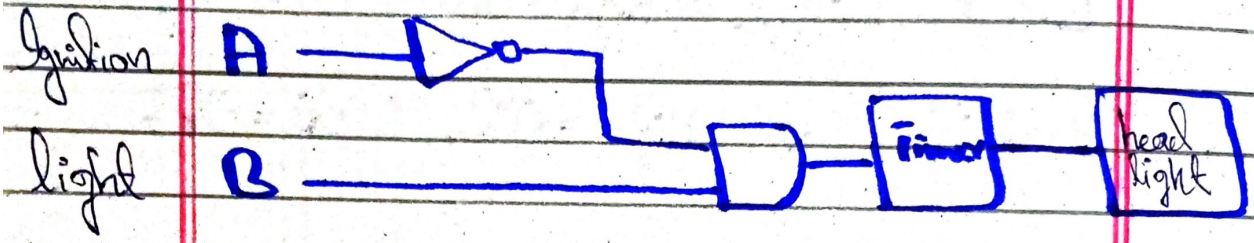
Truth table

Ignition	Light	Headlight
0	0	0
0	1	0
1	0	0
1	1	1

=> Now we know that its an AND gate.

In order to turn off the headlights after 15 seconds, circuit is to be implemented in which ignition switch is off and

light switch is ON. for this, we need a timer which would produce a low after 15 seconds.



We are using an AND gate to operate when one of its input is Low and one input is High. We will use an inverter at one of the inputs where the logic level is Low (ignition switch)

The timer produces a Low output 15 seconds after the AND gate output goes High.