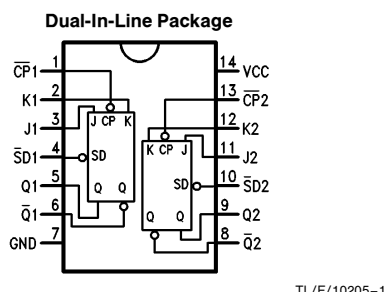


54LS113 Dual JK Edge-Triggered Flip-Flop

General Description

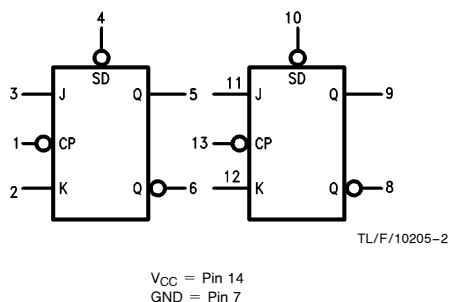
The 54LS113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is HIGH and the bistable will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

Connection Diagram



Order Number 54LS113DMQB,
54LS113FMQB or 54LS113LMQB
See NS Package Number E20A, J14A or W14B

Logic Symbol



Truth Table

Inputs		Output
@ t _n		@ t _n + 1
J	K	Q
L	L	Q _n
L	H	L
H	L	H
H	H	Q _n -bar

t_n = Bit Time before Clock Pulse

t_n + 1 = Bit Time after Clock Pulse

H = HIGH Voltage Level

L = LOW Voltage Level

Asynchronous Input:

Low input to \overline{SD} sets Q to HIGH level

Set is independent of clock

Pin Names	Description
J1, J2, K1, K2	Data Inputs
$\overline{CP}1, \overline{CP}2$	Clock Pulse Inputs (Active Falling Edge)
$\overline{SD}1, \overline{SD}2$	Direct Set Inputs (Active LOW)
Q1, Q2, Q1-bar, Q2-bar	Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” table are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual operation.

Recommended Operating Conditions

Symbol	Parameter	54LS113			Units
		Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	V
V _{IH}	High Level Input Voltage	2			V
V _{IL}	Low Level Input Voltage			0.7	V
I _{OH}	High Level Output Current			−0.4	mA
I _{OL}	Low Level Output Current			4	mA
T _A	Free Air Operating Temperature	−55		125	°C
t _s (H) t _s (L)	Setup Time J _n or K _n to \overline{CP}_n	20 20			ns
t _h (H) t _h (L)	Hold Time J _n or K _n to \overline{CP}_n	0 0			ns
t _w (H) t _w (L)	\overline{CP}_n Pulse Width	20 15			ns
t _w (L)	\overline{SD}_n Pulse Width LOW	15			ns

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = −18 mA			−1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IL} = Max, V _{IH} = Min	2.5			V
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max, V _{IH} = Min, V _{IL} = Max			0.4	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 5.5V	J, K		0.1	mA
			SD		0.3	
			CP		0.4	
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.7V	J, K		20	μA
			SD		60	
			CP		80	
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.5V	J, K	−30	−400	μA
			CP, SD	−60	−800	
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	−20		−100	mA
I _{CC}	Supply Current	V _{CC} = Max (Note 3)			8	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

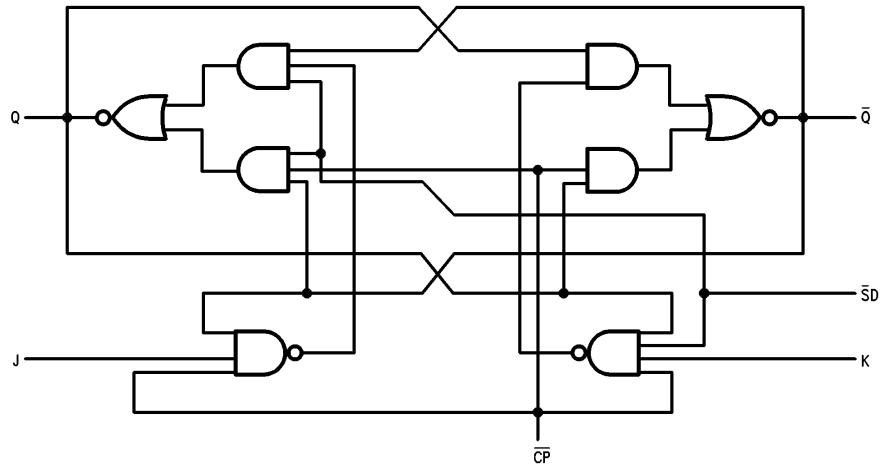
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

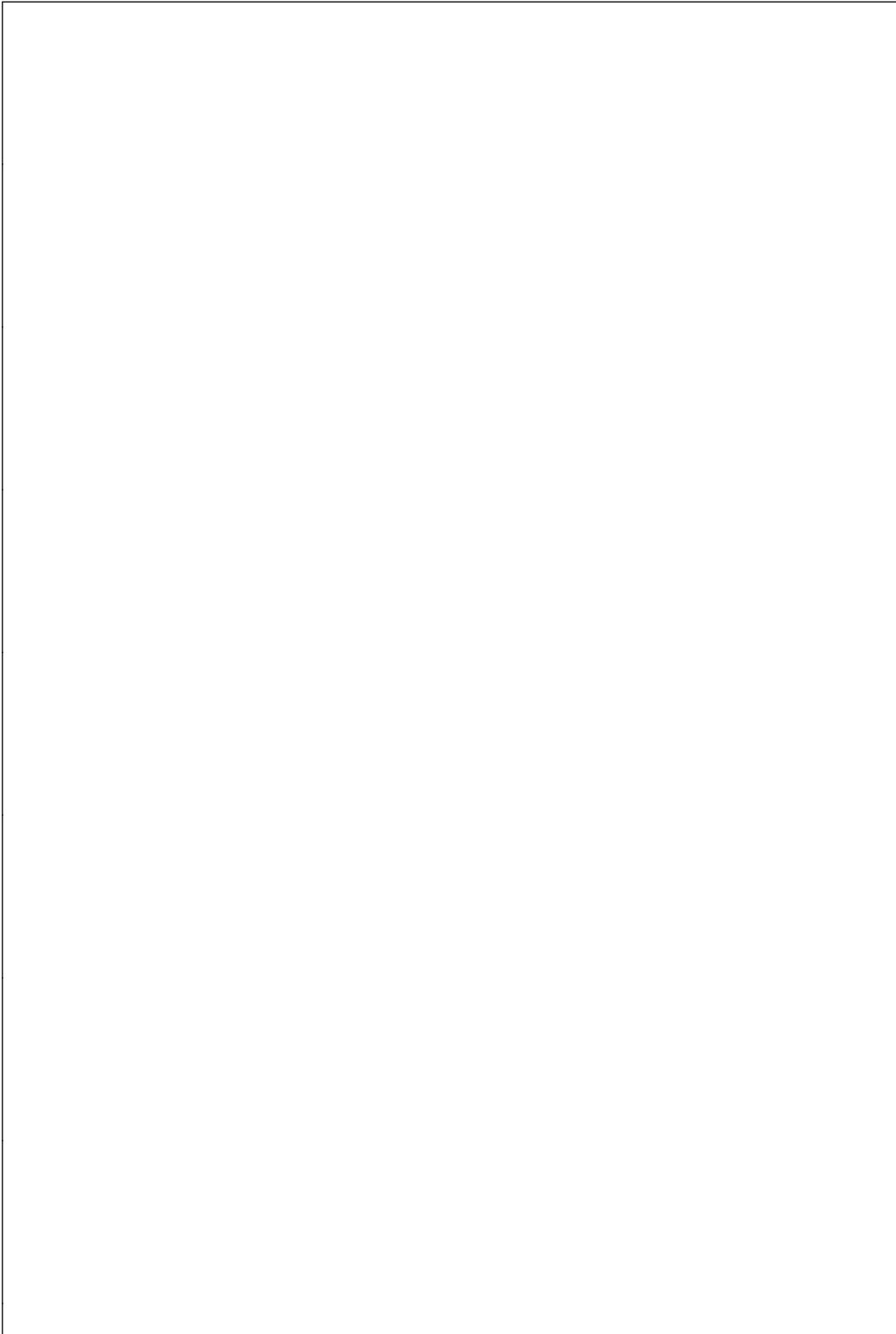
Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25^\circ C$ (See Section 1 for test waveforms and output load)

Symbol	Parameter	54LS113		Units
		C _L = 15 pF		
		Min	Max	
f _{max}	Maximum Clock Frequency	30		MHz
t _{PLH} t _{PHL}	Propagation Delay CP _n to Q _n or Q _n		16 24	ns
t _{PLH} t _{PHL}	Propagation Delay S _{Dn} to Q _n or Q _n		16 24	ns

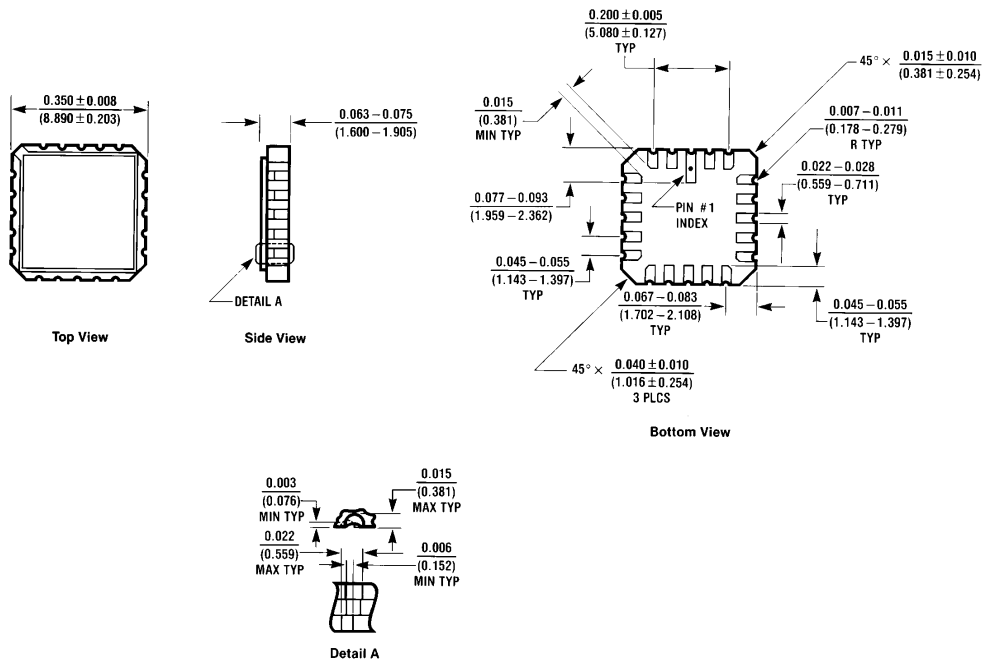
Logic Diagram (one half shown)



TL/F/10205-3

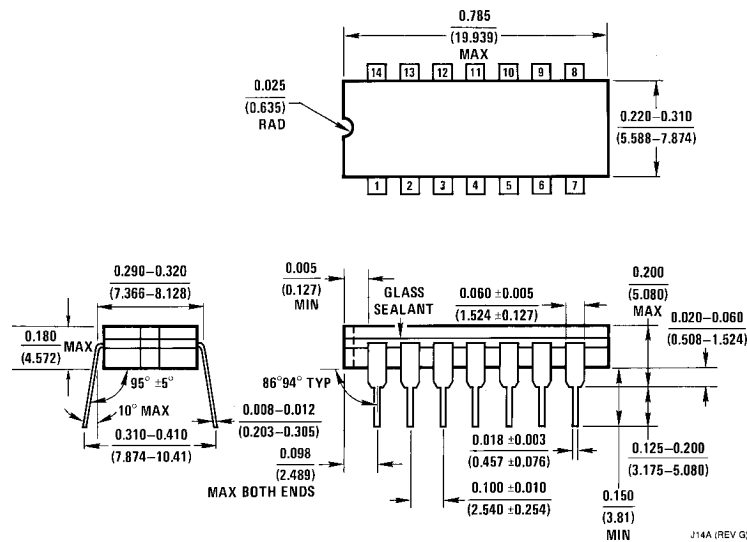


Physical Dimensions inches (millimeters)



Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS113LMQB
NS Package Number E20A

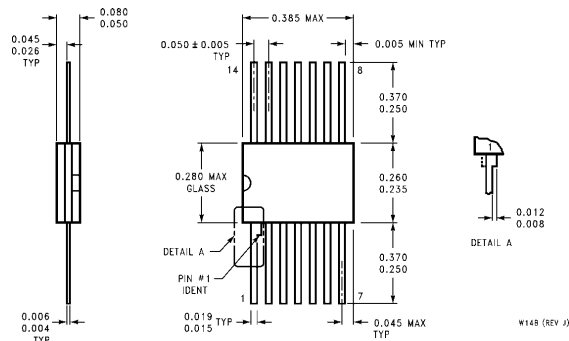
E20A (REV D)



14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS113DMQB
NS Package Number J14A

J14A (REV G)

Physical Dimensions inches (millimeters) (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS113FMQB
NS Package Number W14B

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
19th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.