

54LS173/DM74LS173A TRI-STATE® 4-Bit D-Type Register

General Description

This four-bit register contains D-type flip-flops with totem-pole TRI-STATE® outputs, capable of driving highly capacitive or low-impedance loads. The high-impedance state and increased high-logic-level drive provide these flip-flops with the capability of driving the bus lines in a bus-organized system without need for interface or pull-up components.

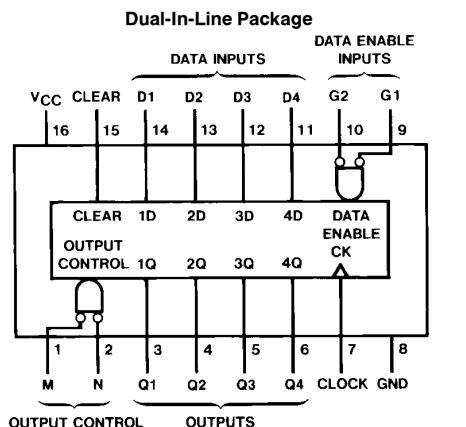
Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the truth table.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Features

- TRI-STATE outputs interface directly with system bus
- Gated output control lines for enabling or disabling the outputs
- Fully independent clock eliminates restrictions for operating in one of two modes:
 - Parallel load
 - Do nothing (hold)
- For application as bus buffer registers

Connection Diagram



Order Number 54LS173DMQB, 54LS173FMQB,
54LS173LMQB, DM74LS173AM or DM74LS173AN
See NS Package Number E20A, J16A,
M16A, N16E or W16A

Function Table

Clear	Clock	Data Enable		Data D	Output Q
		G1	G2		
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

H = High Level (Steady State)

L = Low Level (Steady State)

↑ = Low-to-High Level Transition

X = Don't Care (Any Input Including Transitions)

Q_0 = The Level of Q Before the Indicated Steady State Input Conditions Were Established.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	54LS173			DM74LS173A			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.7			0.8	V
I _{OH}	High Level Output Current			−1			−2.6	mA
I _{OL}	Low Level Output Current			12			24	mA
f _{CLK}	Clock Frequency (Note 1)	30			0		30	MHz
	Clock Frequency (Note 2)				0		20	MHz
t _W	Pulse Width (Note 3)	Clock	20		17			ns
		Clear	17		17			
t _{SU}	Setup Time (Note 3)	Enable	17		23			ns
		Data	15		15			
t _H	Hold Time (Note 3)	Enable	0		0			ns
		Data	5		0			
t _{REL}	Clear Release Time	10			10			ns
T _A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: C_L = 45 pF, R_L = 667Ω, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 150 pF, R_L = 667Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = −18 mA			−1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IL} = Max, V _{IH} = Min	2.4			V
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max	54LS		0.4	V
		V _{IL} = Max, V _{IH} = Min	DM74	0.35	0.5	
		I _{OL} = 4 mA, V _{CC} = Min	DM74	0.25	0.4	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V			0.1	mA
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V			−0.4	mA
I _{OZH}	Off-State Output Current with High Level Output Voltage Applied	V _{CC} = Max, V _O = 2.7V V _{IH} = Min, V _{IL} = Max			20	μA
I _{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V _{CC} = Max, V _O = 0.4V V _{IH} = Min, V _{IL} = Max			−20	μA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 5)	54LS	−20	−100	mA
			DM74	−20	−100	
I _{CC}	Supply Current	V _{CC} = Max (Note 6)		17	30	mA

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	54LS		DM74LS		Units
			C _L = 50 pF		C _L = 50 pF R _L = 667Ω		
			Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency		30		20		ns
t _{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		28		25	ns
t _{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		28		28	ns
t _{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		30		30	ns
t _{PZH}	Output Enable Time to High Level Output	Output Control (M or N) to Any Q		23		26	ns
t _{PZL}	Output Enable Time to Low Level Output	Output Control (M or N) to Any Q		28		24	ns
t _{PHZ}	Output Disable Time from High Level Output (Note 7)	Output Control (M or N) to Any Q		17		17	ns
t _{PLZ}	Output Disable Time from Low Level Output (Note 7)	Output Control (M or N) to Any Q		23		25	ns

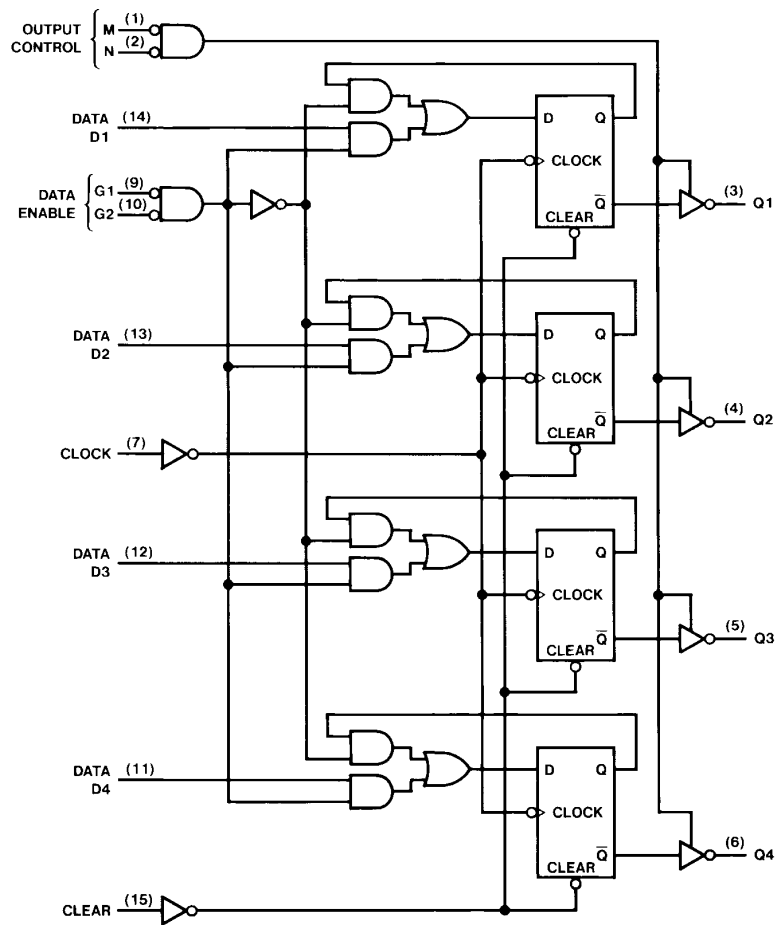
Note 4: All typicals are at $V_{CC} = 5V$, $T_A = 25^\circ C$.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CC} is measured with all outputs open: Clear grounded after a momentary 4.5V; N, G1, G2 and all data inputs grounded; and the CLOCK and M input at 4.5V.

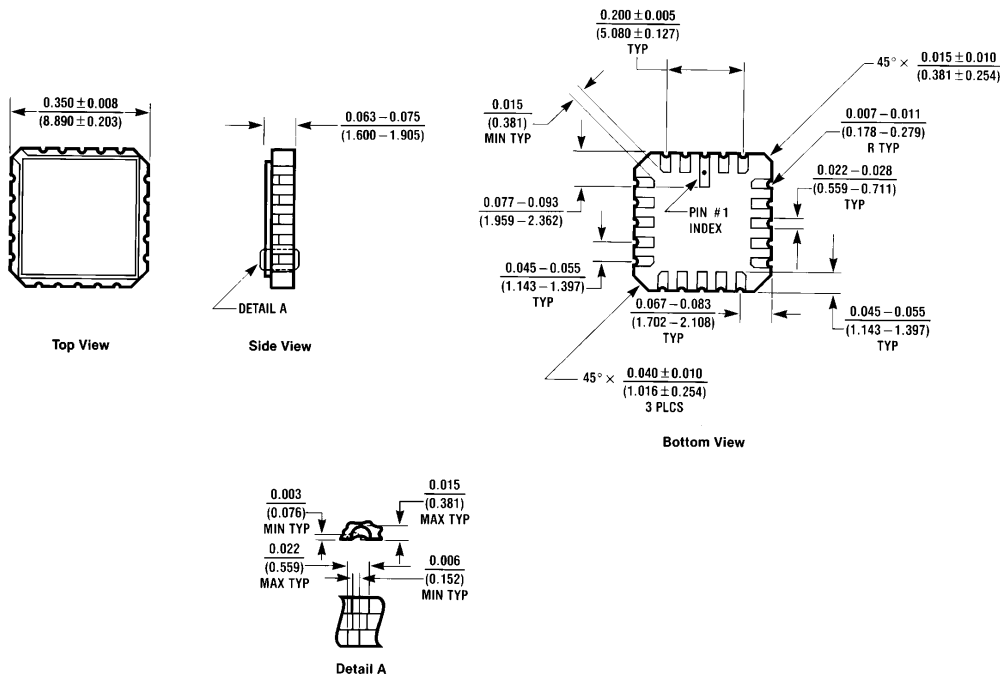
Note 7: $C_L = 5\text{ pF}$.

Logic Diagram



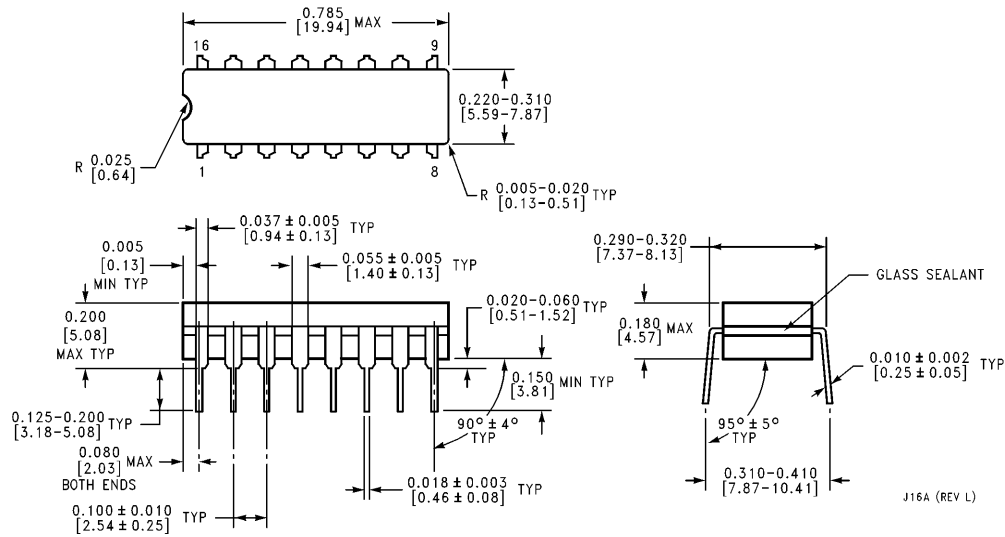
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Physical Dimensions inches (millimeters)



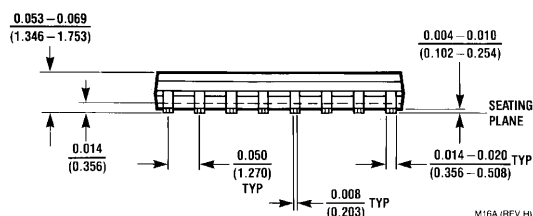
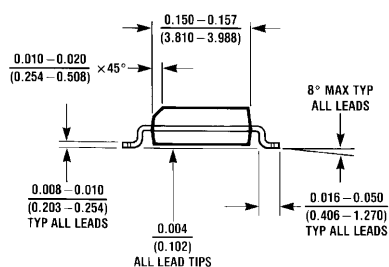
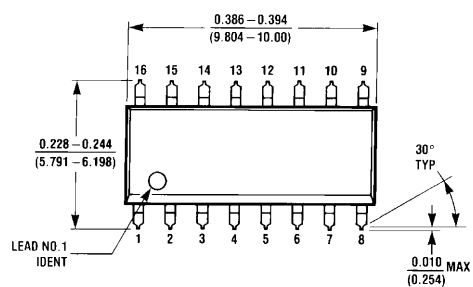
E20A (REV D)

Chip Carrier Package (E)
Order Number 54LS173LMQB
NS Package Number E20A

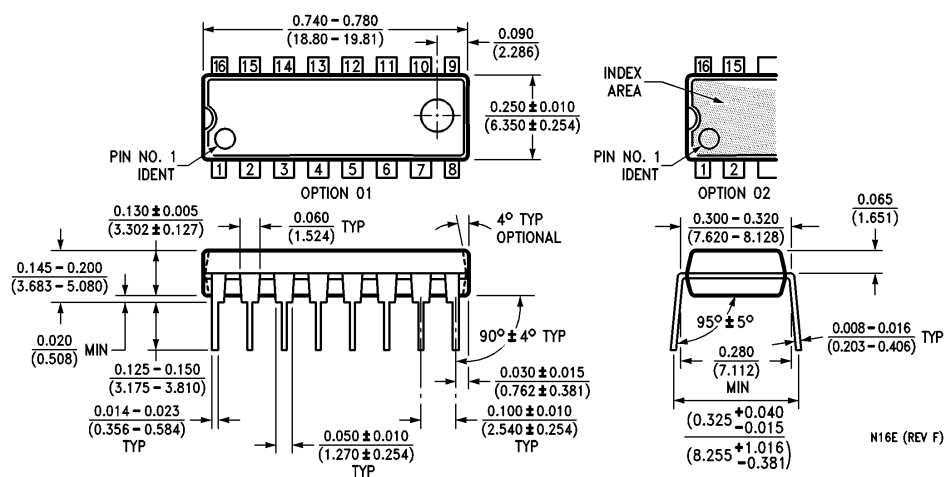


J16A (REV L)

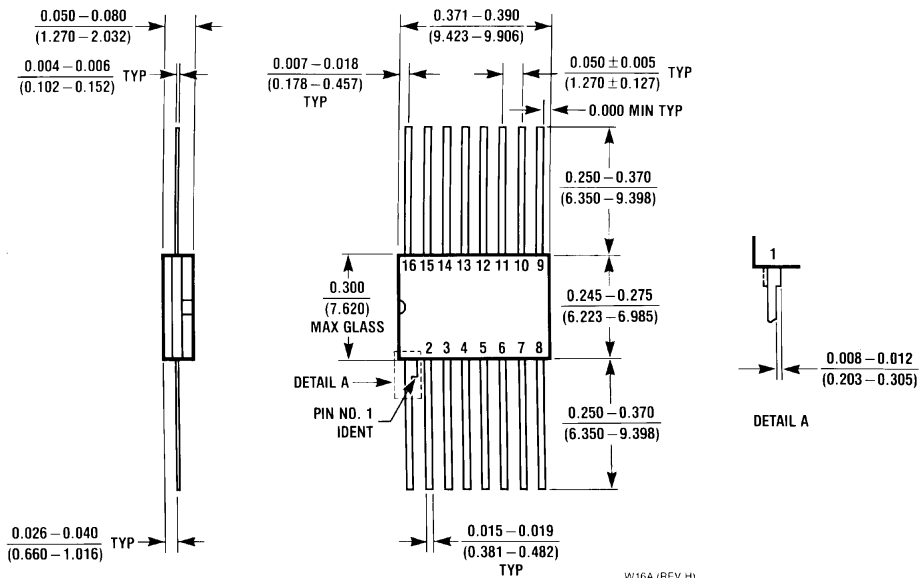
16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS173DMQB
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)

16-Lead Small Outline Molded Package (M)
Order Number DM74LS173AM
NS Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS173AN
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)

16-Lead Ceramic Flat Package (W)
Order Number 54LS173FMQB
NS Package Number W16A

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National Semiconductor Corporation
 1111 West Bardin Road
 Arlington, TX 76017
 Tel: 1(800) 272-9959
 Fax: 1(800) 737-7018

National Semiconductor Europe
 Fax: (+49) 0-180-530 85 86
 Email: cnjwge@tevm2.nsc.com
 Deutsch Tel: (+49) 0-180-530 85 85
 English Tel: (+49) 0-180-532 78 32
 Français Tel: (+49) 0-180-532 93 58
 Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
 19th Floor, Straight Block,
 Ocean Centre, 5 Canton Rd.
 Tsimshatsui, Kowloon
 Hong Kong
 Tel: (852) 2737-1600
 Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
 Tel: 81-043-299-2309
 Fax: 81-043-299-2408