Name : Mrs Ekata Mehul

Profession : Business and Service with Self Employment (Education)

Years of Experience: 25 **Nationality:** Indian

Qualification: Ph. D. (contd.-Education), M. Tech. (ICT), BE (Computer)

Achievements:

- Invited by US Govt. and Alumni for "International Visitor Leadership Program" representing Women in STEAM at INDIA level
- Nominated as "Traveller of Arkansas" for the Arkansas State development in US
- Working as Master Trainer with NSDC in SSC NASSCOM and ESSCI
- Working as Subject Matter Expert for ESSCI
- Received 'Best Employee Award" in 2012, working with eiTRA and eInfochips.
- Nominated as 'Women Entrepreneur Award' at Gujarat level in 2014
- eiTRA receiving Best Industry-Academia Interface award in 2014 at Gujarat level
- 3 Chapters @International Books
- 1 Patent on the "Wireless System for Electrical Metering"
- 25 publications in International journals and conferences

Experience Journey with Key tasks:

Director & CEO, Orena Solutions Pvt. Ltd. (July 2020 – until Date, Baroda)
Director , Blazing Arrows Pvt. Ltd. (Feb 2017 – until Date, Ahmedabad & Baroda)
Setting up the entire eco-system for making the fresher's Industry ready which includes collaboration with Global Knowledge partners and Industries. We setup Research Centres in Universities / Colleges supporting Research work for Idea to Alpha of products and leading to Incubation Technically for people

General Manager, VVDN Technologies Pvt. Ltd. (July 2018 – Mar 2019, Gurugram)
Talent Acquisition PAN India as well as Outside India, Lateral and Fresher including the complete training to make them industry ready was the role. Achievements was hiring 500 laterals in the span of 6 months.

HEAD, eiTRA (Academic Initiative of eInfochips) (May 2011 – September 2016; Ahmedabad)

1. Direct & manage overall execution, functioning and business operations of eiTRA.
2. Networked and developed powerful team of around 250 experts , industry professionals & academicians
3. Undertakes major initiatives of liaison with Govt. Of Gujarat and other Industries
4. Successfully collaborated with academic institutes & technology industries
    a. Board of members - Ganpat University, Nirma Institution of Technology, Dharamsinh Desai Institute of Technology, Gujarat Technological University along with Autonomous colleges
    b. Academic Associations – IIT Bombay, DAIICT Gandhinagar, NID Ahmedabad, L.D. College of Engineering Ahmedabad, Ahmedabad University, Babaria Institute of Technology, Vadodara, Silver Oak College of Engineering & Technology, Techno India NJR Institute of Technology, Udaipur, BVM
    c. Industry Associations - Texas Instruments University Programme, Cypress University Alliance, Venture Studio, Limberlink, Jed-I

5. Designed and structured industry specific learning programmes along with streamlining teaching methodology based on hands-on project based learning.
    a. Higher Education Programme – M. Tech in VLSI & Embedded Systems
    b. Industrial Proficiency Integrated Programmes (IPIP)
    c. Workshops on Cutting Edge Technologies (WCETs)
    d. Faculty Development Programme
    e. Internship for B. Tech & M. Tech Students (IDP)
    f. Expert Lecture Series
6. As devoted mentor and guide, with her own teaching methodology of using examples, she has imparted core technical knowledge in Computer systems, Networking, Computer Architecture, Operating Systems, Data Structures, Network Programming, Wireless Networking, etc.
7. Product Development – In direction of in-house product development, prototyping of couple of products namely "Elderly Assistive Device, Green House Automation, Electronic Badge Systems, Tiles Inspection System, University Portal, DSS for Maternal Care, etc." has been initiated by Ekata and team of M. Tech. students
8. Developing technical eco-system in associations with institutes, she has volunteered in establishment of advance laboratories , research & testing platforms
9. Projects Done:
    - Optimizing ASIC Design Cycle using co-simulation between Matlab & SV
    - Software Defined Radio for Wi-Fi & WiMAX
    - Enhancing Modelling Tool for Embedded Systems (Old Age Assistive Device)
    - Digital Energy Metering using ZigBee Protocol
    - Home Automation
    - Digital Signage

Training Coordinator, (November 2009 – May 2011) (eInfochips Ltd)

- Enhanced the training level within the organization
- Emulated the new training pedagogy which is Research Oriented with Industrial deadline and culture
- Also worked for 3-4 Industrial Projects as team member.
- Became Instrumental for the achievement of CMMi Level 3 for the company.

Head of Department, Computer Science and Faculty Member (BIT, SVIT, MSU)

- 14 years for career in starting and development of Engineering Departments
- Part of Curriculum Development in various Universities Viz. Gujarat University, GTU, Indus, Ganpat University, DDU and Nirma
- Worked as External Professor at DAIICT
- Instrumental and In charge for NBA Accreditation at SVIT for Computer Engineering Department
- External Counsellor at IGNOU
- Have trained >70000 students in career of 14 years
- Part of Examination body and paper setter for various subjects of interest.

Technical contribution & Project details

Project #1 : Smart Digital Metering System **(Customer: Govt. Research Lab**)
Technology **:** Zigbee, IoT and Energy Metering
Role : Project Lead
Team Size **:** 5
Synopsis

- Design for entire product is done

• As a Project lead responsible for Designing the System, testing the same and arranging for manufacturing it as well.
• Guiding and mentoring the team members, delegating the work and conducting weekly meetings as well as maintaining and updating the project plan.
Language and tools used C, PCB Design, Firmware and Hardware, Microchip Microcontroller

Project #2 : Networking Entire GIR Forest **(Customer: Gujarat Govt.)**
Technology **:** Networking-using TetraNet, IoT for Lion belt, tracking on website
Role : Project Lead
Team Size **:** 10
Synopsis
• Design for entire product is done including Research for Belt on Lion. Proposal was designed and demonstrated
• As a Project lead responsible for Designing the System, testing the same and arranging for manufacturing it as well. Done the presentation for IAS officers
• Guiding and mentoring the team members, delegating the work and conducting weekly meetings as well as maintaining and updating the project plan.
Language and tools used Network Programming, IoT, Tracking; Web based programming, Cloud Computing, Intel Microcontroller

Project #3 : Designing Old Age Assistive Device **(Collaborator: NID)**
Technology **:** Embedded Systems, Hardware Design, Firmware design, TI Panda Board, Sensors
Role : Project Lead
Team Size **:** 10
Synopsis
• The Entire Design of the System was done
• Features added to the device is Security, Social Networking, Alarm for reminders, Medical Health Check
• One Master Controller was designed with various other independent modules adding outside gadgets like TV, Projector as well..
Language and tools used TI Panda Board, Sensor, C Programming, Texas Microcontroller

Project #4 : Software for marking on GIS server **(Customer: Gujarat Govt.)**
Technology **: ISRI GIS programming**
Role : Project Lead
Team Size **:** 20
Synopsis
• The driver software is designed that works above GIS server
• Entire Land parcel being measured and plotted on the software designed by us
• Do entire Data Analysis using the software.
Language and tools used .Net Tools, ISRI Server on GIS, SQL DBMS, Texas Microcontroller

Project #5 **Functional Model for FEC and Viterbi Encoder & Decoder (Customer:** In-house)
Technology **:** Digital Communication
Role : Project Lead
Team Size **:** 4
Synopsis
• Error Detection and Correction are the prime functions as a part of any Communication Channel. FEC and Viterbi and mostly used block and convolutions codes for Digital Channel
• As a Project lead responsible for modifying the functional architecture, reviewing the design and test plan with verification documents.
• Guiding and mentoring the team members, delegating the work and conducting weekly meetings as well as maintaining and updating the project plan.
Language and tools used System Verilog, vcs and Matlab, Xilinx FPGA

Project #6 **Project Linting Tool for any HDL or HVL language (In-house)**

Technology **:** Compiler for any language
Role **:** Project Lead
Team Size **:** 4
Synopsis
- Linting Tool was responsible to check the amount of coding guidelines followed. It also used to highlight the place where the guidelines are not followed. It is general enough to work with any language
- As a project lead I was responsible for defining the process, architecture of the tool, reviewing the design and making it general
- Guiding and mentoring the team members, delegating the work and conducting weekly meetings as well as maintaining and updating the project plan.

Language and tools used Perl

Project #7 **Verification of FPGA Tool (Customer – Synopsys)**
Technology **:** Tool Validation
Role **:** Project Lead
Team Size **:** 2
Synopsis
- To verify the performance of the FPGA Tool for Simulation purpose and mainly its working for Xilinx Components
- Guiding and mentoring the team members, delegating the work and conducting weekly meetings as well as maintaining and updating the project plan.
- Weekly meeting with Client

Language and tools used Verilog, VHDL, vcs, modelsim, and vcs, Xilinx fpga

Project #8 **Comparison for Matlab and System Verilog working for DSP Filters**
Customer **:** In-house
Technology **:** Filters
Role **:** Project Lead
Team Size **:** 5
Synopsis
- We needed to understand the working of Matlab with HDL & HVL languages and also measure the performance difference between them in terms of Design & Coding efforts
- Developed the architecture of functional model using Matlab and System Verilog and complete approach for it.
- Responsible for handling 5 people by assigning them work and mentoring them

Language and tools used e Language, Specman elite, IUS (Incisive Simulator)

Project #9 **Optimization for Verification Cycle** (Customer: In-house)
Technology **:** Research Project
Role **:** Project Lead
Team Size **:** 2
Synopsis
- Since verification cycle takes lot of time in case of ASIC Design cycle, we are trying out various methods to check the reduction of time taken by verification cycle

Tools used Matlab, UML, and Ptolemy

Project # 10 Optimization of Code for Memory Usage and Execution time taken (Customer: In-house)
Technology Code Optimization fundamentals with Compilers and Data Structures
Role **:** Project Lead
Team Size **:** 1
Synopsis
- Working to try out various methods for optimizing the hardware functional model in terms of memory usage and time taken for execution
- Methods then can be used for any of such tasks
- To suggest the methodologies to be used, project planning, mentoring the team

Language C++

Project #11 Project Design and Simulation of Compression-Decompression Converter Processor (CDCP)
Technology : Digital Communication
Role : Team Member
Team Size : 4
Synopsis
Supporting all basic instructions and compression and decompression instructions were the part of the basic instruction set. The aim was to justify that if compression decompression is handled by the hardware itself then this processor can be useful for networks as it can directly help in reducing the network traffic. Also the basic arithmetic instructions were implemented using Vedic math algorithms. Tool used was Verilog and simulated at behavioural level.
Language and tools used Verilog, Modelsim and C

Project #12 Project High Speed TCP with Large Congestion Windows
Technology : Computer Networking Protocols
Role : Performer
Team Size : 1
Synopsis
Actually with normal TCP protocol, at the time of Congestion control we deal with it using AIMD algorithm i.e. if no congestion, window size is doubled and in case of congestion, it is halved. This algorithm becomes very slow, if the congestion window is large, which is normally the case currently, due to high-speed data transfers possible now. Sally Floyd has proposed another equation where window increases with a (w) size (in case of no congestion) and reduces by b (w) parameter (in case of congestion). The purpose of the project was to simulate the working of the parameter suggested by her.
Also when such equations work with the link having normal congestion window, the high speed TCP does not chew the whole link and if behaving fairly with the normal TCP window.
Language and tools used Ns2 and tcl / tk & C++

Project #13 Library module for all the data structures
Technology : Data Structures
Role : Performer
Team Size : 1
Synopsis
A basic library module is designed which includes all the operation performed on all the basic data structures viz. arrays, linked lists, stack, queue, priority queue, hashing, trees, graphs. All basic operations like insertion, deletion, searching, etc. are possible with all the data structures.
Language C on Linux

Project #14 Touch Screen
Technology Embedded Systems
Role : Performer
Team Size : 2
Synopsis
The project was part of 8th semester studies. The conceptual model for the same is as follows: Whole screen is divided in the matrix of 16 x 16. Opposite directions having LED transmitters and receivers. LED transmitter is continuously transmitting light, which is received by receivers. Attached with the receivers are the counters. Whenever any finger touches the screen, it automatically blocks the light path. The counters will count the x, y co-ordinate of the LED pair.
We used the calculator application (made in C) to demonstrate the working of touch screen. Hence based on the pair of LED blocked, particular number used to be displayed on the screen
Language and tools used C and PCB was designed

Project #15 Finger Print recognition
Technology : Image Processing

Role **:** Project Lead
Team Size **:** 2
Synopsis
This project is guided and we are using MATLAB, Image processing toolbox for the comparison of the finger print image. Used is the concept of Gabor filter for the comparison. Implemented is the papers published by Anil Jain et. al.
Tools used Matlab, UML, and Ptolemy, STMicroelectronics Microcontroller

Project # 16 **Copy Protection for XML Documents**
Technology Network Security using Steganography
Role **:** Performer
Team Size **:** 1
Synopsis
XML is the format of the communication today on the Internet. Even the concept of Digital Library is very much hot today. Communication through Internet is the fastest mode possible but unfortunately, it is not as reliable as paper communication. Proposed is the scheme for providing copy protection to the XML documents downloaded from the internet. This scheme is for tracing the traitor who has violated the copy protection law. The idea is to provide at least as much security as in case of printed document.
Language VB.Net on Windows

Technical Chapters Published

Technical Papers Published

Education:

Ph. D. (Education) (Contd.) Calorx university, Gandhinagar, Gujarat
Ph. D. (ICT) (Contd...) M. S. University, Baroda, Gujarat
M. Tech. (ICT) 2005, DAIICT Gandhinagar, Gujarat
B. E. (Computer Engg.) 1995, M. S. University, Baroda, Gujarat

Experience Summary:

1) Presently working as CEO and Director, Blazing Arrows (February 2017 – till date)
2) Worked as GM-Talent Acquisition for VVDN Technologies (April 2018 – Feb 2019)
3) Worked as a eiTRA Head (Division of eInfochips) (May 2011 – September 2016)
4) 2 years of experience in Training Engineers and leading project teams in eInfochips Ltd. in the area of VLSI & ASIC, Embedded and Software for C++, Verilog, C and Data Structures, Operating Systems, Linux & Perl. (2009-2011)
5) 14+ Years of Academic experience - Head of department, Computer Science and faculty member (BIT, SVIT, MSU)

Language:

English – Excellent
Hindi – Excellent
Gujarati - Excellent
Marathi - Can understand and speak
Malvi - Can Speak and understand completely

Personal Details:

Resident of Vadodara, Gujarat but Currently Operating from Ahmedabad, Gujarat

Phone: +91 98243 47721 **Email:** ekatamehul@gmail.com **Birthdate:** 24th May 1974