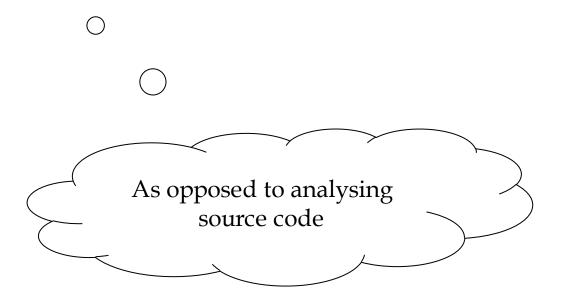
# A Complete Formal Semantics of x86-64 User-Level Instruction Set Architecture (ISA)

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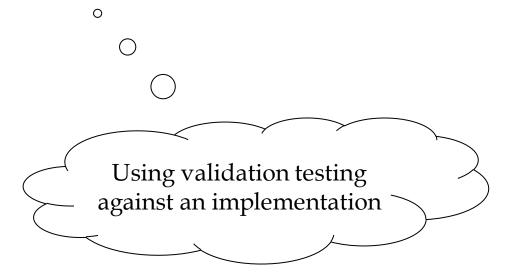
#### Formal ISA Semantics is Useful

Enables <u>direct</u> formal analysis of binary code



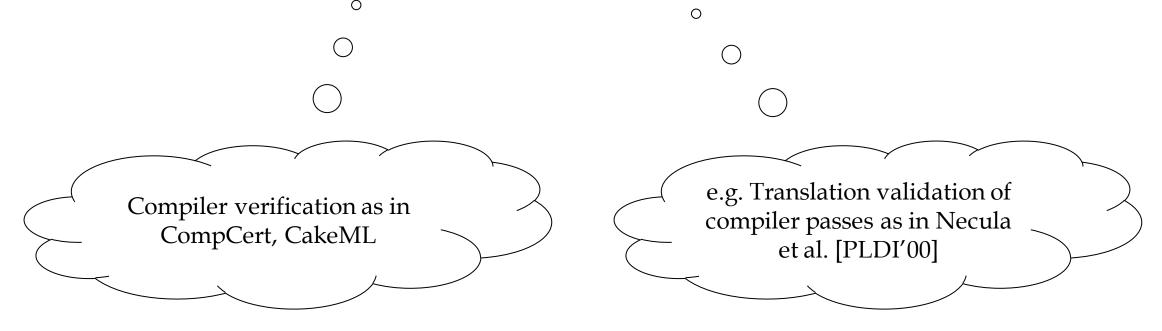
#### Formal ISA Semantics is Useful

Validating ISA reference manuals or processor hardware



#### Formal ISA Semantics is Useful

#### <u>Verification</u> or <u>Translation Validation</u>



# Example Formal ISA Semantics

RISC ISAs		CISC ISAs	
ISA	Formal Semantics	ISA	Formal Semantics
ARM	<ul><li>seL4 '09</li><li>SAIL '19</li><li>Compcert '09</li><li>CakeML '15</li></ul>	x86-32 (or IA32)	<ul> <li>ACL2 x86 '14</li> <li>Compcert '09</li> <li>TSL '13</li> <li>SAIL '17</li> <li>CakeML '14</li> </ul>
RISC-V	<ul><li>SAIL '19</li><li>Compcert '09</li></ul>		
	<ul><li>CakeML'18</li></ul>		A CLO . O. / / 4 11 4
MIPS	• SAIL '19	x86-64	<ul> <li>ACL2 x86-64 '14</li> <li>Strata '16</li> <li>CakeML '14</li> <li>Roessle et al. '19</li> </ul>
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SPARC	• TSL '13		



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# Challenges: from ISA Spec to Semantics



- ☐ 3000+ pages of informal & description
- ☐ 996 unique mnemonics with 3736 variants
- ☐ Inconsistent behavior of variants

# x86-64 Semantics: Previous Work

- □ Direct semantics: Low instruction coverage
   □ Hunt & Goel [FMCAD'14] (~ 33%)
   □ Strata semantics [PLDI'16] (~ 54%)
  - □ Roessle et al. [CPP'19] (~ 49%)
  - ☐ CakeML [POPL'14] (a small fraction)

- $\square$  Indirect semantics (x86  $\rightarrow$  IR)
  - ☐ Bap, Remill, Angretc.



We defined the **most complete** and **thoroughly tested** formal semantics of **user-level** x86-64 ISA



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github.com/kframework/X86-64-semantics

☐ Most complete user-level support (3155 instruction variants)



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- ☐ Most complete user-level support (3155 instruction variants)
- ☐ Thoroughly tested against hardware using 7000+ input states and GCC-c torture tests



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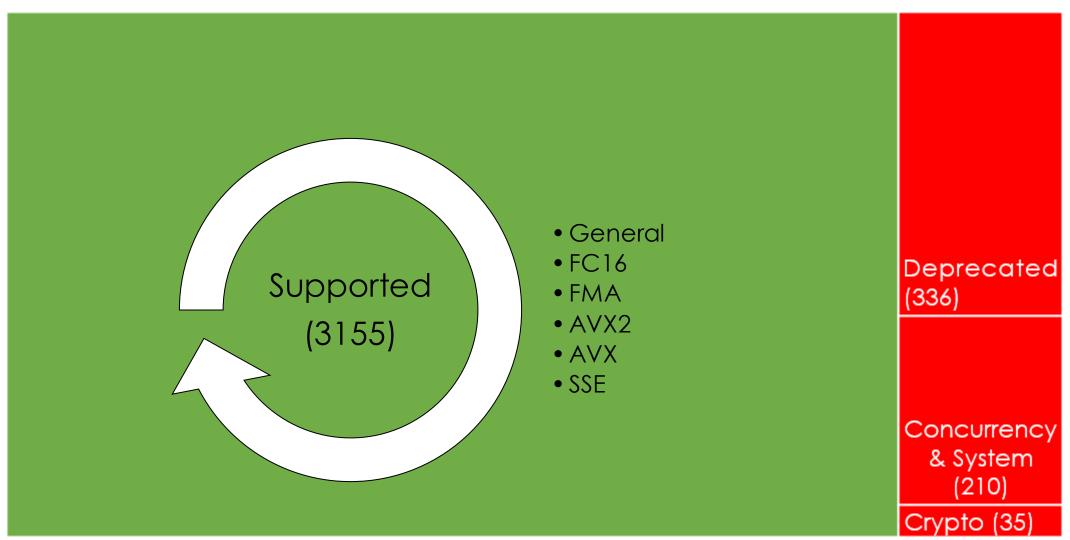
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- ☐ Most complete user-level support (3155 instruction variants)
- ☐ Thoroughly tested against hardware using 7000+ input states and GCC-c torture tests
- ☐ Found bugs in Intel manual and related projects
- ☐ Demonstrated applicability to formal reasoning



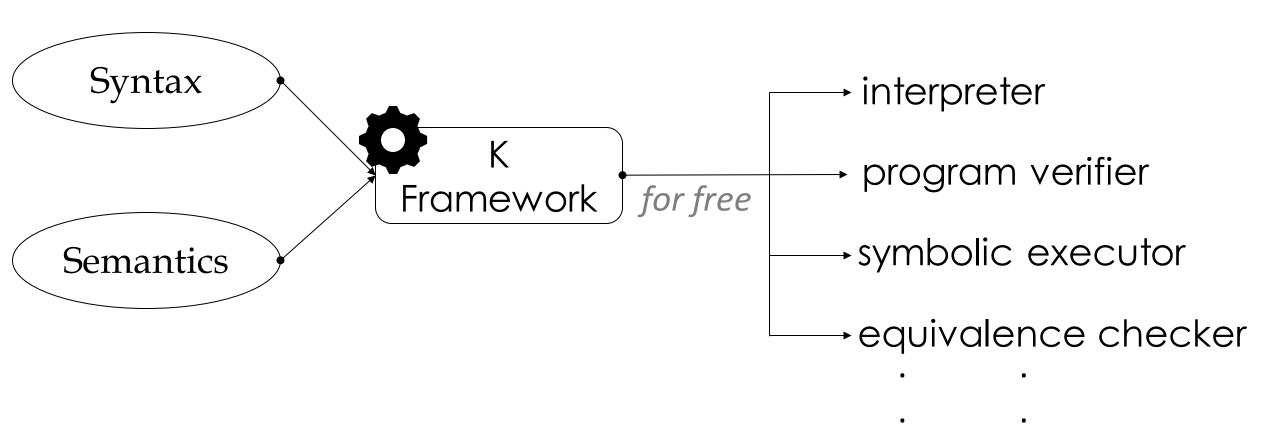
# Scope of Work (3155 / 3736)

Supported (3155)Unsupported (581)



## K Framework [Rosu et al. 2010]

Language semantics engineering framework (kframework.org)

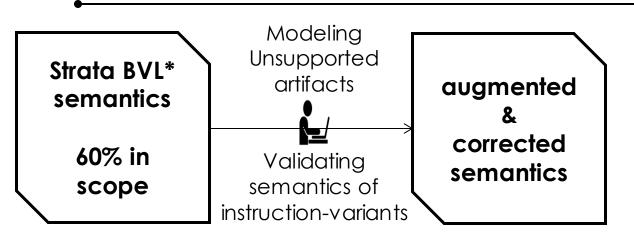




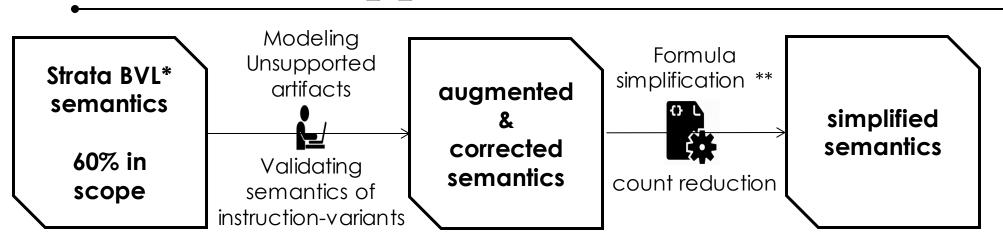
Strata BVL\* semantics

60% in scope

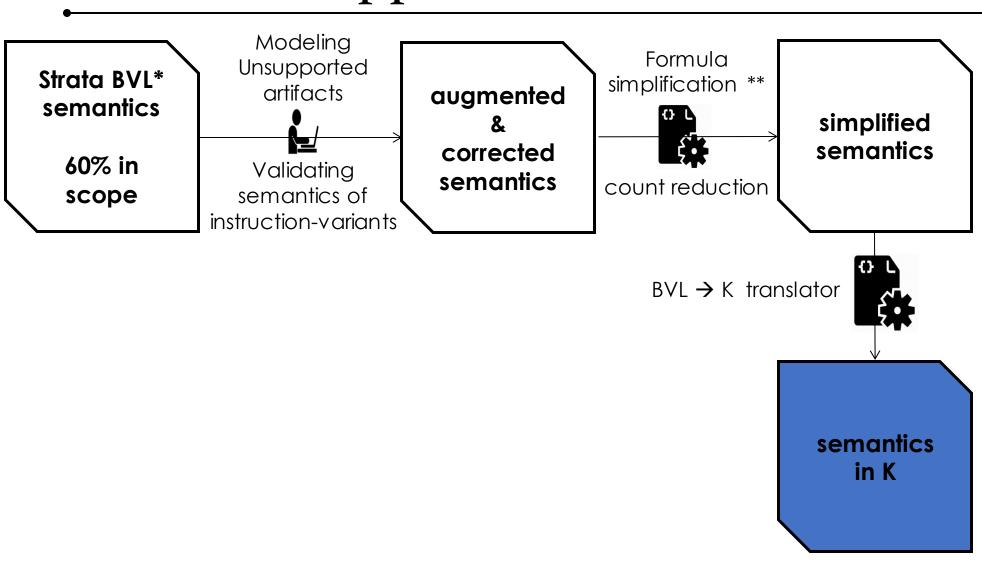
<sup>\*</sup> BVL: Bit-vector logic



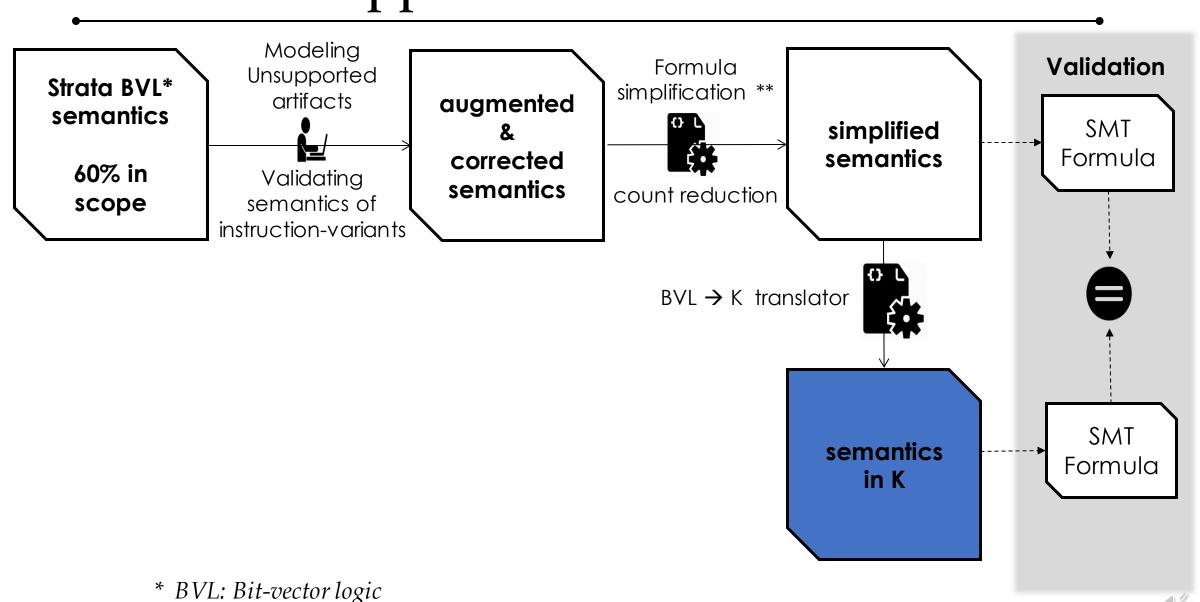
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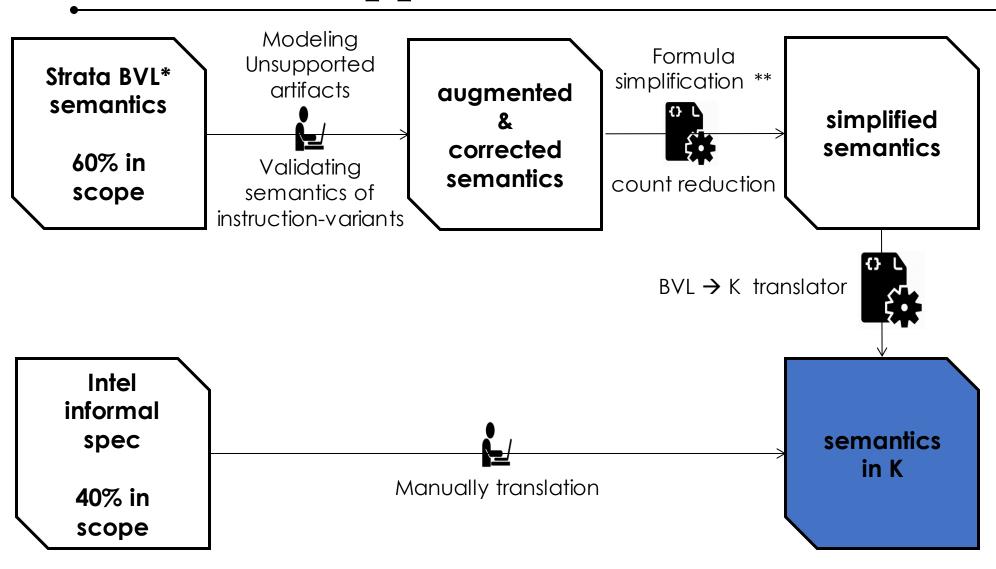
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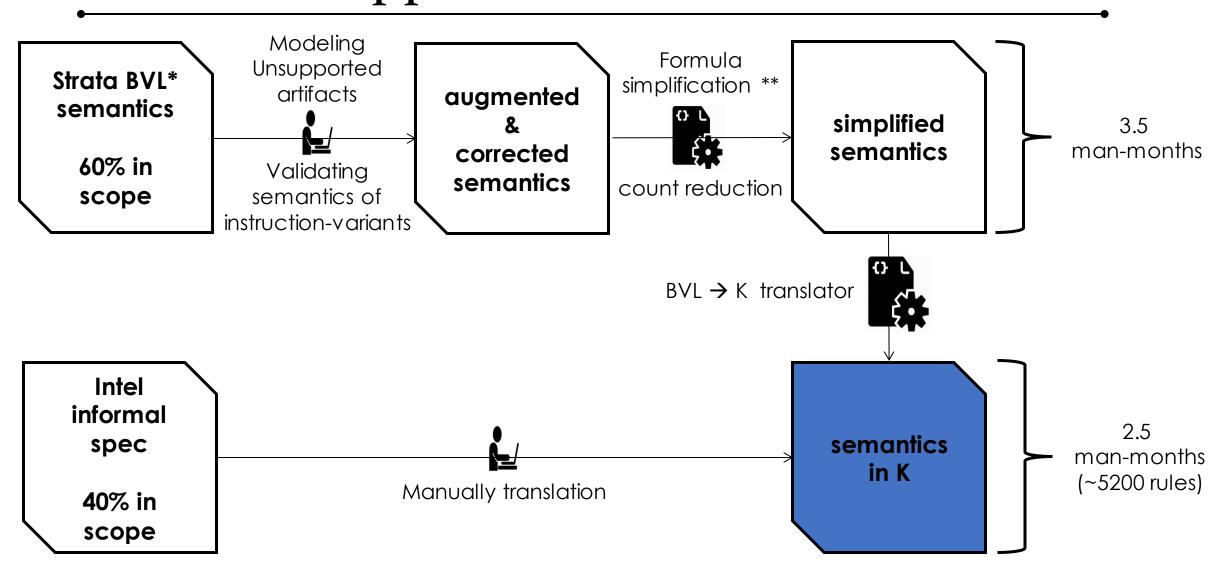


<sup>\*\* 30+</sup> simplification rules. BVL formula of shrxl with 8971 terms simplified to 7 terms



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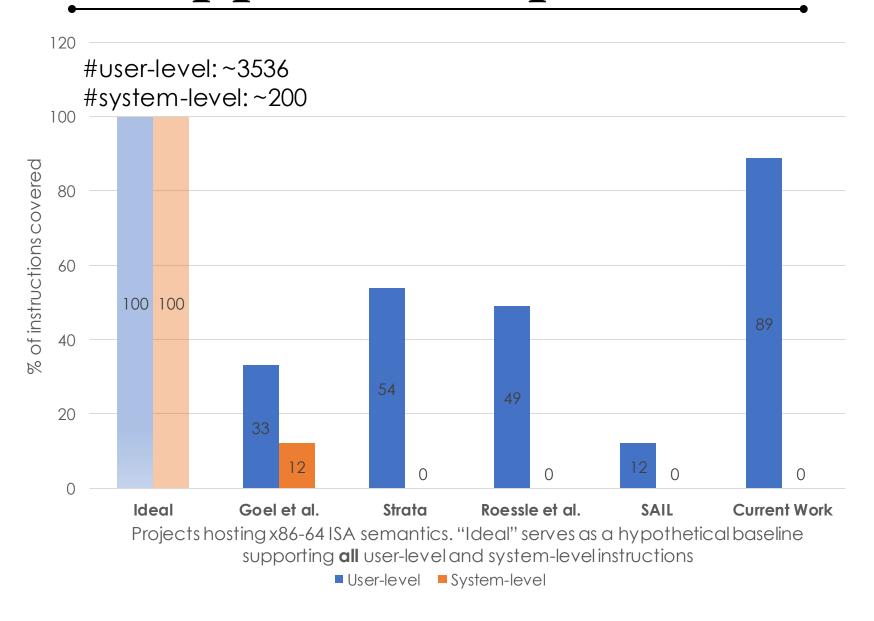
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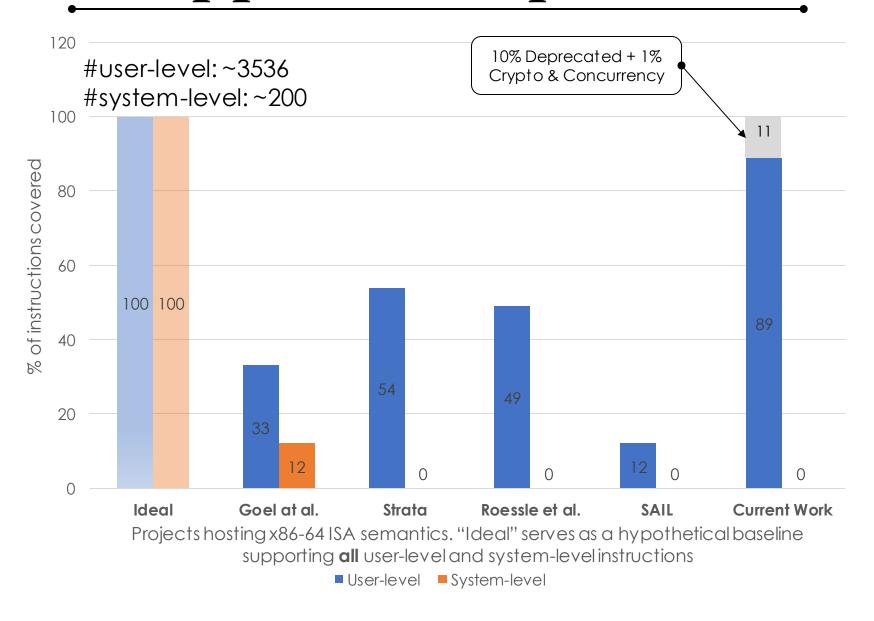
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# Support Comparison



# Support Comparison



#### Validation of Semantics

Instruction Level Testing (7000+ inputs states )

Comparing with hardware

Program Level Testing (GCC-c torture tests)

Comparing with Stoke Comparing SMT formula

12+ Bugs reported

- Intel Manual
- Strata formulas



40+ Bugs reported In Stoke



# A Few Reported Bugs

```
intel Manual Vol. 2: March 2018
```

# VPSRAVD (VEX.128 version) COUNT\_0 ← SRC2[31:0] \_\_(\* Repeat Each COUNT\_i for the 2nd through 4th dwords of SRC2\*) COUNT\_3 ← SRC2[100:96] DEST[31:0] ← SignExtend(SRC1[31:0] >> COUNT\_0);

(\* Repeat shift operation for 2nd through 4th dwords \*)
DEST[127:96] ← SignExtend(SRC1[127:96] >> COUNT\_3);
DEST[MAXVL-1:128] ← 0;



#### VPSRAVD (VEX.128 version)

```
COUNT_0 ← SRC2[31:0]

(* Repeat Each COUNT_i for the 2nd through 4th dwords of SRC2*)

COUNT_3 ← SRC2[127:96];

DEST[31:0] ← SignExtend(SRC1[31:0] >> COUNT_0);

(* Repeat shift operation for 2nd through 4th dwords *)

DEST[127:96] ← SignExtend(SRC1[127:96] >> COUNT_3);

DEST[MAXVL-1:128] ← 0;
```

# A Few Reported Bugs



Stoke Implementation May 2018

```
VCVTSI2SD (VEX.128 encoded version)
```

```
IF 64-Bit Mode And OperandSize = 64
THEN
    DEST[63:0] ← Convert_Integer_To_Double_Precision_Floating_Point(SRC2[63:0]);
ELSE
    DEST[63:0] ← Convert_Integer_To_Double_Precision_Floating_Point(SRC2[31:0]);
FI:
```

DEST[127:64]  $\leftarrow$  (Unmodified)



Intel Manual Vol. 2: May 2019

#### VCVTSI2SD (VEX.128 encoded version)

```
IF 64-Bit Mode And OperandSize = 64
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FI;
DEST[127:64] ←SRC1[127:64]
```

# A Few Reported Bugs

```
皶
```

Stoke Implementation May 2018

```
PSLLD (with 64-bit operand)
```



#### PSLLD (with 64-bit operand)

```
IF (COUNT > 31)  
THEN  
DEST[64:0] \leftarrow 000000000000000H;  
ELSE  
DEST[31:0] \leftarrow ZeroExtend(DEST[31:0] << COUNT);  
DEST[63:32] \leftarrow ZeroExtend(DEST[63:32] << COUNT);  
FI;
```

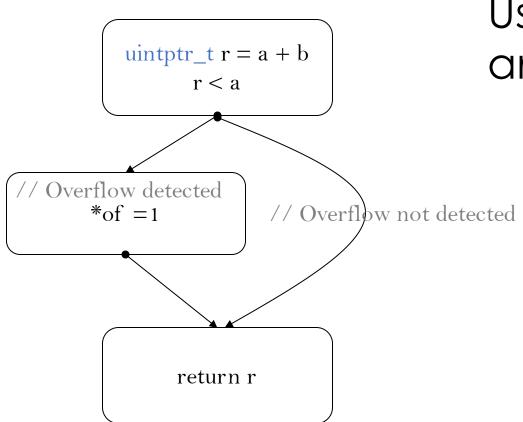
# A Few Potential Applications

- ☐ Program verification
- ☐ Translation validation of compiler optimization
- ☐ Security vulnerability tracking

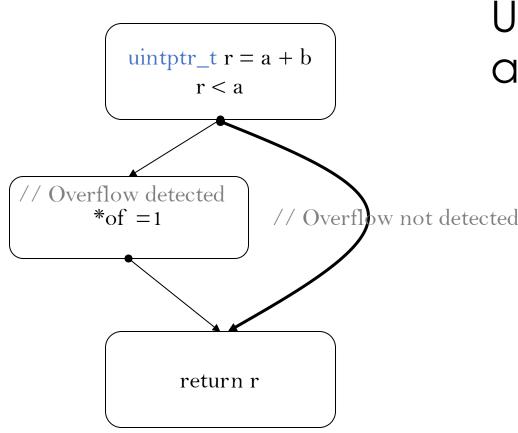


```
uintptr_t r = a + b
uintptr_t safe_addptr (int *of, uint64_t a, uint64_t b)
                                                                            r < a
  uintptr_t r = a + b;
                                                               Overflow detected
                                                                                    // Overflow not detected
                                                                   *of = 1
  if (r < a) // Condition not sufficient to prevent
               // overflow in case of 32-bit compilation
        *of = 1;
  return r;
                                                                           return r
```



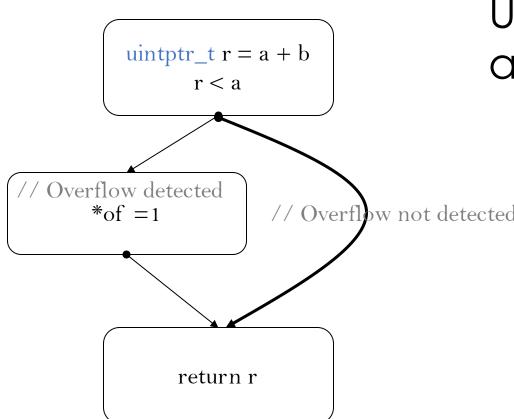


Use symbolic-execution to find an input (a,b) such that



Use symbolic-execution to find an input (a,b) such that

No overflow detectedi.e. (a + b mod 2 ^ 32 ) ≥ a



Use symbolic-execution to find an input (a,b) such that

No overflow detected i.e.  $(a + b \mod 2 \land 32) \ge a$ 

#### And

Overflow occurs i.e.  $a + b \ge 2^32$ 

#### What's Next?

- ☐ To validate the translation in
  - compiler backends
  - decompilers
- ☐ To generate high-coverage test-inputs
- Encourage and support external users of the semantics



# Summary

- ☐ Most complete user-level x86-64 semantics
- ☐ Thoroughly tested
- ☐ Applicable to different formal reasoning setup
- ☐ Publicly available

