36V Single Supply, 7MHz Bandwidth, RRO Op-amps

Features

- **Gain-bandwidth Product: 7MHz**
- **High Slew Rate: 20V/μs**
- **High EMIRR: 84dB at 900MHz**
- **Low Noise: 19 nV/√Hz(f= 1kHz)**
- **Wide Supply Range: 2.7V to 36V**
- **Low Offset Voltage: 1.0mV Maximum**
- **Low Input Bias Current: 3pA Typical**
- **Below-Ground (V-) Input Capability to -0.3V**
- **Rail-to-Rail Output Voltage Range**
- **High Output Current: 80mA (2.0V Drop)**
- **Unit Gain Stable**
- **3mm*2mm DFN Package for TP2274**
- **–40°C to 125°C Operation Range**
- **Robust 3kV – HBM and 2kV – CDM ESD Rating**

Applications

- Digital Servo Control Loops
- Machine and Motion Control Devices
- Photodiode Pre-amp
- Industrial Process Control
- Temperature Measurements
- Strain Gage Amplifier
- Medical Instrumentation

Description

The TP2271/TP2272/TP2274 are EMI Hardened 36V CMOS op-amps featuring EMIRR of 84dB at 900MHz. The devices are unity gain stable with 100pF capacitive load and high-speed with a wide 7MHz bandwidth and 20V/μs high slew rate, which makes the devices appropriated for I/V converters.

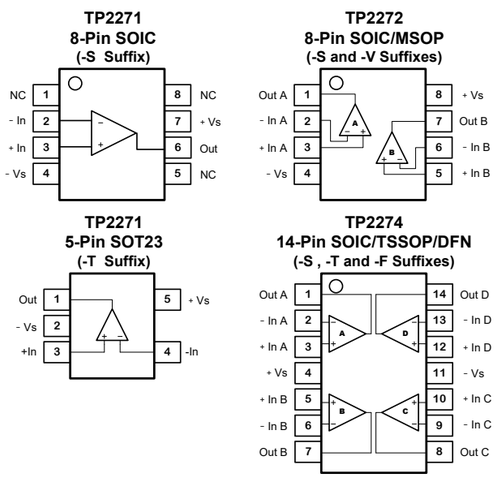
The rail-to-rail output swing and input range that includes V– makes the TP227x ideal choices for interfacing to modern, single-supply and precision data converters.

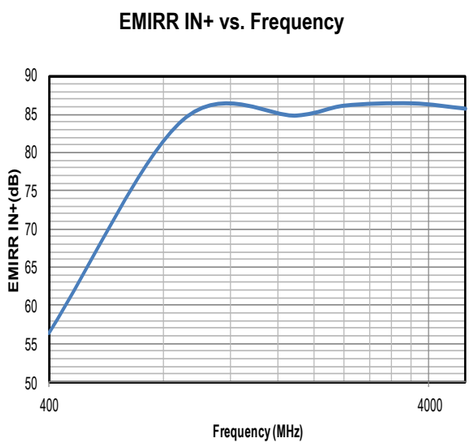
The TP227x op-amps offer lower noise, offset voltage, offset drift over temperature and bias current. In addition, the devices have better common-mode rejection and slew rates.

The TP227x family, exhibiting high input impedance and low noise, is excellent for small signal conditioning for high impedance sources, such as piezoelectric transducers. Because of the micro power dissipation levels, the devices work well in hand held monitoring and remote sensing applications.

The TP2271 is single channel version available in 8-pin SOIC and 5-pin SOT23 packages. The TP2272 is dual channel version available in 8-pin SOIC and MSOP packages. The TP2274 is quad channel version available in 14-pin SOIC, TSSOP and DFN packages.

Pin Configuration (Top View)





36 V单电源、7 MHz带宽、RRO运算放大器

Features

- **Gain-bandwidth Product: 7MHz**
- 高压摆率：20 V/μs
- 高EMIRR：900 MHz时为84 dB
- **Low Noise: 19 nV/√Hz(f= 1kHz)**
- 宽电源范围：2.7V至36 V
- 低失调电压：最大1.0mV
- 低输入偏置电流：3 pA（典型值）
- 地以下（V–）输入能力至–0.3V
- 轨到轨输出电压范围
- 高输出电流：80 mA（2.0V压降）
- 单位增益稳定
- 用于TP 2274的3 mm * 2 mm DFN封装
- 工作温度范围：–40 ° C至125°C
- 稳健的3 kV– HBM和2kV – CDM ESD额定值

Applications

- 数字伺服控制回路
- 机器和运动控制设备
- Photodiode Pre-amp
- 工业过程控制
- 温度测量
- 应变仪放大器
- 医疗仪器

Description

TP 2271/TP 2272/TP 2274是经过EMI加固的36 V CMOS运算放大器，在900 MHz时具有84 dB的EMIRR。 该器件具有100 pF容性负载的单位增益稳定性和7 MHz带宽、20 V/μs压摆率的高速特性，适用于I/V转换器。

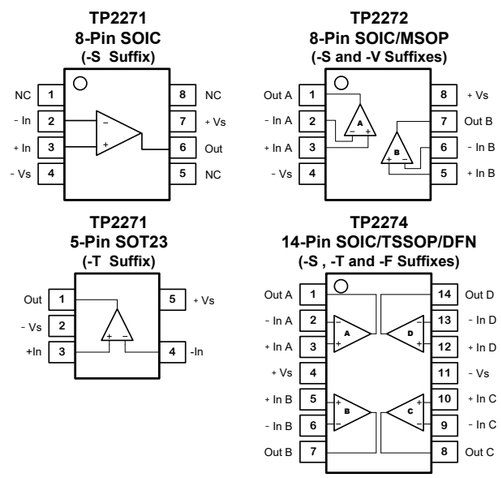
轨到轨输出摆幅和输入范围（包括V–）使TP 227 x成为与现代单电源精密数据转换器接口的理想选择。

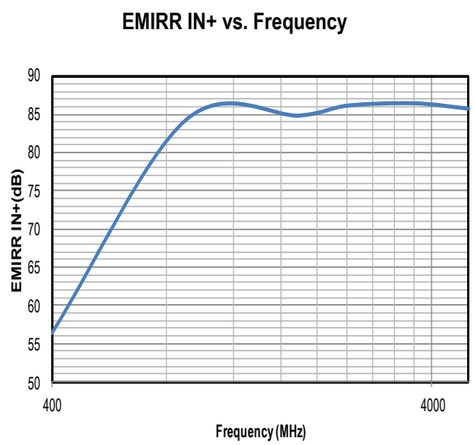
TP 227 x运算放大器具有较低的噪声、失调电压、温度范围内的失调漂移和偏置电流。 此外，这些器件具有更好的共模抑制和压摆率。

TP 227 x系列具有高输入阻抗和低噪声特性，非常适用于高阻抗源（如压电传感器）的小信号调理。 由于微功耗水平，该器件在手持监控和遥感应用中工作良好。

TP 2271为单通道版本，采用8引脚SOIC和5引脚SOT 23封装。 TP 2272是双通道版本，采用8引脚SOIC和MSOP封装。 TP 2274为四通道版本，采用14引脚SOIC、TSSOP和DFN封装。

引脚配置（顶视图）





36V Single supply, 7MHz Bandwidth, RRO Op-amps

Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
TP2271	TP2271-SR	8-Pin SOIC	Tape and Reel, 4,000	TP2271
	TP2271-TR	5-Pin SOT23	Tape and Reel, 3,000	E22
TP2272	TP2272-SR	8-Pin SOIC	Tape and Reel, 4,000	TP2272
	TP2272-VR	8-Pin MSOP	Tape and Reel, 3,000	TP2272
TP2274	TP2274-SR	14-Pin SOIC	Tape and Reel, 2,500	TP2274
	TP2274-TR	14-Pin TSSOP	Tape and Reel, 3,000	TP2274
	TP2274-FR	14-Pin DFN	Tape and Reel, 3,000	2274

Absolute Maximum Ratings Note 1

Supply Voltage: $V^+ - V^-$ Note 2 ..... 40.0V
Input Voltage ..... V^- – 0.3 to V^+ + 0.3
Input Current: +IN, –IN Note 3 ..... ±20mA
Differential Input Voltage Note 4 ..... ±0.5V
Output Short-Circuit Duration Note 5 ..... Indefinite

Current at Supply Pins ..... ±60mA
Operating Temperature Range ..... –40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The op amp supplies must be established simultaneously, with, or before, the application of any input signals.

Note 3: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 4: The differential input voltage must be in the range of Input Voltage: V^- – 0.3 to V^+ + 0.3 V

Note 5: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	3	kV
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
5-Pin SOT23	250	81	°C/W
8-Pin SOIC	158	43	°C/W
8-Pin MSOP	210	45	°C/W
14-Pin SOIC	120	36	°C/W
14-Pin TSSOP	180	35	°C/W
14-Pin DFN	100	34	°C/W

36 V单电源、7 MHz带宽、RRO运算放大器

订单信息

型号名称	订单号	Package	运输介质，数量	Marking Information
TP2271	TP2271-SR	8-Pin SOIC	磁带和卷轴，4，000	TP2271
	TP2271-TR	5-Pin SOT23	磁带和卷轴，3000	E22
TP2272	TP2272-SR	8-Pin SOIC	磁带和卷轴，4，000	TP2272
	TP2272-VR	8-Pin MSOP	磁带和卷轴，3000	TP2272
TP2274	TP2274-SR	14-Pin SOIC	磁带和卷轴，2500	TP2274
	TP2274-TR	14-Pin TSSOP	磁带和卷轴，3000	TP2274
	TP2274-FR	14-Pin DFN	磁带和卷轴，3000	2274

绝对最大额定值注释1

电源电压：V + – V –注2....40.0V
输入电压..... V – – 0.3至V + + 0.3
输入电流：+IN、–IN注3. ±20mA
差分输入电压注释4.....±0.5V
输出短路持续时间注释5... 无限期

电源引脚电流..... ±60mA
工作温度范围.....–40 ° C至125°C
最大结温..... 摄氏150度
存储温度范围.... –65 ° C至150°C
引线温度（焊接，10秒）... 摄氏260度

注1：超出绝对最大额定值所列的应力可能会导致设备永久性损坏。 暴露于任何绝对最大值长期的额定条件可能会影响设备的可靠性和寿命。

注2：运算放大器电源必须与任何输入信号同时建立，或在应用任何输入信号之前建立。

注3：输入由ESD保护二极管保护到每个电源。 如果输入超出电源超过500 mV，则输入电流应限制在10 mA以下。

注4：差分输入电压必须在输入电压范围内：V – – 0.3至V + + 0.3 V

注5：可能需要一个散热器来保持结温低于绝对最大值。 这取决于电源电压和短路的放大器数量。 热阻随连接到封装的PC板金属量而变化。 指定的值适用于连接到引线的短走线。

ESD、静电放电保护

Symbol	Parameter	Condition	最低水平	Unit
HBM	人体模型ESD	MIL-STD-883H Method 3015.8	3	kV
CDM	充电器件模型ESD	JEDEC-EIA/JESD22-C101E	2	kV

热阻

封装类型	θ_{JA}	θ_{JC}	Unit
5-Pin SOT23	250	81	°C/W
8-Pin SOIC	158	43	°C/W
8-Pin MSOP	210	45	°C/W
14-Pin SOIC	120	36	°C/W
14-Pin TSSOP	180	35	°C/W
14-Pin DFN	100	34	°C/W

Electrical Characteristics

The specifications are at T_A = 27°C. V_S = ±15V, V_{CM} = 0V, R_L = 2kΩ, C_L =100pF.Unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = 0V	-1.0	±0.4	+1.0	mV
		V_S = 5V, V_{CM} = 2.5V	-1.0	±0.4	+1.0	mV
V_{OS} TC	Input Offset Voltage Drift	-40°C to 125°C		2		μV/°C
I_B	Input Bias Current	T_A = 27 °C		3		pA
		T_A = 85 °C		250		pA
		T_A = 125 °C		7.7		nA
I_{OS}	Input Offset Current			0.001		pA
V_n	Input Voltage Noise	f = 0.1Hz to 10Hz		2.35		μV_{RMS}
e_n	Input Voltage Noise Density	f = 1kHz		19		nV/√Hz
C_{IN}	Input Capacitance	Differential Common Mode		4 2.5		pF
CMRR	Common Mode Rejection Ratio	V_{CM} = -14.5V to 13V	90	126		dB
V_{CM}	Common-mode Input Voltage Range		V⁻-0.3		V⁺-2.0	V
PSRR	Power Supply Rejection Ratio		90	130		dB
A_{VOL}	Open-Loop Large Signal Gain	R_{LOAD} = 2kΩ	95	118		dB
V_{OL}, V_{OH}	Output Swing from Supply Rail	R_{LOAD} = 100kΩ	50			mV
R_{OUT}	Closed-Loop Output Impedance	G = 1, f =1kHz, I_{OUT} = 0		0.01		Ω
R_O	Open-Loop Output Impedance	f = 1kHz, I_{OUT} = 0		125		Ω
I_{SC}	Output Short-Circuit Current	Sink or source current		80		mA
V_S	Supply Voltage		2.7		36	V
I_Q	Quiescent Current per Amplifier			900		μA
PM	Phase Margin	R_{LOAD} = 2kΩ, C_{LOAD} = 100pF		60		°
GM	Gain Margin	R_{LOAD} = 2kΩ, C_{LOAD} = 100pF		8		dB
GBWP	Gain-Bandwidth Product	f = 1kHz		7		MHz
SR	Slew Rate	A_V = 1, V_{OUT} = 0V to 10V, C_{LOAD} = 100pF, R_{LOAD} = 2kΩ		20		V/μs
FPBW	Full Power Bandwidth Note 1			210		kHz
t_S	Settling Time, 0.1% Settling Time, 0.01%	A_V = –1, 10V Step		1 1		μs
THD+N	Total Harmonic Distortion and Noise	f = 1kHz, A_V =1, R_L = 2kΩ, V_{OUT} = 3.5V_{RMS}		0.0001		%
X_{talk}	Channel Separation	f = 1kHz, R_L = 2kΩ		110		dB

Note 1: Full power bandwidth is calculated from the slew rate FPBW = SR/π • V_{P-P}

电特性

T A = 27°C。 V S = ± 15V，V CM = 0V，R L = 2kΩ，C L = 100pF.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	输入失调电压	V_{CM} = 0V	-1.0	±0.4	+1.0	mV
		V_S = 5V, V_{CM} = 2.5V	-1.0	±0.4	+1.0	mV
V_{OS} TC	输入失调电压漂移	-40°C to 125°C		2		μV/°C
I_B	输入偏置电流	T_A = 27 °C		3		pA
		T_A = 85 °C		250		pA
		T_A = 125 °C		7.7		nA
I_{OS}	输入失调电流			0.001		pA
V_n	输入电压噪声	f = 0.1Hz to 10Hz		2.35		μV_{RMS}
e_n	输入电压噪声密度	f = 1kHz		19		nV/√Hz
C_{IN}	输入电容	Differential 共模		4 2.5		pF
CMRR	共模抑制比	V_{CM} = -14.5V to 13V	90	126		dB
V_{CM}	共模输入电压 Range		V⁻-0.3		V⁺-2.0	V
PSRR	电源抑制比		90	130		dB
A_{VOL}	开环大信号增益	R_{LOAD} = 2kΩ	95	118		dB
VOL，VOH	相对于供电轨的输出摆幅	R_{LOAD} = 100kΩ	50			mV
R_{OUT}	闭环输出阻抗	G = 1, f =1kHz, I_{OUT} = 0		0.01		Ω
R_O	开环输出阻抗	f = 1kHz, I_{OUT} = 0		125		Ω
I_{SC}	输出短路电流	漏电流或源电流		80		mA
V_S	电源电压		2.7		36	V
I_Q	每个放大器的静态电流			900		μA
PM	相位裕度	R_{LOAD} = 2kΩ, C_{LOAD} = 100pF		60		°
GM	增益裕度	R_{LOAD} = 2kΩ, C_{LOAD} = 100pF		8		dB
GBWP	Gain-Bandwidth Product	f = 1kHz		7		MHz
SR	转换速率	A V = 1，V OUT = 0V to 10V，C LOAD = 100pF， R_{LOAD} = 2kΩ		20		V/μs
FPBW	全功率带宽注释1			210		kHz
t_S	稳定时间，0.1% 稳定时间，0.01%	A_V = –1, 10V Step		1 1		μs
THD+N	总谐波失真和 Noise	f = 1kHz, A_V =1, R_L = 2kΩ, V_{OUT} = 3.5V_{RMS}		0.0001		%
X_{talk}	信道分离	f = 1kHz, R_L = 2kΩ		110		dB

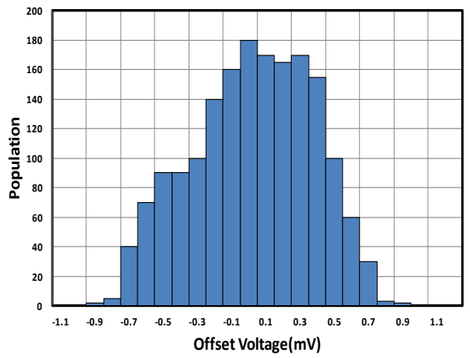
注1：全功率带宽根据压摆率FPBW = SR/π · V P–P计算

36V Single supply, 7MHz Bandwidth, RRO Op-amps

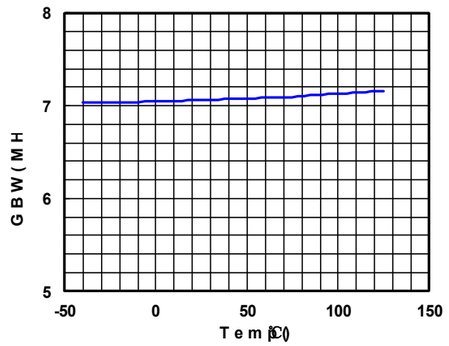
Typical Performance Characteristics

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified.

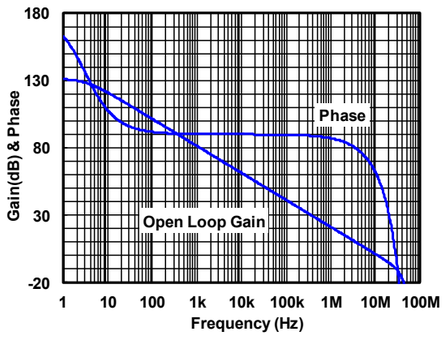
Offset Voltage Production Distribution



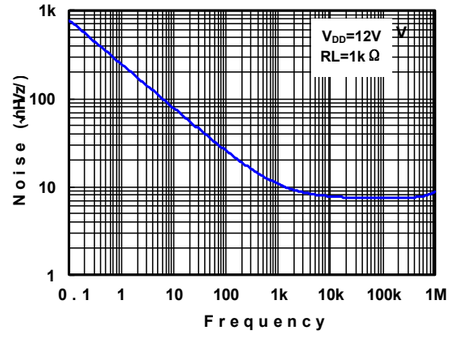
Unity Gain Bandwidth vs. Temperature



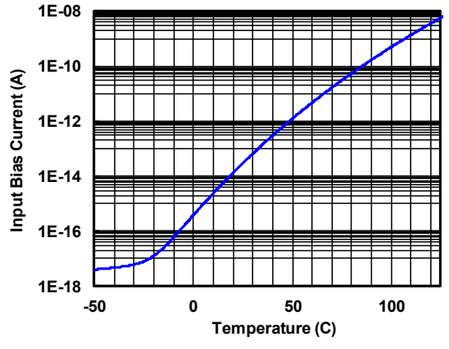
Open-Loop Gain and Phase



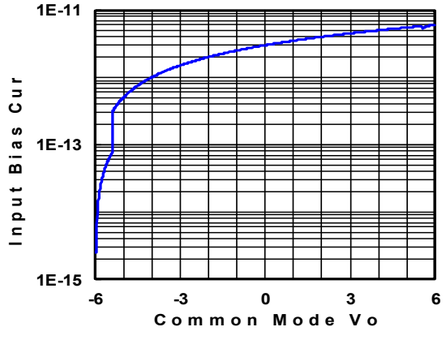
Input Voltage Noise Spectral Density



Input Bias Current vs. Temperature



Input Bias Current vs. Input Common Mode Voltage

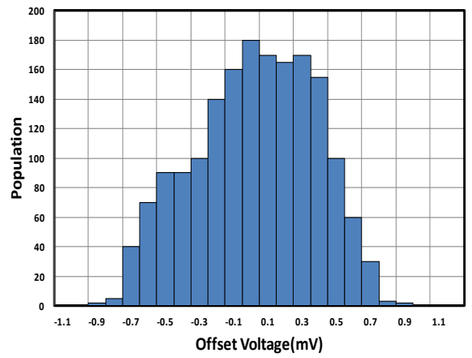


36V单电源、7MHz带宽、RRO运算放大器

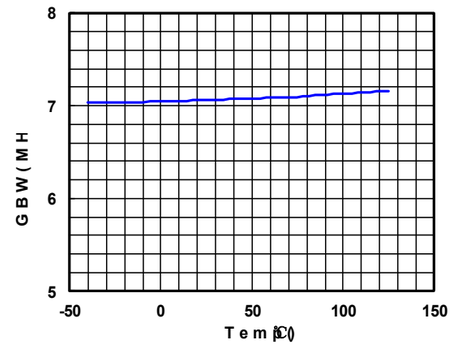
典型性能参数

V S = ±15V，V CM = 0V，R L = Open，除非另有规定。

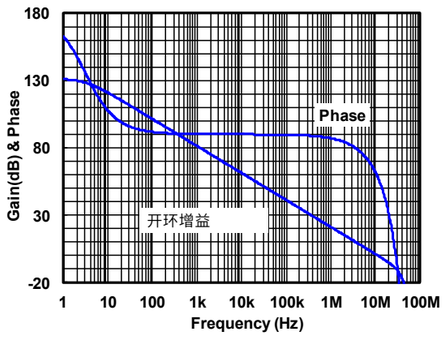
失调电压产生和分配



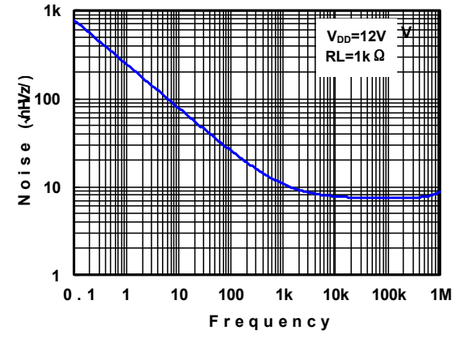
单位增益带宽与温度



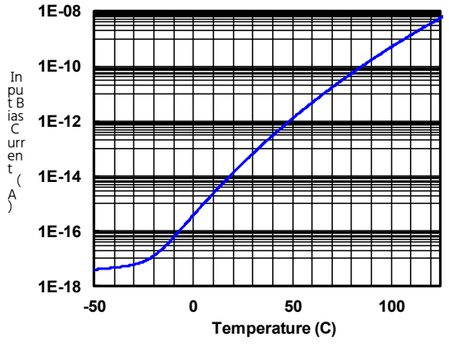
开环增益和相位



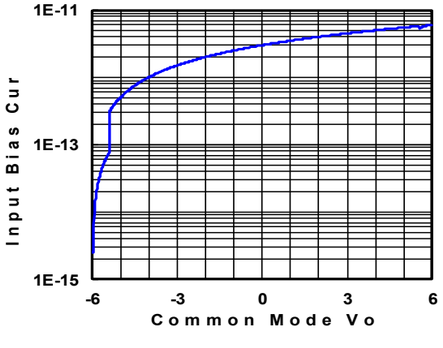
输入电压噪声谱密度



输入偏置电流与温度的关系



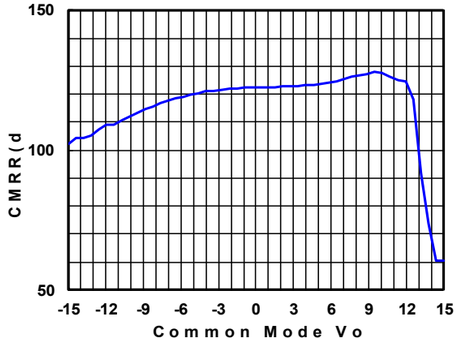
输入偏置电流与输入共模电压



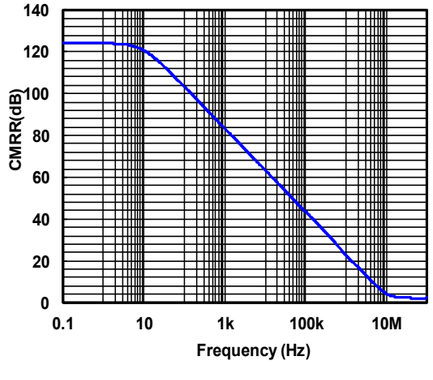
Typical Performance Characteristics

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. (Continued)

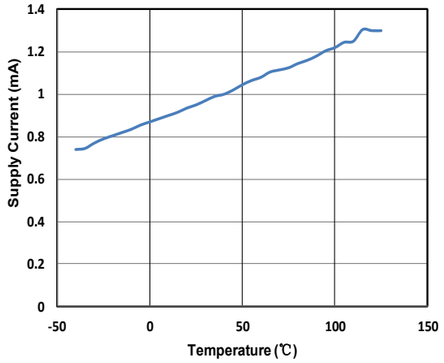
Common Mode Rejection Ratio



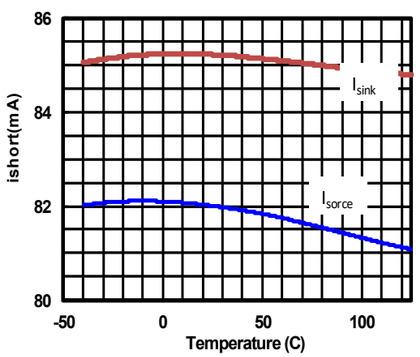
CMRR vs. Frequency



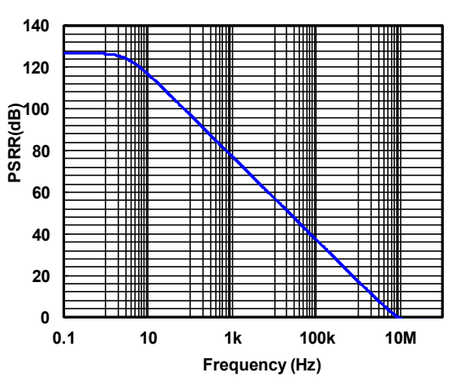
Quiescent Current vs. Temperature



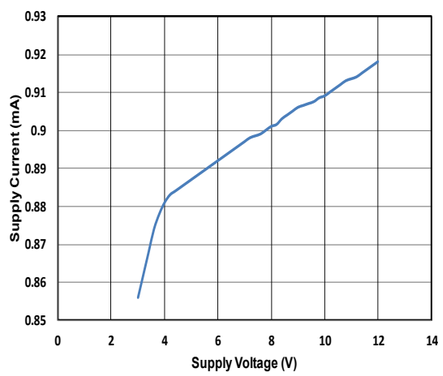
Short Circuit Current vs. Temperature



Power-Supply Rejection Ratio



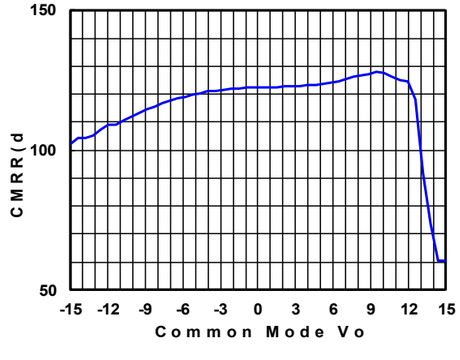
Quiescent Current vs. Supply Voltage



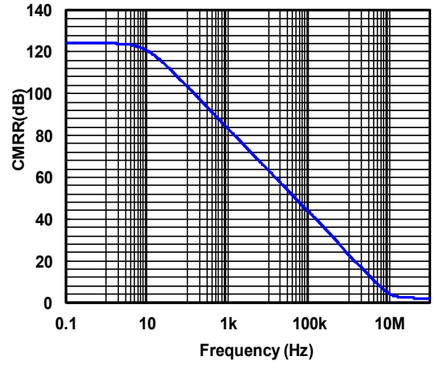
典型性能参数

V S = ±15V，V CM = 0V，R L = Open，除非另有规定。（续）

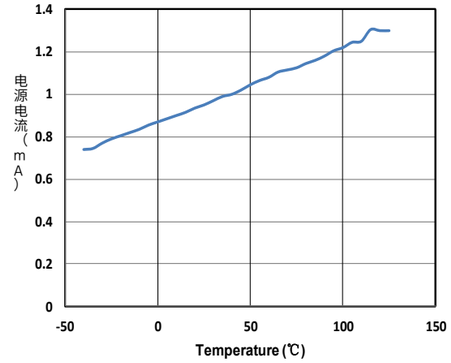
共模抑制比



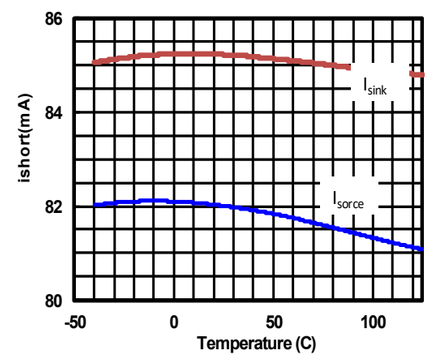
CMRR与频率



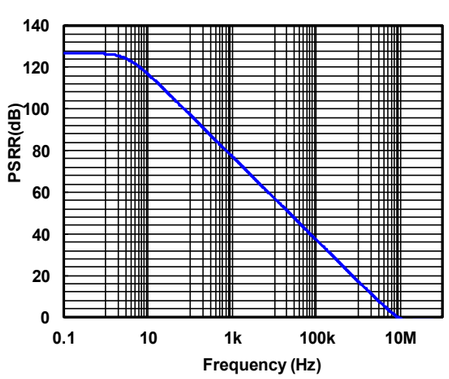
静态电流与温度



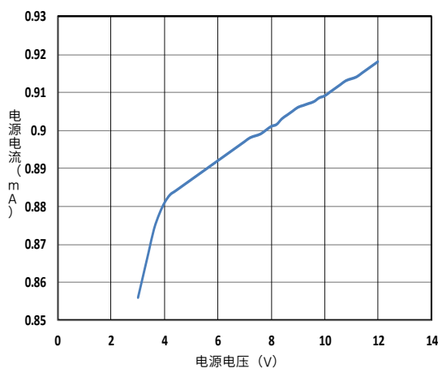
短路电流与温度



电源抑制比



静态电流与电源电压的关系

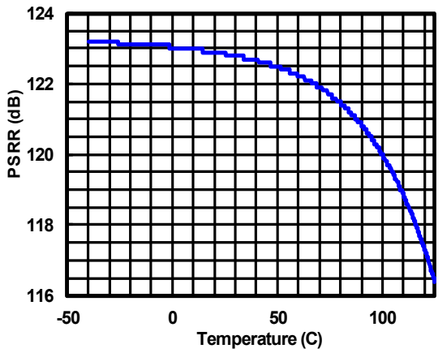


36V Single supply, 7MHz Bandwidth, RRO Op-amps

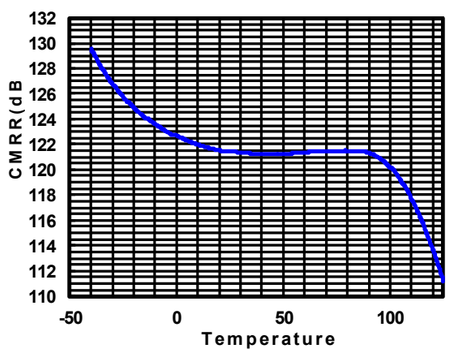
Typical Performance Characteristics

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. (Continued)

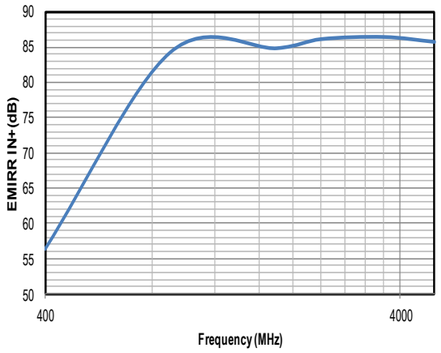
Power-Supply Rejection Ratio vs. Temperature



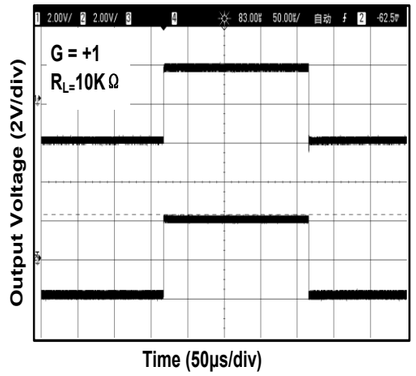
CMRR vs. Temperature



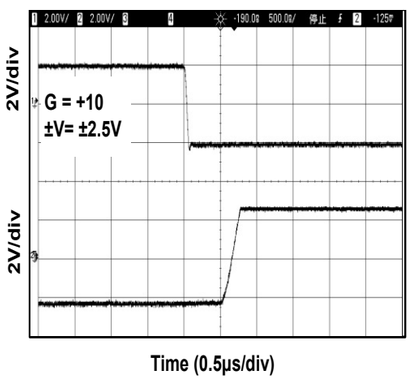
EMIRR IN+ vs. Frequency



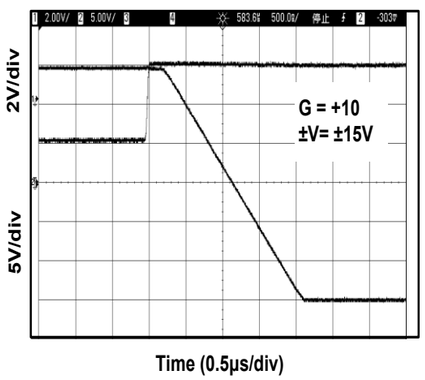
Large-Scale Step Response



Negative Over-Voltage Recovery



Positive Over-Voltage Recovery

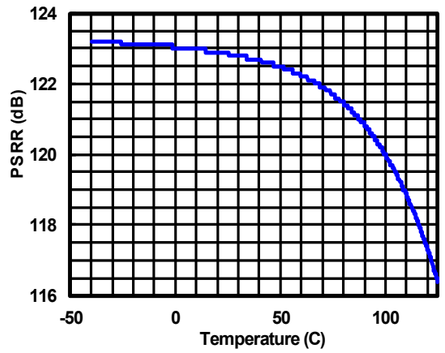


36 V单电源、7 MHz带宽、RRO运算放大器

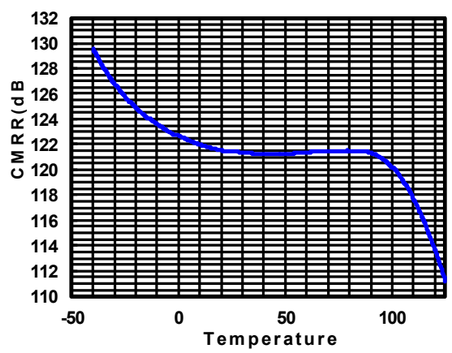
典型性能参数

V S = ± 15 V，V CM = 0 V，R L = Open，除非另有规定。 （续）

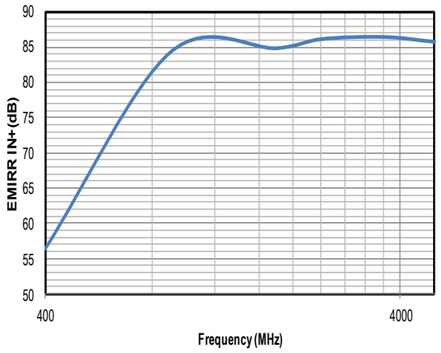
电源抑制比与温度的关系



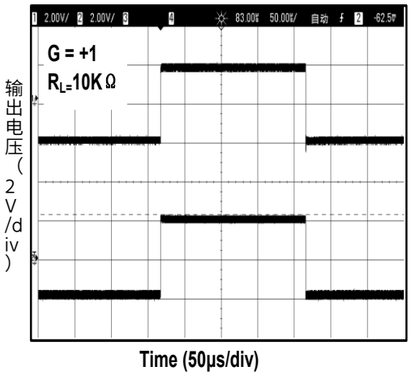
CMRR vs.温度



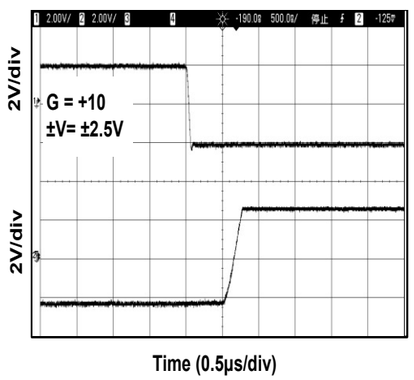
EMIRR IN+ vs.



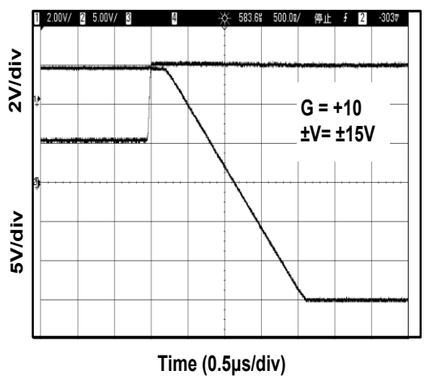
大尺度阶跃响应



负过电压恢复



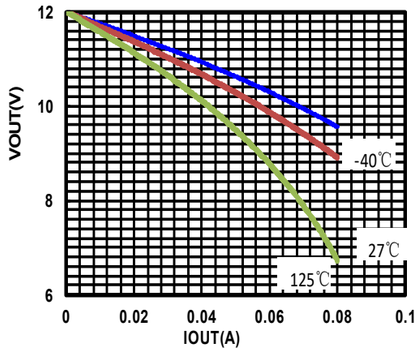
正过压恢复



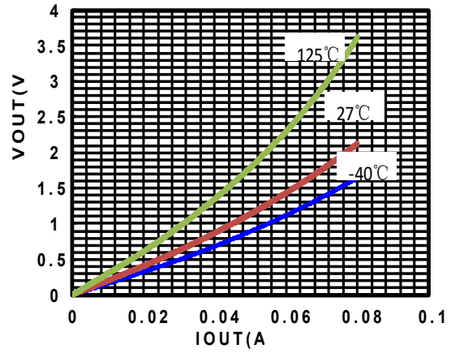
Typical Performance Characteristics

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. (Continued)

Positive Output Swing vs. Load Current



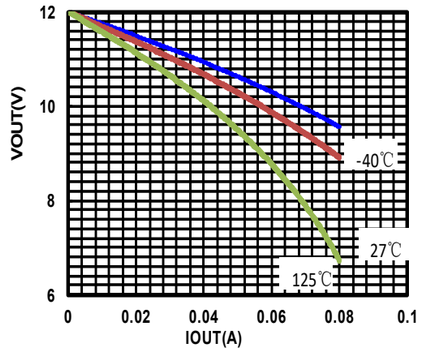
Negative Output Swing vs. Load Current



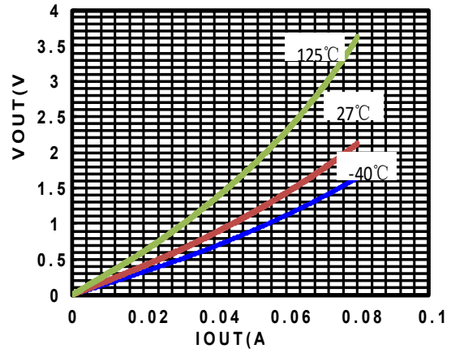
典型性能参数

V S = ±15V，V CM = 0V，R L = Open，除非另有规定。（续）

正输出摆幅与负载电流的关系



负输出摆幅与负载电流



Pin Functions

-IN: Inverting Input of the Amplifier. Voltage range of this pin can go from V^- to (V^+ - 2.0V).

+IN: Non-Inverting Input of Amplifier. This pin has the same voltage range as –IN.

V+ or $+V_S$: Positive Power Supply. Typically the voltage is from 2.7V to 36V. Split supplies are possible as long as the voltage between V+ and V– is between 2.7V and 36V. A bypass capacitor of 0.1µF as close to the part as possible should be used between power supply pins or between supply pins and ground.

V^- or ^-V_S: Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V^+ and V^- is from 2.7V to 36V. If it is not connected to ground, bypass it with a capacitor of 0.1µF as close to the part as possible.

OUT: Amplifier Output. The voltage range extends to within milli-volts of each supply rail.

N/C: No connection.

The exposed thermal pad of DFN package should be left floated.

Operation

The TP227x op-amps have input signal range from V^- to (V^+ – 2.0V). The output can extend all the way to the supply rails. The input stage is comprised of a PMOS differential amplifier. The Class-AB control buffer and output bias stage uses a proprietary compensation technique to take full advantage of the process technology to drive very high capacitive loads. This is evident from the transient over shoot measurement plots in the Typical Performance Characteristics.

Applications Information

EMI Harden

The EMI hardening makes the TP2271/2272/2274 a must for almost all op amp applications. Most applications are exposed to Radio Frequency (RF) signals such as the signals transmitted by mobile phones or wireless computer peripherals. The TP2271/2272/2274 will effectively reduce disturbances caused by RF signals to a level that will be hardly noticeable. This again reduces the need for additional filtering and shielding Using this EMI resistant series of op amps will thus reduce the number of components and space needed for applications that are affected by EMI, and will help applications, not yet identified as possible EMI sensitive, to be more robust for EMI.

Wide Supply Voltage

The TP2271/2272/2274 operational amplifiers can operate with power supply voltages from 2.7V to 36V. Each amplifier draws 0.8mA quiescent current at 36V supply voltage. The TP2271/2272/2274 is optimized for wide bandwidth low power applications. They have an industry leading high GBW to power ratio and the GBW remains nearly constant over specified temperature range.

Low Input Bias Current

The TP2271/2272/2274 is a CMOS OPA family and features very low input bias current in pA range. The low input bias current allows the amplifiers to be used in applications with high resistance sources. Care must be taken to minimize PCB Surface Leakage. See below section on “PCB Surface Leakage” for more details.

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5pA of current to flow,

TP2271 / TP2272 / TP2274

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which is greater than the TP2271/2272/2274 OPA's input bias current at +27°C (±3pA, typical). It is recommended to use multi-layer PCB layout and route the OPA's -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 1 for Inverting Gain application.

1. For Non-Inverting Gain and Unity-Gain Buffer:
   a) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the Common Mode input voltage.
2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op-amp (e.g., V_{DD}/2 or ground).
   b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

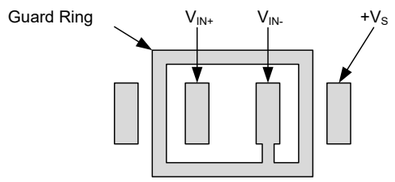


Figure 1 The Layout of Guard Ring

Ground Sensing and Rail to Rail Output

The TP2271/2272/2274 family has excellent output drive capability. It drives 2kΩ load directly with good THD performance. The output stage is a rail-to-rail topology that is capable of swinging to within 50mV of either rail.

The maximum output current is a function of total supply voltage. As the supply voltage to the amplifier increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.3V beyond either supply, otherwise current will flow through these diodes.

Power Supply Layout and Bypass

The TP2271/2272/2274 OPA's power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01μF to 0.1μF) within 2mm for good high frequency performance. It can also use a bulk capacitor (i.e., 1μF or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the OPA's inputs and outputs. To decrease stray capacitance, minimize PC board lengths and resistor leads, and place external components as close to the op amps' pins as possible.

Proper Board Layout

To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads

大于TP 2271/2272/2274 OPA在+27 ° C（± 3 pA，典型值）下的输入偏置电流。 建议使用多层PCB布局，并将OPA的-IN和+IN信号布线在PCB表面下方。

减少表面漏电的有效方法是在敏感引脚（或走线）周围使用保护环。 保护环被偏置在与敏感引脚相同的电压。 图1中显示了这种类型的反相布局示例

增益应用程序。

1. 对于同相增益和单位增益缓冲器：
   a）用不接触PCB表面的导线将同相引脚（V IN +）连接到输入端。
   B）将保护环连接至反相输入引脚（V IN –）。 这会将保护环偏置至共模输入电压。
2. 对于反相增益和跨阻增益放大器（将电流转换为电压，如光电探测器）：
   a）将保护环连接到同相输入引脚（V IN +）。 这将保护环偏置到与运算放大器相同的参考电压（例如， V DD /2或地）。
   B）使用不接触PCB表面的导线将反相引脚（V IN –）连接到输入端。

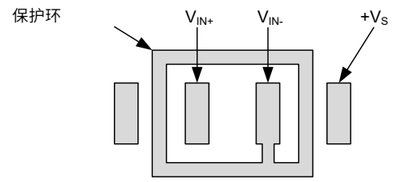


图1保护环布置图

接地检测和轨到轨输出

TP 2271/2272/2274系列具有出色的输出驱动能力。 它直接驱动2k负载，具有良好的THD性能。 输出级采用轨到轨拓扑结构，能够在任一供电轨的50 mV范围内摆幅。

最大输出电流是总电源电压的函数。 随着放大器电源电压的升高， 输出电流能力也增加。 必须注意保持IC的结温低于150°C 当输出连续短路时。 放大器的输出端具有反偏ESD二极管，连接至 每个供应商。“ 输出不应超过任一电源0.3V ，否则电流将流过 这些二极管。

电源布局和旁路

TP 2271/2272/2274 OPA的电源引脚（单电源为V DD）应有一个本地旁路电容（即： 0.01μF至0.1μF），以获得良好的高频性能。 也可以使用大容量电容器（即， 1μF或更大），以提供大而慢的电流。 该大容量电容可与其他模拟器件共享。

接地布局可降低OPA输入和输出端的杂散电容和噪声，从而提高性能。 为降低杂散电容，应尽量减少PC板长度和电阻引线，并将外部元件尽可能靠近运算放大器引脚放置。

正确的主板布局

为确保PCB级的最佳性能，电路板布局设计必须谨慎。 为避免漏电流，电路板表面应保持清洁和无水分。 表面涂层可防止湿气积聚，并有助于降低电路板上的寄生电阻。

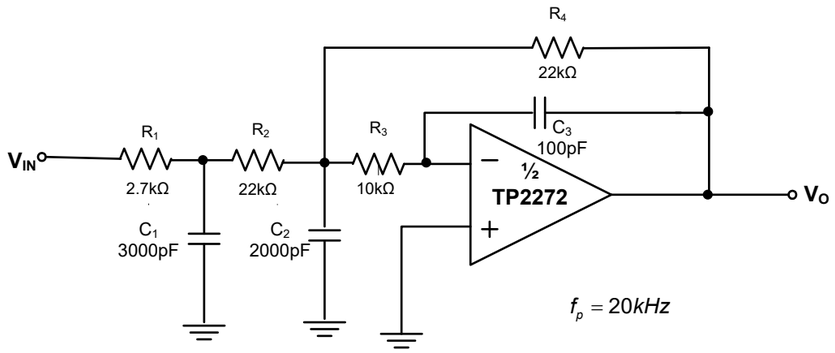
保持电源走线较短并适当旁路电源，可最大限度地降低输出电流变化（例如将交流信号驱动至重负载时）引起的电源干扰。 旁路电容应尽可能靠近器件电源引脚。 杂散电容是放大器输出端和输入端的一个问题。 建议将信号走线与电源线保持至少5 mm的距离，以最大限度地减少耦合。

PCB上的温度变化会导致焊点和其他不同金属接触点处的塞贝克电压不匹配，从而导致热电压误差。 为了最大限度地减少这些热电偶效应，调整电阻器的方向，使热源均匀地加热两端。 输入信号路径应包含匹配数量和类型的元件，尽可能与热电偶结的数量和类型匹配。 例如，零值电阻等虚拟元件可用于匹配相反输入路径中的真实的电阻。匹配元件应靠近放置，且方向应相同。 确保销售线索

36V Single supply, 7MHz Bandwidth, RRO Op-amps

are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

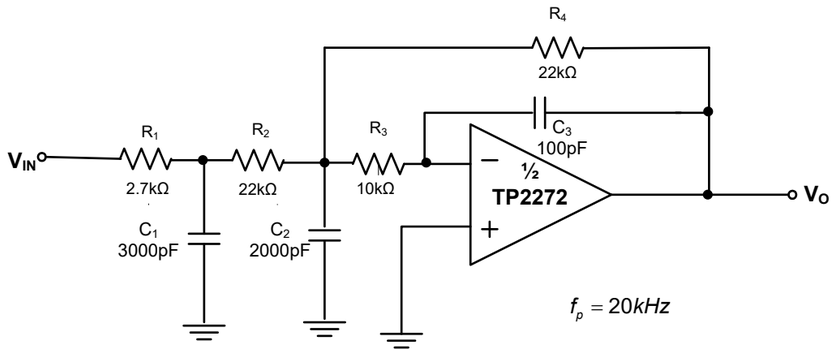


Three-Pole Low-Pass Filter

36V单电源、7MHz带宽、RRO运算放大器

长度相等，因此热传导处于平衡状态。 PCB上的热源应尽可能远离放大器输入电路。

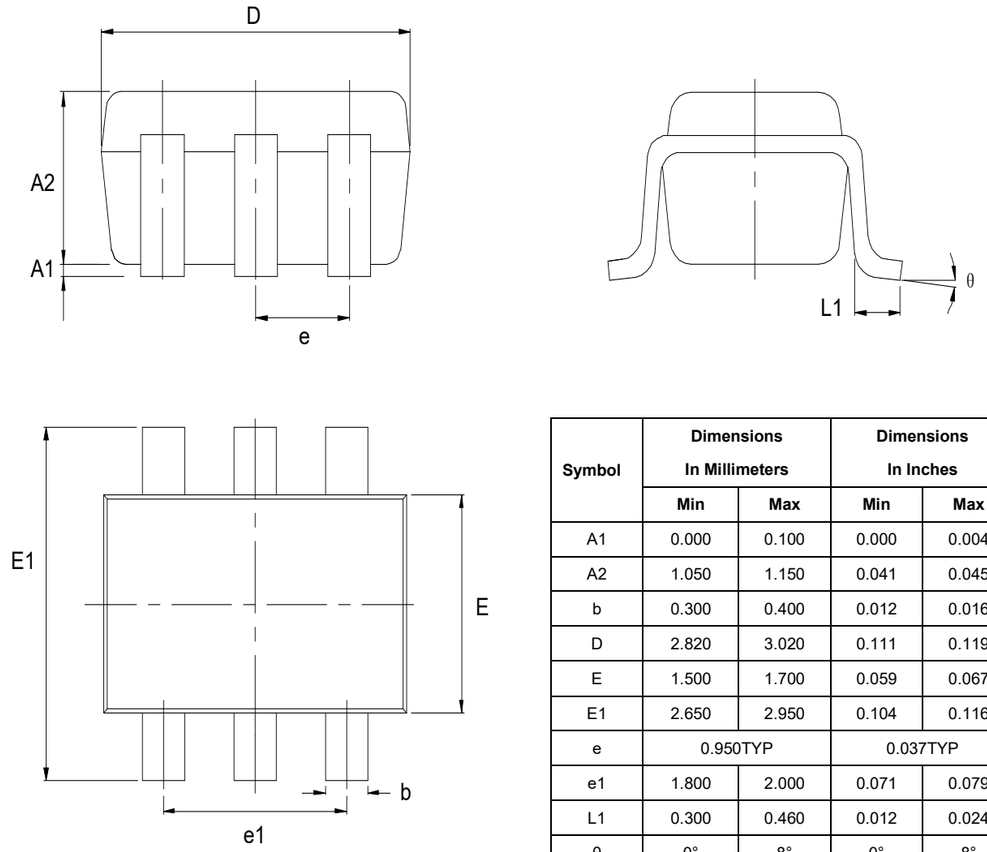
强烈建议使用接地层。 接地层可降低EMI噪声，还有助于保持电路板上的恒定温度。



Three-Pole Low-Pass Filter

Package Outline Dimensions

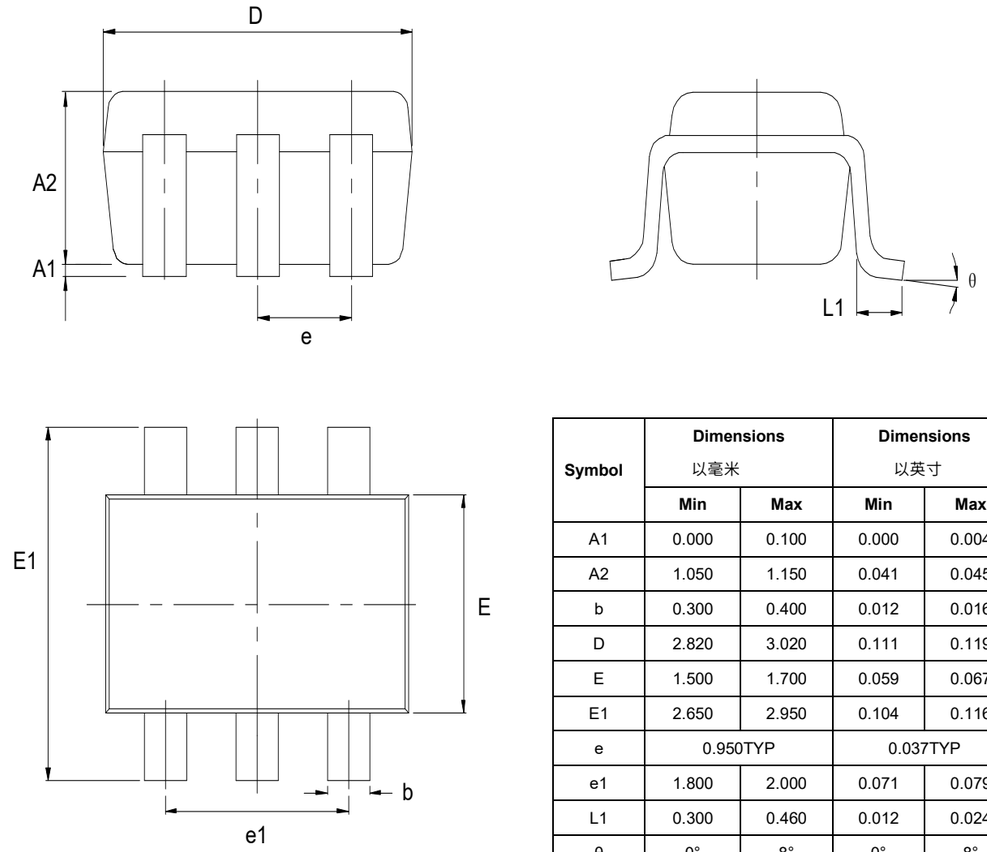
SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L1	0.300	0.460	0.012	0.024
θ	0°	8°	0°	8°

封装外形尺寸

SOT23-5



Symbol	Dimensions 以毫米		Dimensions 以英寸	
	Min	Max	Min	Max
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
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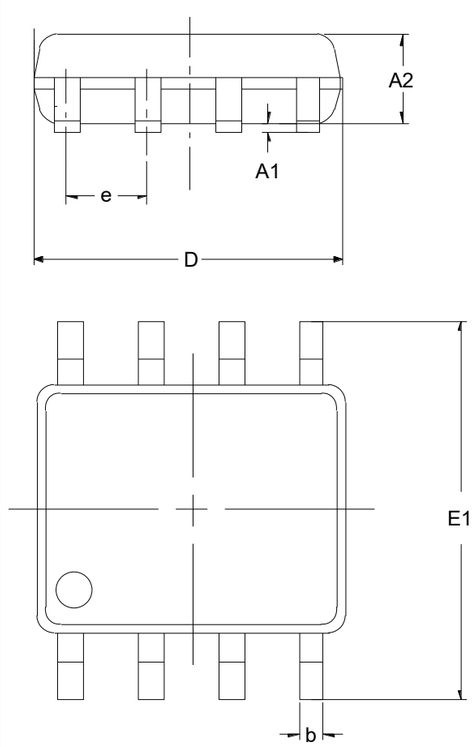
θ	0°	8°	0°	8°

36V Single supply, 7MHz Bandwidth, RRO Op-amps

Package Outline Dimensions

SO-8 (SOIC-8)

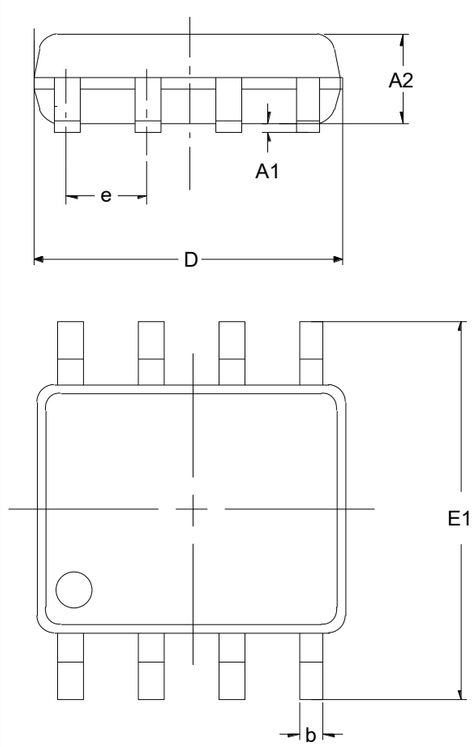


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270 TYP		0.050 TYP	
L1	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

36V单电源、7MHz带宽、RRO运算放大器

封装外形尺寸

SO-8 (SOIC-8)



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	Min	Max	Min	Max
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C	0.190	0.250	0.007	0.010
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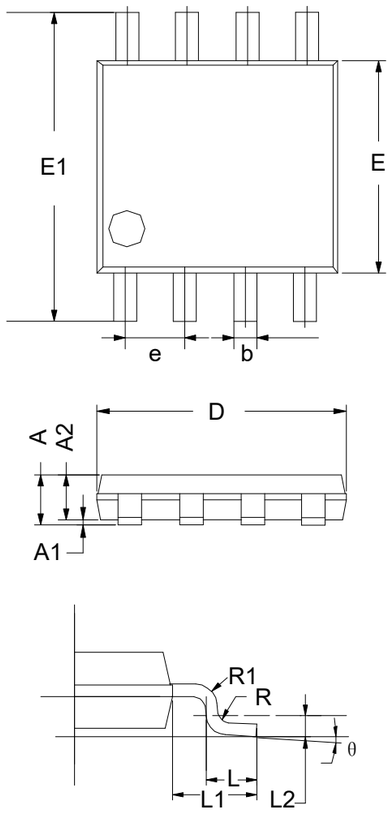
E1	5.800	6.300	0.228	0.248
e	1.270 TYP		0.050 TYP	
L1	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Outline Dimensions

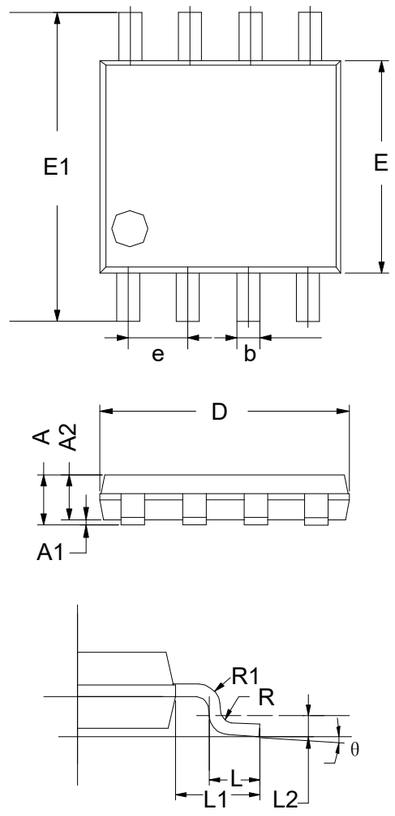
MSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L1	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

封装外形尺寸

MSOP-8



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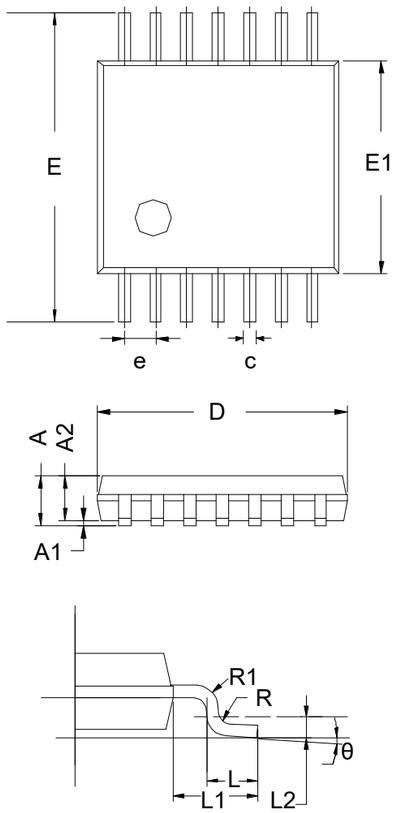
36V Single supply, 7MHz Bandwidth, RRO Op-amps

Package Outline Dimensions

TSSOP-14

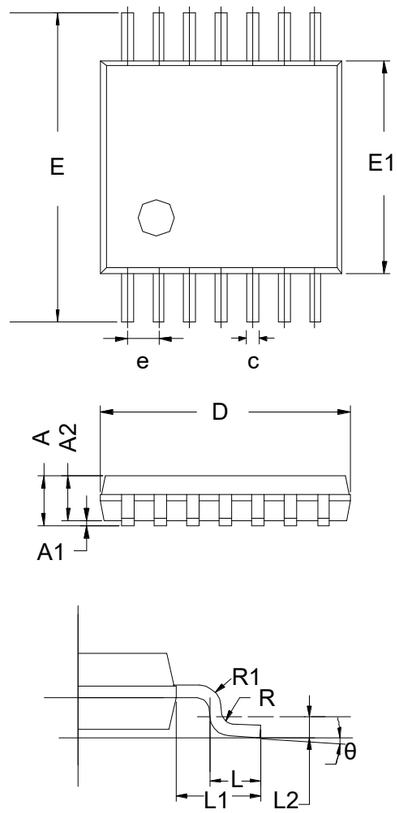


Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
b	0.20	-	0.28
c	0.10	-	0.19
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
R	0.09	-	-
θ	0°	-	8°

36V单电源、7MHz带宽、RRO运算放大器

封装外形尺寸

TSSOP-14



Symbol	Dimensions 以毫米		
	MIN	TYP	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
b	0.20	-	0.28
c	0.10	-	0.19
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
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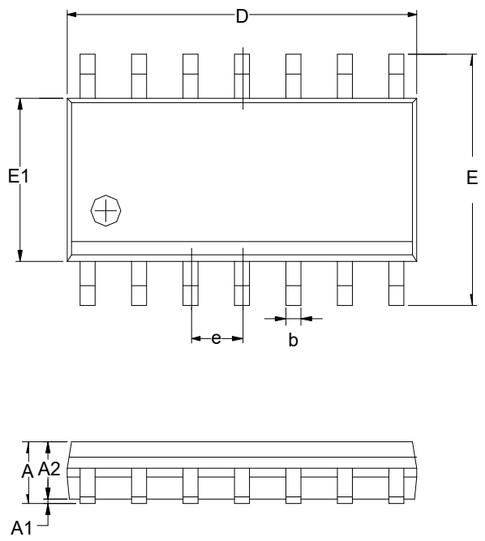
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
R	0.09	-	-
θ	0°	-	8°

Package Outline Dimensions

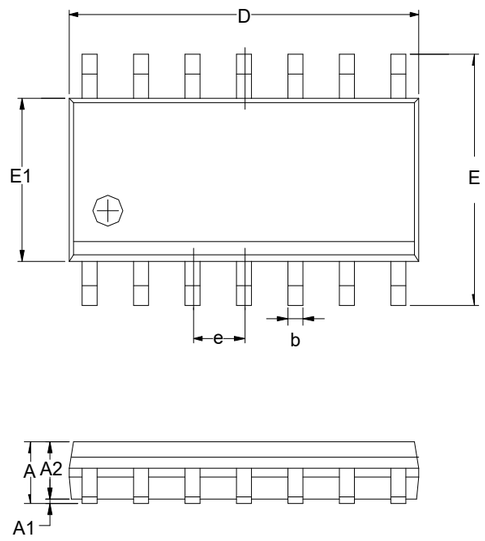
SO-14 (SOIC-14)



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
b	0.36		0.49
D	8.53	8.63	8.73
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25 BSC		
θ	0°		8°

封装外形尺寸

SO-14 (SOIC-14)

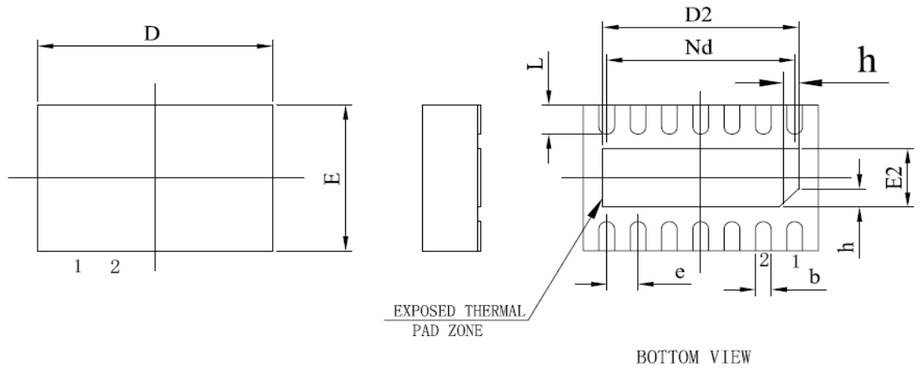


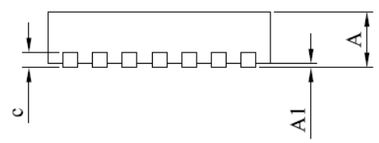
Symbol	Dimensions 以毫米		
	MIN	TYP	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
b	0.36		0.49
D	8.53	8.63	8.73
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25 BSC		
θ	0°		8°

36V Single supply, 7MHz Bandwidth, RRO Op-amps

Package Outline Dimensions

DFN-14



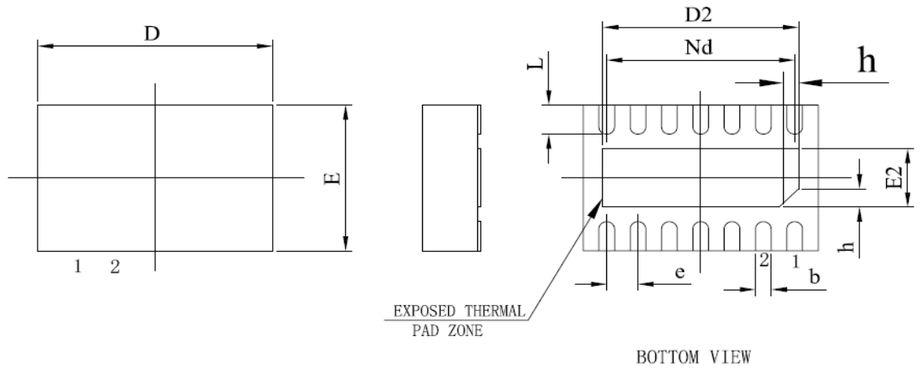


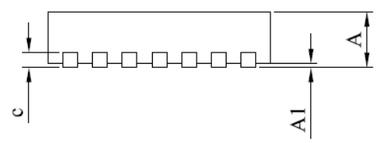
Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	0.7	0.75	0.8
A1		0.02	0.05
b	0.15	0.18	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
e		0.40	
Nd		2.40	
E	1.90	2.00	2.10
E2	0.70	0.80	0.90
L	0.30	0.35	0.40
H	0.20	0.25	0.30

36V单电源、7MHz带宽、RRO运算放大器

封装外形尺寸

DFN-14





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D	2.90	3.00	3.10
D2	2.40	2.50	2.60
e		0.40	
Nd		2.40	
E	1.90	2.00	2.10
E2	0.70	0.80	0.90
L	0.30	0.35	0.40
H	0.20	0.25	0.30