Table of Contents

1. GENERAL DESCRIPTIONS

The W25Q128JV (128M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 1μA for power-down. All devices are offered in space-saving packages.

The W25Q128JV array is organized into 65,536 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q128JV has 4,096 erasable sectors and 256 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See Figure 2.)

The W25Q128JV supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI: Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 and I/O3. SPI clock frequencies of W25Q128JV of up to 133MHz are supported allowing equivalent clock rates of 266MHz (133MHz x 2) for Dual I/O and 532MHz (133MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories.

Additionally, the device supports JEDEC standard manufacturer and device ID and SFDP, and a 64-bit Unique Serial Number and three 256-bytes Security Registers.

2. FEATURES

- **New Family of SpiFlash Memories**
  - W25Q128JV: 128M-bit / 16M-byte
  - Standard SPI: CLK, /CS, DI, DO
  - Dual SPI: CLK, /CS, IO_0, IO_1
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - Software & Hardware Reset(1)
- **Highest Performance Serial Flash**
  - 133MHz Single, Dual/Quad SPI clocks
  - 266/532MHz equivalent Dual/Quad SPI
  - 66MB/S continuous data transfer rate
  - Min. 100K Program-Erase cycles per sector
  - More than 20-year data retention
- **Efficient "Continuous Read"**
  - Continuous Read with 8/16/32/64-Byte Wrap
  - As few as 8 clocks to address memory
  - Allows true XIP (execute in place) operation
- **Low Power, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - <1μA Power-down (typ.)
  - -40°C to +85°C operating range
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector/Block Erase (4K/32K/64K-Byte)
  - Program 1 to 256 byte per programmable page
  - Erase/Program Suspend & Resume
- **Advanced Security Features**
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down
  - Special OTP protection
  - Top/Bottom, Complement array protection
  - Individual Block/Sector array protection
  - 64-Bit Unique ID for each device
  - Discoverable Parameters (SFDP) Register
  - 3X256-Bytes Security Registers with OTP locks
  - Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging**
  - 8-pin SOIC 208-mil
  - 16-pin SOIC 300-mil (additional /RESET pin)
  - 8-pad WSON 6x5-mm / 8x6-mm
  - 24-ball TFBGA 8x6-mm (6x4/5x5 ball array)
  - Contact Winbond for KGD and other options

Note: 1. Hardware /RESET pin is only available on TFBGA or SOIC16 packages

3. PACKAGE TYPES AND PIN CONFIGURATIONS

3.1 Pin Configuration SOIC 208-mil

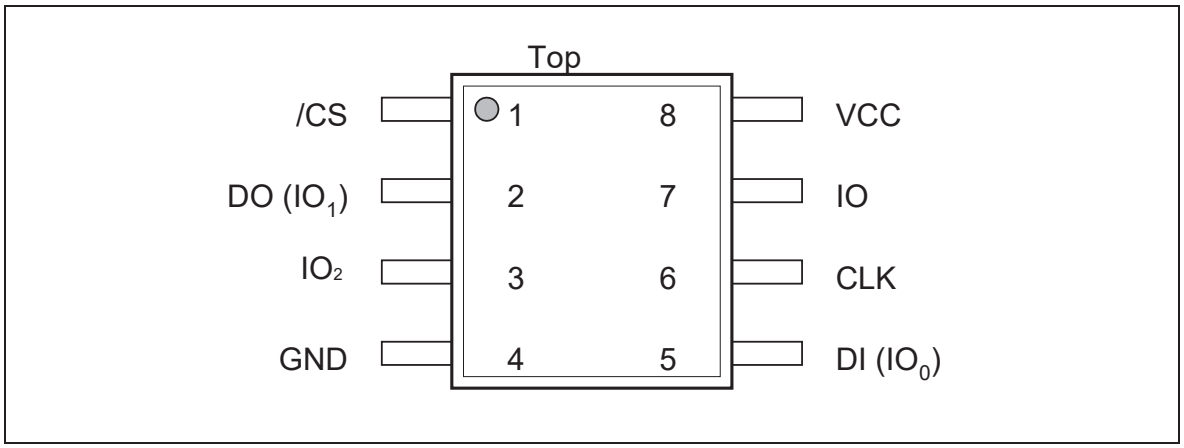

Figure 1a. W25Q128JV Pin Assignments, 8-pin SOIC 208-mil (Package Code S)

3.2 Pad Configuration WSON 6x5-mm/ 8x6-mm

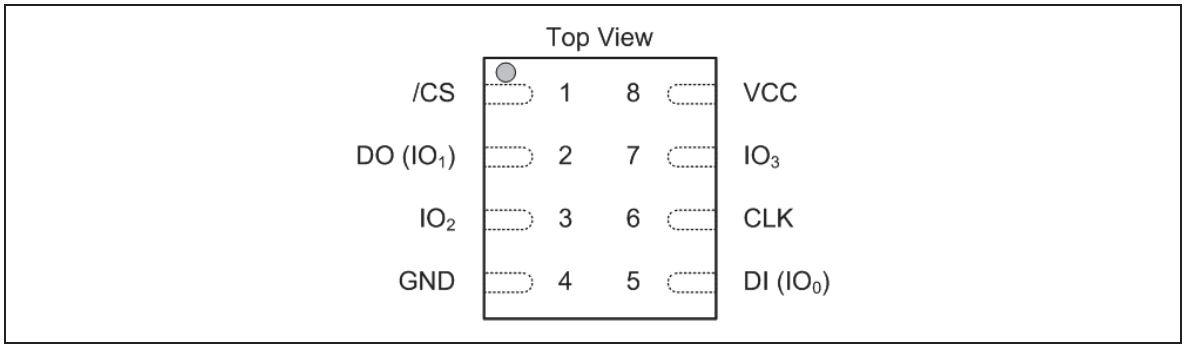

Figure 1b. W25Q128JV Pad Assignments, 8-pad WSON 6x5-mm/ 8x6-mm (Package Code P/E)

3.3 Pin Description SOIC 208-mil, WSON 6x5-mm / 8x6-mm

PAD NO.	PAD NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
3	IO2	I/O	Data Input Output 2(2)
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	IO3	I/O	Data Input Output 3(2)
8	VCC		Power Supply

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions (factory default for Quad Enabled part numbers with ordering option "IQ")

3.4 Pin Configuration SOIC 300-mil

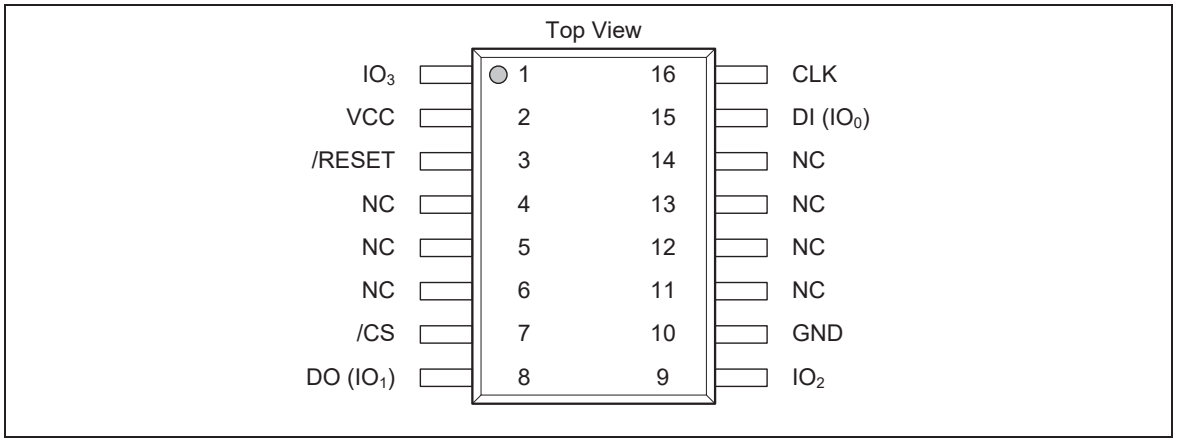

Figure 1c. W25Q128JV Pin Assignments, 16-pin SOIC 300-mil (Package Code F)

3.5 Pin Description SOIC 300-mil

PIN NO.	PIN NAME	I/O	FUNCTION
1	IO3	I/O	Data Input Output 3(2)
2	VCC		Power Supply
3	/RESET	I	Reset Input(3)
4	N/C		No Connect
5	N/C		No Connect
6	N/C		No Connect
7	/CS	I	Chip Select Input
8	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
9	IO2	I/O	Data Input Output 2(2)
10	GND		Ground
11	N/C		No Connect
12	N/C		No Connect
13	N/C		No Connect
14	N/C		No Connect
15	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
16	CLK	I	Serial Clock Input

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions.
3. The /RESET pin is a dedicated hardware reset pin regardless of device settings or operation states. If the hardware reset function is not used, this pin can be left floating or connected to VCC in the system.

3.6 Ball Configuration TFBGA 8x6-mm (5x5 or 6x4 Ball Array)

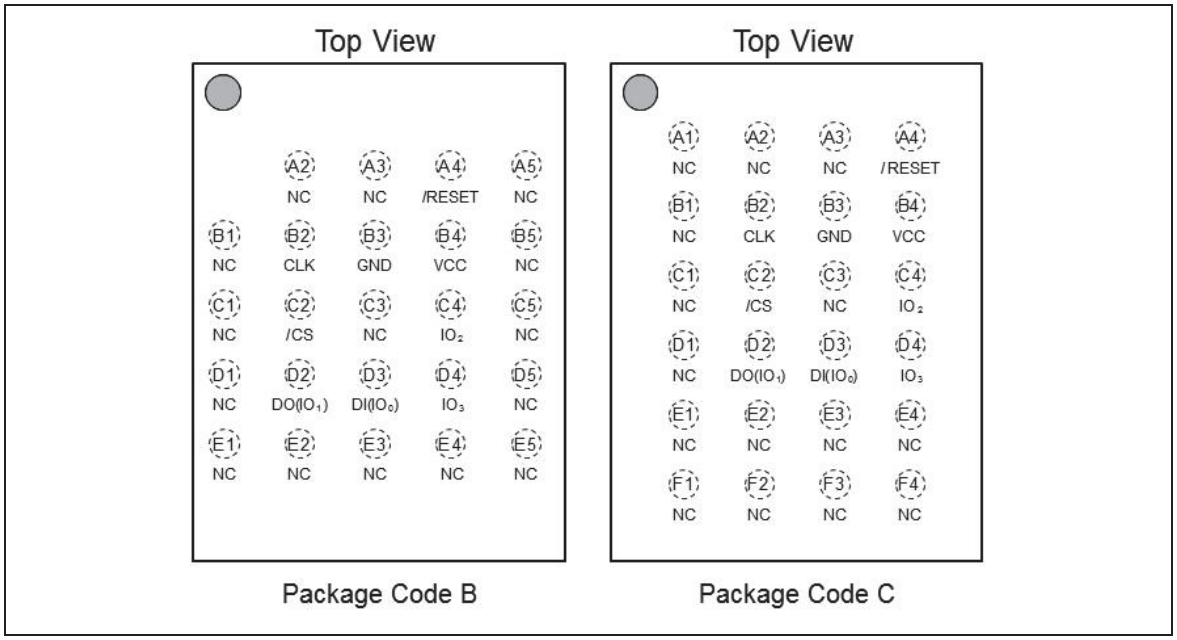

Figure 1d. W25Q128JV Ball Assignments, 24-ball TFBGA 8x6-mm (Package Code B/C)

3.7 Ball Description TFBGA 8x6-mm

BALL NO.	PIN NAME	I/O	FUNCTION
A4	/RESET	I	Reset Input(3)
B2	CLK	I	Serial Clock Input
B3	GND		Ground
B4	VCC		Power Supply
C2	/CS	I	Chip Select Input
C4	IO2	I/O	Data Input Output 2(2)
D2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
D3	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
D4	IO3	I/O	Data Input Output 3(2)
Multiple	NC		No Connect

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions

2. IO0 – IO3 are used for Quad SPI instructions (factory default for Quad Enabled part numbers with ordering option “IQ”).

3. The /RESET pin is a dedicated hardware reset pin regardless of device settings or operation states. If the hardware reset function is not used, this pin can be left floating or connected to VCC in the system

4. PIN DESCRIPTIONS

4.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see “Write Protection” and Figure 58). If needed a pull-up resister on the /CS pin can be used to accomplish this.

4.2 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The W25Q128JV supports Standard SPI, Dual SPI and Quad SPI operation. All 8-bit instructions are shifted into the device through DI (IO0) pin, address and data are shifted in and out of the device through either DI & DO pins for Standard SPI instructions, IO0 & IO1 pins for Dual SPI instructions, or IO0-IO3 pins for Quad SPI instructions.

4.3 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

4.4 Reset (/RESET)

A dedicated hardware /RESET pin is available on SOIC-16 and TFBGA packages. When it’s driven low for a minimum period of ~1µS, this device will terminate any external or internal operations and return to its power-on state.

Note: Hardware /RESET pin is available on SOIC-16 or TFBGA; please contact Winbond for this package.

5. BLOCK DIAGRAM

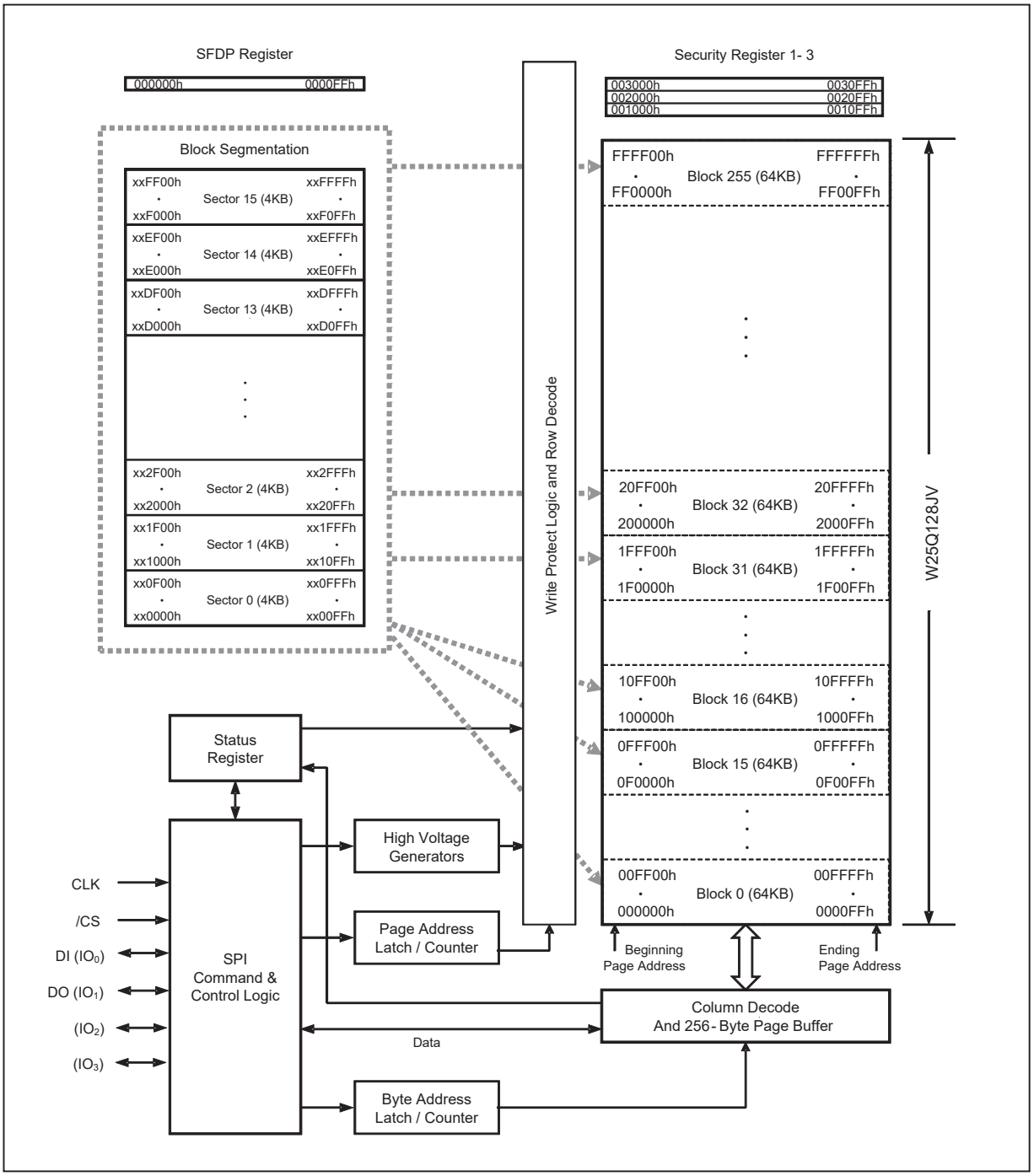

Figure 2. W25Q128JV Serial Flash Memory Block Diagram

6. FUNCTIONAL DESCRIPTIONS

6.1 Standard SPI Instructions

The W25Q128JV is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

6.2 Dual SPI Instructions

The W25Q128JV supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

6.3 Quad SPI Instructions

The W25Q128JV supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, and “Fast Read Quad I/O (EBh). These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the DI and DO pins become bidirectional IO0 and IO1, with the additional I/O pins: IO2, IO3. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

6.4 Software Reset & Hardware /RESET pin

The W25Q128JV can be reset to the initial power-on state by a software Reset sequence. This sequence must include two consecutive instructions: Enable Reset (66h) & Reset (99h). If the instruction sequence is successfully accepted, the device will take approximately 30μS (t_{RST}) to reset. No instruction will be accepted during the reset period. For the SOIC-16 and TFBGA packages, W25Q128JV provides a dedicated hardware /RESET pin. Drive the /RESET pin low for a minimum period of ~1μS (tRESET*) will interrupt any on-going external/internal operations and reset the device to its initial power-on state. Hardware /RESET pin has higher priority than other SPI input signals (/CS, CLK, IOs).

Note:

1. Hardware /RESET pin is available on SOIC-16 or TFBGA; please contact Winbond for his package.
2. While a faster /RESET pulse (as short as a few hundred nanoseconds) will often reset the device, a 1us minimum is recommended to ensure reliable operation.
3. There is an internal pull-up resistor for the dedicated /RESET pin on the SOIC-16 and TFBGA-24 package. If the reset function is not needed, this pin can be left floating in the system.

6.5 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25Q128JV provides several means to protect the data from inadvertent writes.

6.5.1 Write Protect Features

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after erase or program
- Software write protection using Status Registers
- Additional Individual Block/Sector Locks for array protection
- Write Protection using Power-down instruction
- Lock Down write protection for Status Register until the next power-up
- One Time Program (OTP) write protection for array and Security Registers using Status Register*

  * Note: This feature is available upon special order. Please contact Winbond for details.

Upon power-up or at power-down, the W25Q128JV will maintain a reset condition while VCC is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels and Figure 43). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached, and it must also track the VCC supply level at power-down to prevent adverse command sequence. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRL) and Block Protect (CMP, SEC, TB, BP[2:0]) bits. These settings allow a portion or the entire memory array to be configured as read only.

The W25Q128JV also provides another Write Protect method using the Individual Block Locks. Each 64KB block (except the top and bottom blocks, total of 126 blocks) and each 4KB sector within the top/bottom blocks (total of 32 sectors) are equipped with an Individual Block Lock bit. When the lock bit is 0, the corresponding sector or block can be erased or programmed; when the lock bit is set to 1, Erase or Program commands issued to the corresponding sector or block will be ignored. When the device is powered on, all Individual Block Lock bits will be 1, so the entire memory array is protected from Erase/Program. An “Individual Block Unlock (39h)” instruction must be issued to unlock any specific sector or block.

The WPS bit in Status Register-3 is used to decide which Write Protect scheme should be used. When WPS=0 (factory default), the device will only utilize CMP, SEC, TB, BP[2:0] bits to protect specific areas of the array; when WPS=1, the device will utilize the Individual Block Locks for write protection.

7. STATUS AND CONFIGURATION REGISTERS

Three Status and Configuration Registers are provided for W25Q128JV. The Read Status Register-1/2/3 instructions can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, Erase/Program Suspend status, output driver strength, power-up. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting, Security Register OTP locks, and output driver strength. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRL), the Write Enable instruction, and during Standard/Dual SPI operations

7.1 Status Registers

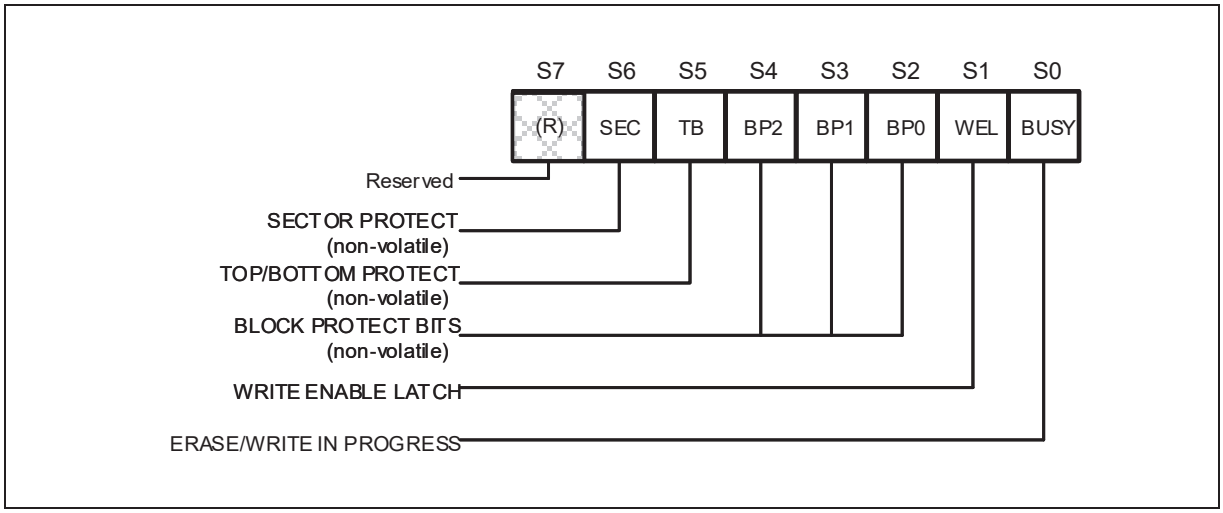

Figure 4a. Status Register-1

7.1.1 Erase/Write In Progress (BUSY) – *Status Only*

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status/security register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

7.1.2 Write Enable Latch (WEL) – *Status Only*

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register.

7.1.3 Block Protect Bits (BP2, BP1, BP0) – *Volatile/Non-Volatile Writable*

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tW in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

7.1.4 Top/Bottom Block Protect (TB) – *Volatile/Non-Volatile Writable*

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP, SRL and WEL bits.

7.1.5 Sector/Block Protect Bit (SEC) – *Volatile/Non-Volatile Writable*

The non-volatile Sector/Block Protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The default setting is SEC=0.

7.1.6 Complement Protect (CMP) – *Volatile/Non-Volatile Writable*

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 64KB block can be protected while the rest of the array is not; when CMP=1, the top 64KB block will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.

7.1.7 Status Register Protect (SRL)

The Status Register Lock bit (SRL) is a volatile/non-volatile read/write bit in the status register (S8). The SRL bit controls the method of write protection to the Status Registers: temporary Power Lock-Down or permanently One Time Program OTP.

SRL	Status Register Lock	Description
0	Non-Lock	Status Registers are unlocked.
1	Power Lock-Down (Temporary/Volatile)	Status Registers are locked and cannot be written to until the next power-down, power-up cycle to reset SRL=0.
	One Time Program(1) (Permanently/Non-Volatile)	A special instruction flow can be used to permanently OTP lock the Status Registers.

Note: Please contact Winbond for details regarding the special instruction sequence.

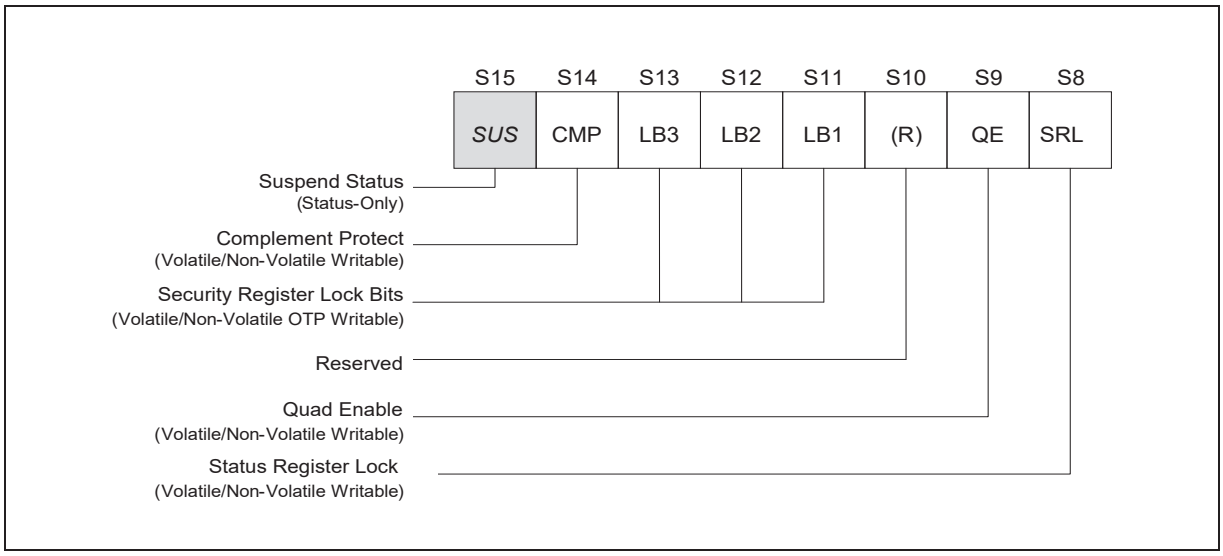

Figure 4b. Status Register-2

7.1.8 Erase/Program Suspend Status (SUS) – *Status Only*

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

7.1.9 Security Register Lock Bits (LB3, LB2, LB1) – *Volatile/Non-Volatile OTP Writable*

The Security Register Lock Bits (LB3, LB2, LB1) are non-volatile One Time Program (OTP) bits in Status Register (S13, S12, S11) that provide the write protect control and status to the Security Registers. The default state of LB3-1 is 0, Security Registers are unlocked. LB3-1 can be set to 1 individually using the Write Status Register instruction. LB3-1 are One Time Programmable (OTP), once it's set to 1, the corresponding 256-Byte Security Register will become read-only permanently.

7.1.10 Quad Enable (QE) – *Volatile/Non-Volatile Writable*

The Quad Enable (QE) bit is set to 1 by default in the factory, therefore the device supports Standard/Dual SPI as well as Quad SPI after power on. This bit cannot be reset to 0.

Note: QE bit is set to a 0 state, factory default for part numbers with ordering options "IM; please see W25Q128JV-DTR data sheet.

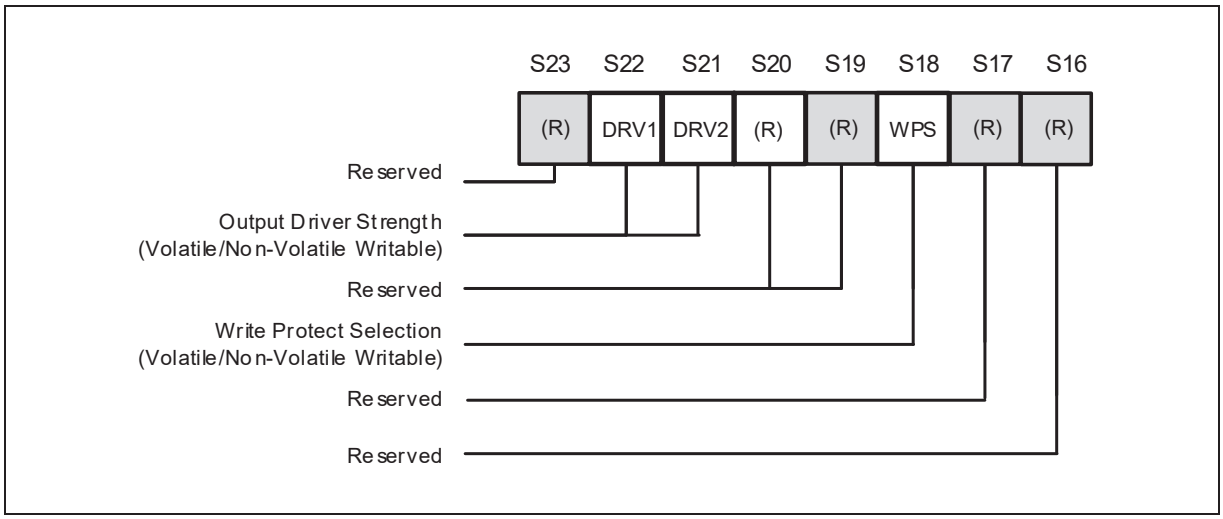

Figure 4c. Status Register-3

7.1.11 Write Protect Selection (WPS) – *Volatile/Non-Volatile Writable*

The WPS bit is used to select which Write Protect scheme should be used. When WPS=0, the device will use the combination of CMP, SEC, TB, BP[2:0] bits to protect a specific area of the memory array. When WPS=1, the device will utilize the Individual Block Locks to protect any individual sector or blocks. The default value for all Individual Block Lock bits is 1 upon device power on or after reset.

7.1.12 Output Driver Strength (DRV1, DRV0) – *Volatile/Non-Volatile Writable*

The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.

DRV1, DRV0	Driver Strength
0, 0	100%
0, 1	75%
1, 0	50%
1, 1	25% (default)

7.1.13 Reserved Bits – *Non Functional*

There are a few reserved Status Register bits that may be read out as a "0" or "1". It is recommended to ignore the values of those bits. During a "Write Status Register" instruction, the Reserved Bits can be written as "0", but there will not be any effects.

7.1.14 W25Q128JV Status Register Memory Protection (WPS = 0, CMP = 0)

STATUS REGISTER[1]					W25Q128JV (128M-BIT) MEMORY PROTECTION[3]			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION[2]
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	252 thru 255	FC0000h – FFFFFFh	256KB	Upper 1/64
0	0	0	1	0	248 thru 255	F80000h – FFFFFFh	512KB	Upper 1/32
0	0	0	1	1	240 thru 255	F00000h – FFFFFFh	1MB	Upper 1/16
0	0	1	0	0	224 thru 255	E00000h – FFFFFFh	2MB	Upper 1/8
0	0	1	0	1	192 thru 255	C00000h – FFFFFFh	4MB	Upper 1/4
0	0	1	1	0	128 thru 255	800000h – FFFFFFh	8MB	Upper 1/2
0	1	0	0	1	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/64
0	1	0	1	0	0 thru 7	000000h – 07FFFFh	512KB	Lower 1/32
0	1	0	1	1	0 thru 15	000000h – 0FFFFFh	1MB	Lower 1/16
0	1	1	0	0	0 thru 31	000000h – 1FFFFFh	2MB	Lower 1/8
0	1	1	0	1	0 thru 63	000000h – 3FFFFFh	4MB	Lower 1/4
0	1	1	1	0	0 thru 127	000000h – 7FFFFFh	8MB	Lower 1/2
X	X	1	1	1	0 thru 255	000000h – FFFFFFh	16MB	ALL
1	0	0	0	1	255	FFF000h – FFFFFFh	4KB	U - 1/4096
1	0	0	1	0	255	FFE000h – FFFFFFh	8KB	U - 1/2048
1	0	0	1	1	255	FFC000h – FFFFFFh	16KB	U - 1/1024
1	0	1	0	X	255	FF8000h – FFFFFFh	32KB	U - 1/512
1	1	0	0	1	0	000000h – 000FFFh	4KB	L - 1/4096
1	1	0	1	0	0	000000h – 001FFFh	8KB	L - 1/2048
1	1	0	1	1	0	000000h – 003FFFh	16KB	L - 1/1024
1	1	1	0	X	0	000000h – 007FFFh	32KB	L - 1/512

Notes:
1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

7.1.15 W25Q128JV Status Register Memory Protection (WPS = 0, CMP = 1)

STATUS REGISTER(1)					W25Q128JV (128M-BIT) MEMORY PROTECTION(3)			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION(2)
X	X	0	0	0	0 thru 255	000000h - FFFFFFh	16MB	ALL
0	0	0	0	1	0 thru 251	000000h - FBFFFFh	16,128KB	Lower 63/64
0	0	0	1	0	0 thru 247	000000h – F7FFFFh	15,872KB	Lower 31/32
0	0	0	1	1	0 thru 239	000000h - EFFFFFh	15MB	Lower 15/16
0	0	1	0	0	0 thru 223	000000h - DFFFFFh	14MB	Lower 7/8
0	0	1	0	1	0 thru 191	000000h - BFFFFFh	12MB	Lower 3/4
0	0	1	1	0	0 thru 127	000000h - 7FFFFFh	8MB	Lower 1/2
0	1	0	0	1	4 thru 255	040000h - FFFFFFh	16,128KB	Upper 63/64
0	1	0	1	0	8 thru 255	080000h - FFFFFFh	15,872KB	Upper 31/32
0	1	0	1	1	16 thru 255	100000h - FFFFFFh	15MB	Upper 15/16
0	1	1	0	0	32 thru 255	200000h - FFFFFFh	14MB	Upper 7/8
0	1	1	0	1	64 thru 255	400000h - FFFFFFh	12MB	Upper 3/4
0	1	1	1	0	128 thru 255	800000h - FFFFFFh	8MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 thru 255	000000h – FFEFFFh	16,380KB	L - 4095/4096
1	0	0	1	0	0 thru 255	000000h – FFDFFFh	16,376KB	L - 2047/2048
1	0	0	1	1	0 thru 255	000000h – FFBFFFh	16,368KB	L - 1023/1024
1	0	1	0	X	0 thru 255	000000h – FF7FFFh	16,352KB	L - 511/512
1	1	0	0	1	0 thru 255	001000h – FFFFFFh	16,380KB	U - 4095/4096
1	1	0	1	0	0 thru 255	002000h – FFFFFFh	16,376KB	U - 2047/2048
1	1	0	1	1	0 thru 255	004000h – FFFFFFh	16,368KB	U -1023/1024
1	1	1	0	X	0 thru 255	008000h – FFFFFFh	16,352KB	U - 511/512

Notes:
1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

7.1.16 W25Q128JV Individual Block Memory Protection (WPS=1)

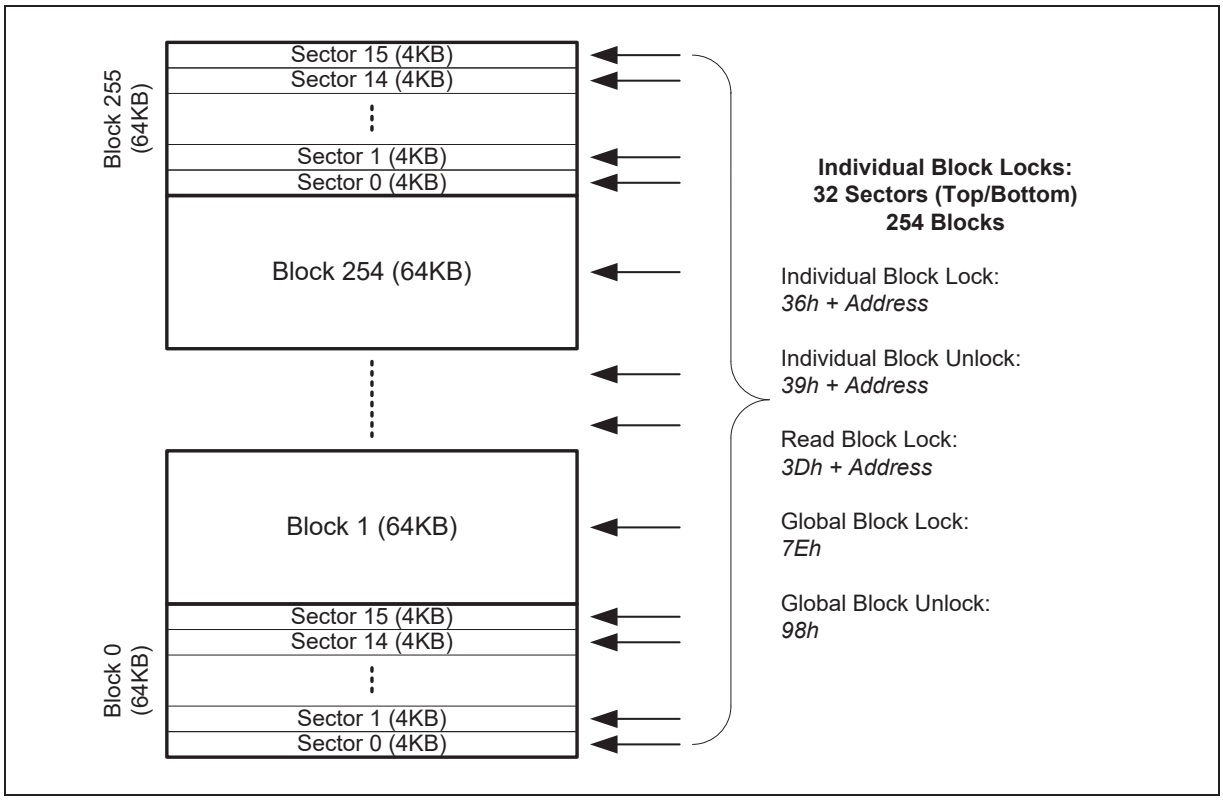

Figure 4d. Individual Block/Sector Locks

Notes:

1. Individual Block/Sector protection is only valid when WPS=1.
2. All individual block/sector lock bits are set to 1 by default after power up, all memory array is protected.