9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings (1)

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to 4.6	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.6 to VCC+0.4	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–2.0V to VCC+2.0V	V
Storage Temperature	TSTG		–65 to +150	°C
Lead Temperature	TLEAD		See Note (2)	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(3)	–2000 to +2000	V

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

9.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage(1)	VCC	F_R = 133MHz, f_R = 50MHz	3.0	3.6	V
		F_R = 104MHz, f_R = 50MHz	2.7	3.0	V
Ambient Temperature, Operating	TA	Industrial	–40	+85	°C

Note:

1. VCC voltage during Read can operate across the min and max range but should not exceed ±10% of the programming (erase/write) voltage.

9.3 Power-Up Power-Down Timing and Requirements

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to /CS Low	t_{VSL}(1)	20		µs
Time Delay Before Write Instruction	t_{PUW}(1)	5		ms
Write Inhibit Threshold Voltage	V_{WI}(1)	1.0	2.0	V

Note:

1. These parameters are characterized only.

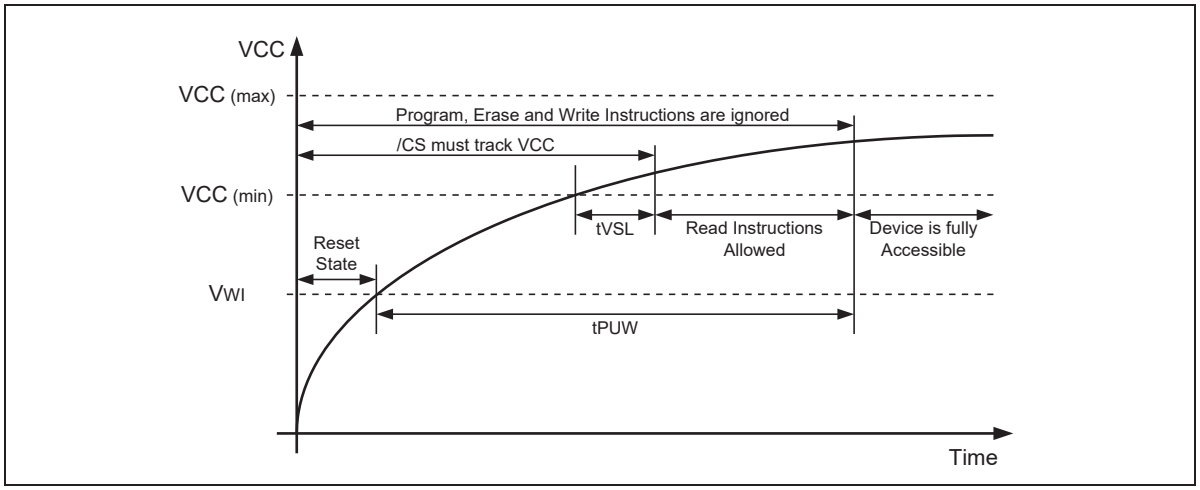


Figure 58a. Power-up Timing and Voltage Levels

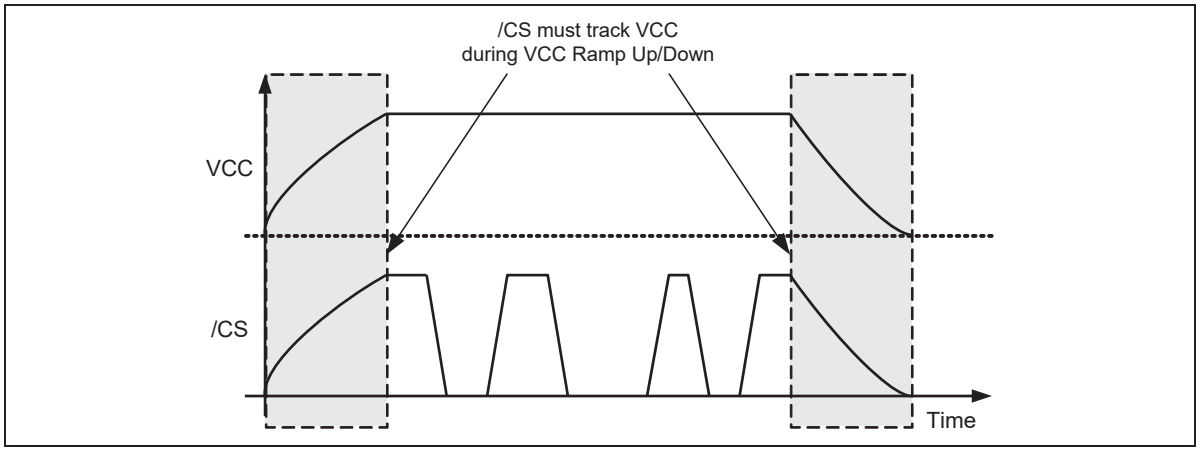


Figure 58b. Power-up, Power-Down Requirement

9.4 DC Electrical Characteristics-

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	C_{IN}(1)	V_{IN} = 0V(1)			6	pF
Output Capacitance	C_{out}(1)	V_{OUT} = 0V(1)			8	pF
Input Leakage	I_{LI}				±2	µA
I/O Leakage	I_{LO}				±2	µA
Standby Current	I_{CC1}	/CS = VCC, VIN = GND or VCC		10	60	µA
Power-down Current	I_{CC2}	/CS = VCC, VIN = GND or VCC		1	20	µA
Current Read Data / Dual /Quad 50MHz(2)	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open			15	mA
Current Read Data / Dual /Quad 80MHz(2)	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open			18	mA
Current Read Data / Dual /Quad 104MHz(2)	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open			20	mA
Current Write Status Register	I_{CC4}	/CS = VCC		20	25	mA
Current Page Program	I_{CC5}	/CS = VCC		20	25	mA
Current Sector/Block Erase	I_{CC6}	/CS = VCC		20	25	mA
Current Chip Erase	I_{CC7}	/CS = VCC		20	25	mA
Input Low Voltage	V_{IL}		–0.5		VCC x 0.3	V
Input High Voltage	V_{IH}		VCC x 0.7		VCC + 0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 100 µA			0.2	V
Output High Voltage	V_{OH}	I_{OH} = –100 µA	VCC – 0.2			V

Notes:

1. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 3.0V.
2. Checker Board Pattern.

9.5 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	C_L		30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

Note:

1. Output Hi-Z is defined as the point where data out is no longer driven.

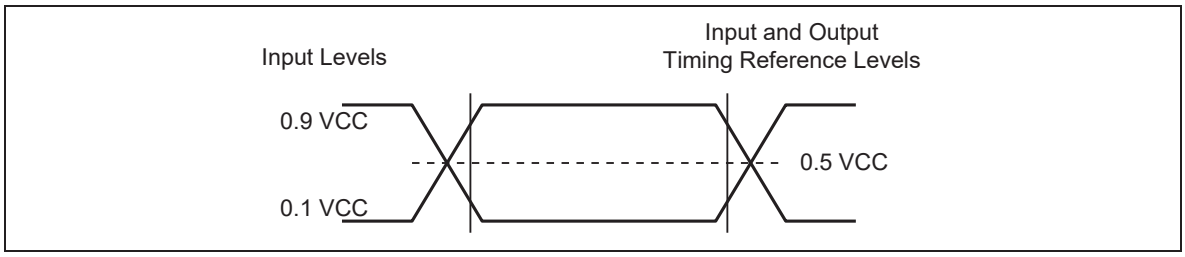


Figure 59. AC Measurement I/O Waveform

9.6 AC Electrical Characteristics(6)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency except for Read Data (03h) instructions (3.0V-3.6V)	F_R	f_{C1}	D.C.		133	MHz
Clock frequency except for Read Data (03h) instructions(2.7V-3.0V)	F_R	f_{C2}	D.C.		104	MHz
Clock frequency for Read Data instruction (03h)	f_R		D.C.		50	MHz
Clock High, Low Time for all instructions except for Read Data (03h)	t_{CLH}, t_{CLL}(1)		45% PC			ns
Clock High, Low Time for Read Data (03h) instruction	t_{CRLH}, t_{CRLL}(1)		45% PC			ns
Clock Rise Time peak to peak	t_{CLCH}(2)		0.1			V/ns
Clock Fall Time peak to peak	t_{CHCL}(2)		0.1			V/ns
/CS Active Setup Time relative to CLK	t_{SLCH}	t_{CSS}	5			ns
/CS Not Active Hold Time relative to CLK	t_{CHSL}		5			ns
Data In Setup Time	t_{DVCH}	t_{DSU}	2			ns
Data In Hold Time	t_{CHDX}	t_{DH}	3			ns
/CS Active Hold Time relative to CLK	t_{CHSH}		3			ns
/CS Not Active Setup Time relative to CLK	t_{SHCH}		3			ns
/CS Deselect Time (for Read)	t_{SHSL1}	t_{CSH}	10			ns
/CS Deselect Time (for Erase or Program or Write)	t_{SHSL2}	t_{CSH}	50			ns
Output Disable Time	t_{SHQZ}(2)	t_{DIS}			7	ns
Clock Low to Output Valid	t_{CLQV}	t_V			6	ns
Output Hold Time	t_{CLQX}	t_{HO}	1.5			ns

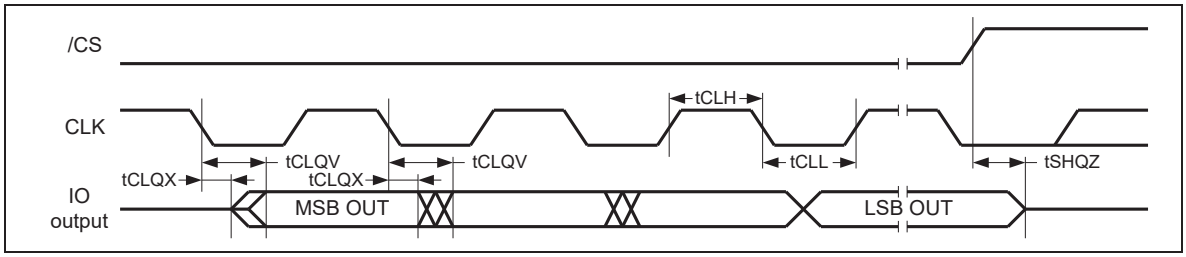
Continued – next page AC Electrical Characteristics (cont'd)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
/CS High to Power-down Mode	t_{DP}(2)				3	µs
/CS High to Standby Mode without ID Read	t_{RES1}(2)				3	µs
/CS High to Standby Mode with ID Read	t_{RES2}(2)				1.8	µs
/CS High to next Instruction after Suspend	t_{SUS}(2)				20	µs
/CS High to next Instruction after Reset	t_{RST}(2)				30	µs
/RESET pin Low period to reset the device	t_{RESET}(2)		1(4)			µs
Write Status Register Time	t_W			10	15	ms
Page Program Time	t_{PP}			0.7	3	ms
Sector Erase Time (4KB)	t_{SE}			45	400	ms
Block Erase Time (32KB)	t_{BE1}			120	1,600	ms
Block Erase Time (64KB)	t_{BE2}			150	2,000	ms
Chip Erase Time	t_{CE}			40	200	s

Notes:

1. Clock high or Clock low must be more than or equal to 45%Pc. Pc = 1/fc(max).
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write Status Register instruction when SRP=1.
4. It's possible to reset the device with shorter t_{RESET} (as short as a few hundred ns), a 1us minimum is recommended to ensure reliable operation.
5. Tested on sample basis and specified through design and characterization data. T_A = 25° C, VCC = 3.0V, 25% driver strength.
6. 4-bytes address alignment for Quad Read

9.7 Serial Output Timing



9.8 Serial Input Timing