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CMS Pixel Upgrade for the Phase I: Module Production and Qualification

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Abstract

The present CMS pixel detector has been designed to be fully efficient up to a LHC luminosity of 10^{34} cm^{-2} s^{-1}. However, the luminosity will increase by a factor of two in the coming years. Therefore it is planned to build and install a new detector in the extended year-end technical stop (YETS) in 2016-17. Barrel pixel modules are in production since Spring/Summer 2015 in five different centers. Module production requires bump bonding, wire bonding and gluing processes to finally assemble a full module. To have a uniform performance of all modules standard qualification procedures have been developed. All modules will be subjected to 10 termal cycles between +17°C and -25°C and then electrically tested. In addition, module performance will be verified under high rate X-rays, and internal calibrate signals used for electrical tests will be calibrated in units of electrons using well defined X-ray fluorescence lines from different target materials. The qualification criteria, based on which modules are selected to be used in the final system, will be explained in details.

Keywords: CMS, Phase I, pixel detector, BPIX, module production

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1. CMS Pixel Upgrade for Phase I

The excellent performance of the Large Hadron Collider (LHC) during Run 1 will allow to achieve the design luminosity of 10^{34} cm^{-2} s^{-1} at 25 ns bunch spacing already in 2015. Under these conditions, CMS will experience

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an average of about 25 inelastic interactions per bunch crossing (pile-up) [1]. Based on this, it is anticipated that a peak luminosity of 2×10^{34} cm^{-2} s^{-1} is reached already before 2018. As a result, CMS should be prepared to operate the rest of this decade with an average pile-up up to and exceeding 50.

The present pixel detector will not sustain these extreme operating conditions. Therefore it is planned to exchange the system with a new device, referred to as the Phase-1 pixel detector [2], during the winter technical stop 2016-2017. This new system will consist of four barrel layers/three disks per side and represents a low mass silicon pixel tracker capable of delivering high tracking performance in the high luminosity environment.

2. BPIX Module Production

The upgraded pixel detector will have 1184 modules in the barrel layers (BPIX) compared to 768 modules in the present detector. The BPIX module (Fig. 1) is equipped with 2×8-Readout Chips (ROC) [3] connected via bump bonding to the silicon sensor forming a detector unit called Bare Module. It has 66560 pixels with a size of $100 \times 150\,\mu\text{m}^2$ each. There is only one type of sensor with n$^+$-in-n technology [4] with dimensions of 16.2×64.8 mm^2 and a thickness of 285 μm.

ROC peripheries with wirebond pads extend 2 mm beyond the sensor along the two long sides of the module. The high density interconnect (HDI) is a printed flexible circuit equipped with passive elements (capacitors and resistors). It is located on top of the sensor with wirebond pads to connect to the corresponding pads on the ROCs. It accepts the data from the ROCs and transmits them to the central data acquisition system. The serialization of the data is perfomed by the token bit manager (TBM) which is a logic chip glued and wirebonded onto the HDI. In addition, the HDI provides the power distribution for the ROCs and the bias voltage to the silicon sensor. Layers 2-4 modules have 200 μm thick Si_3N_4 base-strips glued to the backside of the ROCs which permits mounting the modules on the mechanical structure.

Barrel module production happens at several independent production centers in Switzerland, Italy, Germany and CERN. All components are carefully tested before being used in the module assembly. Completed HDIs with the TBM mounted and bare modules are tested to verify that the HDI and ROCs are still functional and to measure the sensor leakage current and the bump bonding yield of the whole bare module.

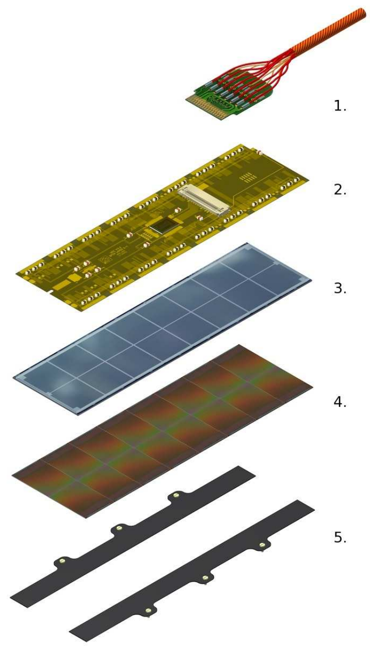

Figure 1: Pixel module components: 1. Signal and power cable, 2. High Density Interconnect + Token Bit Manager, 3. Silicon sensor, 4. Readout chip layer, 5. Base strips (not included in layer 1 modules).

The module assembly procedure comprises two gluing steps. First, a bare module is glued on a set of base strips. The glue is applied via stamps with the appropriate pattern. Afterwards, in a gluing jig previously aligned, both components are joined together. A curing time, depending on the glue characteristics, is needed for a correct assembly. The identical procedure is used for the second gluing step. A HDI is glued onto the top side of a bare module. The dedicated tools designed for this project assure fast and safe operation. They include a precisely machined base-plate and a lifting mechanism equipped with a vacuum system to keep the components in place until the glue has cured. The gluing setup also contains a micro-screw system for alignment to achieve the 50 μm of precision required. Finally, wire bonding to connect the ROCs to the HDI is performed.

3. Pixel Module Qualification

The goal of the module qualification is to verify that all pixels function correctly, that each ROC can be programmed properly, and that all calibrations of a module produce reasonable results. In the following, a brief description of the module tests is provided. A more detailed description can be found in [2].

3.1. Module tests in a cooling box

The full module is subjected to 10 thermal cycles between +17°C and -25°C. This test ensures that the module can be operated at working temperature determining all relevant parameters. The module performance will be checked twice at -20°C (before and after the thermal cycles) and also at +17°C after the thermal cycles. The complete list of tests and the grading are described in the following.

First, the communication with all ROCs is verified and a basic operational state is set by adjusting some of the default settings. For example, the analog current is set to the nominal value of 24 mA by adjusting the corresponding analog voltage. This subtest ensures that the ROC is programmable.

Secondly, the number of pixel defects per ROC is determined from different tests: 1. *Pixel Alive* test to check that each pixel responds to an internal calibrate signal, to the correct pixel address and that pixels can be masked. 2. *Bump-bonding test* to check missing bump connections. 3. Trim bit test to test the functionality of the four trim bits used for threshold unification (*trimming* test). 4. The noise is measured for each pixel as seen in Fig. 2 for a ROC. A pixel is considered noisy if the mean noise is greater than 500 e^-. In addition to the pixel defects listed above, a pixel is counted as defective if the response of the pulse height calibration test is not linear.

A module is graded as *A* if the fraction of pixel defects is less than 1%, graded as *B* if the fraction is in the 1-4% range, and graded as *C* in the case that the number of defects is above 4%.

In a third step, the main characteristics of a module are determined by the following tests: 1. *Trimming* test, as mentioned above, sets the threshold of each pixel to obtain a uniform response over the whole module and, 2. Pulse Height Calibration to stablish the dependency of the pulse height amplitude on the injected charge. Missing charge has an impact on the hit resolution. The charge information depends on the pixel threshold and on the pulse height calibration [2].

Finally, the sensor leakage current versus bias voltage is measured to detect eventual sensor damage during assembly. The current at 150 V and at T=+17°C should not exceed 2 μA to be grade *A*. If the current is less than 10 μA, the grade will be *B*. Otherwise, the module will be graded as *C*.

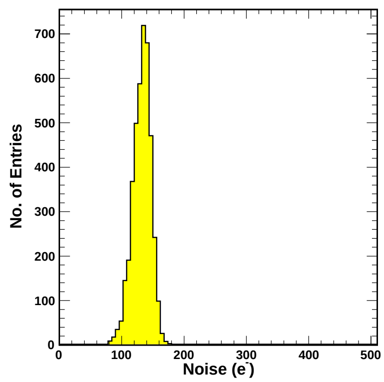

Figure 2: Noise measured for all the 4160 pixels in a ROC. The distribution shows a mean noise of 132 e^-.

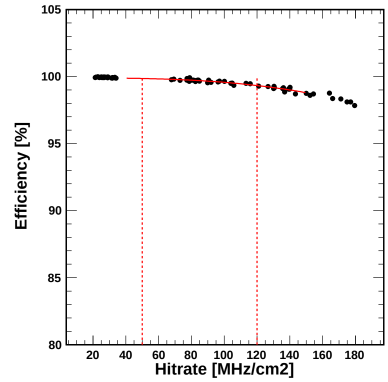

Figure 3: Efficiency versus the hit rate for a ROC. The efficiency at 50 and 120 MHz/cm^2 is interpolated. Each point corresponds to one double column.

To ensure reasonable behaviour at operating voltages, the ratio between the current at 150 V and 100 V should be less than 2. Otherwise, the module will be graded as *B*.

3.2. Module tests and calibration with X-rays

Module tests with X-rays allow to verify the module response to an external charge injected to the silicon sensor at high rates and check the readout chain performance. The pixel hit efficiency versus hit rate is measured for every ROC in a module as seen in Fig 3. The efficiency is interpolated from two hit rates (50 and 120 MHz/cm^2) and used for grading the module. The efficiency should be greater than 98% to be a grade *A* module and should not be less than 95% to be graded as *B*.

In addition, it is needed to calibrate the internal calibration signal from electronic units to electrons. This will be done using a primary X-ray source and different target materials with well defined fluorescence lines (e.g. Zn (8639 eV), Mo (17479 eV), Ag (22163 eV) and Sn(25272 eV)). The spectrum measured for every target is fitted by a gaussian function in order to get the mean of the pulse height corresponding to the fluorescence line. Then an absolute calibration curve can be determined. This curve relates the charge generated in the silicon sensor to the measured signal in the detector. The parameters of a linear fit quantify the ratio between the electronic unit (V_{cal}) and collected charge. Figure 4 shows a slope of 50.91 e^- per V_{cal}.

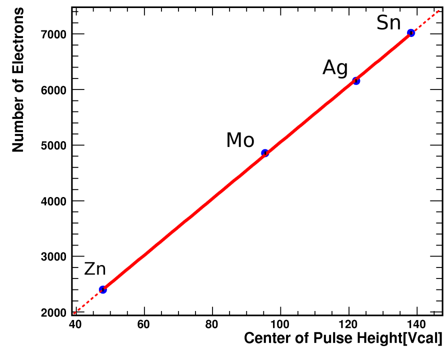

Figure 4: Energy charge calibration of internal pulses using different fluorescence target materials. The pulse height in V_{cal} is compared to the number of electrons produced in silicon, based on literature values of the corresponding lines.

4. Conclusions

The BPIX module production is well advanced. Bare modules of high quality are produced and tested in all production centers. The module qualification procedure is already defined at the time of writing. In addition to the High Rate Test and V_{cal} Calibration, the final programme of X-ray tests includes the identification of pixel defects and hot pixels. The double column readout uniformity is also checked. The analysis of test results is fully automated with a dedicated software integrated in a database.

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