LAB 2

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Problem

Use the following code fragment:

loop: LD R1,0(R2)

DADDI R1,R1,1

SD 0(R2),R1

DADDI R2,R2,4

DSUB R4,R3,R2

BNEZ R4,loop

Assume that the initial value of R3 is R2+396. Throughout this exercise use the classic RISC five-stage integer pipeline in H&P. Specifically, assume that:

1) branches are resolved in the second stage of the pipeline;
2) there are separate instruction and data memories;
3) all memory accesses take 1 clock cycle.

a. Show the timing of this instruction sequence for the RISC pipeline without any forwarding or bypassing hardware but assuming a register read and a write in the same clock cycle "forwards" through the register file. Assume that the branch is handled by flushing the pipeline. If all memory references take 1 cycle, how many cycles does this loop take to execute?

Clock Cycle	1	2	3	4	5	6	7	8	9	10	11	12
1: LD R1	IF	ID	EX	MEM	WB							
2: DADDI		IF	ID	stall	stall	EX	MEM	WB				
3: SD			IF	ID	stall	stall	stall	stall	EX	ME	WB	
4: DADDI				IF	ID	EX	ME	WB				
5: DSUB					IF	ID	stall	stall	EX	ME	WB	
6: BNEZ						IF	ID	stall	stall	stall	stall	EX
7: Next Seq							IF	stall	stall	stall	stall	Flush

Cycles per Loop Iteration: **12 cycles**

b. Show the timing of this instruction sequence for the RISC pipeline with normal forwarding and bypassing hardware. Assume that the branch is handled by predicting it as not taken. If all memory references take 1 cycle, how many cycles does this loop take to execute?

Full Forwarding: Results from EX/MEM stages are available to be forwarded to the EX/ID stages of subsequent instructions to minimize stalls.

Load-Use Hazard: A 1-cycle stall still occurs if an instruction needs the result of a LD in the immediately following cycle

Predict-Not-Taken: The pipeline assumes the branch (BNEZ) will not be taken and fetches the next sequential instruction

Clock Cycle	1	2	3	4	5	6	7	8
1: LD	IF	ID	EX	ME	WB			
2: DADDI		IF	ID	stall	EX	ME	WB	
3:SD			IF	ID	EX	ME	WB	
4: DADDI				IF	ID	EX	ME	WB
5: DSUB					IF	ID	EX	ME
6: BNEZ						IF	ID	EX
7: Next Seq							IF	Flush

Cycles per Loop Iteration: **8 cycles**

c. Assume the RISC pipeline with a single-cycle delayed branch and normal forwarding and bypassing hardware. Schedule the instructions in the loop including the branch delay slot. You may reorder instructions and modify the individual instructions operands, but do not undertake other loop transformations that change the number or opcode of the instructions in the loops. Show a pipeline timing diagram and compute the number of cycles needed to execute the entire loop.

Scheduled Code

loop: LD R1, 0(R2)

DADDI R1, R1, 1

DSUB R4, R3, R2

SD 0(R2),

BNEZ R4, loop

DADDI R2, R2, 4

Clock Cycle	1	2	3	4	5	6	7
1: LD	IF	ID	EX	ME	WB		
2: DADDI		IF	ID	stall	EX	ME	WB
5: DSUB			IF	ID	EX	ME	WB
3: SD R1				IF	ID	EX	ME
6: BNEZ					IF	ID	EX
4: DADDI						IF	ID
7: LD (loop)						IF	