MOSFET Optimization in Deep Submicron Technology for Charge Amplifiers

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***Abstract*—The optimization of the input MOSFET for charge amplifiers in deep submicron technologies is discussed. After a review of the traditional approach, the impact of properly modeling the equivalent series noise and gate capacitance of the MOSFET is presented. It is shown that the enhanced MOSFET model, when compared to the classical, produces a different resolution estimate and input MOSFET optimization result. The minimum channel length and the maximum allocated power are not always the best choice in terms of resolution. Also, in an optimized front-end, the low frequency noise contribution to the Equivalent Noise Charge may depend on the time constant of the filter. As an example, results from the commercial TSMC 0.25 μm CMOS technology are reported.**

***Index Terms*—Charge amplifier, CMOS, MOSFET.**

I. Introduction

APPLICATION specific integrated circuits (ASICs) can be a valuable solution in front-end electronics for radiation sensors. Detection systems with high sensor pixellation can benefit from low power, low parasitics, high front-end channel density, and low cost per channel. In addition the ASICs are characterized by good radiation tolerance [1]–[3] and can integrate large amount of additional signal processing and functions in analog, mixed-signal and digital domains, thus offering further advantage in terms of power and area.

In a properly designed front-end, the resolution is limited by the noise from the input transistor. Consequently a relevant phase of the design consists of optimizing the input MOSFET with respect to sensor, interconnects and the specific application. The choice of the optimum polarity (n- or p-channel), size (length L and width W) and operating point (drain current density $\mathrm{J_d}$ and drain-to-source voltage $\mathrm{V_{ds}}$) is determinant in achieving the best performance. The optimization process relies on equations, models, and parameters that can be strongly dependent on the technology. As deep submicron CMOS technologies are developed and characterized for digital design, the process of optimizing the input MOSFET can become very challenging. This contribution would like to provide low-noise front-end designers with techniques to keep pace with the rapid evolution of CMOS technology.

After a review of the traditional optimization process, the impact of properly modeling the series noise and gate capacitance of the MOSFET is discussed. It is shown that the enhanced MOSFET model, when compared to the classical, produces a different resolution estimate and input MOSFET optimization result. As an example, the commercial TSMC 0.25 μm CMOS technology is characterized and investigated for the best achievable resolution.

Manuscript received October 30, 2004; revised April 5, 2005 and August 24, 2005. This work was supported by the US Department of energy, Contact no. DE-AC0298CH10886.

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Digital Object Identifier 10.1109/TNS.2005.862938

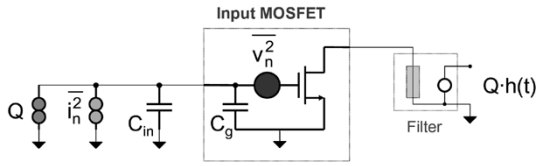


Fig. 1. Schematic of the front-end. The components relevant to the evaluation of the ENC are shown.

II. The ENC Equation

The resolution of a front-end can be measured in terms of equivalent noise charge (ENC) [4]–[7]. The ENC corresponds to the charge that must be delivered to the front-end in order to achieve an output signal-to-noise ratio equal to the unity.

In the following we will assume that the resolution of the front-end is dominated by the noise from the input MOSFET, characterized by a gate length L, a gate width W, and a drain current density $\mathrm{J_d} = \mathrm{I_d}/\mathrm{W}$. We will also assume that the front-end implements a time invariant filter with overall pulse response to a charge Q equal to $\mathrm{Q} \cdot \mathrm{h(t)}$, and characterized by a maximum $\mathrm{Q} \cdot \mathrm{h(t)}|_{\max}$.

In Fig. 1 a schematic of the front-end for the evaluation of the ENC is shown. The parallel noise contribution $\overline{\mathrm{i_n^2}}$, characterized by a unilateral power spectral density $\mathrm{S_{in}}$, is typically related to the sensor leakage current, to its bias circuitry and to the charge amplifier feedback circuitry. In the following, we will initially assume a white density $\mathrm{S_{in}} = \mathrm{S_p}$. Later, since this contribution is not relevant to the optimization of the input MOSFET, this term will be neglected. The series noise contribution $\overline{\mathrm{v_n^2}}$, characterized by a unilateral power spectral density $\mathrm{S_{vn}}$, is dominated by noise processes in the input MOSFET. In the following, we will initially assume a density $\mathrm{S_{vn}} = \mathrm{A}_f/f + \mathrm{S_w}$ where A_f is the amplitude coefficient of the $1/f$ noise, and it is dependent on the technology. The white term is related to the transconductance $\mathrm{g_m}$ of the MOSFET. The input capacitance $\mathrm{C_{in}}$ includes the sensor capacitance, the feedback capacitance, and any parasitic connected to the input node not dependent on the size (W,L) of the input MOSFET. The gate capacitance $\mathrm{C_g}$ includes any term dependent on the size (W and/or L) of the input MOSFET.

The ENC can be expressed as follows:

$$\mathrm{ENC}^2 = \frac{\frac{1}{2\pi}\int_0^\infty \left[\mathrm{S_{in}}|\mathrm{H(j\omega)}|^2 + (\mathrm{C_{in}}+\mathrm{C_g})^2\,\omega^2\mathrm{S_{vn}}|\mathrm{H(j\omega)}|^2\right]\mathrm{d}\omega}{\mathrm{h(t)}|^2_{\max}} \quad (1)$$

where H(s) is the Laplace transform of the pulse response h(t). Introducing the typical spectral densities previously discussed, the ENC can be written as shown in (2) at the bottom of the page, where the time is normalized to an arbitrary time constant τ, and $\tau \cdot \mathrm{H}(\mathrm{s}\tau)$ is the Laplace transform of $\mathrm{h}(\mathrm{t}/\tau)$. Substituting the pulse peaking time τ_p, calculated from 1% to the peak, into (2), yields

$$\mathrm{ENC}^2 = (\mathrm{C_{in}} + \mathrm{C_g})^2 \left[\frac{\mathrm{S_w}}{\tau_\mathrm{p}}\mathrm{a_w} + \mathrm{A}_f 2\pi \mathrm{a}_f\right] + \mathrm{S_p}\tau_\mathrm{p}\mathrm{a_p} \quad (3)$$

where the three ENC coefficients

$$\mathrm{a_w} = \frac{\int_0^\infty |\mathrm{H(jx)}|^2 \mathrm{x}^2 \mathrm{dx}}{2\pi \cdot \mathrm{h}(\mathrm{t}/\tau_\mathrm{p})|^2_{\max}}, \quad \mathrm{a}_f = \frac{\int_0^\infty |\mathrm{H(jx)}|^2 \mathrm{x dx}}{2\pi \cdot \mathrm{h}(\mathrm{t}/\tau_\mathrm{p})|^2_{\max}},$$
$$\mathrm{a_p} = \frac{\int_0^\infty |\mathrm{H(jx)}|^2 \mathrm{dx}}{2\pi \cdot \mathrm{h}(\mathrm{t}/\tau_\mathrm{p})|^2_{\max}} \quad (4)$$

depend only on the type of filter, and H(jx) is obtained by substituting ω with $\mathrm{x}/\tau_\mathrm{p}$ in $\mathrm{H}(\mathrm{j}\omega\tau_\mathrm{p})$. In Table I the coefficients for some commonly adopted time invariant filters are reported, along with the ratio between the pulsewidth τ_w, calculated from 1% amplitude before peak to 1% after peak, and the peaking time τ_p, calculated from 1% to the peak. The R-type filters have real coincident poles only while the C-type filters, commonly adopted in commercial discrete shapers, have complex conjugate poles [8]. The order of the filters in Table I ranges from 2nd to 7th. It can be observed that, as the order increases, the ratio $\tau_\mathrm{w}/\tau_\mathrm{p}$ decreases making the high-order filters more suitable for high rate applications. Also, at equal order, the C-type filters offer a better $\tau_\mathrm{w}/\tau_\mathrm{p}$ ratio than the R-type filters. Finally, the advantage of zero area for bipolar filters, which in absence of effective baseline stabilization at high rate can be relevant, is compensated by worse values in the series coefficients $\mathrm{a_w}$ and a_f, especially for high orders.

Without loss of generality we will simplify our analysis by assuming $\mathrm{a_w} = 1, \mathrm{a}_f = 0.5$, and $\mathrm{a_p} = 0.5$, which are close to the typical values for a good time invariant unipolar shaper.

In the rest of the analysis the parallel noise contribution $\mathrm{S_p}$, not relevant for the optimization of the input MOSFET, will be neglected, and the general expression for the ENC in (3) will be simplified as follows:

$$\mathrm{ENC}^2 = (\mathrm{C_{in}} + \mathrm{C_g})^2 \left[\frac{\mathrm{S_w}}{\tau_\mathrm{p}} + \pi \mathrm{A}_f\right]. \quad (5)$$

III. Constraints, Variables and Models

The input MOSFET must be optimized for the minimum ENC. The ENC depends on some parameters not related to the input MOSFET, specifically the input capacitance $\mathrm{C_{in}}$, the peaking time τ_p, and the maximum power $\mathrm{P_{d\_max}}$ allocated to the input MOSFET. Typically the input capacitance $\mathrm{C_{in}}$ is set by the sensor and interconnects, the maximum power $\mathrm{P_{d\_max}}$ depends on system level constraints, and the peaking time τ_p is set to satisfy requirements on pulse rate or signal formation time in the detector. In the presence of nonnegligible parallel noise contribution a further constraint on the peaking time may occur.

The typical optimization process consequently assumes $\mathrm{C_{in}}, \tau_\mathrm{p}$, and $\mathrm{P_{d\_max}}$ as constraints. One further constraint results from the use of a single supply $\mathrm{V_{dd}}$

$$\mathrm{I_d} = \frac{\mathrm{P_d}}{\mathrm{V_{dd}}} \Rightarrow \mathrm{J_d} = \frac{\mathrm{I_d}}{\mathrm{W}} \quad (6)$$

where $\mathrm{J_d}$ is the MOSFET drain current density. The relation shown in (6) establishes a constraint on the $\mathrm{J_d} \times \mathrm{W}$ product. It follows that, once $\mathrm{C_{in}}, \tau_\mathrm{p}$, and $\mathrm{P_d}$ are defined, the ENC depends only on two the variables W (or $\mathrm{J_d}$) and L and on the polarity (n- or p- channel) of the input device. The optimization process will consequently return the two optimum values $\mathrm{W_{opt}}$ (or $\mathrm{J_{d\_opt}}$) and $\mathrm{L_{\_opt}}$ that give the minimum ENC ($\mathrm{ENC_{opt}}$).

In order to proceed with the optimization of the input MOSFET, the parameters $\mathrm{C_g}, \mathrm{S_w}$ and A_f must be expressed as functions of W (or $\mathrm{J_d}$) and L. In the following sections, the modeling of these parameters will be discussed, starting from the solution that the CMOS designers frequently adopted in the past, before the advent of the deep submicron CMOS technologies.

IV. Classical (C) Model $\mathrm{C_G}, \mathrm{S_W}$, and A_f

In the past, the front-end designers frequently adopted the following models [9]–[13]

$$\mathrm{C_g} = \mathrm{C_{ox}WL}, \quad \mathrm{S_w} = \frac{2}{3}\frac{4\mathrm{kT}}{\mathrm{g_m}(\mathrm{J_d}, \mathrm{L})}, \quad \mathrm{A}_f = \frac{\mathrm{K}_f}{\mathrm{C_{ox}WL}} \quad (7)$$

where $\mathrm{C_{ox}}$ is the oxide capacitance per unit of area, k is Boltzmann's constant, T is the absolute temperature, $\mathrm{g_m}$ is the MOSFET transconductance dependent on $\mathrm{J_d}$ and L, and K_f is the $1/f$ noise coefficient. We will refer to this model as C-model.

Substituting (7) in (5) produces

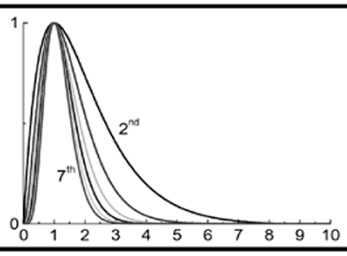
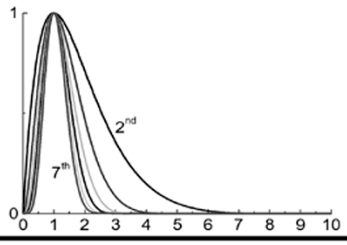
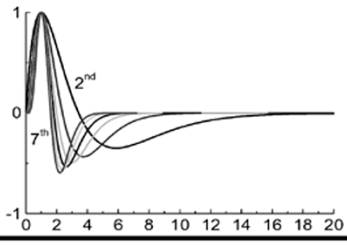
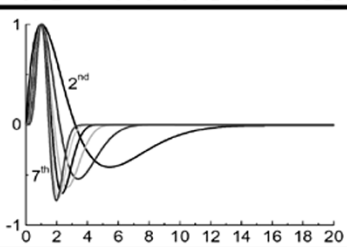
$$\mathrm{ENC}^2 = (\mathrm{C_{in}} + \mathrm{C_{ox}WL})^2 \left[\frac{1}{\tau_\mathrm{p}}\frac{2}{3}\frac{4\mathrm{kT}}{\mathrm{g_{mw}}(\mathrm{J_d}, \mathrm{L}) \cdot \mathrm{W}} + \pi\frac{\mathrm{K}_f}{\mathrm{C_{ox}WL}}\right] \quad (8)$$

where $\mathrm{g_{mw}}(\mathrm{J_d}, \mathrm{L})$ is the transconductance per unit of W.

The function $\mathrm{g_{mw}}(\mathrm{J_d}, \mathrm{L})$ can be easily extracted for specific values of L from simulations using the model and parameters

$$\mathrm{ENC}^2 = \frac{(\mathrm{C_{in}} + \mathrm{C_g})^2 \left[\mathrm{S_w}\int_0^\infty |\tau \mathrm{H}(\mathrm{j}\omega\tau)|^2 \omega^2 \mathrm{d}\omega + \mathrm{A}_f 2\pi \int_0^\infty |\tau \mathrm{H}(\mathrm{j}\omega\tau)|^2 \omega \mathrm{d}\omega\right]}{2\pi \cdot \mathrm{h}(\mathrm{t}/\tau)|^2_{\max}} + \frac{\mathrm{S_p}\int_0^\infty |\tau \mathrm{H}(\mathrm{j}\omega\tau)|^2 \mathrm{d}\omega}{2\pi \cdot \mathrm{h}(\mathrm{t}/\tau)|^2_{\max}} \quad (2)$$

TABLE I
COMMONLY ADOPTED TIME INVARIANT FILTERS AND CORRESPONDING ENC COEFFICIENTS. THE RATIO τ_w/τ_p IS ALSO REPORTED

Filter	Shape	a_w	a_f	a_p	τ_w/τ_p
Triang.		1	0.44	0.33	2
RU-2		0.92	0.59	0.92	7.66
RU-3		0.82	0.54	0.66	5.04
RU-4		0.85	0.53	0.57	4.17
RU-5		0.89	0.52	0.52	3.73
RU-6		0.92	0.52	0.48	3.46
RU-7		0.94	0.51	0.46	3.27
CU-2		0.93	0.59	0.88	6.31
CU-3		0.85	0.54	0.61	3.92
CU-4		0.91	0.53	0.51	3.16
CU-5		0.96	0.52	0.46	2.84
CU-6		1.01	0.52	0.42	2.66
CU-7		1.04	0.51	0.40	2.55
RB-2		1.03	0.75	1.01	16.6
RB-3		1.11	0.77	0.76	9.87
RB-4		1.30	0.81	0.66	7.68
RB-5		1.47	0.84	0.62	6.60
RB-6		1.61	0.87	0.59	5.94
RB-7		1.74	0.89	0.57	5.53
CB-2		1.08	0.79	1.02	12.9
CB-3		1.27	0.86	0.76	7.29
CB-4		1.58	0.93	0.67	5.60
CB-5		1.86	0.98	0.63	4.81
CB-6		2.11	1.02	0.59	4.37
CB-7		2.31	1.06	0.58	4.11

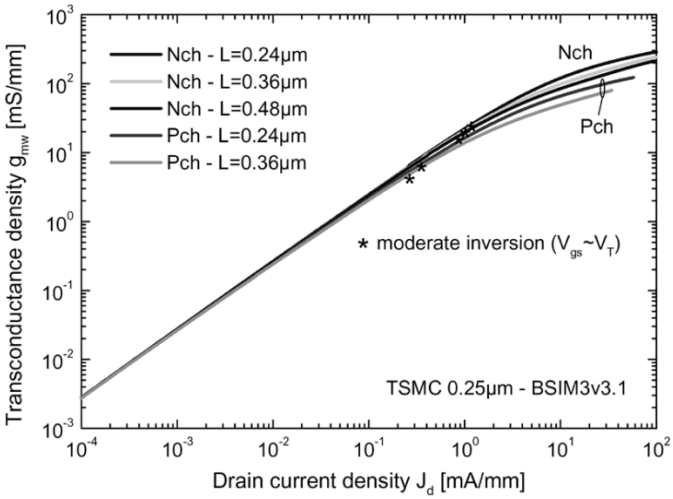


Fig. 2. Simulated g_{mw} versus J_d of n- and p-channel devices with different L in TSMC 0.25 μm. Center of moderate inversion (*) is also indicated.

available for the technology. The coefficient K_f can be extracted from a measurement of the input noise spectral density, it is assumed to be independent of L and it may differ for n-channel (K_{fn}) and p-channel (K_{fp}) devices.

For the TSMC 0.25 μm technology $C_{ox} \approx 6.1$ fF/μm^2 and $g_{mw}(J_d, L)$ can be found from PSPICE [14] simulations using advanced models such as BSIM3v3.1 [15] which have been extensively validated against experimental measurements in all regions of device operation (Fig. 2). Our measurements on samples with minimum L at 1 kHz give $K_{fn} \approx 6 \times 10^{-24}$ J and $K_{fp} \approx 0.3 \times 10^{-24}$ J.

In Fig. 3, the optimum ENC for $C_{in} = 1$ pF and $\tau_p = 1$ μs, calculated for n- and p-channel devices with different L as function of P_d is shown. To obtain this plot, a table of $g_{mw}(J_d, L)$ values was generated using PSPICE with the BSIM3v3.1 parameters extracted from a typical run of this technology. The optimum device width W_{opt} for each I_d was then selected by minimizing (8) numerically. For minimum L the white and $1/f$ components and the optimum W are also reported. It can be observed that, due to the lower K_f, the p-channel devices offer a better resolution than the n-channel devices (lower K_f) and this is generally true, except at the shortest τ_p. It also indicates that the choice $L_{opt} = L_{min}$ and $P_{d\_opt} = P_{d\_max}$ offers better

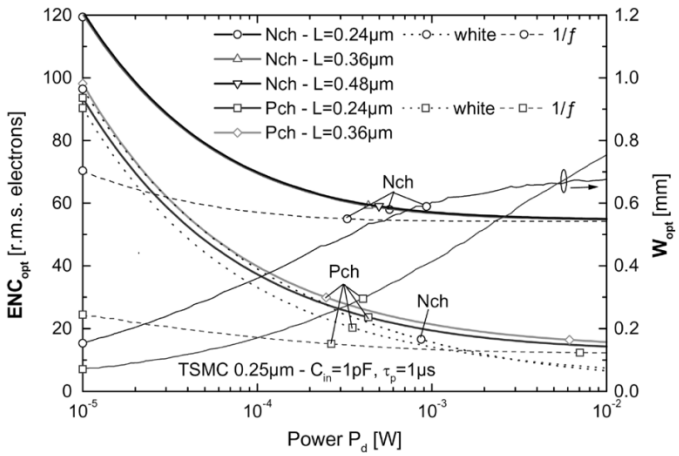


Fig. 3. Simulated $\mathrm{ENC_{opt}}$ versus $\mathrm{P_d}$ for n- and p-channel devices with different channel lengths in TSMC 0.25 μm adopting the C-model (7). For minimum L the corresponding white contribution (dotted line), $1/f$ contribution (dashed line), and optimum W (right scale) are also shown.

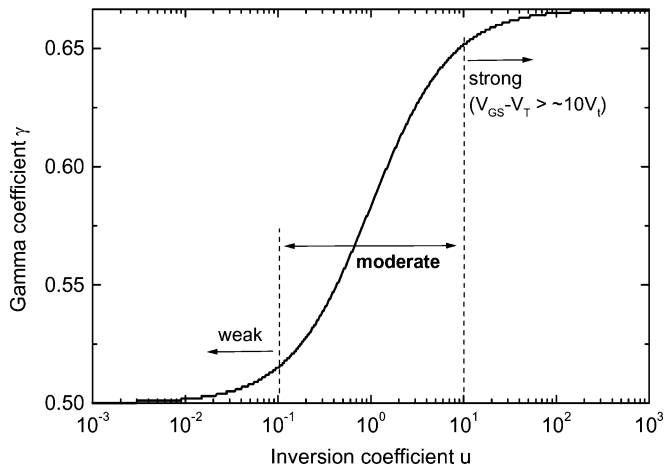


Fig. 4. Gamma coefficient γ versus inversion coefficient u. The three regions of operation of the MOSFET are also indicated.

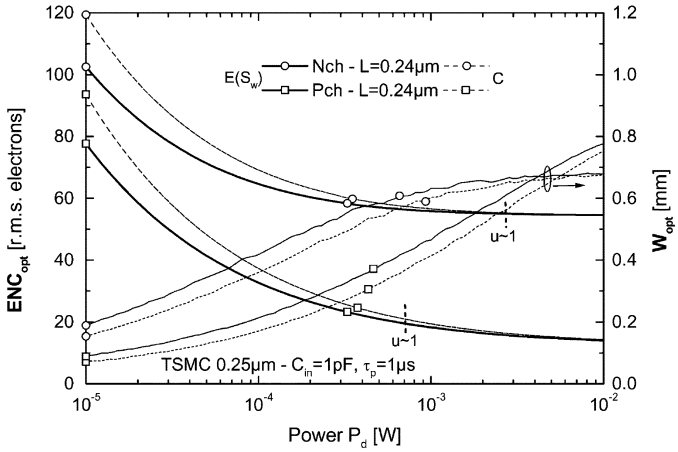


Fig. 5. Simulated $\mathrm{ENC_{opt}}$ and $\mathrm{W_{opt}}$ (right scale) versus $\mathrm{P_d}$ for n- and p-channel devices with different channel lengths in TSMC 0.25 μm adopting the E-model for $\mathrm{S_w}$. The center of moderate inversion ($\mathrm{u} = 1$) is indicated. For comparison the curves for the C-model are also shown (dashed lines).

results in an amount that depends on the white contribution relative to the $1/f$ contribution.

V. Enhanced (E) Model for $\mathrm{S_W}$

The model for the white noise spectral density $\mathrm{S_w}$ in (7) provides a crude estimation valid for long channel MOSFETs operating in strong inversion. In most cases the input MOSFET of the front-ends operate in moderate to weak inversion, and a more accurate model is required. In addition, in deep submicron MOSFETs an excess noise factor above unity has been frequently reported.

An equation that better estimates the white noise in all regions of operation can be found in [16]–[19]

$$\mathrm{S_{vw}^2} = \alpha_\mathrm{w} 4\mathrm{kT}\frac{\mu_\mathrm{eff}|\mathrm{Q_I}|}{\mathrm{L^2}}\frac{1}{\mathrm{g_m^2}} \tag{9}$$

where μ_eff is the electron or hole mobility, $\mathrm{Q_I}$ is the total inversion charge, and α_w is the excess noise factor. This equation can be approximated with [18]

$$\mathrm{S_{vw}^2} = \alpha_\mathrm{w}\mathrm{n}\gamma(\mathrm{J_d},\mathrm{L})\frac{2\mathrm{kT}}{\mathrm{g_{mw}}(\mathrm{J_d},\mathrm{L})\mathrm{W}} \tag{10}$$

where $\mathrm{n} \approx (\mathrm{g_{mb}}+\mathrm{g_m})/\mathrm{g_m}$ is the subthreshold slope coefficient ranging around 1.2–1.3 and $\gamma(\mathrm{J_d},\mathrm{L})$ is a dimensionless coefficient ranging between $1/2$ and $2/3$. The same authors of [18] proposed the following interpolation function

$$\gamma(\mathrm{J_d},\mathrm{L}) = \frac{1}{1+\mathrm{u}(\mathrm{J_d},\mathrm{L})}\left[\frac{1}{2}+\frac{2}{3}\mathrm{u}(\mathrm{J_d},\mathrm{L})\right],$$
$$\mathrm{u}(\mathrm{J_d},\mathrm{L}) = \frac{\mathrm{J_d L}}{\mu_\mathrm{eff}\mathrm{C_{ox}}2\mathrm{n}\mathrm{V_t^2}} \tag{11}$$

where $\mathrm{u}(\mathrm{J_d},\mathrm{L})$ is known as inversion coefficient and $\mathrm{V_t} = \mathrm{kT/q}$. From other authors is a simpler approximation for $\gamma(\mathrm{J_d},\mathrm{L})$ dependent on $\mathrm{g_m}$ and $\mathrm{I_d}$ [19].

A slower interpolation function is reported in [17] and [2], along with the companion model for the gate capacitance. A comparison to $\mathrm{C_g}$ modeling and to noise measurements [2] suggests that (11), here adopted, might be more accurate. In Fig. 4 the gamma coefficient $\gamma(\mathrm{J_d},\mathrm{L})$ versus the inversion coefficient $\mathrm{u}(\mathrm{J_d},\mathrm{L})$ is shown. The regions of operation for the MOSFET are also indicated. In most cases the optimized input MOSFET operates in the moderate region.

Introducing the enhanced (E) model (10)–(11) into (5) produces

$$\mathrm{ENC^2} = (\mathrm{C_{in}}+\mathrm{C_{ox}WL})^2\left[\frac{1}{\tau_\mathrm{p}}\frac{\alpha_\mathrm{w}\mathrm{n}\gamma(\mathrm{J_d},\mathrm{L})\,4\mathrm{kT}}{\mathrm{g_{mw}}(\mathrm{J_d},\mathrm{L})\cdot\mathrm{W}} + \pi\frac{\mathrm{K}_f}{\mathrm{C_{ox}WL}}\right]. \tag{12}$$

For the TSMC 0.25-μm technology $\mathrm{n_{nch}} \approx 1.2, \mathrm{n_{pch}} \approx 1.3$ and, from our measurements, $\alpha_\mathrm{w} \approx 1$ whenever $\mathrm{u} < 10$ (weak and moderate inversion) and $\mathrm{V_{ds}}-\mathrm{V_{ds\_sat}}$ is small ($\mathrm{V_{ds\_sat}}$ is the drain-source saturation voltage). Good agreement with these results can be found in the literature [2], [20]–[22].

In Fig. 5 the optimum ENC from (12) for $\mathrm{C_{in}} = 1$ pF and $\tau_\mathrm{p} = 1$ μs, calculated for n- and p-channel devices with minimum L as function of $\mathrm{P_d}$, is shown, compared to C-model results (dashed lines). The optimum W (right scale) is also reported. It can be observed that the E-model provides a different ENC estimate especially at low power, where the white noise

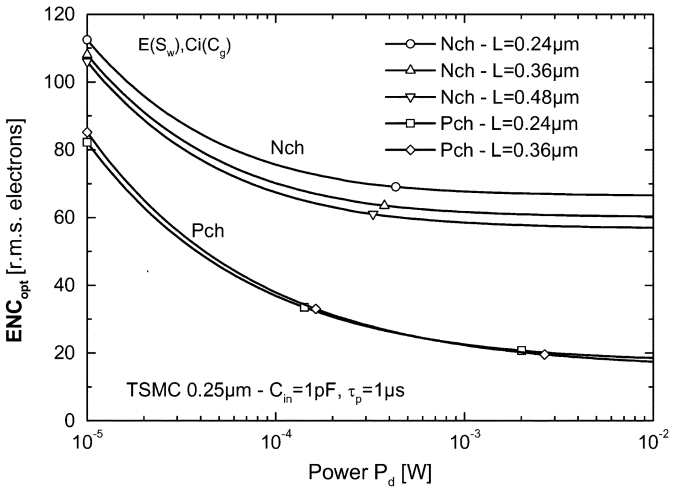


Fig. 6. Simulated $\mathrm{ENC_{opt}}$ versus $\mathrm{P_d}$ for n- and p-channel devices with differ-ent channel lengths in TSMC 0.25 μm adopting the E-model for $\mathrm{S_w}$ and the Ci-model for Cg.

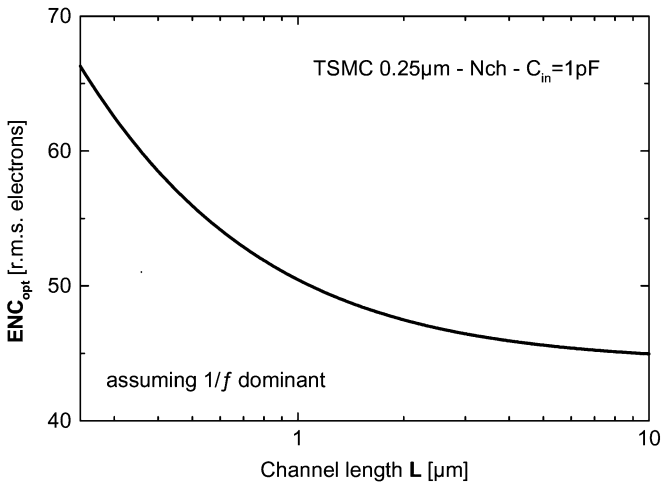


Fig. 7. Simulated $\mathrm{ENC_{opt}}$ versus L for n-channel MOSFET and $\mathrm{C_{in}} = 1$ pF assuming $1/f$ dominant.

component dominates. A relatively small difference in terms of optimization ($\mathrm{W_{opt}}$) can also be observed. The $\mathrm{L_{opt}} = \mathrm{L_{min}}$ and $\mathrm{P_{d\_opt}} = \mathrm{P_{d\_max}}$ still appears the best choice.

VI. Enhanced (E) Model for $\mathrm{C_G}$

The gate capacitance $\mathrm{C_g}$ in (5) must include any term dependent on the size (W,L) of the input MOSFET. A more accurate estimate of $\mathrm{C_g}$ should consider the gate-to-source and gate-to-drain overlap components [17]. These extrinsic terms are proportional to the width W of the MOSFET and, in deep submicron technologies, are typically not negligible. In addition, the intrinsic component of $\mathrm{C_g}$ in saturation is a fraction $\approx 2/3$ of $\mathrm{C_{ox}}$ WL [17]. An improved model for $\mathrm{C_g}$, here referred as Ci-model, is

$$\mathrm{C_g} = 2\mathrm{C_{ov}W} + \frac{2}{3}\mathrm{C_{ox}WL} \tag{13}$$

where $\mathrm{C_{ov}}$ is the overlap capacitance density, equal for drain and source. Introducing (13) in (12) it follows

$$\mathrm{ENC^2} = \left(\mathrm{C_{in}} + 2\mathrm{C_{ov}W} + \frac{2}{3}\mathrm{C_{ox}WL}\right)^2 \times \left[\frac{1}{\tau_\mathrm{p}}\frac{\alpha_\mathrm{w}\mathrm{n}\gamma\left(\mathrm{J_d},\mathrm{L}\right)4\mathrm{kT}}{\mathrm{g_{mw}}\left(\mathrm{J_d},\mathrm{L}\right)\cdot\mathrm{W}} + \pi\frac{\mathrm{K}_f}{\mathrm{C_{ox}WL}}\right]. \tag{14}$$

For the TSMC 0.25 μm technology typical values for $\mathrm{C_{ov}}$ are in the range 300–600 fF/mm, where the lower values are reported by TSMC and the higher values are reported by the MOSIS Service [23].

In Fig. 6, the optimum ENC from (14) for $\mathrm{C_{in}} = 1$ pF and $\tau_\mathrm{p} = 1$ μs, calculated for n- and p-channel devices with minimum L as function of $\mathrm{P_d}$, is shown. When compared to Figs. 3 and 5 it can be observed that the choice $\mathrm{L_{opt}} = \mathrm{L_{min}}$ does not apply anymore. Both n- and p-channel devices can offer a better resolution for L higher than $\mathrm{L_{min}}$.

This conclusion is valid whenever $1/f$ noise dominates, and can be understood by rewriting (14) for this case

$$\mathrm{ENC^2} \approx \left(\mathrm{C_{in}} + 2\mathrm{C_{ov}W} + \frac{2}{3}\mathrm{C_{ox}WL}\right)^2 \pi\frac{\mathrm{K}_f}{\mathrm{C_{ox}WL}}. \tag{15}$$

By calculating the derivative of (15) with respect to W, the optimum width $\mathrm{W_{opt}}$ for the minimum ENC can be calculated for each L

$$\mathrm{W_{opt}} = \frac{\mathrm{C_{in}}}{2\mathrm{C_{ov}} + \frac{2}{3}\mathrm{C_{ox}L}}. \tag{16}$$

Capacitive matching applies ($\mathrm{C_g} = \mathrm{C_{in}}$, as in the classical case) and, by superposition, the $\mathrm{ENC_{opt}}$ can be written

$$\mathrm{ENC^2_{opt}} \approx \frac{8}{3}\mathrm{C_{in}}\pi\mathrm{K}_f\left(1 + \frac{3\mathrm{C_{ov}}}{\mathrm{C_{ox}L}}\right). \tag{17}$$

The plot in Fig. 7, derived from (17) for n-channel MOSFETs, illustrates the impact of L on the optimum ENC for the case of dominant $1/f$ noise. Intuitively, as L increases the $1/f$ noise contribution decreases more rapidly than the increase in gate capacitance.

The Ci-model (13) for $\mathrm{C_g}$ still does not take into account the dependence of the intrinsic gate capacitance on the drain current density $\mathrm{J_d}$. This dependence in deep submicron technologies can be relevant, especially in the transition from weak, thorough moderate, to strong inversion. An enhanced (E) model for $\mathrm{C_g}$ can be written as

$$\mathrm{C_g} = \mathrm{C_{gw}}\left(\mathrm{J_d},\mathrm{L}\right)\cdot\mathrm{W} \tag{18}$$

where $\mathrm{C_{gw}}(\mathrm{J_d},\mathrm{L})$ is the gate capacitance density, and it includes the bias dependence, intrinsic, and extrinsic components.

As for $\mathrm{g_{mw}}(\mathrm{J_d},\mathrm{L})$, the function $\mathrm{C_{gw}}(\mathrm{J_d},\mathrm{L})$ can be extracted for specific values of L from a Spice simulation using the model and parameters available for the technology. For the TSMC 0.25-μm $\mathrm{C_{gw}}(\mathrm{J_d},\mathrm{L})$ can be obtained from BSIM3v3.1 simulations as shown in Fig. 8. The results for C- and Ci-models for the n-channel device at minimum L are reported for comparison. It is worth noting that the cutoff frequency of the MOSFET, given by $\mathrm{g_m}/(2\pi\mathrm{C_g})$, remains an increasing function of $\mathrm{J_d}$ and, in the regions of interest it easily exceed tens of MHz.

Substitution of (18) into (12) yields

$$\mathrm{ENC^2} = \left[\mathrm{C_{in}} + \mathrm{C_{gw}}\left(\mathrm{J_d},\mathrm{L}\right)\cdot\mathrm{W}\right]^2\left[\frac{1}{\tau_\mathrm{p}}\frac{\alpha_\mathrm{w}\mathrm{n}\gamma\left(\mathrm{J_d},\mathrm{L}\right)4\mathrm{kT}}{\mathrm{g_{mw}}\left(\mathrm{J_d},\mathrm{L}\right)\cdot\mathrm{W}} + \pi\frac{\mathrm{K}_f}{\mathrm{C_{ox}WL}}\right]. \tag{19}$$

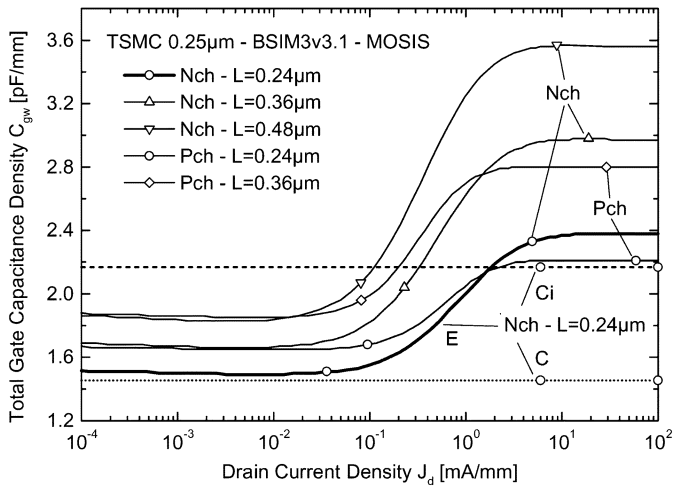


Fig. 8. Simulated $\mathrm{C_{gw}}$ versus J_d of n- and p-channel devices with different L in TSMC 0.25 μm. The C- and Ci-models for the minimum L n-channel device are also reported.

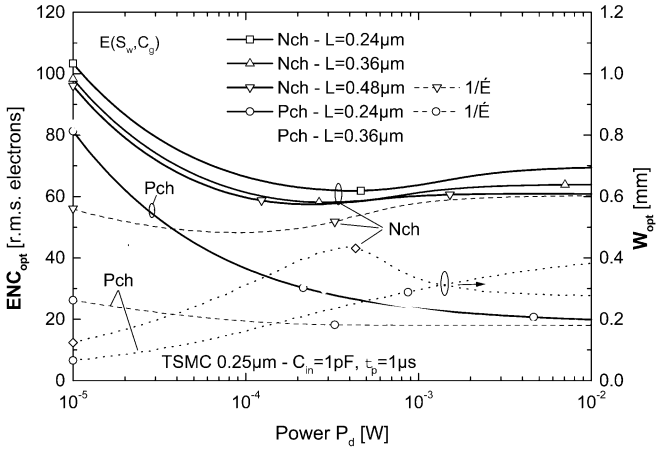


Fig. 9. Simulated $\mathrm{ENC_{opt}}$ versus $\mathrm{P_d}$ for n- and p-channel devices with different L in TSMC 0.25 μm adopting the E-model for $\mathrm{S_w}$ and $\mathrm{C_g}$. For two cases (n-ch. $\mathrm{L} = 0.48$ μm and p-ch. $\mathrm{L} = 0.24$ μm) the $1/f$ component (dashed line) and the $\mathrm{W_{opt}}$ (right scale, dotted lines) are also shown.

In Fig. 9, the optimum ENC from (19) for $\mathrm{C_{in}} = 1$ pF and $\tau_\mathrm{p} = 1\,\mu$s, calculated for n- and p-channel devices with different L as function of $\mathrm{P_d}$, is shown. For two cases the $1/f$ component (dashed line) and the optimum W (right scale) are also reported. It can be observed again that the choice $\mathrm{L_{opt}} = \mathrm{L_{min}}$ does not apply. In addition, for the n-channel MOSFET, the choice $\mathrm{P_{d\_opt}} = \mathrm{P_{d\_max}}$ does not apply, since a better resolution can be achieved at $\mathrm{P_d}$ lower than the maximum allocated.

This conclusion is valid whenever $1/f$ noise dominates, and can be understood by rewriting (19) for this case

$$\mathrm{ENC}^2 \approx \left[\mathrm{C_{in}} + \mathrm{C_{gw}}\left(\mathrm{J_d}, \mathrm{L}\right)\mathrm{W}\right]^2 \pi \frac{\mathrm{K}_f}{\mathrm{C_{ox}WL}}. \qquad (20)$$

By taking into account (6) and calculating the derivative of (20) with respect to W, the optimum width for the minimum ENC can be calculated for each L

$$\mathrm{W_{opt}} = \frac{\mathrm{C_{in}}}{\mathrm{C_{gw}}\left(\mathrm{J_d}, \mathrm{L}\right)\left[1 - 2\frac{\mathrm{J_d}}{\mathrm{C_{gw}(J_d,L)}}\frac{\partial \mathrm{C_{gw}(J_d,L)}}{\partial \mathrm{J_d}}\right]}. \qquad (21)$$

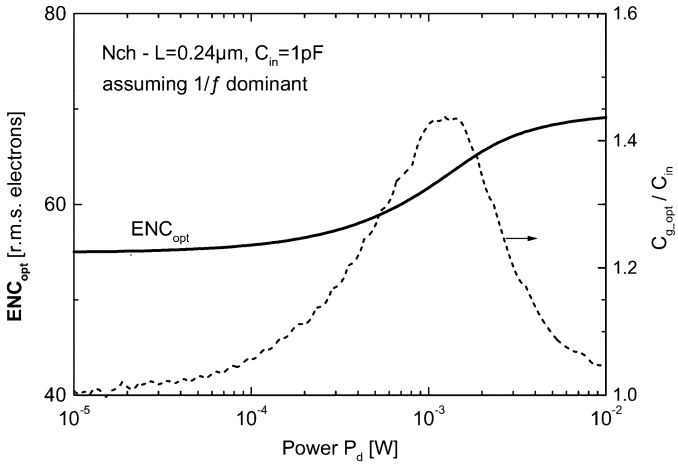


Fig. 10. Simulated $\mathrm{ENC_{opt}}$ versus $\mathrm{P_d}$ for minimum L n-channel device and $\mathrm{C_{in}} = 1$ pF assuming $1/f$ dominant. The ratio $\mathrm{C_{g\_opt}/C_{in}}$ is also shown (right scale, dashed line).

Capacitive matching does not apply except for the regions where $\partial \mathrm{C_{gw}}/\partial \mathrm{J_d} = 0$ and, by superposition, the $\mathrm{ENC_{opt}}$ turns out to be

$$\begin{cases} \mathrm{ENC_{opt}^2} \approx \left(1 + \frac{1}{\eta(\mathrm{J_d},\mathrm{L})}\right)\mathrm{C_{in}}\pi \mathrm{K}_f \frac{\eta(\mathrm{J_d},\mathrm{L})\mathrm{C_{gw}(J_d,L)}}{\mathrm{C_{ox}L}}. \\ \eta(\mathrm{J_d},\mathrm{L}) = 1 - 2\frac{\mathrm{J_d}}{\mathrm{C_{gw}(J_d,L)}}\frac{\partial \mathrm{C_{gw}(J_d,L)}}{\partial \mathrm{J_d}}. \end{cases} \qquad (22)$$

The plot in Fig. 10, derived from (22) for n-channel device with minimum L and $\mathrm{C_{in}} = 1$ pF, illustrates the impact of $\mathrm{P_d}$ on the optimum ENC for cases of dominant $1/f$ noise. The ratio $\mathrm{C_{g\_opt}/C_{in}}$ (right scale, dashed line) is also reported. Intuitively, as $\mathrm{P_d}$ increases the gate capacitance increases while the $1/f$ noise contribution does not change.

VII. Enhanced (E) Model for Low-Frequency Noise

In Fig. 11, the typical equivalent input noise spectral densities measured on n- and p-channel devices in TSMC 0.25 μm with different L are shown, and compared to the $1/f$ slope. Two relevant results should be observed. The first concerns the slope, which differs from $1/f$, being in this case higher for p-channel devices and lower for n-channel devices. The second concerns the ratio between spectra, which is higher ($\approx$2.4 for $\mathrm{L} = 0.24$ μm versus $\mathrm{L} = 0.48$ μm) compared to the square root of the ratio between L (≈ 1.4 for $\mathrm{L} = 0.24$ μm versus $\mathrm{L} = 0.48$ μm). A similar trend for short channel devices in deep submicron technologies was reported by other authors [2], [24]–[28].

In Fig. 12 the typical spectra for n- and p-channel devices with $\mathrm{L} = 0.24$ μm at different drain current densities $\mathrm{J_d}$ are shown. The dependence of the low-frequency component on the bias point appears negligible. This result seems in agreement with others reported in the literature for MOSFETs operating from weak inversion up to the border between moderate and strong inversion [3], [29]–[32], which is the region of interest for our applications. Some authors have reported an increase moving toward very strong inversion [31]–[33].

The results reported in Figs. 11 and 12 indicate that the low-frequency component of the noise power spectral density could

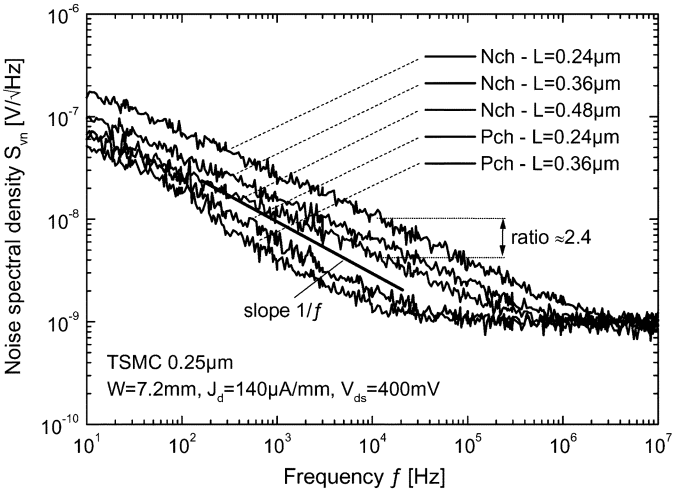


Fig. 11. Measured equivalent input noise spectra for n- and p-channel devices with different L in TSMC 0.25 μm. The $1/f$ slope is also shown.

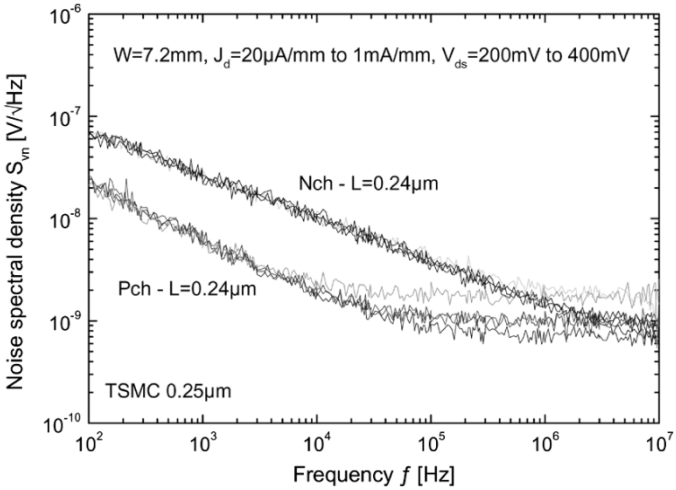


Fig. 12. Measured equivalent input noise spectra for n- and p-channel devices with minimum L and different J_d in TSMC 0.25 μm.

be better approximated by using the following enhanced (E) model

$$\mathrm{S}_f = \frac{\mathrm{A}_f}{f^{\alpha_f}} = \frac{\mathrm{K}_f(\mathrm{L})}{\mathrm{C_{ox}WL}f^{\alpha_f}} \tag{23}$$

where $\mathrm{K}_f(\mathrm{L})$ now depends on L, and the slope depends on the coefficient α_f.

The non-$1/f$ slope requires a review of the low-frequency component $\mathrm{ENC_{LF}}$ of the ENC. The second term of (2) now becomes

$$\mathrm{ENC}_{\mathrm{LF}}^2 = \frac{(\mathrm{C_{in}}+\mathrm{C_g})^2\mathrm{A}_f(2\pi)^{\alpha_f}\int_0^\infty |\tau\mathrm{H}(\mathrm{j}\omega\tau)|^2\omega^{2-\alpha_f}\mathrm{d}\omega}{2\pi\cdot\mathrm{h(t/\tau)}|_{\max}^2} \tag{24}$$

and (3) can be rewritten

$$\mathrm{ENC}^2 = (\mathrm{C_{in}}+\mathrm{C_g})^2 \times\left[\frac{\mathrm{S_w}}{\tau_\mathrm{p}}\mathrm{a_w}+\mathrm{A}_f\frac{(2\pi)^{\alpha_f}}{\tau_\mathrm{p}^{1-\alpha_f}\mathrm{A}_f}(\alpha_f)\right]+\mathrm{S_p}\tau_\mathrm{p}\mathrm{A_p} \tag{25}$$

TABLE II
RATIO $\rho_f = \mathrm{a}_f(\alpha_f)/\mathrm{a}_f(1)$ VERSUS α_f FOR THE FILTERS REPORTED IN TABLE I

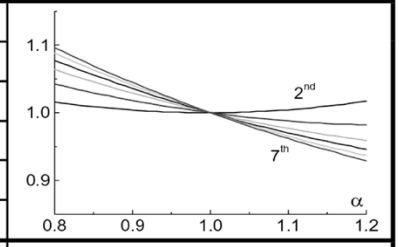
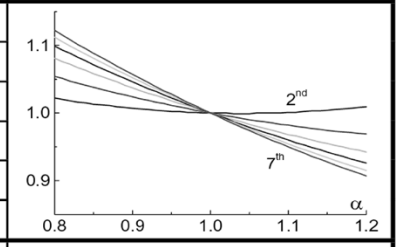
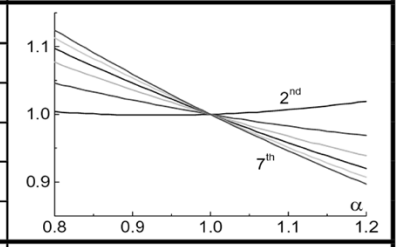
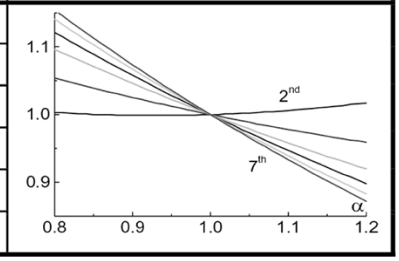
Filter	Relative coeff. ρ_f
RU-2	
RU-3	
RU-4	
RU-5	
RU-6	
RU-7	
CU-2	
CU-3	
CU-4	
CU-5	
CU-6	
CU-7	
RB-2	
RB-3	
RB-4	
RB-5	
RB-6	
RB-7	
CB-2	
CB-3	
CB-4	
CB-5	
CB-6	
CB-7	

TABLE III
TYPICAL VALUES OF K_f AND α_f FOR THE TSMC 0.25 μm TECHNOLOGY

	Nch-0.24μm	*Nch-0.36μm*	*Nch-0.48μm*	*Pch-0.24μm*	*Pch-0.36μm*
$\mathbf{K_f}$	**2.71**×10^{-24}	**1.40**×10^{-24}	**0.97**×10^{-24}	**0.60**×10^{-24}	**0.50**×10^{-24}
$\boldsymbol{\alpha_f}$	0.85	0.85	0.85	1.08	1.08

where the ENC coefficient $\mathrm{a}_f(\alpha_f)$ is given by

$$\mathrm{A}_f(\alpha_f) = \frac{\int_0^\infty |\mathrm{H(jx)}|^2\mathrm{x}^{2-\alpha_f}\mathrm{dx}}{2\pi\cdot\mathrm{h(t/\tau_p)}|_{\max}^2}. \tag{26}$$

Concerning the two other coefficients in (4) it is worth noting that $\mathrm{a_w} = \mathrm{a}_f(0)$ and $\mathrm{a_p} = \mathrm{a}_f(2)$. In Table II the ratio $\rho_f = \mathrm{a}_f(\alpha_f)/\mathrm{a}_f(1)$ is calculated for the filters in Table I.

The final expression for the ENC related to series noise, adopting the E-model for $\mathrm{S_w}, \mathrm{C_g}$, and S_f, becomes

$$\mathrm{ENC}^2 = [\mathrm{C_{in}}+\mathrm{C_{gw}(J_d,L)\cdot W}]^2 \times\left[\frac{1}{\tau_\mathrm{p}}\frac{\alpha_\mathrm{w}\mathrm{n}\gamma(\mathrm{J_d,L})4\mathrm{kT}}{\mathrm{g_{mw}(J_d,L)\cdot W}}+\frac{\mathrm{K}_f}{\mathrm{C_{ox}WL}}\frac{(2\pi)^{\alpha_f}}{\tau_\mathrm{p}^{1-\alpha_f}}\mathrm{a}_f(\alpha_f)\right]. \tag{27}$$

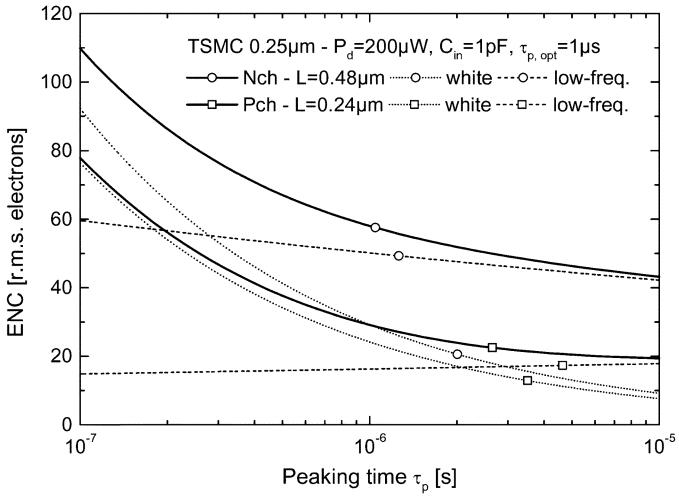


Fig. 13. Simulated ENC versus $\tau_{\rm p}$ for a design optimized for $\rm C_{in} = 1$ pF, $\rm P_d = 200\ \mu W$, and $\tau_{\rm p_opt.} = 1\ \mu$s. The white (dotted line) and low-frequency (dashed line) components are also shown.

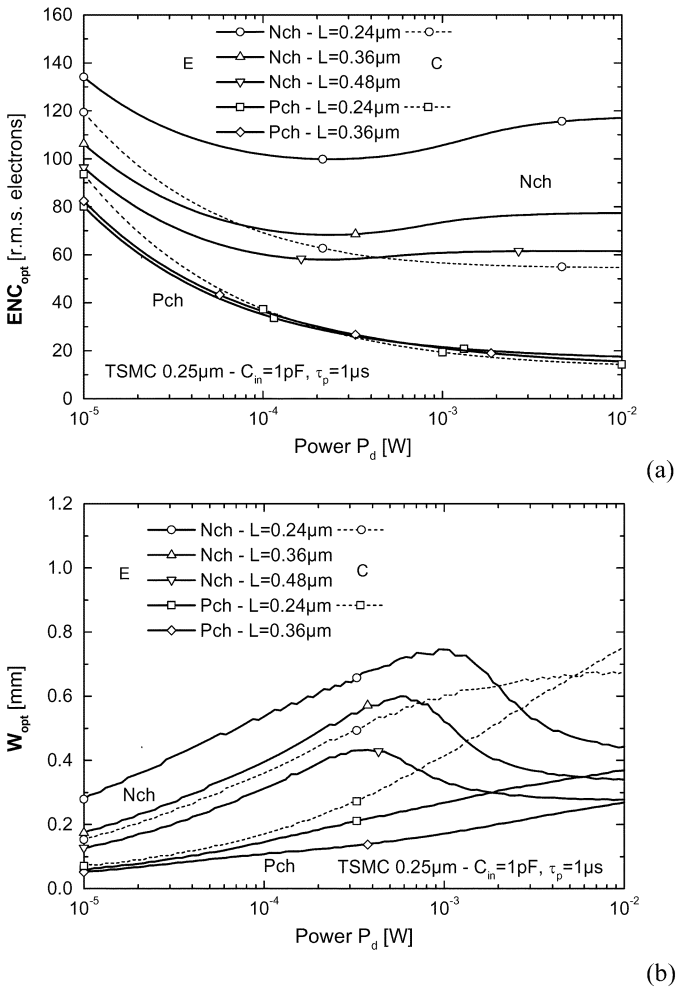


Fig. 14. Simulated (a) $\rm ENC_{opt}$ versus $\rm P_d$ and (b) corresponding $\rm W_{opt}$ versus $\rm P_d$ for n- and p-channel devices with different L in TSMC 0.25 μm adopting the full E-model. Results from the C-model for minimum L (dashed line) are also shown.

For the TSMC 0.25 μm technology typical values for $\rm K_f$ and α_f are reported in Table III. As in previous cases we will simplify our analysis by assuming $\rho_f = 1.05$ for n-channel devices

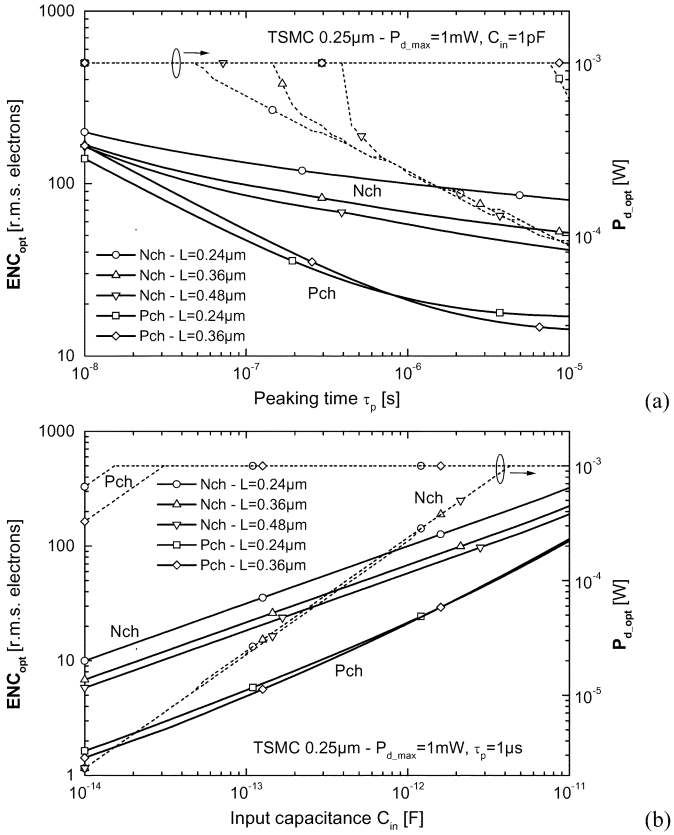


Fig. 15. Simulated $\rm ENC_{opt}$ (solid line, left scale) and $\rm P_{d\_opt}$ (dashed line, right scale) versus (a) $\tau_{\rm p}$ and (b) $C_{\rm in}$ for n- and p-channel devices with different L in TSMC 0.25 μm adopting the full E-model.

and $\rho_f = 0.95$ for p-channel devices, values close to the typical for a good time invariant unipolar shaper.

As consequence of the non-$1/f$ slope, a front-end optimized for a given peaking time $\tau_{\rm p\_opt}$ will show in the ENC a low-frequency noise component dependent on $\tau_{\rm p}$, as shown in Fig. 13 for the case $\rm C_{in} = 1$ pF, $\rm P_d = 200\ \mu W$, $\tau_{\rm p_opt} = 1\ \mu$s.

VIII. Achievable Resolution in TSMC 0.25 μm

By applying the final (27) to the TSMC 0.25-μm CMOS, it is possible to estimate the ENC achievable with this technology. The results will give a general idea of what to expect. An exhaustive analysis in this sense is beyond the scope of this paper.

In Fig. 14(a) and (b), the $\rm ENC_{opt}$ and $\rm W_{opt}$ for $\rm C_{in} = 1$ pF and $\tau_{\rm p} = 1\ \mu$s, calculated using the full E-model for n- and p-channel devices with different L as functions of $\rm P_d$ are shown. For comparison, the two minimum L cases for the C-model are reported. The difference between E- and C-model in the estimate of the achievable $\rm ENC_{opt}$ for the n-channel devices is relevant, while for the p-channel devices may appear small. On the other hand, the difference in terms of MOSFET size optimization $(\rm W_{opt})$ is in both cases relevant. The enhanced model not only provides a more accurate ENC estimate, but it also provides a better MOSFET size optimization and, eventually, a better resolution.

In Fig. 15(a) and (b), the $\rm ENC_{opt}$ and $\rm P_{d\_opt}$ for $\rm C_{in} = 1$ pF versus $\tau_{\rm p}$ and for $\tau_{\rm p} = 1\ \mu$s versus $\rm C_{in}$, calculated using the E-model for n- and p-channel devices with different L, are

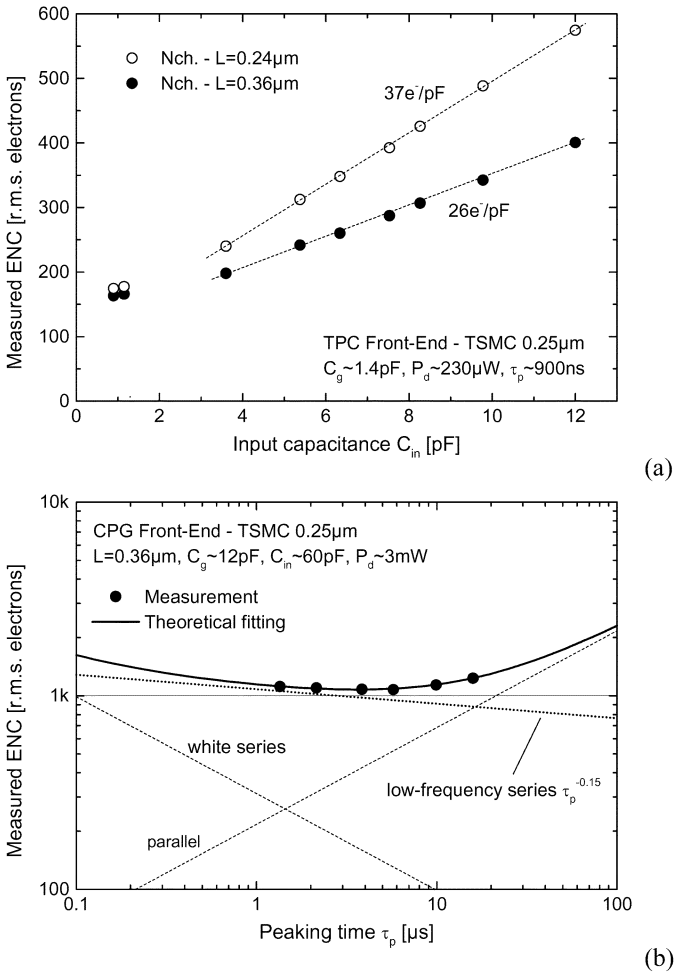


Fig. 16. ENC measurements on front-end ASICs for (a) a TPC and (b) a Coplanar Grid Sensor.

shown, assuming a power budget limit of $\mathrm{P_{d\_max}} = 1$ mW. In the case of Fig. 15(a) the reduction in $\mathrm{P_{d\_opt}}$ can be observed for higher values of τ_p. In the case of Fig. 15(b), the reduction in $\mathrm{P_{d\_opt}}$ can be observed for smaller values of $\mathrm{C_{in}}$. In both cases, this is consequence of the dependence of the gate capacitance on the drain current density, which pushes the input MOSFET toward the weak inversion. The enhanced model not only provides a more accurate ENC estimate, but it also provides a better power optimization.

In Fig. 16(a) and (b), we report, as examples, some experimental results from two front-end ASICs recently developed in TSMC 0.25-μm CMOS. In Fig. 16(a), the ENC versus $\mathrm{C_{in}}$ from a prototype for a time projection chamber (TPC) [34] is shown. The ASIC implements 32 front-end channels with n-MOS inputs, 16 with $\mathrm{L} = 0.24$ μm and 16 with $\mathrm{L} = 0.36$ μm. The gate capacitance was, in both cases, on the order of 1.4 pF. We observed a $\approx 40\%$ difference in ENC slope with better resolution for the longer channel, a result that appears in line with the discussion presented here. In Fig. 16(b), the ENC versus τ_p from an ASIC prototype for a Coplanar Grid Sensor [35] is shown. The ASIC implements an n-MOS input with $\mathrm{L} = 0.36$ μm. The gate and input capacitances were on the order of 12 and 60 pF, respectively. A low-frequency noise component proportional to $\approx \tau_\mathrm{p}^{-0.15}$, in agreement with $\alpha_f \approx 0.85$, can be observed.

IX. Conclusion

The optimization of the input MOSFET for charge amplifiers in deep submicron technology requires proper modeling of the series noise and gate capacitance. The ENC relation (27) presented here, based on modern MOS models which accurately simulate submicron device behavior in moderate inversion, serves this purpose. It allows a more accurate ENC estimate and a better MOSFET optimization. The results indicate that the traditional choice of selecting the minimum channel length and the maximum allocated power do not always offer the best resolution. Also, for an optimized front-end, the low-frequency noise contribution to the ENC may depend on the time constant of the filter. The results here reported, based on the commercial TSMC 0.25 μm CMOS, can be easily extended to other deep submicron technologies.

Acknowledgment

The authors are grateful to G. Anelli (CERN), V. Radeka (BNL), and A. Dragone (Bari Polytechnic) for helpful discussions.

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