micro-TCA DAQ Benchmark Test Discussion – 10/22/14
-Lunch Break with Harley

Experiment proposed:

- First take one FPGA and write to TCA over PCI Express
- Then have TCA write to FPGA over PCI Express
- Slap time stamp of packet coming out of FIFO
- Slap time stamp at receiving end
- Calculate throughput, etc.

Need to research:

- CoreGen (IP Generator)
- How to generate real-time Clock
- FIFO (First In First Out) for buffering and ordering of the packets
- PCI Express