Asst. Prof. Ahmet Can Erten **Due Date: 31.10.2019**

EHB205 Introduction to Logic Design
2nd Homework

a_1	a_0	b_1	b_0	c_2	c_1	c_0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

Boolean functions for the outputs $c_2(a_1,a_0,b_1,b_0)$, $c_1(a_1,a_0,b_1,b_0)$ and $c_0(a_1,a_0,b_1,b_0)$ shown by the above truth table will be implemented.

1) Create a new project as explained in your first homework.
2) Take “OR_gate.vhd” and “OR_gate_tb.vhd” files from Ninova. You will design your circuit by changing these files. Save these files by giving proper names that represent your two different designs described below.
3) Add your “*.vhd” by “Add Sources”, “Add or create design sources” to your project.
4) Add your “*_tb.vhd” by “Add Sources”, “Add or create simulation sources” to your project.
5) Change the number of inputs and outputs according to your circuit.
6) Change the data types of inputs and outputs according to the examples given in

http://www.csit-sun.pub.ro/courses/Masterat/Materiale_Suplimentare/Xilinx%20Synthesis%20Technology/toolbox.xilinx.com/docsan/xilinx4/data/docs/xst/vhdl3.html
https://startingelectronics.org/software/VHDL-CPLD-course/tut13-VHDL-data-types-and-operators/
http://www.brunel.ac.uk/~eestmba/hdl/dtypevhdl1.html
https://en.wikibooks.org/wiki/Programmable_Logic/VHDL_Data_Types
https://web.engr.oregonstate.edu/~sllu/vhdl/lec2e.html

7) Describe the functionality of your circuit under “architecture” by using “case statement” as given in the following web pages

https://www.ics.uci.edu/~jmoorkan/vhdlref/cases.html
https://www.nandland.com/vhdl/examples/example-case-statement.html
https://www.allaboutcircuits.com/technical-articles/sequential-vhdl-if-and-case-statements/
http://vhdl.renerta.com/mobile/source/vhd00014.htm
https://insights.sigasi.com/tech/signal-assignments-vhdl-withselect-whenelse-and-case/

8) Make sure that "*.vhd" is your top module. You can change top module by right clicking to the module that you would like to implement and choose "Set as Top" from the list. Produce the RTL schematic of your design.
9) Write the test bench file to test your design by using "*_tb.vhd". Simulate your design.
10) Simplify the $c_2(a_1,a_0,b_1,b_0)$, $c_1(a_1,a_0,b_1,b_0)$ and $c_0(a_1,a_0,b_1,b_0)$ functions.
11) Add your second "*.vhd" to your project. Describe the functionality of your circuit under "architecture begin" by using "data flow modelling" as given in the following web pages

https://vhdlguide.readthedocs.io/en/latest/vhdl/dataflow.html
https://www.oreilly.com/library/view/vhdl/9788131732113/xhtml/chapter005.xhtml
https://buzztech.in/vhdl-modelling-styles-behavioral-dataflow-structural/
https://www.technobyte.org/vhdl-code-for-an-encoder-dataflow/

12) Make sure that your second "*.vhd" is your top module. Produce the RTL schematic of your design.
13) Write the test bench file to test your design by using your second "*_tb.vhd". Simulate your design.

References

1) Frank Vahid, **Digital design, with RTL design, VHDL, and Verilog,** Hoboken, NJ : John Wiley, 2010
2) Peter D Minns, **FSM-based digital design using Verilog HDL,** Chichester, England : J. Wiley & Sons , c2008
3) Pong P. Chu, **FPGA prototyping by Verilog examples Xilinx Spartan -3 version**, Hoboken, N.J. : J. Wiley & Sons, c2008