Po Jui (Elton) Shih

CONTACT INFORMATION

Computer Science Building (K17), Engineering Rd
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beeb.page

RESEARCH FOCUS

computer architecture, *embedded systems*, *hardware acceleration*, *computer networks*, *bioinformatics*

EDUCATION

University of New South Wales, Sydney, Australia
B.Eng. (Class I Honours in Computer Engineering), WAM: 84/100 — Feb 2018 - Dec 2021

- Thesis title: *Hardware Accelerated Real-Time Selective Genome Sequencing*
- Advisor: *Prof. Sri Parameswaran*
- Selected Coursework: *Digital Circuits and Systems*, *Computer Architecture*, *Extended Operating Systems*, *Extended Algorithms and Programming Techniques*, *Design Project B (Hardware Accelerator Design)*, *Mobile Data Networking*

HONORS AND AWARDS

First Class Honours, *UNSW Faculty of Engineering* — 2021
Outstanding Undergraduate Thesis, *UNSW School of CSE (one of 10)* — 2021
Dean's Honours List, *UNSW Faculty of Engineering* — 2018, 2019, 2020

PUBLICATIONS

Peer-reviewed Journal Articles

Efficient real-time selective genome sequencing on resource-constrained devices.
Po Jui Shih, Hassaan Saadat, Sri Parameswaran, and Hasindu Gamaarachchi.
GigaScience 12 (2023): giad046.

TALKS

Poster Presentation

Efficient real-time selective genome sequencing on resource-constrained devices.
Po Jui Shih, Hassaan Saadat, Sri Parameswaran, and Hasindu Gamaarachchi.
Australian Bioinformatics And Computational Biology Society Conference (ABACBS), Dec 2023

Hardware accelerated real-time selective genome sequencing
Po Jui Shih.
Outstanding Undergraduate Thesis Showcase, UNSW School of CSE, Dec 2021

WORK AND RESEARCH EXPERIENCE

Audinate, Sydney, Australia

Research Engineer II — Aug 2022 - present
Research Engineer I — Jan 2022 - Aug 2023
Research and Development Engineering Intern — Winter 2021
Research and Development Engineering Intern — Summer 2020
Research and Development Engineering Intern — Summer 2019

School of CSE, UNSW, Sydney, Australia

Casual Academic — Feb 2020 - Present

Embedded Systems Research Group, UNSW, Sydney, Australia

Undergraduate Researcher — Nov 2020 - May 2022

- Worked on accelerating selective genome sequencing on resource-constrained edge devices through hw-sw co-design [GigaScience 2023]
- Supervisor: Prof. Sri Parameswaran (co-advised by Dr. Hasindu Gamaarachchi, and Dr. Hassaan Saadat)

Teaching Experience

23T3, COMP3601 Design Project A, UNSW, Sydney, Australia
Guest Lecturer.
Content includes: *MPSoC*, *FPGA*, *device drivers*, *embedded systems*

23T2, DESN2000 Eng Design & Prof Practice (COMP), UNSW, Sydney, Australia
Academic Tutor & Guest Lecturer, 51 students.
Content includes: *AVR ISA*, *embedded systems*, *computer architecture*

22T3, COMP3601 Design Project A, UNSW, Sydney, Australia
Course Coordinator & Guest Lecturer, 46 students.
Content includes: *hw-sw co-design*, *FPGA*, *device drivers*, *audio signal processing*

21T3, COMP3601 Design Project A, UNSW, Sydney, Australia
Academic Tutor, 48 students.
Content includes: *hw-sw co-design*, *cryptography hardware accelerator*, *approx. arithmetic*

21T2, COMP1521 Computer Systems Fundamentals, UNSW, Sydney, Australia
Academic Tutor & Lab Assistant, 46 students.
Content includes: *MIPS ISA*, *C programming language*, *UNIX*, *POSIX*

20T1, COMP2121 Microprocessor and Interfacing, UNSW, Sydney, Australia
Academic Tutor, 43 students.
Content includes: *AVR ISA*, *embedded systems*, *computer architecture*

Advising

Undergraduate Honours Students

Katelyn Mak (with H. Gamaarachchi), UNSW, 2023-

Professional services

External Reviewer: ASP-DAC 2024

Open-source Software

HARU: A hw-sw co-design for real-time selective sequencing on low-cost edge devices. [Github]
sigfish-haru: A fast selective sequencing software using HARU for acceleration. [Github]
RUscripts-R9: An upgraded RUscripts supporting Python3, R9 flowcell, slow5 and more. [Github]
HARU-HLS: An early POC for HARU using HLS (HW) and client-server architecture (SW). [Github]

Computer Skills

Programming languages: *C/C++*, *VHDL*, *Verilog*, *Python*, *Go*
Tools: *Vivado*, *Vitis HLS*, *Chisel*, *PetaLinux*, *Yocto*, *Buildroot*, *Matlab*, *Wireshark*
RTOS: *Zephyr RTOS*, *FreeRTOS*, *ThreadX*
Microprocessor architectures: *ARM*, *RISC-V*, *AVR*, *MIPS*, *Xtensa*
Others: *eXpress Data Path (XDP)*, *BPF*, *JTAG & OpenOCD*

Other/Personal

Languages: *English* (native proficiency), *Traditional Chinese Mandarin* (native proficiency)
Citizenship: *Australian*