

Po Jui (Elton) Shih

CONTACT INFORMATION	Computer Science Building (K17), Engineering Rd UNSW Sydney, Kensington, NSW, Australia 2052	eshih.pj@gmail.com beeb.page
RESEARCH FOCUS	<i>computer architecture, embedded systems, hardware acceleration, computer networks, bioinformatics</i>	
EDUCATION	University of New South Wales, Sydney, Australia B.Eng. (Class I Honours in Computer Engineering), WAM: 84/100 <ul style="list-style-type: none">Thesis title: <i>Hardware Accelerated Real-Time Selective Genome Sequencing</i>Advisor: <i>Prof. Sri Parameswaran</i>Selected Coursework: <i>Digital Circuits and Systems, Computer Architecture, Extended Operating Systems, Extended Algorithms and Programming Techniques, Design Project B (Hardware Accelerator Design), Mobile Data Networking</i>	Feb 2018 - Dec 2021
HONORS AND AWARDS	First Class Honours, <i>UNSW Faculty of Engineering</i> Outstanding Undergraduate Thesis, <i>UNSW School of CSE (one of 10)</i> Dean's Honours List, <i>UNSW Faculty of Engineering</i>	2021 2021 2018, 2019, 2020
PUBLICATIONS	<i>Peer-reviewed Journal Articles</i> Efficient real-time selective genome sequencing on resource-constrained devices <u>Po Jui Shih</u> , Hassaan Saadat, Sri Parameswaran, and Hasindu Gamaarachchi. <i>GigaScience</i> 12 (giad046), 2023. <i>Dissertation</i> Hardware accelerated real-time selective genome sequencing <u>Po Jui Shih</u> . <i>B.Eng. Honours Thesis, UNSW, 2021.</i>	
TALKS	<i>Poster Presentations</i> Efficient real-time selective genome sequencing on resource-constrained devices <u>Po Jui Shih</u> , Hassaan Saadat, Sri Parameswaran, and Hasindu Gamaarachch. <i>Australian Bioinformatics And Computational Biology Society (ABACBS) Conference 2023, Dec 2023.</i> Efficient real-time selective genome sequencing on resource-constrained devices <u>Po Jui Shih</u> , Hassaan Saadat, Sri Parameswaran, and Hasindu Gamaarachch. <i>COBINE Symposium 2023, Dec 2023.</i> Hardware accelerated real-time selective genome sequencing <u>Po Jui Shih</u> . <i>Outstanding Undergraduate Thesis Showcase, UNSW School of CSE, Dec 2021.</i>	
WORK AND RESEARCH EXPERIENCE	Audinate, Sydney, Australia <i>Research Engineer II</i> <i>Research Engineer I</i> <i>Research and Development Engineering Intern</i> <i>Research and Development Engineering Intern</i> <i>Research and Development Engineering Intern</i>	Aug 2022 - present Jan 2022 - Aug 2023 Winter 2021 Summer 2020 Summer 2019

School of CSE, UNSW, Sydney, Australia

Casual Academic

Feb 2020 - Present

Embedded Systems Research Group, UNSW, Sydney, Australia

Undergraduate Researcher

Nov 2020 - May 2022

- Worked on accelerating selective genome sequencing on resource-constrained edge devices through hw-sw co-design [GigaScience 2023]
- Supervisor: Prof. Sri Parameswaran (co-advised by Dr. Hasindu Gamaarachchi, and Dr. Hasaan Saadat)

TEACHING
EXPERIENCE

2023 Term 3, COMP3601 Design Project A, *Guest lecturer*, UNSW

2023 Term 2, DESN2000 Eng Design & Prof Practice (COMP), *Academic Tutor & Guest lecturer*, UNSW

2022 Term 3, COMP3601 Design Project A, *Course Coordinator & Guest lecturer*, UNSW

2021 Term 3, COMP3601 Design Project A, *Academic Tutor*, UNSW

2021 Term 2, COMP1521 Computer Systems Fundamentals, *Academic Tutor & Lab Assistant*, UNSW

2020 Term 1, COMP2121 Microprocessor and Interfacing, *Academic Tutor*, UNSW

ADVISING

Undergraduate Honours Students

Katelyn Mak (with H. Gamaarachchi), UNSW, 2023-

PROFESSIONAL
SERVICES

External Reviewer: ASP-DAC 2024

OPEN-SOURCE
SOFTWARE

HARU: A hw-sw co-design for real-time selective sequencing on low-cost edge devices. [\[Github\]](#)

sigfish-haru: A fast selective sequencing software using HARU for acceleration. [\[Github\]](#)

RUscripts-R9: An upgraded RUscripts supporting Python3, R9 flowcell, slow5 and more. [\[Github\]](#)

HARU-HLS: An early POC for HARU using HLS and client-server architecture. [\[Github\]](#)

COMPUTER SKILLS

Programming languages: C/C++, VHDL, Verilog, Python, Go

Tools: Vivado, Vitis HLS, Chisel, PetaLinux, Yocto, Buildroot, Matlab, Wireshark

RTOS: Zephyr RTOS, FreeRTOS, ThreadX

Microprocessor architectures: ARM, RISC-V, AVR, MIPS, Xtensa

Others: eXpress Data Path (XDP), BPF, JTAG & OpenOCD

OTHER/PERSONAL

Languages: *English* (native proficiency), *Traditional Chinese Mandarin* (native proficiency)

Citizenship: *Australian*