

Лабораторная работа 2

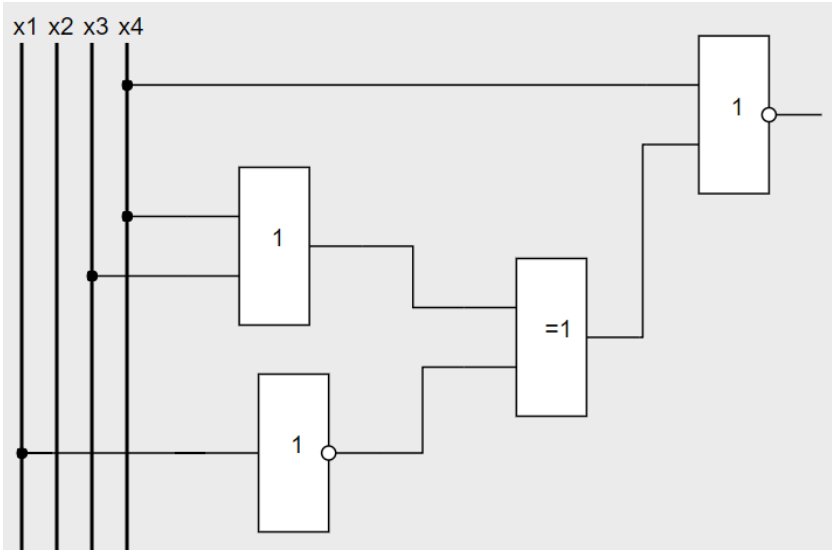
Проектирование нейронной сети на персептронах Розенблатта

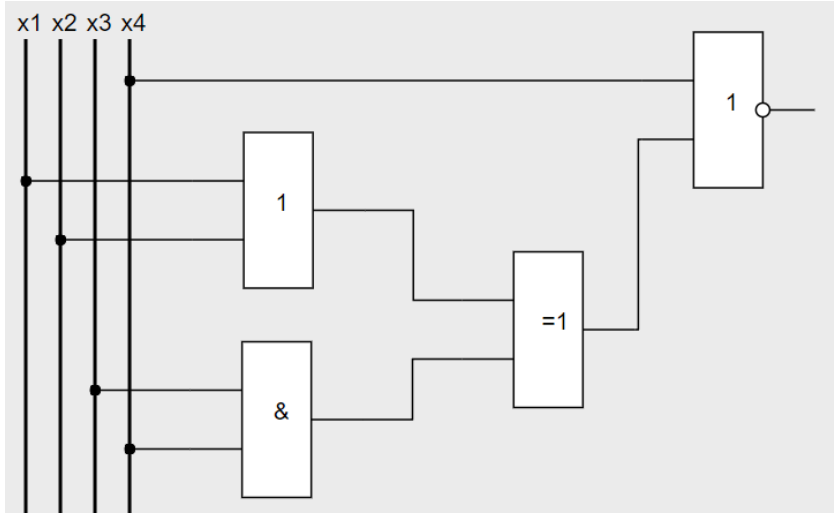
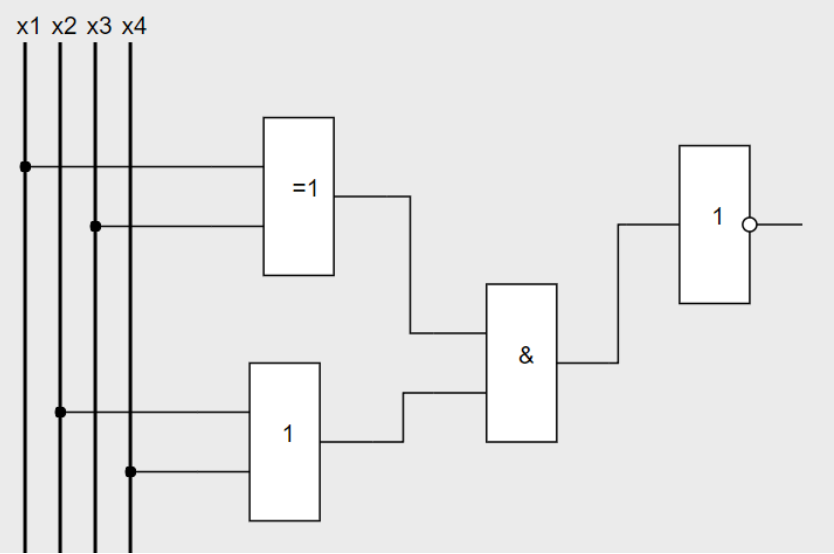
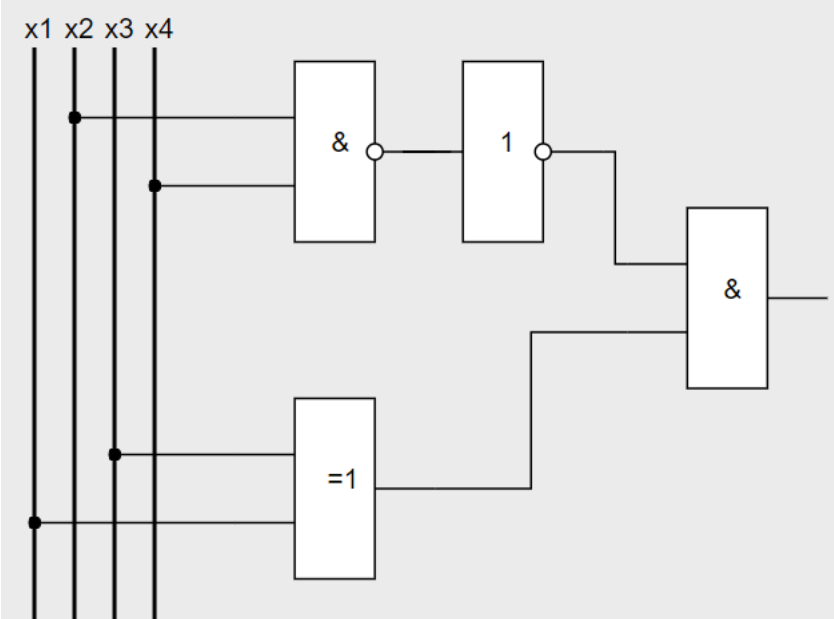
Для заданной в таблице схемы, соответствующей вашему варианту:

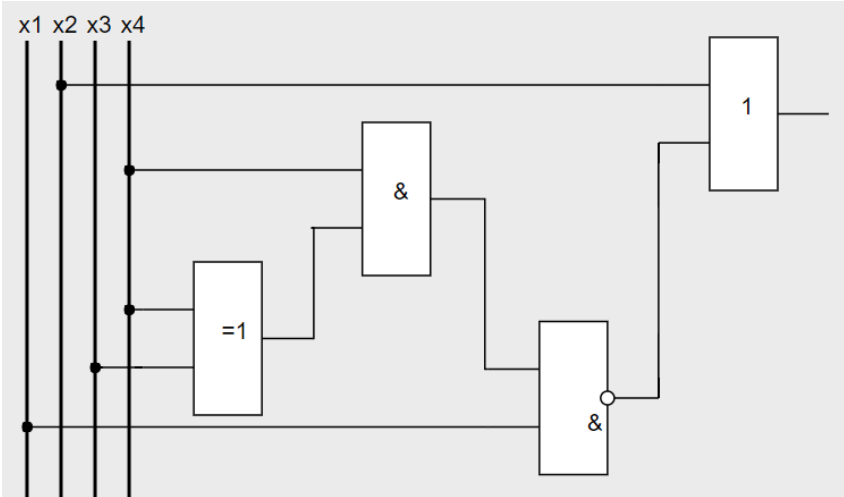
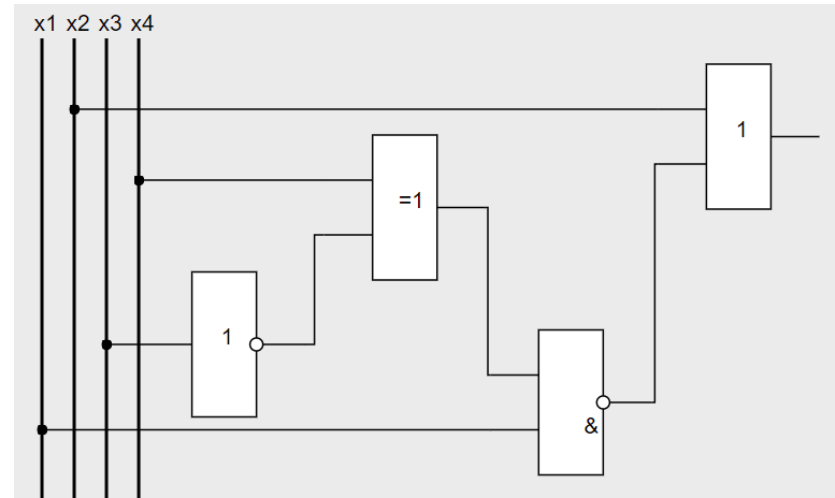
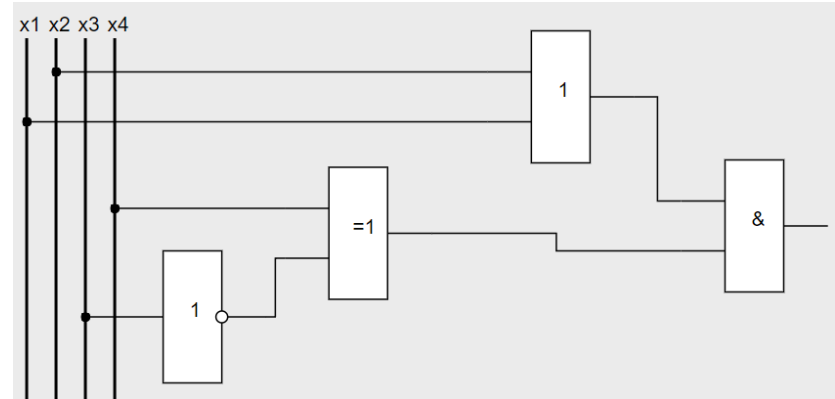
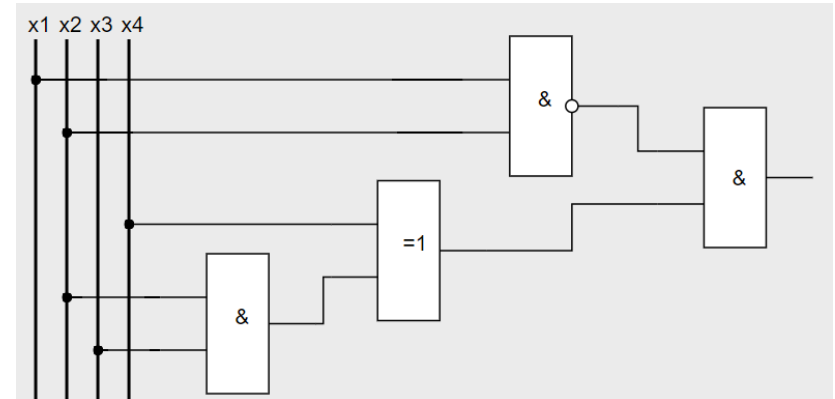
- 1) составьте таблицу истинности, включающую состояния выходов промежуточных элементов схемы;
- 2) нарисуйте нейронную сеть, реализующую полученную таблицу истинности с помощью персептронов;
- 3) напишите программу, реализующую:
 - обучение отдельных блоков нейронной сети, отвечающих за реализацию функций соответствующих логических элементов схемы;
 - вывод результатов обучения на каждой итерации обучения в текстовой и графической форме (графики) для каждого блока;
 - проверку корректной работы нейронной сети на тестовых входных данных — всех вариантах исходной таблицы истинности, с выводом таблицы истинности, аналогичной по структуре исходной таблице.

При написании программ обязательно используйте формалистику линейной алгебры (тензорное/матричное/векторное представление), применяйте скалярное произведение, используйте функции библиотеки NumPy.

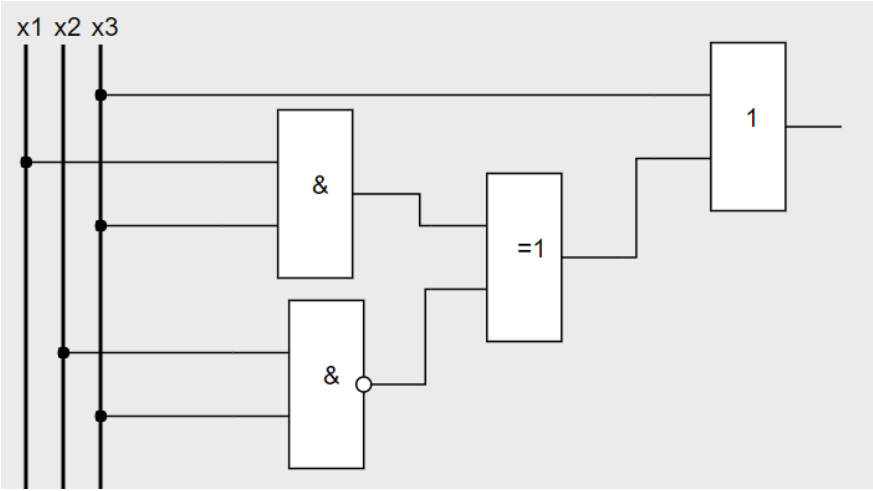
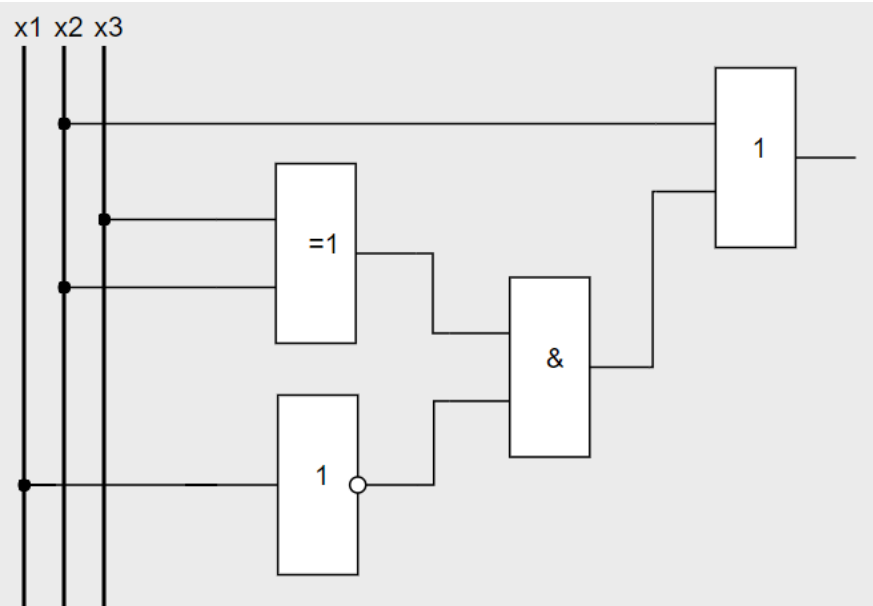
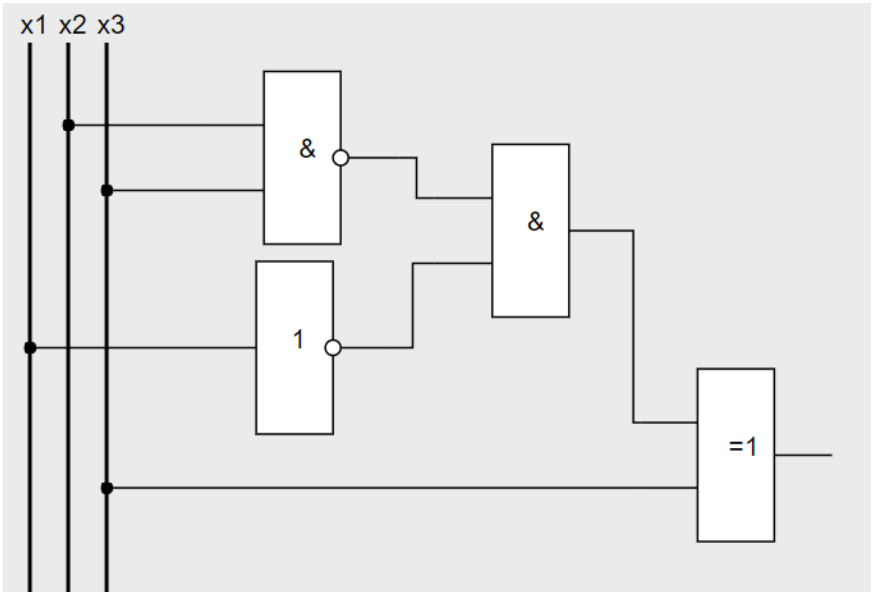
Таблица 1 — Варианты схем выбираются по порядковому номеру студента в списке группы

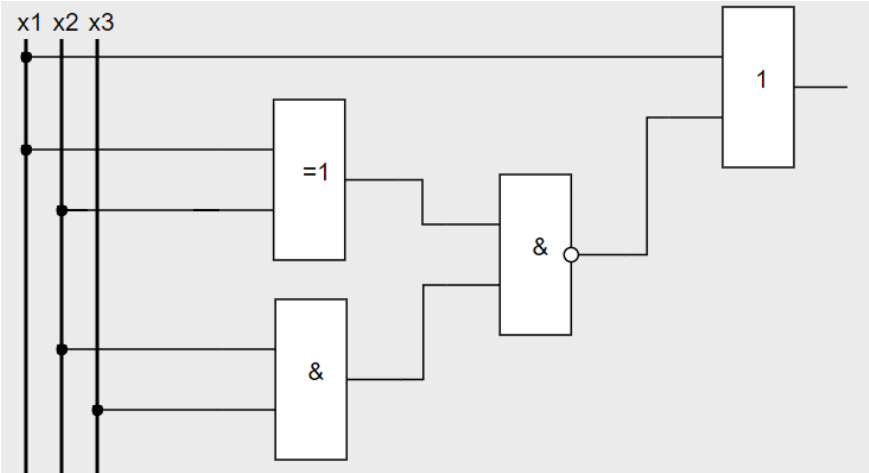
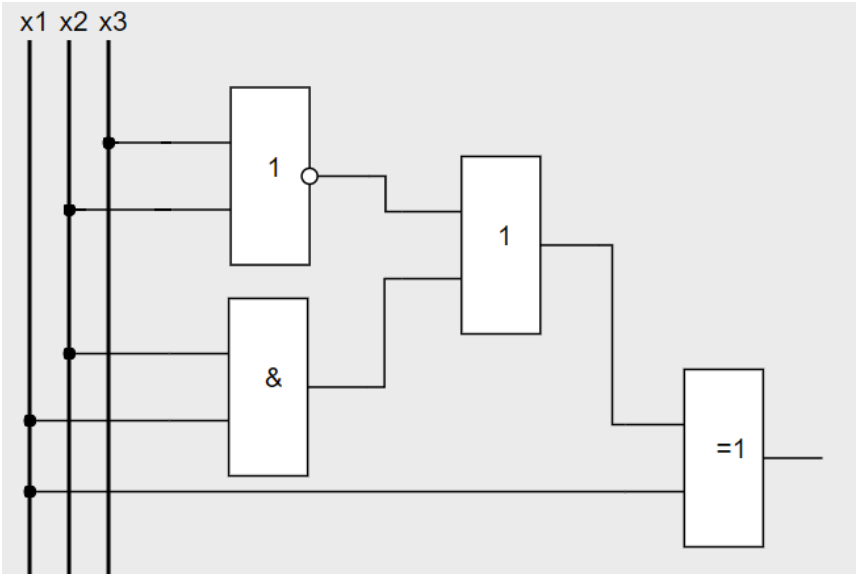
№	Схема эквивалентного устройства на логических элементах
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2	 <p>Logic circuit diagram for row 2. Inputs: x1, x2, x3, x4. The circuit consists of three logic blocks: a block labeled '1' (OR gate) with inputs x1 and x2; a block labeled '&' (AND gate) with inputs x3 and x4; and a final block labeled '1' (OR gate) with inputs from the output of the first '1' block and the output of the '&' block. The output of the final '1' block is the result of the circuit.</p>
3	 <p>Logic circuit diagram for row 3. Inputs: x1, x2, x3, x4. The circuit consists of three logic blocks: a block labeled '=1' (XOR gate) with inputs x1 and x2; a block labeled '1' (OR gate) with inputs x3 and x4; and a final block labeled '1' (OR gate) with inputs from the output of the '=1' block and the output of the '1' block. The output of the final '1' block is the result of the circuit.</p>
4	 <p>Logic circuit diagram for row 4. Inputs: x1, x2, x3, x4. The circuit consists of three logic blocks: a block labeled '&' (AND gate) with inputs x2 and x3; a block labeled '1' (OR gate) with inputs x1 and the output of the first '&' block; and a final block labeled '&' (AND gate) with inputs from the output of the '1' block and the output of a block labeled '=1' (XOR gate) with inputs x1 and x4. The output of the final '&' block is the result of the circuit.</p>

5	 <p>Logic circuit diagram for row 5. Inputs: x1, x2, x3, x4. The circuit consists of: <ul style="list-style-type: none"> A NOT gate (1) with input x2. An AND gate (&) with inputs x3 and x4. An XOR gate (=1) with inputs x1 and x3. A NOT gate (1) with input x1. An AND gate (&) with inputs (x1 NOT) and (x3 AND x4). A final AND gate (&) with inputs (x2 NOT) and the output of the previous AND gate. </p>
6	 <p>Logic circuit diagram for row 6. Inputs: x1, x2, x3, x4. The circuit consists of: <ul style="list-style-type: none"> A NOT gate (1) with input x2. An XOR gate (=1) with inputs x3 and x4. A NOT gate (1) with input x1. An AND gate (&) with inputs (x1 NOT) and (x3 XOR x4). A final AND gate (&) with inputs (x2 NOT) and the output of the previous AND gate. </p>
7	 <p>Logic circuit diagram for row 7. Inputs: x1, x2, x3, x4. The circuit consists of: <ul style="list-style-type: none"> A NOT gate (1) with input x2. An XOR gate (=1) with inputs x3 and x4. A NOT gate (1) with input x1. An AND gate (&) with inputs (x1 NOT) and (x3 XOR x4). A final AND gate (&) with inputs (x2 NOT) and the output of the previous AND gate. </p>
8	 <p>Logic circuit diagram for row 8. Inputs: x1, x2, x3, x4. The circuit consists of: <ul style="list-style-type: none"> A NOT gate (1) with input x2. An AND gate (&) with inputs x3 and x4. An XOR gate (=1) with inputs x1 and x3. A NOT gate (1) with input x1. An AND gate (&) with inputs (x1 NOT) and (x3 AND x4). A final AND gate (&) with inputs (x2 NOT) and the output of the previous AND gate. </p>

9	<p>Logic diagram for problem 9. Inputs: x_1, x_2, x_3, x_4. The circuit includes an AND gate (&) with inputs x_1 and x_2, an equality gate (=1) with inputs x_3 and x_4, a NOT gate (1) with input x_1, and a final OR gate (1) with inputs from the AND gate and the NOT gate.</p>
10	<p>Logic diagram for problem 10. Inputs: x_1, x_2, x_3. The circuit includes an equality gate (=1) with inputs x_1 and x_2, a NOT gate (1) with input x_3, an AND gate (&) with inputs from the equality gate and the NOT gate, and a final OR gate (1) with inputs from the equality gate and the AND gate.</p>
11	<p>Logic diagram for problem 11. Inputs: x_1, x_2, x_3. The circuit includes an equality gate (=1) with inputs x_1 and x_2, a NOT gate (1) with input x_3, an AND gate (&) with inputs from the equality gate and the NOT gate, and a final OR gate (1) with inputs from the AND gate and the NOT gate.</p>
12	<p>Logic diagram for problem 12. Inputs: x_1, x_2, x_3. The circuit includes two equality gates (=1), one with inputs x_1 and x_2, and another with inputs x_2 and x_3. It also includes a NOT gate (1) with input x_1, and a final AND gate (&) with inputs from the first equality gate and the NOT gate.</p>

13	 <p>Logic circuit diagram for row 13. Inputs are x1, x2, and x3. The circuit consists of two AND gates, one OR gate, and one NOT gate. The first AND gate takes x1 and x2 as inputs. The second AND gate takes x2 and x3 as inputs. The output of the first AND gate is connected to the top input of the OR gate. The output of the second AND gate is connected to the bottom input of the OR gate. The output of the OR gate is connected to the input of the NOT gate. The output of the NOT gate is the final output of the circuit.</p>
14	 <p>Logic circuit diagram for row 14. Inputs are x1, x2, and x3. The circuit consists of two AND gates, one OR gate, and one NOT gate. The first AND gate takes x1 and x2 as inputs. The second AND gate takes x2 and x3 as inputs. The output of the first AND gate is connected to the top input of the OR gate. The output of the second AND gate is connected to the bottom input of the OR gate. The output of the OR gate is connected to the input of the NOT gate. The output of the NOT gate is the final output of the circuit.</p>
15	 <p>Logic circuit diagram for row 15. Inputs are x1, x2, and x3. The circuit consists of two AND gates, one OR gate, and one NOT gate. The first AND gate takes x1 and x2 as inputs. The second AND gate takes x2 and x3 as inputs. The output of the first AND gate is connected to the top input of the OR gate. The output of the second AND gate is connected to the bottom input of the OR gate. The output of the OR gate is connected to the input of the NOT gate. The output of the NOT gate is the final output of the circuit.</p>

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