# Practical 3: FIR Filter Implementation

## Aim:

The purpose of this assignment is to implement an FIR filter in Vivado using the Xilinx FIR compiler to generate an FIR IP block. You will test this block by simulating in Vivado and measuring the amplitude of your filter output for sinusoidal inputs of various frequencies.

## Learning Outcomes:

On completing this practical you will be able to:

- Use Vivado FIR compiler to generate an IP block for use in your design
- Understand the impact of various design parameters on utilisation and system performance
- Generate sinusoidal test signals and derive their dB amplitude from the binary output of your filter

## Problem Description:

On Blackboard you will find the following files needed for the FIR test system that you will be using in this lab:

- fir_filter_test.sv
  - Top level of the DUT, instantiates the sinewave generator, FIR filter and peak detector.
- sig_gen.sv
  - Uses phase accumulator and CORDIC blocks to produce a sinusoid of tuneable frequency.
- simple_peak_detector.sv
  - Simple peak detection done by tracking maximum during one full period of test signal
- tb_fir_filter_test.sv
  - Tunes the sinusoid frequency and will be used to check amplitude_out.
- filter_taps.csv
  - Contains the floating point version of your filter taps for the lab. Assume the desired specification is
    - fc = 0.24Fs,
    - TB Width = 0.1 Fs,
    - PB Ripple = +/- 0.05dB,
    - SB Attenuation = -40dB

## Configuring the FIR IP:

To begin with you will need to add an FIR to your FPGA design using Vivado's IP Catalog. Open the IP Catalog from Project Manager, and search for FIR Compiler. Double click to begin configuring to add to your system.

In the Customize IP GUI, you can view the frequency response of the current taps and configuration. You can estimate the number of DSP slices (specialised FPGA blocks for multiply-add operations) required by your configuration under the "Detailed Implementation" tab. You will need to modify several configuration parameters and comment on their impact on the frequency performance, and the number of DSP slices to be used.

Configure the block to use the desired filter **coefficient values** from Blackboard.

Under "Channel Specification" tab, set both **input sampling frequency** and **clock frequency** to 100 MHz (our Basys3 board rate). When making this change, note the impact it has on the number of DSP slices required to implement the FIR. What causes this?

Next we want to configure the quantisation to meet the spectral requirements of our filter with the minimum possible resources. Under “Implementation”, set Quantization to “Quantize only” and modify the coefficient width and fractional length to be appropriate values for your filter tap values. Note the impact on the Frequency Response on the right hand side, and the number of DSP slices required, when you change these values. Explain what changes you see and why they occur in your report. (Note that you can assume your input data is Signed 16bit, and output data is also 16 bits noting your chosen Output Rounding Mode).

When you are content that your frequency response will meet your requirements and with the lowest number of DSP slices, you can click “Ok” and move on to simulating your FIR system.

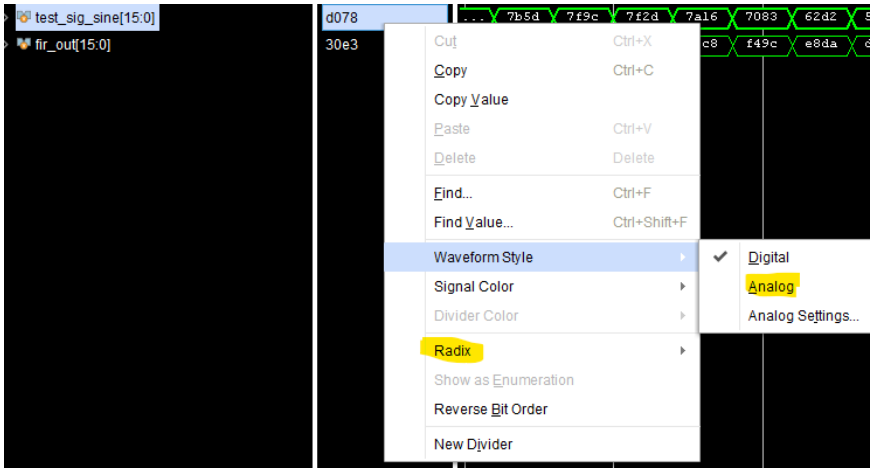
## Simulation and Testing the System:

First you should check that the FIR IP generated matches the name of the block used in fir_filter_test.sv (the default is fir_compiler_0). Once this is confirmed, you should be able to simulate the block.

You can change the frequency being generated by sig_gen using “fcw”, Frequency Control Word. This is a counter increment that should cause a 16 bit counter to wrap with the same period of your desired sinusoid. Select fcw based on the following formula:

$$\frac{2^{16}}{fcw} * T_{clk} = T_{signal}$$

You should be able to view the output of sig_gen block in your waveform as a sinusoid by selecting analog waveform style and Signed Decimal radix.




You can calculate the amplitude of your output in dB using the formula:

$$20 \log_{10} \frac{Vpeak}{Vmax}$$

Where Vpeak is the amplitude of your measured signal, and Vmax is the max possible value it could have.

For your report, modify the provided testbench to test with various sine frequencies in different parts of your frequency response. Calculate the output amplitude in dB and, comparing this to the expected frequency response, confirm that your FIR gives the desired performance. Take screen captures of your waveforms and include your calculations in your report.

## Synthesis and Implementation:

The last stage of this assignment is to run through synthesis and implementation (confirming there are no warnings or issues). In order to have realistic timing report data, you will need to add an xdc file that has defines your clock frequency (be sure that it matches the 100 MHz used in the FIR configuration!).

Once this is done you can view the WNS (Worst Negative Slack) under Timing in Project Summary. This is how much margin you have on the critical path of your system. Using this and your current clock period, calculate the Fmax of your system. Include these calculations in your report.

In your report, comment on what strategies might be used in the implementation of an FIR to improve this Fmax figure.

## Submission:

You must submit the following items in a zipped folder via Blackboard:

- Short write-up named pract3p2_surnameinitial.pdf, e.g. called pract3p2_WadeR.pdf. (Note the pdf format).
- Zip your Vivado project folder and submit it with your write-up on Blackboard.
- **Confirm that all project files are in your Vivado project folder before submission**

Deadline: **Thurs 25th of March**. Refer to first lecture for Late Assignment Policy.

## Plagiarism

'Plagiarism is interpreted by the University as the act of presenting the work of others as one's own work, without acknowledgement. Plagiarism is considered as academically fraudulent, and an offence against University discipline. The University considers plagiarism to be a major offence, and subject to the disciplinary procedures of the University.'

Above is an extract from the College Regulations on Plagiarism. Plagiarism will result in loss of **ALL** marks for this assignment, for the owners of both the original and copied work.