

4C1 Integrated Systems Design

REPORT: Lab-4 Basys3 Hex Calculator

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Calculator Design & Specifications:

1. The calculator takes a two-digit input using 4 switches per digit to capture a 16-bit binary number. Therefore, the greatest number that can be inserted is 'FF'. These numbers are displayed on the display as you enter them.
2. The result of the calculation occupies the entire seven segment to display the answer. Therefore, the greatest answer that can be displayed using the seven segment LEDs is 'FFFF'. There is no way to determine overflow in case it occurs.
3. Similarly, there is no way to determine carry value for results more than 4 hex digits.
4. Three functions namely addition, subtraction and equate have been specified to operate upon inputs. They use 'btnR', 'btnL', and 'btnC' respectively to perform these operations.
5. Additionally, a block has been created that stores the result of previous operation and can be used as an input in a new calculation.
6. Latches were not used in the design of the calculator.
7. Below is a schematic diagram of the designed Hex Calculator.

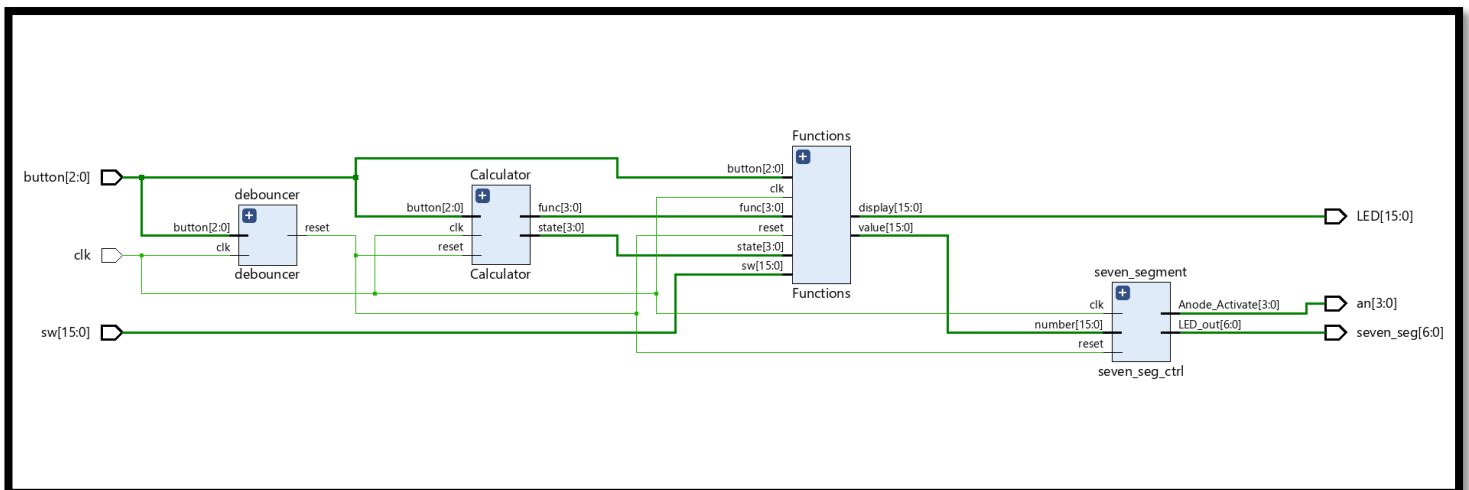


Figure 1: Schematic Diagram of Hex Calculator

Furthermore, I tried to insert more functionality to the calculator by adding more operations like multiplication and division using IP modules. I was not able to implement the functionality due to some unresolved errors.

Therefore, the designed Hex calculator is basic with just addition and subtraction operations.

Errors/Warnings:

During the generation of the bit-stream, no single warnings or errors were reported. Below attached is the project summary displaying the same.

Project Summary

Overview | Dashboard

Settings | Edit

Project name:Hex_Calculator

Project location:C:/Users/hp/Desktop/Integrated Systems Design/Hex_Calculator

Product family:Artix-7

Project part:xc7a35tcpg236-1

Top module name:Top

Target language:Verilog

Simulator language:Mixed

Synthesis

Status:Complete

Messages:No errors or warnings

Part:xc7a35tcpg236-1

Strategy:Vivado Synthesis Defaults

Report Strategy:Vivado Synthesis Default Reports

Incremental synthesis:None

DRC Violations

No DRC violations were found.

Implemented DRC Report

Implementation

Status:Complete

Messages:No errors or warnings

Part:xc7a35tcpg236-1

Strategy:Vivado Implementation Defaults

Report Strategy:Vivado Implementation Default Reports

Incremental implementation:None

Timing

Worst Negative Slack (WNS):5.847 ns

Total Negative Slack (TNS):0 ns

Number of Failing Endpoints:0

Total Number of Endpoints:299

Implemented Timing Report

Summary | Route Status

Setup | Hold | Pulse Width

Figure 2: Project Summary