Using Sound Terminal ® STA3xyBWz devices
in 2.1-channel applications

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Introduction

The purpose of the document is to show different possibilities of using STA3xyBWz devices in 2.1-channel applications.

The first part of the document is dedicated to a single device solution while the second part of the document is dedicated to a solution using two devices.

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1 Overview

In the LCD-TV market the tendency to constantly reduce the thickness of thin-screen TVs forces speaker manufacturers to design new components with very small dimensions.

The result of this process negatively impacts the quality of the sound reproduction because the frequency response of the full range is very narrow and the sensitivity is quite low.

To reduce this issue, in high-quality LCD-TV sets the speaker system is often implemented using a 2.1-channel active solution: 2 channels are dedicated to reproduce the mid and high frequencies (for both left and right channels) while the lowest portion of the audio band, usually below 200 Hz, is reproduced using a single large speaker (subwoofer channel) enclosed in a suitable box. Each speaker is driven by a dedicated power amplifier (3 in total) and the crossover filters are implemented using the DSP already present in the audio chain.

Although this solution should provide good performance, the audio quality the final user perceives is not optimal because of the inferior quality of the speakers assembled in the TV set.

All Sound Terminal® devices for the STA3xyBWz family can use different output configurations.

The standard application for this kind of device is a stereo BTL configuration for left and right channels. There are other possibilities:

1. Two BTL channels (left and right) + third channel for external bridge;

2. Two single-ended for left and right channels + third channel in BTL;

3. Mono BTL configuration.

With this scenario it is possible to have a three-channel output using one or two devices.

2 2.1-channel application using one device

2.1 Schematic

Figure 1. 2.1-channel application with one device

In this configuration only one device has been used. The CONFIG pin must be connected to GND.

2.1.1 Component selection

The selection of components is a key factor for the cost of the entire application.

The following list includes components grouped according to different sections of the schematic:

-Decoupling capacitors on VDD_DIG and PLL_VDD pins are 100 nF low voltage;

-Decoupling capacitors on VCC pins (100 nF, 1 uF and 100 uF) must be aligned with the external power supply used. If 24 V is used, the rate for the capacitors must be 35 V;

-Decoupling capacitors on the internal regulator (C6 and C7 in the schematic) can have a low voltage rate. This because they are 3.3 V regulators;

-Coil saturation current is compatible with the peak current of the application;

-The size of the resistor divider (R5, R6, R7 and R8) must be selected according to the VCC selected;

-The rate for the capacitors divider (C19, C20, C21 and C22) must be selected according to the VCC selected;

-The size of the resistor and capacitor dividers must be selected according to the output load and desired curve response. In *Section 2.1.7: DC cut*, there is a detailed explanation.

2.1.2 Decoupling capacitors

Figure 2. Schematic for decoupling
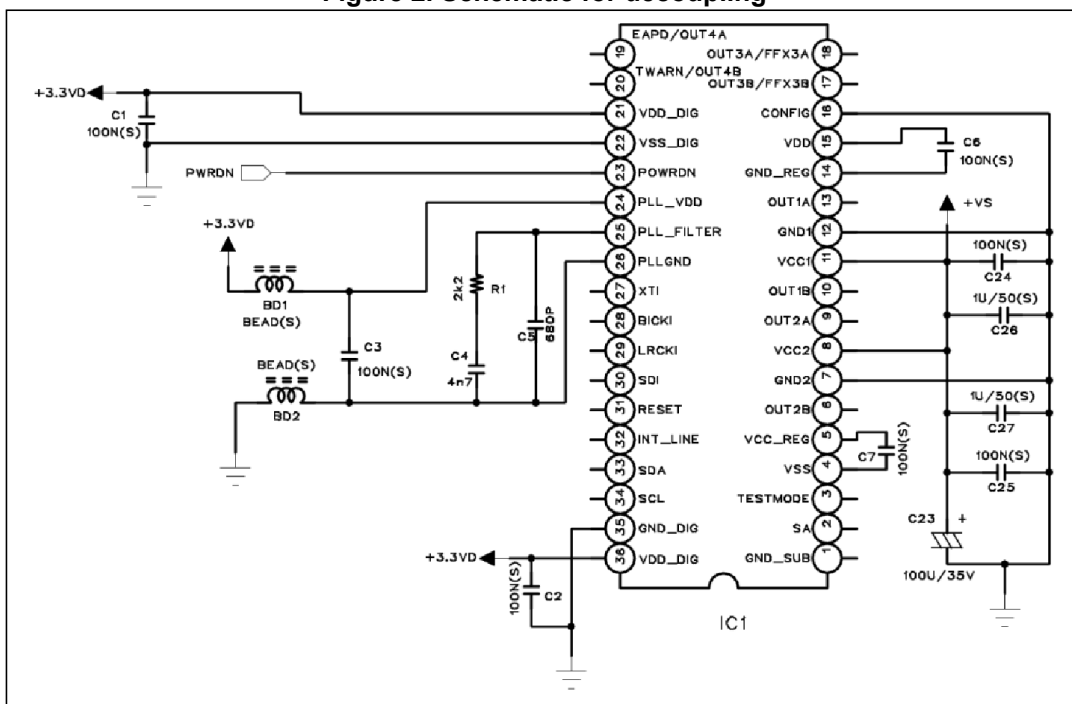
The decoupling capacitors on high-voltage pins (C24, C25, C26 and C27) must be placed as close as possible to the VCC pins. This is in order to avoid parasitic induction with the copper wires on the PC board. For each VCC pin, two capacitors are needed (100 nF and 1 µF). The meaning of each decoupling component is as follows:

- C23 is a part of the power supply and it is used as a far tank capacitor.
- The 100 nF capacitors (C24 and C25) smooth the high-frequency spikes
- The 1 µF capacitors (C26 and C27) smooth the low-frequency spikes and they are also used as a close tank for the 100 nF capacitor.

The decoupling capacitors on the VDD_DIG and PLL_VDD pins (C1, C2 and C3) are placed close the pins.

The reason that the VDD_DIG and PLL_VDD pins are separated with beads is to avoid high frequencies on VDD_DIG. It is possible to eliminate these components if the layout is done with a right star connection.

The decoupling capacitors on the regulators (C6 and C7) are also placed close to the device.

All decoupling capacitors must be X7R. This dielectric is preferable because the X7R capacitor is stable over temperature changes (±15%).

For example, the Y5V dielectric is very unstable (specs are +22% -82%).

The following figure shows the THD at different values of the tank capacitor (C23) in the ST demo board using the bench power supply. The minimum THD is similar using 10 µF or 1000 µF capacitors. The main difference is at medium-high power where the tank is not enough to guarantee the peak current.
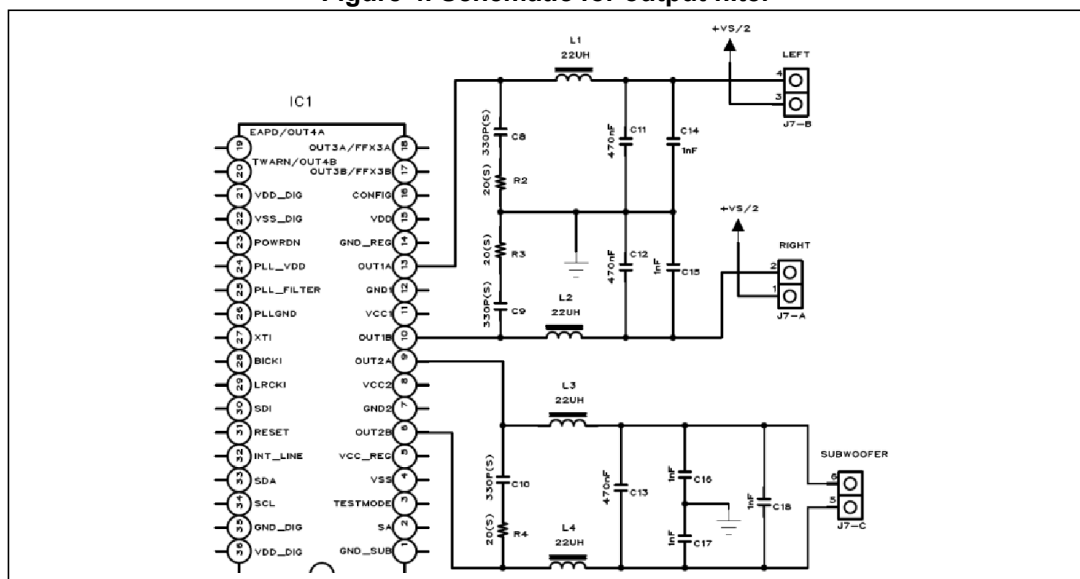
Figure 3. THD + Noise ratio with different values of the tank capacitor
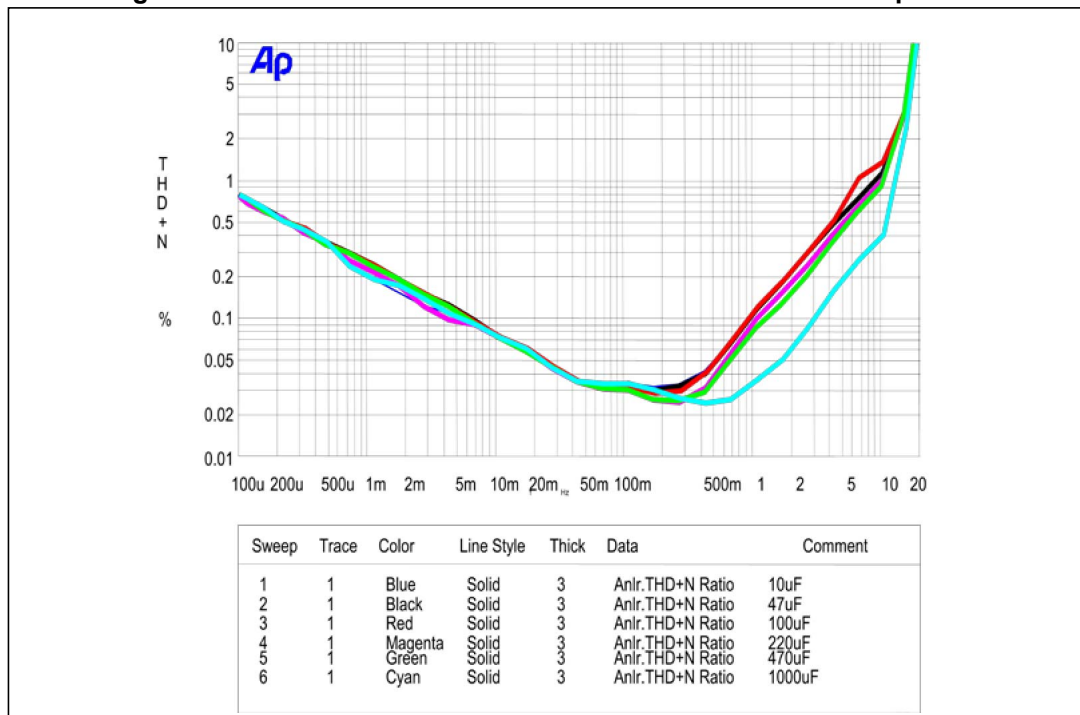
2.1.3 Output filter

Figure 4 shows the output filter scheme for a 2.1-channel application.
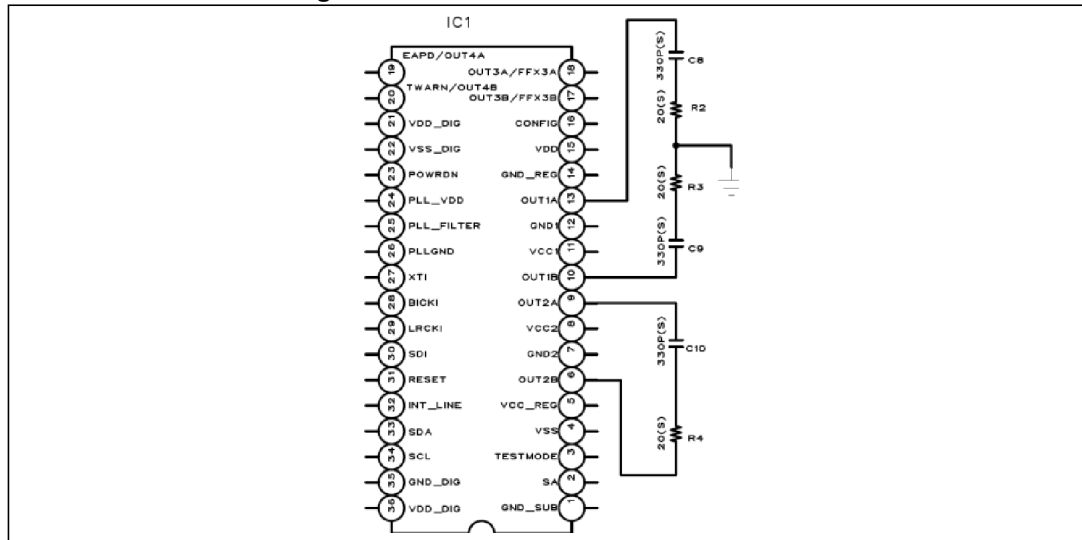
Figure 4. Schematic for output filter

The output filter is composed of three different sections:

- Snubber network
- Main filter
- EMI filter

2.1.4 Snubber network

Figure 5. Schematic for snubber section

The function of a snubber network is to absorb energy from reactance in the power circuit. The purpose of the RC snubber is to avoid unnecessary high pulse energy such as a spike in the power circuit which is dangerous to the system. By using the snubber network, the energy (big spike) is transferred within the snubber network, allowing safe operation of the system.

The snubber network is a part of the schematic that is layout dependent. The values shown in the schematic (R = 22 ohm, C = 330 pF) represent the best solution for the ST demo board.

In *Figure 5* there are two types of snubber: BTL and single-ended.

Differential snubber

The power on this network is dependent on the power supply, frequency and capacitor value using the following formula:

$$P_{Diff} = C * f * (2 * V_{CC})^2$$

The power must be dissipated on the series resistor.

Single-ended snubber

This type of snubber is used to increase the efficiency or, otherwise, must be used if the output configuration is single-ended. In a single-ended snubber the power on the network is:
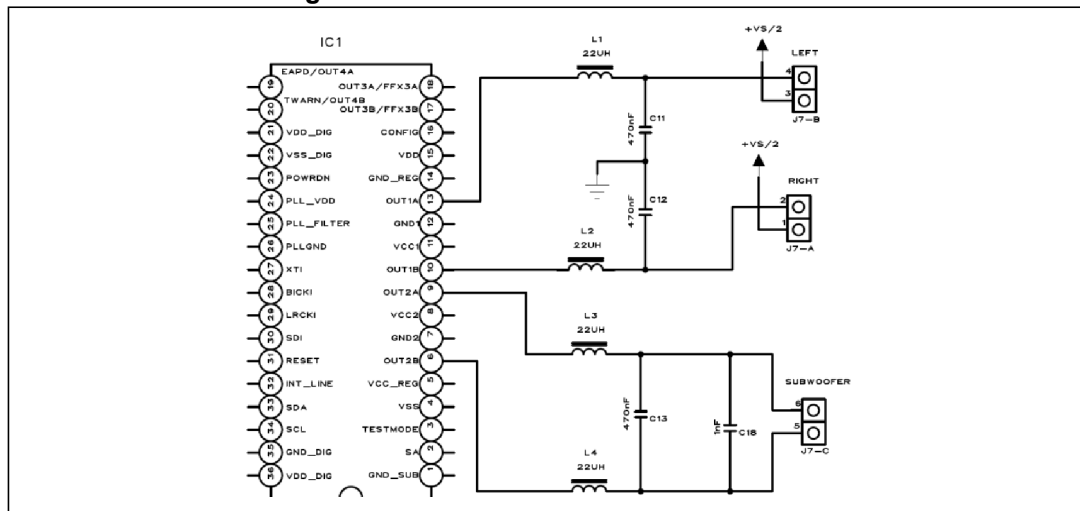
Equation 1

2.1-channel single device - power on snubber

$$P_{SE} = C * f * (V_{CC})^2$$

$$P_{SE} = P_{Diff} / 4$$

2.1.5 Main filter

Figure 6. Schematic for main filter section

The purpose of the main filter is to cut off the frequency above the audible range of 20 kHz. The main filter is designed using the Butterworth method to define the cutoff frequency. In order to have a clean amplifier, a cutoff frequency above 20 kHz is mandatory.

For class-D amplifiers, the output load is a part of the filter. The following formulas are used to verify the values of the LC components.

Equation 2

Main filter equation for SE and BTL

$$C_{load} = C11 = C12 = C13 = \frac{1}{2 \bullet \pi \bullet R_{load} \bullet f_{cutoff}} \bullet L_{load} = L3 = L4 = \frac{R_{load}}{2 \bullet \pi \bullet \sqrt{2} \bullet f_{cutoff}}$$

$$L_{SE} = L1 = L2 = \frac{R_{load}}{\pi \bullet \sqrt{2} \bullet f_{cutoff}}$$

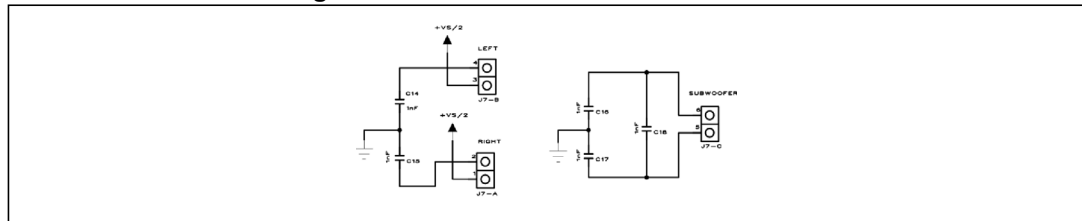$$f_{cutoff} = \frac{1}{2 \bullet \pi \bullet \sqrt{2 \bullet L_{load} \bullet C_{load}}}$$

Following table show typical component value for standard output load.

Table 1. Component values for 2.1-channel, single-device applications

R_{load}	8 Ω	6 Ω	4 Ω	3 Ω
L1, L2	47 µH	33 µH	22 µH	15 µH
C11, C12	390 nF	470 nF	680 nF	1 µH
L3, L4	22 µH	15 µH	10 µH	10 µH
C13	470 nF	680 nF	1 µF	1 µF

2.1.6 EMI filter

Figure 7. Schematic for EMI filter section

The purpose of the EMI filter is to avoid radiated emission. It is composed of two 1 nF capacitors that must be connected to GND. The values of these capacitors must be trimmed in the application.

2.1.7 DC cut

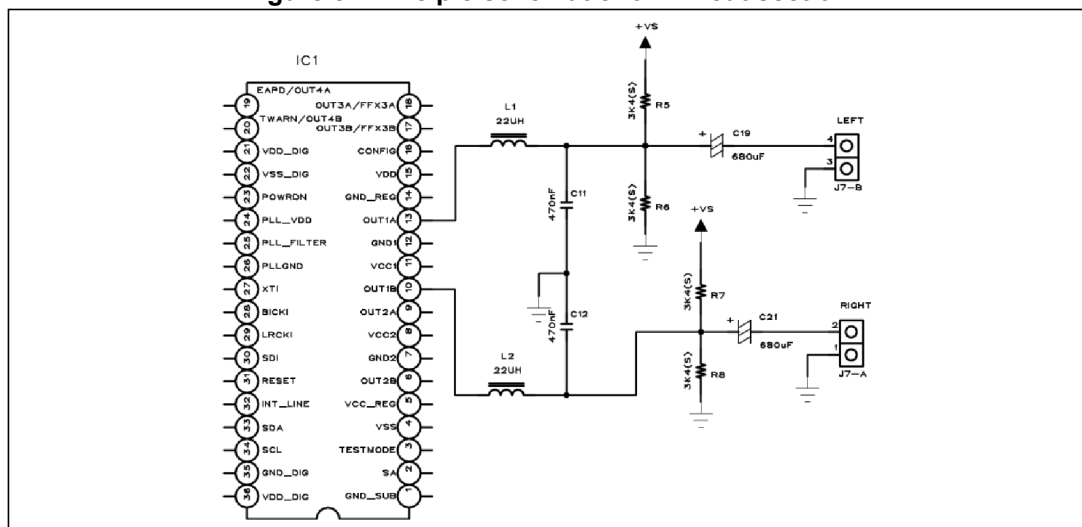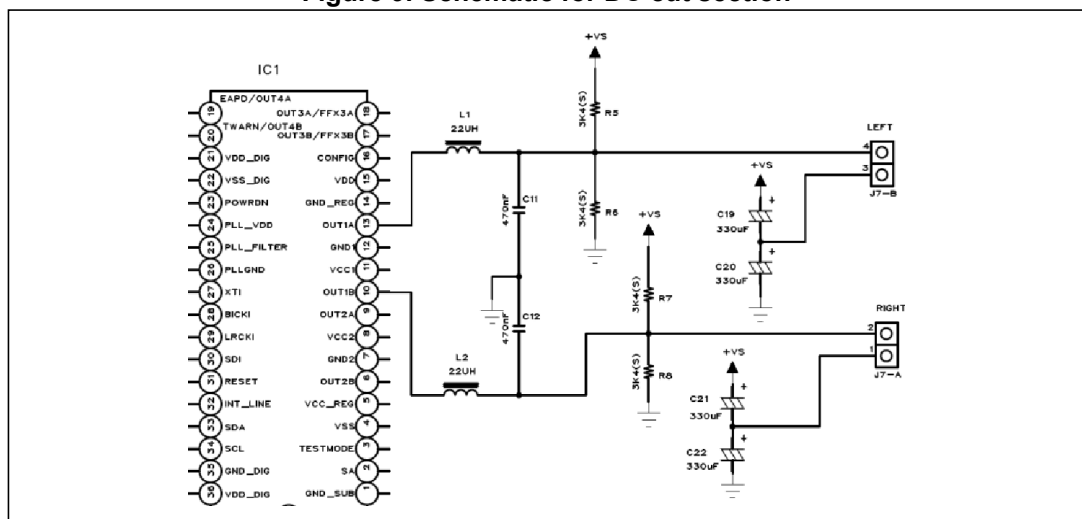**Figure 8. Principle schematic for DC cut section**

Figure 9. Schematic for DC cut section

In single-ended applications the output signal must vary between -Vcc/2 and +Vcc/2 instead of -Vcc +Vcc as in BTL mode. For this reason a dedicated electrolytic capacitor must be connected between the PWM output and speaker as shown in *Figure 8*.

The purpose of the resistive divider (R5 and R6 for OUT1, R7 and R8 for OUT2) is to take the output at half the supply when the device is in tri-state. The aim is to charge slowly the decoupling capacitor at the turn-on of the power supply in order to avoid "pops".

The value of the electrolytic capacitor is related to the load impedance and the lower limit of the audio bandwidth. The value is determined using the following formula:

Equation 3

Series capacitor value in SE configuration

$$C_{19} = C_{21} = \frac{1}{2 \bullet \pi \bullet f_{3dB} \bullet Z_{spkr}}$$

To improve the audio performance (pop and noise) and to reduce the size of components, it is possible to split the electrolytic capacitor into two capacitors of equal value (half the value), as shown in *Figure 9*.

In this case the output speaker is not connected to GND, but it is connected to the same potential as the PWM output (virtual GND). To avoid a "pop", the bridge must be muted for 4 or more R * C time constant where R = R7 and C = C22.

The recommended schematic is shown in *Figure 9*.

Table 2. DC cut - resistor and capacitor values

Rload	8 Ω	6Ω	4 Ω	3 Ω
R5, R6, R7, R8	6.2 kΩ	4.7 kΩ	3.3 kΩ	2.7 kΩ
C19, C20, C21, C22	82 µF	100 µF	180 µF	220 µF

2.2 Software configuration

In order to set the device in 2.1-channel configuration, change the register configuration 0x05 (configuration register F) from 0x5C (default) to 0x5D.

To switch on the power bridge, set to one the bit D7 of register 0x05.

3 2.1-channel applications using two devices

3.1 Schematics

Figure 10. Schematic of stereo BTL configuration
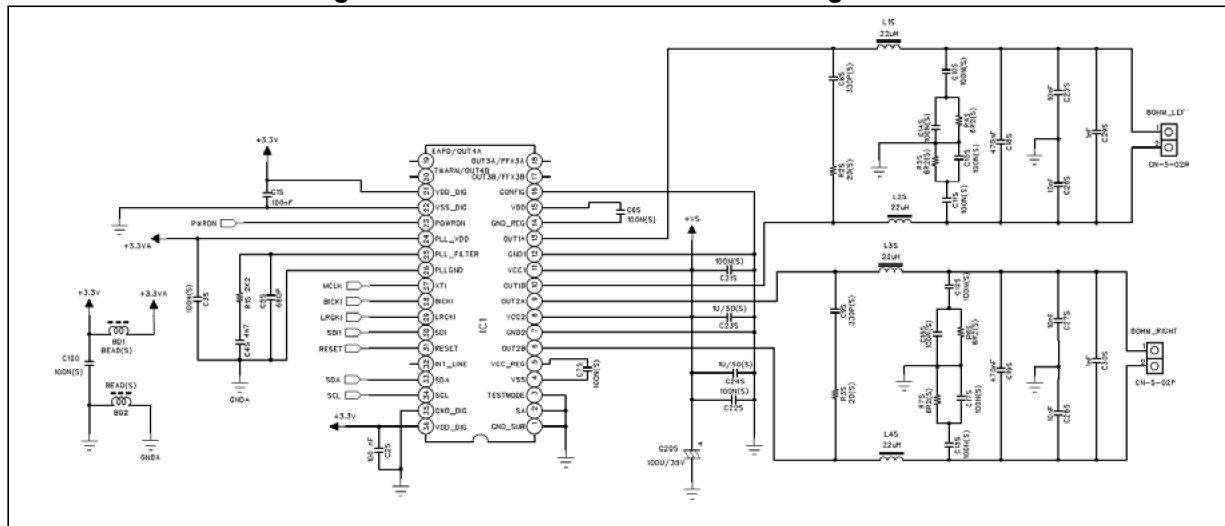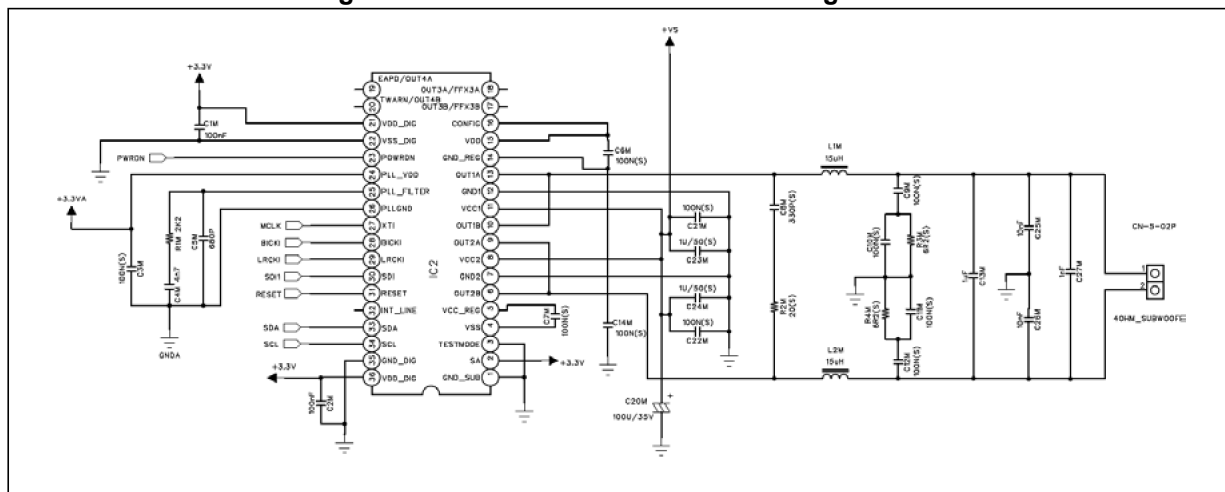

Figure 11. Schematic of mono BTL configuration

In this configuration, two devices must be used.

The I^{2}C address pin (SA) must be set to 0 in one device and to 3.3 V in the other.

The CONFIG pin must be connected to GND for the device that is configured in stereo BTL mode and it must be connected to Vdd (pin 15) for the device that is configured in mono BTL.

3.1.1 Component selection

The selection of components is a key factor for the cost of the whole application.

The following list includes components grouped according to different sections of the schematic:

- Decoupling capacitors on VDD_DIG and PLL_VDD pins are 100 nF low voltage;

- Decoupling capacitors on VCC pins (100 nF, 1 µF and 100 µF) must be aligned with the external power supply used. If 24 V is used, the rate for the capacitors must be 35 V;

- Decoupling capacitors on the internal regulator (C6S, C6M, C7S, C7M and C14M in the schematic) can have a low-voltage rate. This because they are 3.3 V regulators;

- Coil saturation current must be compatible with the peak current of the application.

3.1.2 Decoupling capacitors

Figure 12. Schematics for decoupling
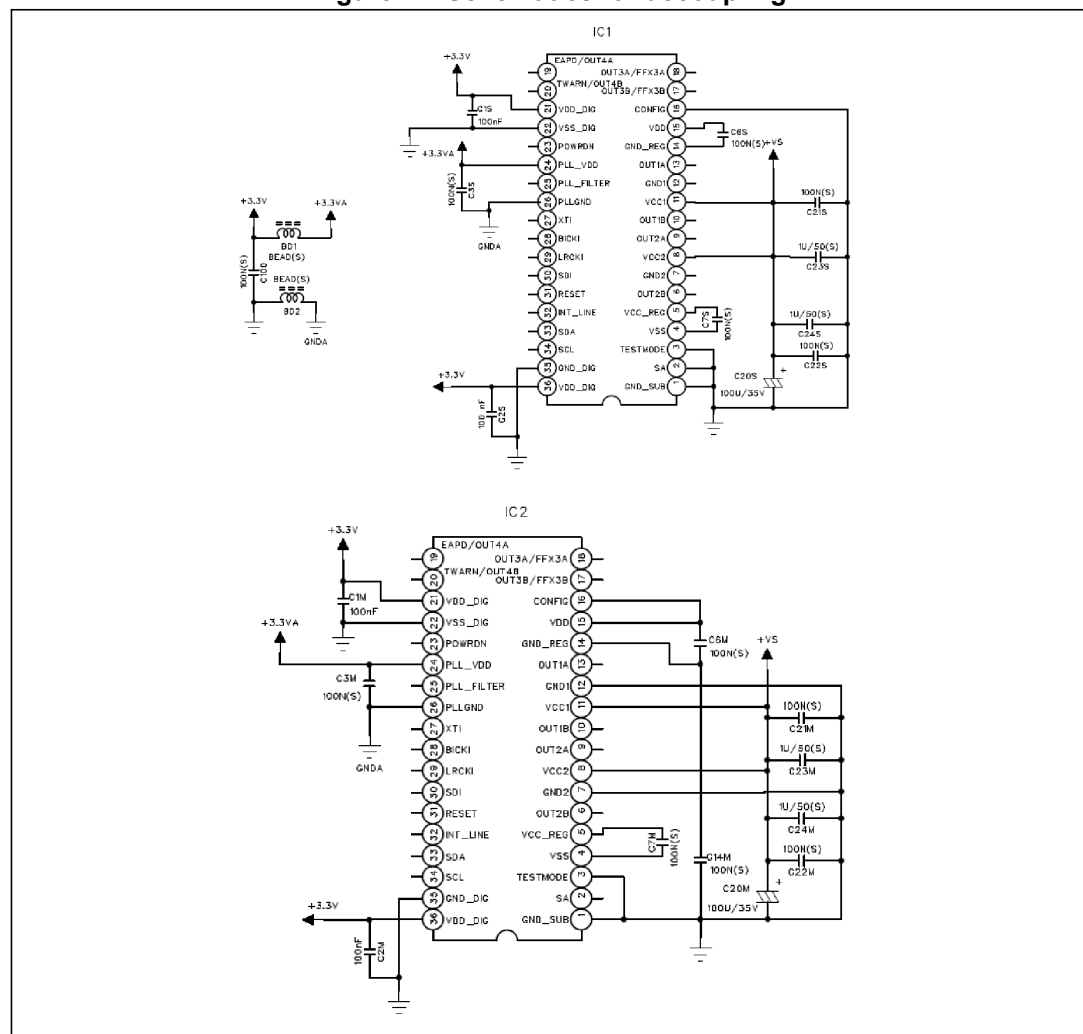
The decoupling capacitors on high-voltages pins, (C21S/M, C22 S/M, C23 S/M and C24 S/M) must be placed as close as possible to the VCC pins. This is in order to avoid parasitic

inductance with the copper wires on the PC board. For each VCC pin, two capacitors are needed (100 nF and 1 µF). The meaning of each decoupling component is as follows:

- C23S and C24M are part of the power supply and they are used as a far tank capacitor.
- The 100 nF capacitors (C24S, C24M, C25S and C25M) smooth the high-frequency spikes
- The 1 µF capacitors (C26 and C27) smooth the low-frequency spikes and they are also used as a close tank for the 100 nF capacitor.

The decoupling capacitors on the VDD_DIG and PLL_VDD pins (C1, C2 and C3) are placed close to the pins.

The reason why the VDD_DIG and PLL_VDD are separated with beads is to avoid high frequencies on VDD_DIG. It is possible to avoid these components if the layout is done with the right star connections.

Decoupling capacitors on regulators (C6 and C7) are placed close to the device.

All decoupling capacitors must be X7R. This is because the X7R capacitor is stable over temperature (±15%).

For example, the Y5V dielectric is very unstable (specs are +22% -82%).

The next figure shows THD at different values of the tank capacitor (C23) in the ST demo board using the bench power supply. The minimum THD is similar using 10 µF or 1000 µF capacitors. The main difference is at medium-high power where the tank is not sufficient to guarantee the peak current.
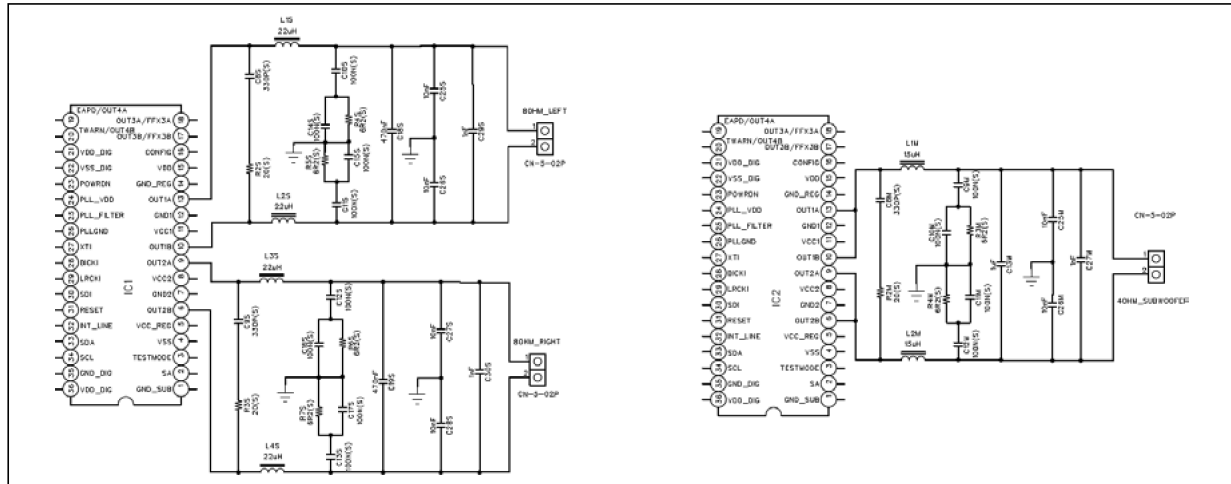
Figure 13. THD+Noise ratio with different values of the tank capacitor
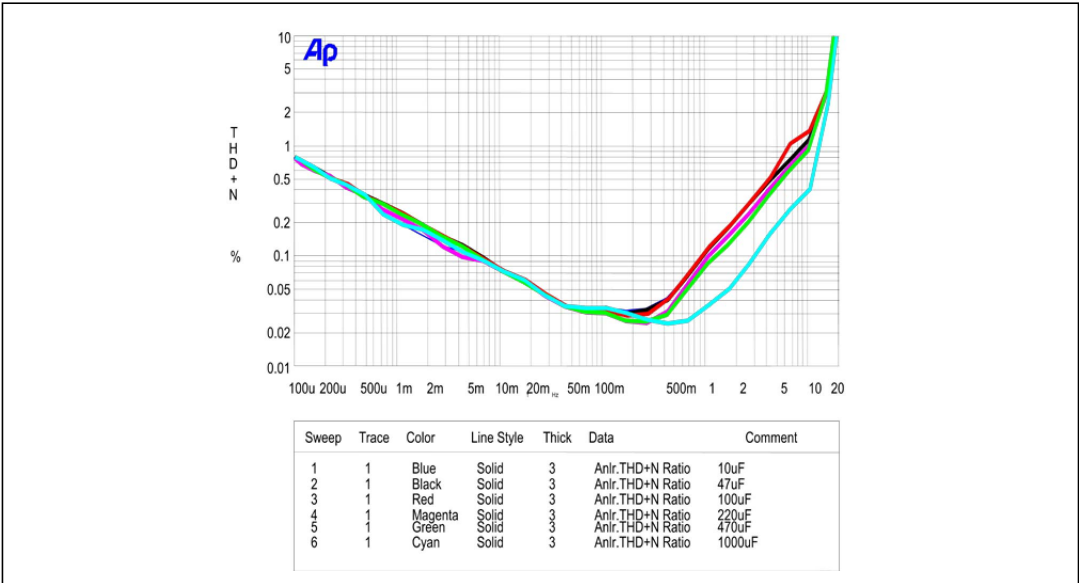
3.1.3 Output filter

Figure 14 shows the output filter scheme for a 2.1-channel application.

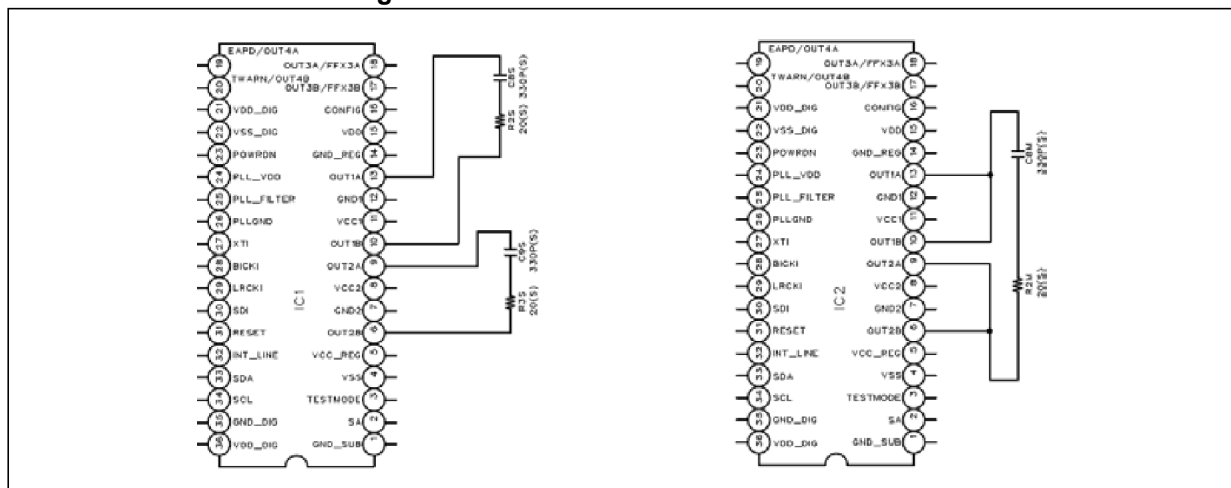**Figure 14. Schematics for output filter**

The output filter is composed of three different sections:

- Snubber network
- Main filter
- EMI filter

3.1.4 Snubber network

Figure 15. Schematics for snubber section

The function of a snubber network is to absorb energy from reactance in the power circuit. The purpose of the RC snubber is in order to avoid unnecessary high pulse energy such as spike in power circuit which is dangerous to the system. By using the snubber network, the energy (big spike) is transferred within the snubber network, allowing safe operation of the system.

The snubber network is a part of schematic that is layout dependent. The values shown in the schematic (R = 22 ohm, C = 330 pF) represent the best solution for the ST demo board.

In *Figure 15* there are two types of snubber: BTL and single-ended. It is possible to select a differential or single-ended snubber according to the power dissipation on the resistor and within layout constraints.

Differential snubber

The power on this network is dependent on the power supply, frequency and capacitor value using the following formula:

$$P_{Diff} = C \bullet f \bullet (2 \bullet V_{CC})^2$$

The power must be dissipated on the series resistor.

Single-ended snubber

This type of snubber is used to increase the efficiency or, otherwise, must be used if the output configuration is single-ended. For a single-ended snubber the power on the network is given in the equation below.
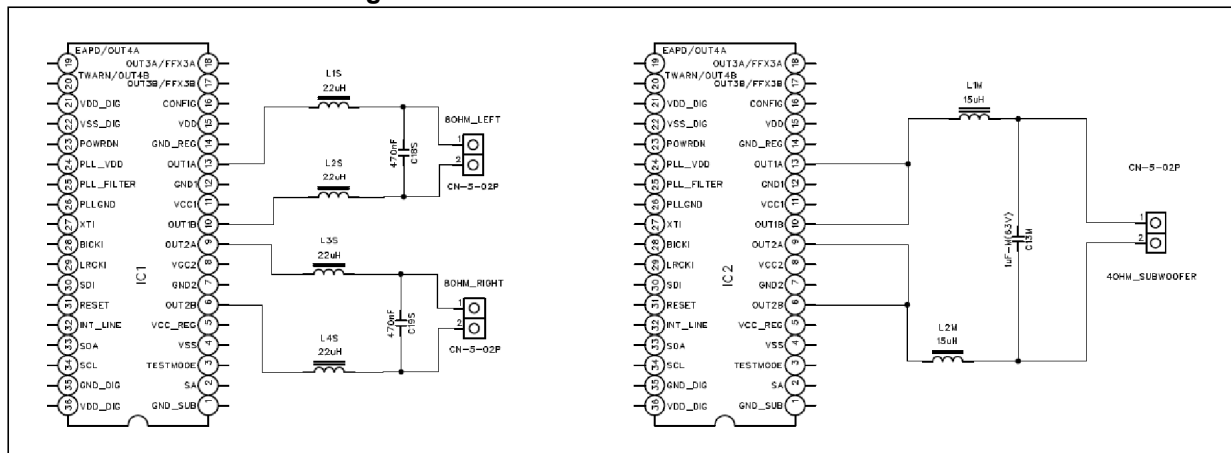
Equation 4

2.1 channels, two devices - power on snubber

$$P_{SE} = C \bullet f \bullet (V_{CC})^2$$

$$P_{SE} = P_{Diff} / 4$$

3.1.5 Main filter

Figure 16. Schematics for main filter section

The purpose of the main filter is to cut off the frequency above the audible range of 20 kHz. The main filter is designed using the Butterworth method to define the cutoff frequency. In order to have a clean amplifier, a cutoff frequency above 20 kHz is mandatory.

For class D amplifiers, the output load is a part of the filter. The following formulas are used to verify the values of LC components.

Equation 5

2.1 channels, two devices - main filter

$$C_{load} = C11 = C12 = C13 = \frac{1}{2 \bullet \pi \bullet R_{load} \bullet f_{cutoff}}$$

$$L_{load} = L1S = L2S = L3S = L4S = L1M = L2M = \frac{R_{load}}{2 \bullet \pi \bullet \sqrt{2} \bullet f_{cutoff}}$$

$$f_{cutoff} = \frac{1}{2 \bullet \pi \bullet \sqrt{2 \bullet L_{load} \bullet C_{load}}}$$
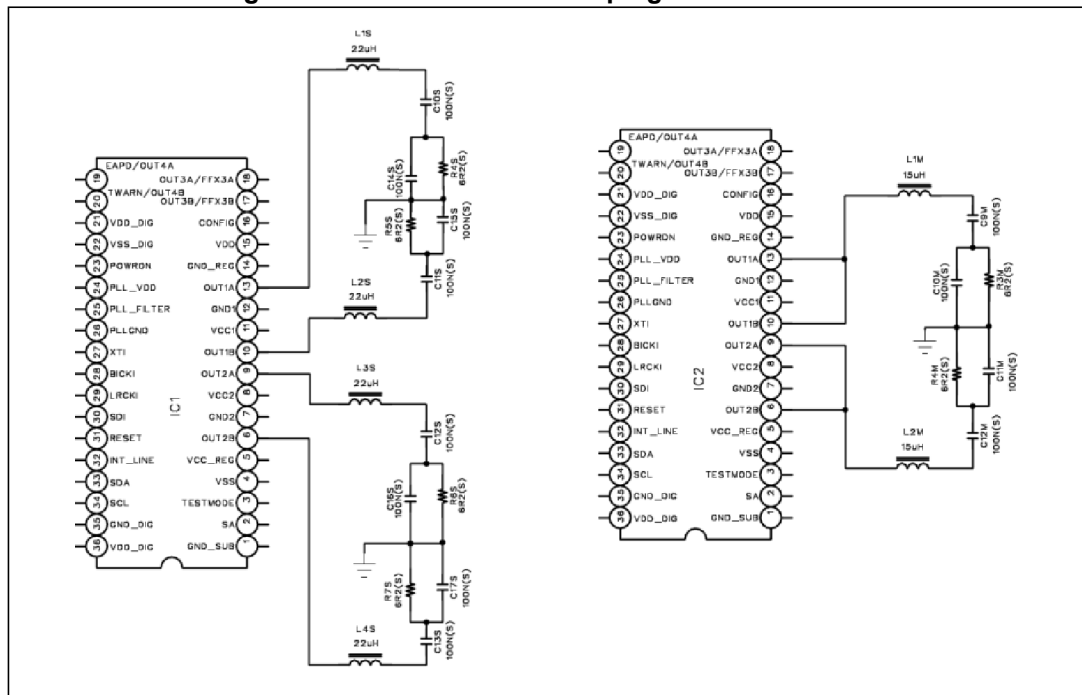
The following table shows the recommended values for the components.

Table 3. Component values for 2.1-channel applications, two devices

R_{load}	8 Ω	6 Ω	4 Ω	3 Ω
L1S, L2S, L3S, L4S, L1M, L2M	22 µH	15 µH	10 µH	10 µH
C18S, C19S, C13M	470 nF	680 nF	1 µF	1 µF

3.1.6 Damping network

Figure 17. Schematics for damping network section

The purpose of the damping network is to avoid the high-frequency oscillation issue on the output circuit. After using the damping network the THD can be improved and the damping network can also avoid the inductive copper on the PCB routing when the system is working on high frequency with the PWM or PCM.

The C-R-C is mainly intended for high inductive loads.

The following table shows the recommended values for the components.

Table 4. 2.1 channels, two devices - damping network values

R_{load}	8 Ω	6 Ω	4 Ω	3 Ω
C10S, C11S, C12S, C13S, C9M, C12M	100 nF	100 nF	220 nF	220 nF
C14S, C15S, C16S, C17S, C10M, C11M	100 nF	100 nF	220 nF	220 nF
R4S, R5S, R6S, R7S, R3M, R4M	6.2	4.7	3.3	2.7

3.1.7 EMI filter

Figure 18. Schematics for EMI filter section
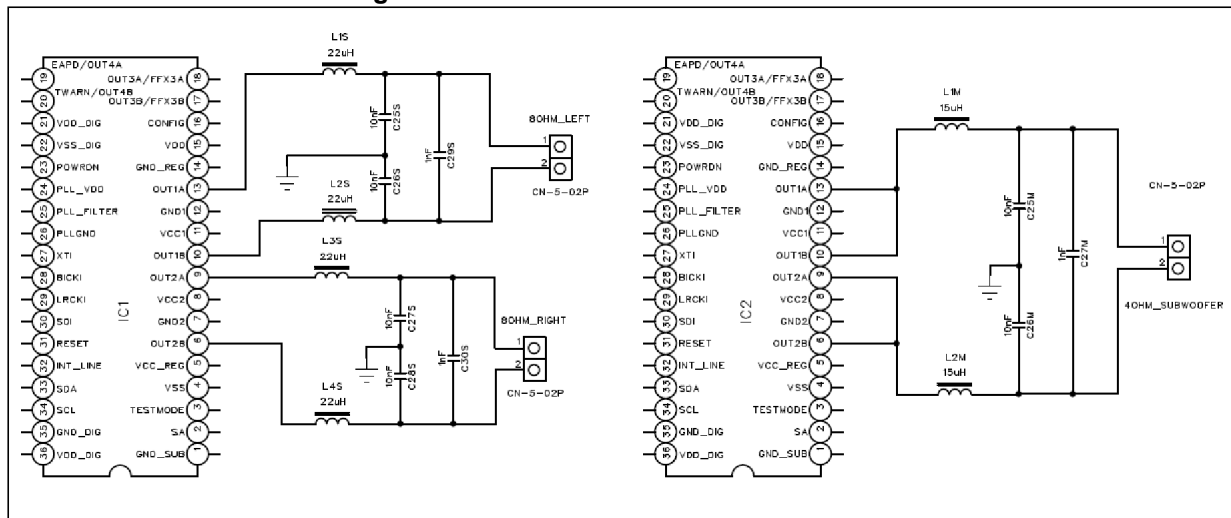
The purpose of the EMI filter is to avoid radiated emission. It is composed of three capacitors: two 10 nF capacitors must be connected to GND and one 1nF capacitor must be connected parallel to the speaker. The values of this capacitor must be trimmed in the application.

3.2 Software configuration

No SW modifications are needed for the device that works in stereo BTL mode.

For the device that works in mono BTL mode, change the register configuration 0x05 (configuration register F) from 0x5C (default) to 0x5F to set to a single channel configuration.

To switch on the power bridge, set to one the bit D7 of register 0x05.

To adjust the volume using a mono BTL device, change the channel 3 volume register (address 0x0A).

4 Layout

4.1 Decoupling

- Use electrolytic capacitors first to separate the Vcc branches;

Figure 19. Electrolytic capacitor

Separate from the E-cap
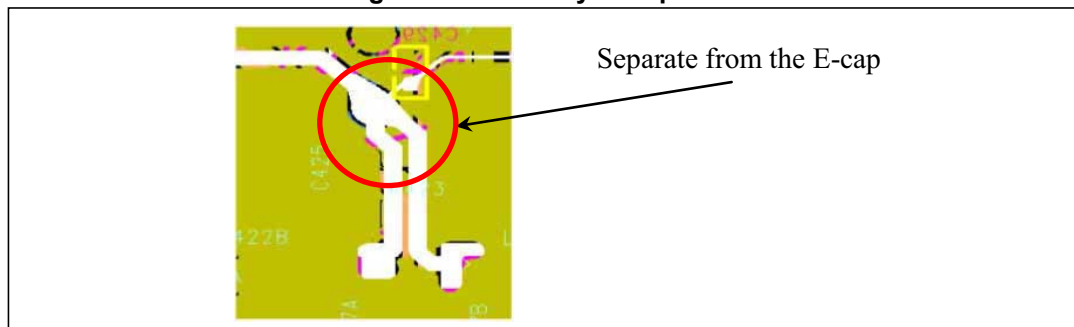
- Minimize the path between the Vcc pins and ground pin in order to avoid inductive paths;

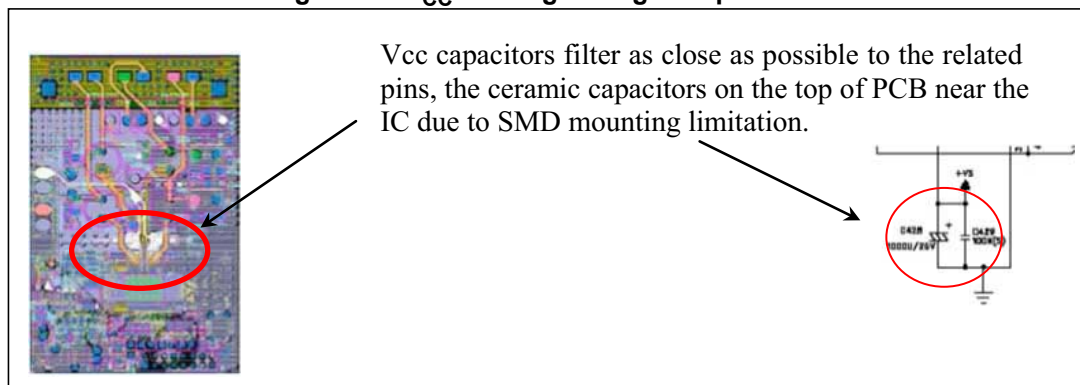**Figure 20. V_{CC} - GND paths**

V_{CC} and ground
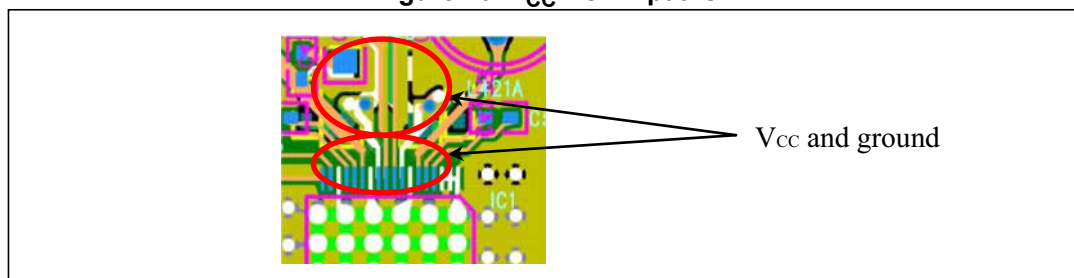
- Vcc routing. The purpose of a "star routing" for the Vcc supply is in order to avoid the interference between different signals such as part A idle and another part B working with full load. Under this condition the interference would evidently happen if no star connection were implemented.

Figure 21. Star connection
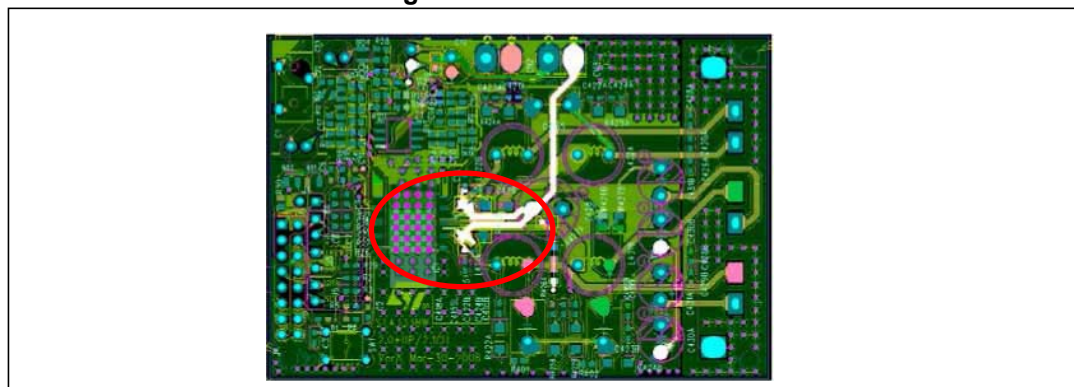
- Vcc filter for high frequency

Figure 22. V$_{CC}$ filtering for high frequencies

Vcc capacitors filter as close as possible to the related pins, the ceramic capacitors on the top of PCB near the IC due to SMD mounting limitation.

The purpose of this filter is to avoid an inductive coil generated by the copper wire because the system is working in PWM with fast switching (the frequency is about 340 kHz) so the longer copper wire can easily become an inductor. To improve this we recommend using a ceramic capacitor to balance the reactance. The ceramic capacitor must be placed as close as possible to the related pins. The recommended distance between the capacitor to the related pins is 5 mm maximum.

- Decoupling capacitors

Solder the decoupling capacitors as close as possible to the related IC pin, the purpose of which is to reduce the inductive coil with copper wire (parasitic inductor).

Figure 23. Correct layout for decoupling capacitors
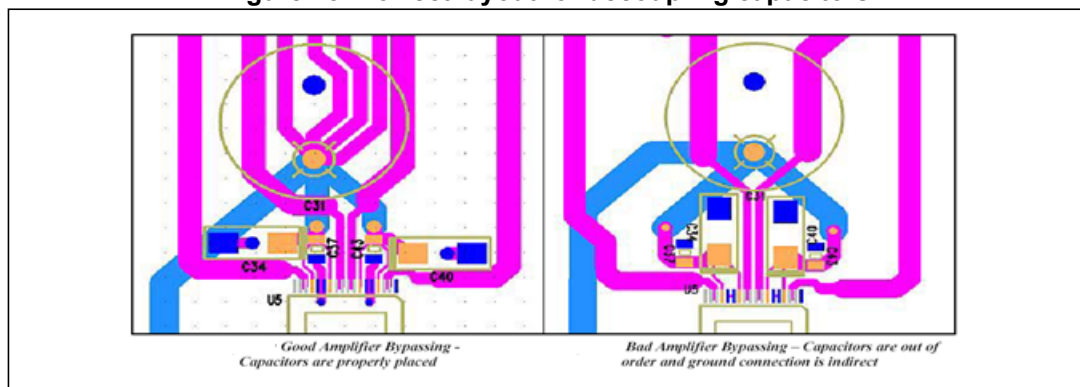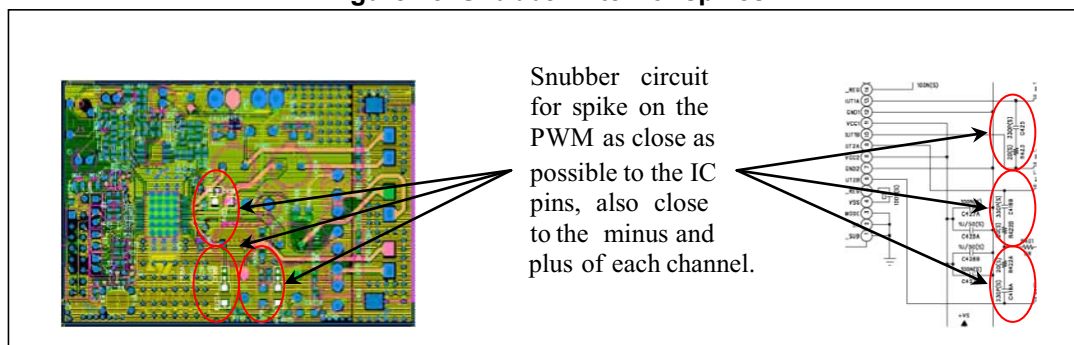
4.2 Snubber

- Solder the snubber network as close as possible to the related IC pin;

Figure 24. Snubber network
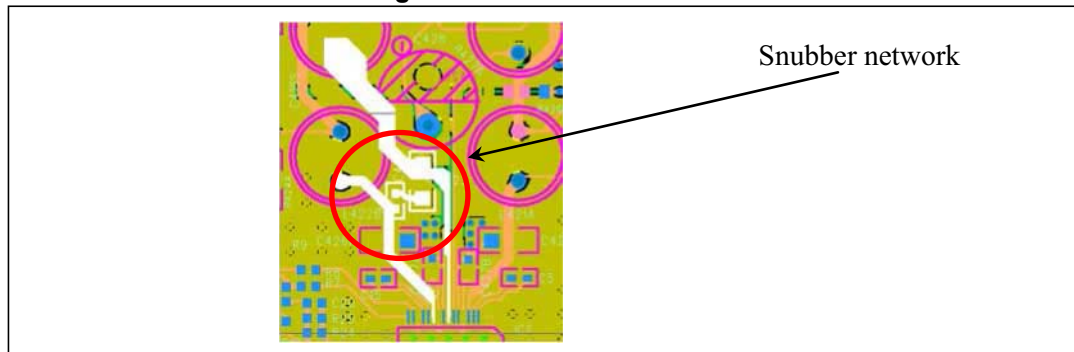
- Snubber filter for high-frequency spike on the PWM;

Figure 25. Snubber filter for spikes

Snubber circuit for spike on the PWM as close as possible to the IC pins, also close to the minus and plus of each channel.

As shown in the figure below, there are two different examples given (single-ended and differential snubber networks).

Figure 26. Differential and single-ended layout for snubber network

Good Common-Mode Snubber Placement *Good Differential Snubber Placement*
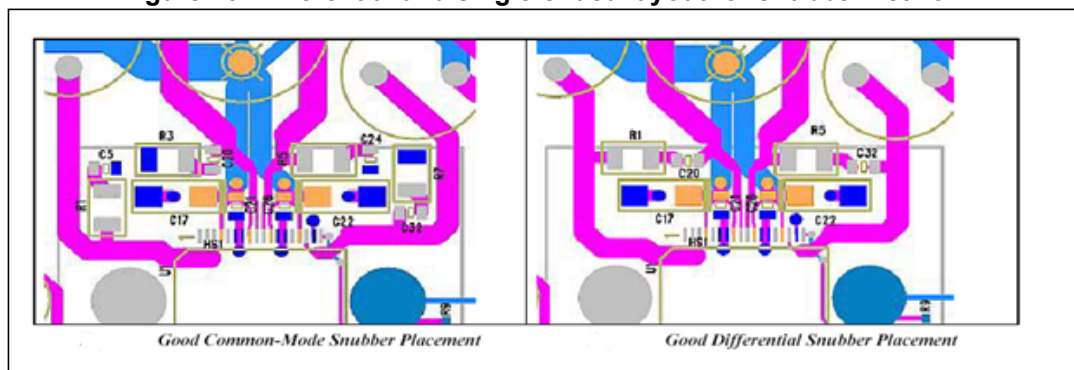
A strong spike could happen if there is a long distance between the snubber network and the pins, the IC could even be burnt by the big spike. It's recommended that the distance between snubber network be within 3 mm, which takes into consideration the width of the copper wire.

4.3 PLL filter

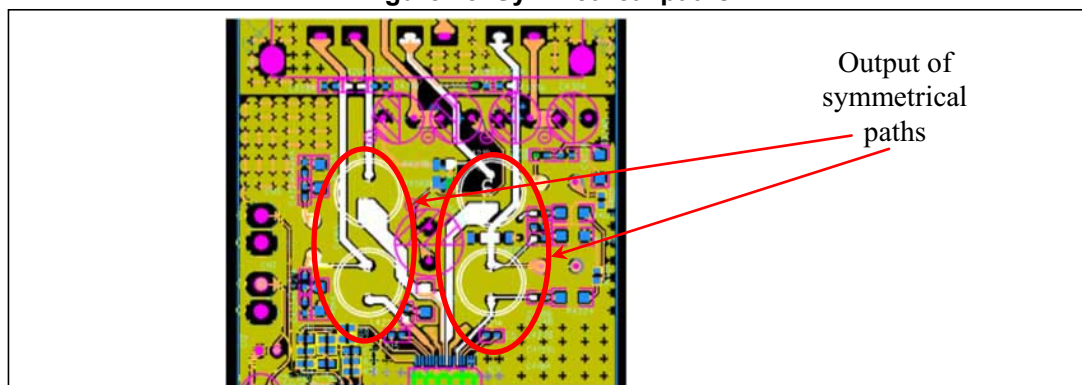- Solder the PLL filter as close as possible to the FILT pin;

Figure 27. PLL filter
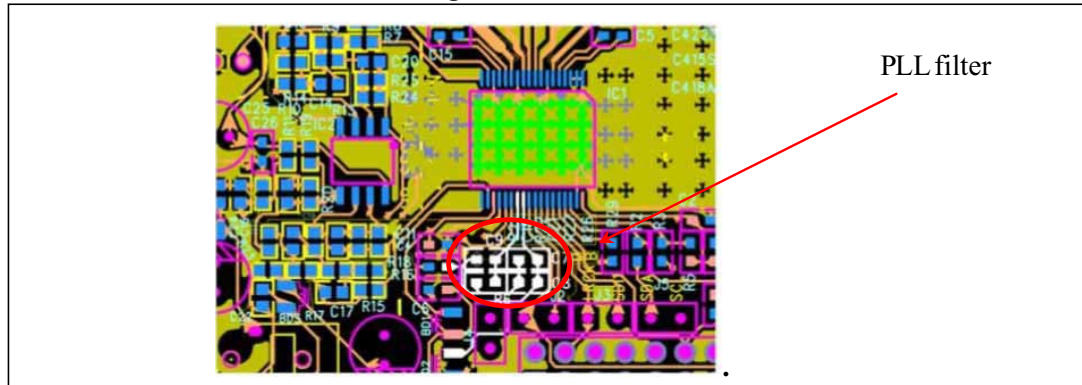
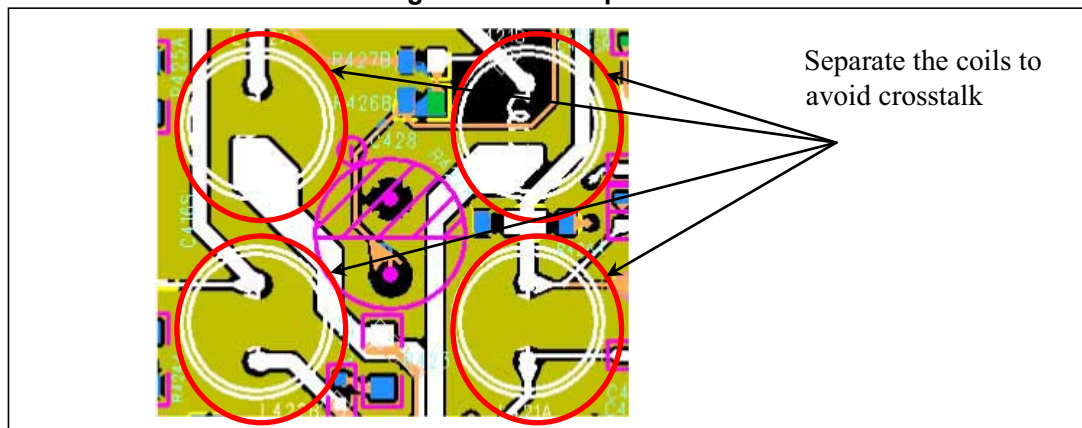## 4.4 Audio performance

- For differential applications create symmetrical paths for the output stage;

Figure 28. Symmetrical paths

- Separate the coil in order to avoid crosstalk;

Figure 29. Coil separation

- Ground consideration of layout. To avoid interference between power ground and small signal ground, the different ground planes must be separated as shown in the following figure.

Figure 30. Different GND planes

- Output routing

Figure 31. Output routing

Good Output Routing
Traces grow wider as space allows
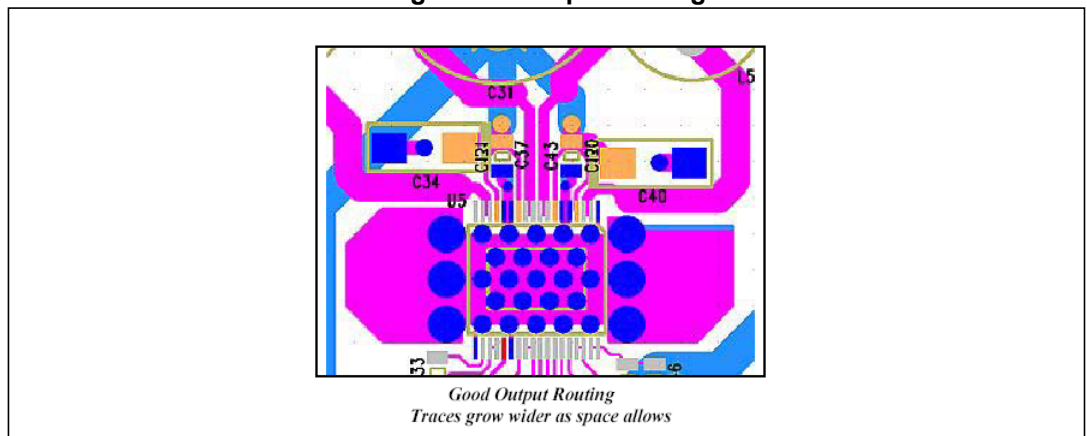
Figure 32. Good and bad output routing

Good Output Routing
Area between outputs is small

Bad Output Routing
Area between outputs is large
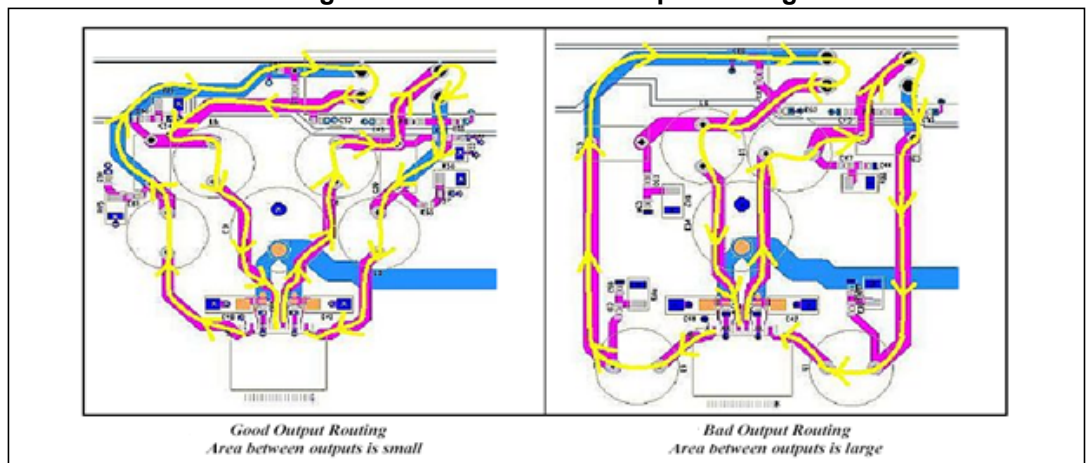
4.5 Thermal dissipation

- To dissipate heat, it is mandatory to have a big ground plane on both (top and bottom) layers and solder the slug on the PCB;
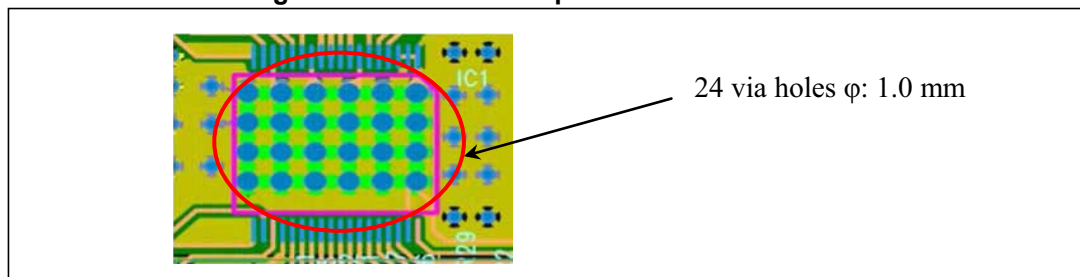
Figure 33. Thermal dissipation

Big ground plane
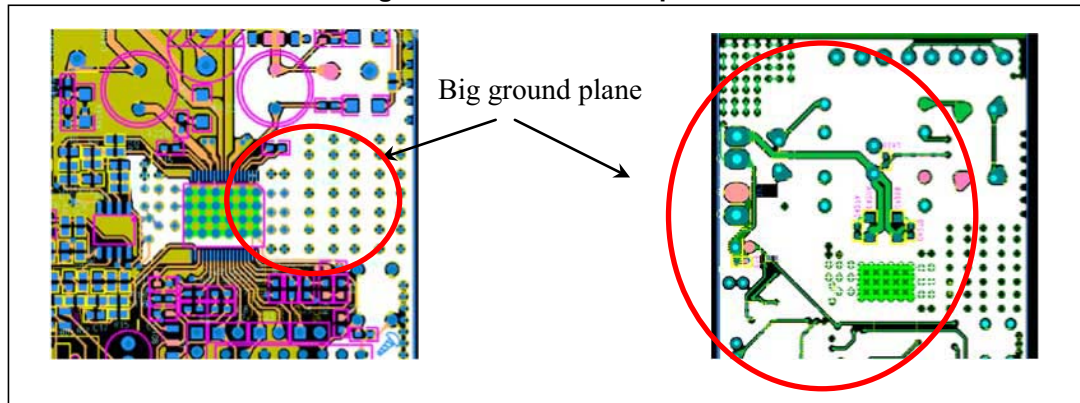
- Thermal layout with big ground (1/3 for top and bottom layers)

Figure 34. Thermal layout for top and bottom layer

Thermal layout on top layer

Thermal layout on bottom layer
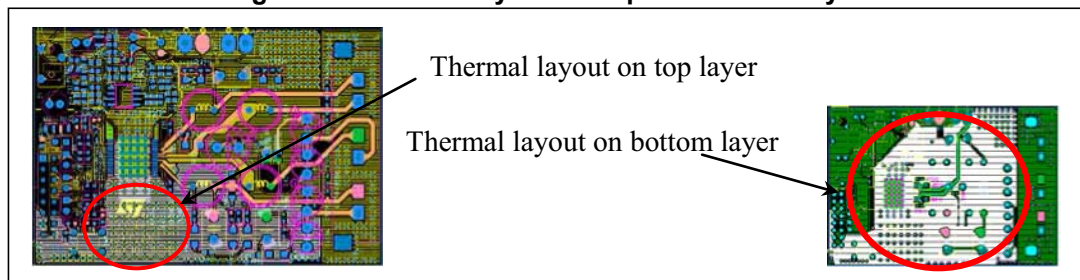
- Thermal layout with large ground (2/3 for thermal and soldering holes)

Figure 35. Thermal dissipation - holes under IC

24 via holes φ: 1.0 mm

The thermal resistance junction in the bottom of the STA3xyBWz in order to maintain ambient temperature is obtainable with a ground copper area of 4x4 cm and with 24 via holes (refer to the example shown in the figure above).

5 Conclusion

For 2.1-channel applications, the better choice in terms of audio quality is to use two different ICs (one in stereo BTL mode and the other one configured in mono BTL).

If two ICs are selected, the mono BTL device must use an additional capacitor between the GND_REG pin and GND plane.

If two ICs are selected, it is possible configure the output filter as filter-lite. Using a 2.1-channel configuration with only one IC, all PWM outputs are configured in binary modulation and for this reason it is not possible to use a filter-lite solution.

If it is mandatory to use all SMD components in the whole application (for example in TV applications due to thickness constraints), the only possibility is to use two ICs because for Left and Right channels it is mandatory to use two electrolytic capacitors for the channel.

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
13-Oct-2014	1	Initial release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY