IPC-2221B
2012 - November

Generic Standard on Printed Board Design

Supersedes IPC-2221A
May 2003

A standard developed by IPC

Association Connecting Electronics Industries

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In May 1995 the IPC's Technical Activities Executive Committee (TAEC) adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

Standards Should:

- Show relationship to Design for Manufacturability (DFM) and Design for the Environment (DFE)
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

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- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

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IPC-2221B

Generic Standard on Printed Board Design

Developed by the IPC-2221 Task Group (D-31b) of the Rigid Printed Board Committee (D-30) of IPC

Supersedes:
IPC-2221A - May 2003
IPC-2221 - February 1998

Users of this publication are encouraged to participate in the development of future revisions.

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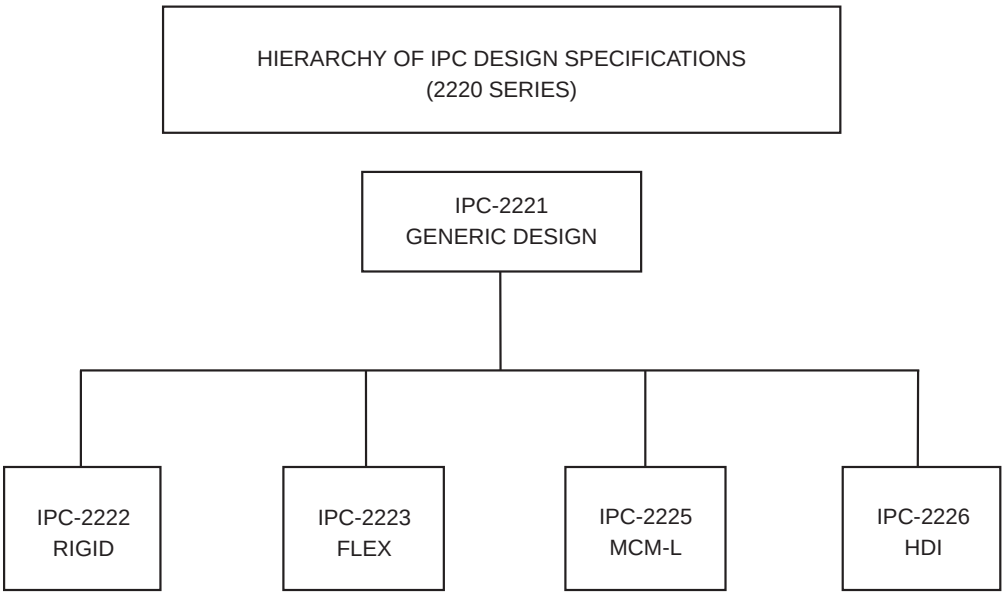

FOREWORD

This standard is intended to provide information on the generic requirements for organic printed board design. All aspects and details of the design requirements are addressed to the extent that they can be applied to the broad spectrum of those designs that use organic materials or organic materials in combination with inorganic materials (metal, glass, ceramic, etc.) to provide the structure for mounting and interconnecting electronic, electromechanical, and mechanical components. It is crucial that a decision pertaining to the choice of product types be made as early as possible. Once a component mounting and interconnecting technology has been selected the user should obtain the sectional document that provides the specific focus on the chosen technology.

It may be more effective to consider alternative printed board construction types for the product being designed. As an example the application of a rigid-flex printed wiring board may be more cost or performance effective than using multiple printed wiring boards, connectors and cables.

IPC's documentation strategy is to provide distinct documents that focus on specific aspect of electronic packaging issues. In this regard document sets are used to provide the total information related to a particular electronic packaging topic. A document set is identified by a four digit number that ends in zero (0).

Included in the set is the generic information which is contained in the first document of the set and identified by the four digit set number. The generic standard is supplemented by one or many sectional documents each of which provide specific focus on one aspect of the topic or the technology selected. The user needs, as a minimum, the generic design document, the sectional of the chosen technology, and the engineering description of the final product.

As technology changes specific focus standards will be updated, or new focus standards added to the document set. The IPC invites input on the effectiveness of the documentation and encourages user response through completion of ''Suggestions for Improvement'' forms located at the end of each document.

Acknowledgment

Any document involving a complex technology draws material from a vast number of sources. While the principal members of the IPC-2221 Task Group (D-31b) of the Rigid Printed Board Committee (D-30) are shown below, it is not possible to include all of those who assisted in the evolution of this Standard. To each of them, the members of the IPC extend their gratitude.

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Generic Standard on Printed Board Design

1 SCOPE

This standard establishes the generic requirements for the design of organic printed boards and other forms of component mounting or interconnecting structures, including PC card form factors. The organic materials may be homogeneous, reinforced, or used in combination with inorganic materials; the interconnections may be single, double, or multilayered.

1.1 Purpose The requirements contained herein are intended to establish design principles and recommendations that **shall** be used in conjunction with the detailed requirements of a specific interconnecting structure sectional standard (see 1.2) to produce detailed designs intended to mount and connect components. This standard is not intended for use as a performance specification for finished printed boards nor as an acceptance document for electronic assemblies.

1.2 Documentation Hierarchy This standard identifies generic physical design principles, and is supplemented by various sectional standards that provide sharper focus on specific aspects of printed board technology. These include:

IPC-2222 Rigid organic printed board design
IPC-2223 Flexible printed board design
IPC-2225 Organic, MCM-L, printed board design
IPC-2226 High Density Interconnect (HDI) printed board design

The documents are a part of the Family of Design Documents which is identified as IPC-2220. The number IPC-2220 is for ordering purposes only and includes this standard and the four listed above.

Note: IPC-2224, a sectional design standard for PC card form factors, was cancelled by the IPC. Relevant PC form factor design information has been transferred to this revision of IPC-2221 and to IPC-2222.

1.3 Presentation All dimensions and tolerances in this standard are expressed in hard SI (metric) units and parenthetical soft imperial (inch) units. Users of this standard are expected to use metric dimensions. All dimensions greater than or equal to 0.1 mm [0.0039 in] will be expressed in millimeters and inches. All dimensions less than 0.1 mm [0.0039 in] will be expressed in micrometers and microinches.

1.3.1 Dimensional Units The following is taken from National Institute of Standards and Technology - Metric Information and Conversions: ''Beginning January 1, 2010, the European Union Council Directive 80/181/EEC (Metric Directive) allowed the use of only metric units, and prohibited the use of any other measurements for most products sold in the European Union (EU). The Metric Directive made the sole use of metric units obligatory in all aspects of life in the European Union, extending to areas such as product literature and advertising.''

Most component datasheets are provided in metric units. Many printed board designers spend a lot of time converting between imperial (inch) and SI (metric). Round-off errors, when converting units, can result in inaccuracies that result in marginal or failed designs. However, the printed board fabrication vendors often default to imperial units. Electronic Computer Aided Design (ECAD) tools accommodate both metric and imperial library components being placed on the same printed board because dimensional precision is large enough to describe most standard components accurately.

Problems arise when importing information from third party software or trying to mix units during printed board layout. For example, if a portion of the printed board design is an imported Drawing Exchange Format (.DXF) file with metric units that needs to interface with a digital portion done in imperial units, a problem can occur where the data from the two grids are mixed. Unlike importing from libraries, a conversion to printed board units is not always done when importing DXF.

While a user can convert printed board units from metric to imperial in modern day tools without problems, this should not be done too often during the design phase as repeated conversions can introduce unexpected errors. A single set of units should be used in the layout of the printed board. If imported data is in metric units, the layout portion of the process should use metric units. Once the layout is complete and verified, the designer can convert the printed board to imperial units for documentation, if necessary.

1.4 Interpretation ''**Shall**,'' the imperative form of the verb, is used throughout this standard whenever a requirement is intended to express a provision that is mandatory. Deviation from a ''**shall**'' requirement may be considered if sufficient data is supplied to justify the exception.

The words ''should'' and ''may'' are used whenever it is necessary to express nonmandatory provisions. ''Will'' is used to express a declaration of purpose.

To assist the reader, the word ''**shall**'' is presented in bold characters.

1.5 Definition of Terms The definition of all terms used herein **shall** be in accordance with IPC-T-50 and as defined in 1.5.1.

1.5.1 Microvia A microvia is defined as a blind structure (as plated) with a maximum aspect ratio of 1:1 when measured in accordance with Figure 1-1, terminating on or penetrating a target land, with a total length of no more than 0.25 mm [0.00984 in] measured from the structure's capture land foil to the target land.

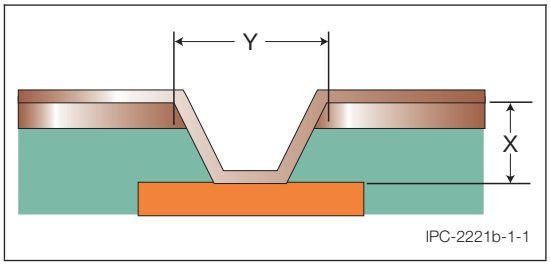


Figure 1-1 Microvia Definition

Note: X/Y = Microvia Plating Aspect Ratio, with X ≤0.25 mm [0.00984 in] and aspect ratio ≤1:1.

1.6 Classification of Products This standard recognizes that printed boards and printed boards assemblies are subject to classifications by intended end item use. Classification of producibility is related to complexity of the design and the precision required to produce the particular printed board or printed board assembly.

Any producibility level or producibility design characteristic may be applied to any end-product equipment category. Therefore, a high-reliability product designated as Class ''3'' (see 1.6.2), could require level ''A'' design complexity (preferred producibility) for many of the attributes of the printed board or printed board assembly (see 1.6.3).

1.6.1 Printed Board Type This standard provides design information for different printed board types. Printed board types vary per technology and are thus classified in the design sectionals.

1.6.2 Performance Classification This standard recognizes that electrical and electronic products are subject to classifications by intended end-item use. Three general end-product classes have been established to reflect differences in producibility, complexity, functional performance requirements, and verification (inspection/test) frequency. It should be recognized that there may be overlaps of product between classes.

The user is responsible for defining the product class. The procurement documentation package **shall** state the product class and any exceptions to specific parameters, where appropriate.

Criteria defined in this document reflect three classes, which are as follows:

Class 1 General Electronic Products – Includes limited life products suitable for applications where the requirement is function of the completed product.

Class 2 Dedicated Service Electronic Products – Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical.

Class 3 High Reliability Electronic Products – Includes products where continued high performance or performance-on-demand is critical, product downtime cannot be tolerated, and the product must function when required.

1.6.3 Producibility Level When appropriate, this standard will provide three design producibility levels of features, tolerances, measurements, assembly, testing of completion or verification of the manufacturing process that reflect progressive increases in sophistication of tooling, materials or processing and, therefore progressive increases in fabrication cost. These levels are:

Level A General Design Producibility-Preferred
Level B Moderate Design Producibility-Standard
Level C Least Design Producibility-Reduced

The producibility levels **shall not** to be interpreted as a design requirement, but rather as a method of communicating the degree of difficulty of a feature between design and fabrication/assembly facilities. The use of one level for a specific feature does not mean that other features must be of the same level. Selection should always be based on the minimum need, while recognizing that the precision, performance, conductive pattern density, equipment, assembly and testing requirements determine the design producibility level. The numbers listed within the numerous tables are to be used as a guide in determining what the level of producibility will be for any feature. The specific requirement for any feature that **shall** be controlled on the end item **shall** be specified on the master drawing of the printed board or the printed board assembly drawing.

1.7 Revision Level Changes Changes made to this revision of the IPC-2221 are indicated throughout by gray-shading of the relevant subsection(s). Changes to a figure or table are indicated by gray-shading of the Figure or Table header.

2 APPLICABLE DOCUMENTS

The following documents form a part of this document to the extent specified herein. If a conflict of requirements exists between IPC-2221 and those listed below, IPC-2221 takes precedence.

2.1 IPC[1]

IPC-TR-001 An Introduction to Tape Automated Bonding Fine Pitch Technology

IPC-A-43 Ten-Layer Multilayer Artwork

IPC-A-47 Composite Test Pattern Ten-Layer Phototool

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-CF-152 Composite Metallic Material Specification for Printed Wiring Boards

IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

IPC-D-322 Guidelines for Selecting Printed Wiring Board Sizes Using Standard Panel Sizes

IPC-D-356 Bare Substrate Electrical Test Data Format

IPC-D-422 Design Guide for Press Fit Rigid Printed Board Backplanes

IPC-TM-650 Test Methods Manual[2]

2.4.22 Bow and Twist
2.5.5.7 Characteristic Impedance Lines on Printed Boards by TDR
2.5.6 Dielectric Breakdown of Rigid Printed Wiring Material
2.5.7 Dielectric Withstanding Voltage, PWB
2.5.7.2 Dielectric Withstand Voltage (HiPot Method) - Thin Dielectric Layers for Printed Boards
2.6.8 Thermal Stress, Plated-Through Holes
2.6.27 Thermal Stress, Convection Reflow Assembly Simulation

IPC-CM-770 Printed Board Component Mounting

IPC-SM-780 Component Packaging and Interconnecting with Emphasis on Surface Mounting

IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments

IPC-MC-790 Guidelines for Multichip Module Technology Utilization

IPC-CC-830 Qualification and Performance of Electrical Insulating Compound for Printed Boards

IPC-HDBK-840 Solder Mask Handbook

IPC-SM-840 Qualification and Performance of Permanent Polymer Coating (Solder Mask) for Printed Boards

IPC-1601 Printed Board Handling and Storage Guidelines

IPC-2141 Controlled Impedance Circuit Boards and High Speed Logic Design

IPC-2251 Design Guide for High Speed/High Frequency Electronic Packaging

1. www.ipc.org
2. Current and revised IPC Test Methods are available on the IPC Web site (www.ipc.org/html/testmethods.htm)

IPC-2316 Design Guide for Embedded Passive Device Printed Boards

IPC-2511 Generic Requirements for Implementation of Product Manufacturing Description Data and Transfer Methodology

IPC-2611 Generic Requirements for Electronic Product Documentation

IPC-2615 Printed Board Dimensions and Tolerances

IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards

IPC-4103 Specification for Base Materials for High Speed/High Frequency Applications

IPC-4202 Flexible Base Dielectrics for Use in Flexible Printed Circuitry

IPC-4203 Adhesive Coated Dielectric Films for Use as Cover Sheets for Flexible Printed Wiring and Flexible Bonding Films

IPC-4204 Flexible Metal-Clad Dielectrics for Use in Fabrication of Flexible Printed Circuitry

IPC-4552 Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards

IPC-4553 Specification for Immersion Silver Plating for Printed Boards

IPC-4554 Specification for Immersion Tin Plating for Printed Circuit Boards

IPC-4562 Metal Foil for Printed Wiring Applications

IPC-4563 Resin Coated Metal Foil for Printed Boards

IPC-4761 Design Guide for Protection of Printed Board Via Structures

IPC-6011 Generic Performance Specification for Printed Boards

IPC-6012 Qualification and Performance Specification for Rigid Printed Boards

IPC-7094 Design and Assembly Process Implementation for Flip Chip and Die Size Components

IPC-7095 Design and Assembly Process Implementation for BGAs

IPC-7351 Generic Requirements for Surface Mount Design and Land Pattern Standard

IPC-7525 Stencil Design Guideline

IPC-9701 Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments

IPC-9252 Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards

IPC-9631 Users Guide for IPC-TM-650, Method 2.6.27, Thermal Stress, Convection Reflow Assembly Simulation

2.2 Joint Industry Standards[3]

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

JP002 Current Tin Whiskers Theory and Mitigation Practices Guideline

J-STD-003 Solderability Tests for Printed Boards

J-STD-005 Requirements for Soldering Pastes

J-STD-006 Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

3. www.ipc.org

2.3 Society of Automotive Engineers[4]

SAE-AMS-QQ-A-250 Aluminum Alloy, Plate and Sheet

SAE-AMS-QQ-N-290 Nickel Plating (Electrodeposited)

2.4 American Society for Testing and Materials[5]

ASTM-B-152 Copper Sheet, Strip and Rolled Bar

ASTM-B-488 Standard Specification for Electrodeposited Coatings of Gold for Engineering Use

ASTM-B-579 Standard Specification for Electrodeposited Coating of Tin-Lead Alloy (Solder Plate)

2.5 Underwriters Labs[6]

UL-94 Test for Flammability of Plastic Materials for Parts in Devices and Appliances

UL-746E Standard Polymeric Materials, Material used in Printed Wiring Boards

2.6 IEEE[7]

IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture

2.7 ANSI[8]

ANSI/EIA 471 Symbol and Label for Electrostatic Sensitive Devices

2.8 ANSI/ESD[9]

ANSI/ESD-S-20.20 Protection of Electrical and Electronic Parts, Assemblies and Equipment

2.9 PCMCIA[10]

PC Card Standard Physical Specification

4. www.sae.org
5. www.astm.org
6. www.ul.org
7. www.ieee.org
8. www.ansi.org
9. www.esda.org
10. www.pcmcia.org

3 GENERAL REQUIREMENTS

The information contained in this section describes the general parameters to be considered by all disciplines prior to and during the design cycle.

Designing the physical features and selecting the materials for a printed board involves balancing the electrical, mechanical and thermal performance as well as the reliability, manufacturing and cost of the printed board. The tradeoff checklist (see Table 3-1) identifies the probable effect of changing each of the physical features or materials. The items in the checklist need to be considered if it is necessary to change a physical feature or material from one of the established rules. Cost can also be affected by these parameters as well as those in Table 5-1.

How to read Table 3-1: As an example, the first row of the table indicates that if the dielectric thickness to ground is increased, the lateral crosstalk also increases and the resultant performance of the printed board is degraded (because lateral crosstalk is not a desired property).

Table 3-1 PCB Design/Performance Tradeoff Checklist

Design Feature	Class Electrical Performance (EP) Mechanical Performance (MP) Reliability (R) Manufacturability/ Yield (M/Y)	Performance Parameter	Impact if Design Feature is Increased			
			Performance Parameter is:		Resulting Performance or Reliability is:	
			Increased	Decreased	Enhanced	Degraded
Dielectric Thickness to Ground	EP	Lateral Crosstalk	X			X
	EP	Vertical Crosstalk	X			X
	EP	Characteristic Impedance	X		Design Driven	
	MP	Physical Size/Weight	X			X
Line Spacing	EP	Lateral Crosstalk		X	X	
	EP	Vertical Crosstalk		X	X	
	MP	Physical Size/Weight	X			X
	M/Y	Electrical Isolation	X		X	
Coupled Line Length	EP	Lateral Crosstalk	X			X
	EP	Vertical Crosstalk	X			X
Line Width	EP	Lateral Crosstalk		X	X	
	EP	Vertical Crosstalk	X			X
	EP	Characteristic Impedance		X	Design Driven	
	MP	Physical Size/Weight	X		Design Driven	
	R	Signal Conductor Integrity	X		X	
	M/Y	Electrical Continuity	X		X	
Line Thickness	EP	Lateral Crosstalk	X			X
	R	Signal Conductor Integrity	X		X	
Vertical Line Spacing	EP	Vertical Crosstalk		X	X	
Z_o of PCB vs. Z_o of Device	EP	Reflections		X	X	
Distance between Via Walls	R	Electrical Isolation	X		X	
Annular Ring (capture and target land to via)	M/Y	Producibility	X		X	
Signal Layer Quantity	MP	Physical Size/Weight	X			X
	M/Y	Layer-to-Layer Registration		X		X

Design Feature	Class Electrical Performance (EP) Mechanical Performance (MP) Reliability (R) Manufacturability/ Yield (M/Y)	Performance Parameter	Impact if Design Feature is Increased			
			Performance Parameter is:		Resulting Performance or Reliability is:	
			Increased	Decreased	Enhanced	Degraded
Component I/O Pitch Board Thickness	MP	Physical Size/Weight	X			X
	R	Via Integrity		X		X
	M/Y	Via Plating Thickness		X		X
Copper Plating Thickness	R	Via Integrity	X		X	
Aspect Ratio	R	Via Integrity		X		X
	M/Y	Producibility		X		X
Overplate (Nickel -Kevlar only)	R	Via Integrity	X		X	
Via Diameter	M/Y	Via Plating Thickness	X		X	
	R	Via Integrity	X		X	
Laminate Thickness (Core)	EP	Lateral Crosstalk	X			X
	EP	Vertical Crosstalk		X	X	
	EP	Characteristic Impedance	X		Design Driven	
	MP	Physical Size/Weight	X			X
	R	Via Integrity		X		X
	MP	Flatness Stability	X		X	
Prepreg Thickness (Core)	EP	Lateral Crosstalk	X			X
	EP	Vertical Crosstalk		X	X	
	EP	Characteristic Impedance	X		Design Driven	
	EP	Physical Size/Weight	X			X
	R	Via Integrity		X		X
Dielectric Constant	EP	Reflections	X			X
	EP	Characteristic Impedance		X	Design Driven	
	EP	Signal Speed		X	Design Driven	
CTE (out-of-plane)	R	Via Integrity		X		X
CTE (in-plane)	R	Solder Joint Integrity		X		X
	R	Signal Conductor Integrity		X		X
Resin T_g	R	Via Integrity	X		X	
	R	PTH Solder Joint Integrity	X		X	
Copper Ductility	R	Via Integrity	X		X	
	R	Signal Conductor Integrity	X		X	
Copper Peel Strength	R	Component Land Adhesion to Dielectric	X		X	
Dimensional Stability	M/Y	Layer-to-Layer Registration	X		X	
Resin Flow	M/Y	PWB Resin Voids		X	X	
Rigidity	MP	Flexural Modulus	X		Design Driven	
Volatile Content	M/Y	PWB Resin Voids	X			X

3.1 Information Hierarchy

3.1.1 Order of Precedence In the event of conflict, the following order of precedence **shall** apply:

1. The procurement contract.
2. The master drawing or assembly drawing (supplemented by an approved deviation list, if applicable).
3. This standard.
4. Other applicable documents.

3.1.2 End-Product Performance Requirements The end-product performance requirements **shall** be defined prior to design start-up. Maintenance and serviceability requirements are important factors which should be addressed during the design phase. Frequently, these factors affect layout and conductor routing. Finished printed boards **shall** meet the performance requirements of IPC-6011 and its applicable sectional specification (i.e., IPC-6012, IPC-6013, IPC-6018, etc.).

3.2 Design Considerations The design process should include a formal design review of details by as many affected disciplines within the company as possible, including fabrication, assembly and testing. The approval of the layout concepts by representatives of the affected disciplines will ensure that these production-related factors have been considered in the design.

The success or failure of an interconnecting structure design depends on many interrelated considerations. From an end-product usage standpoint, the impact on the design by the following typical parameters should be considered:

- Equipment environmental conditions, such as ambient temperature, heat generated by the components, ventilation, shock and vibration.
- If an assembly is to be maintainable and repairable, consideration **shall** be given to component/circuit density, the selection of printed board/conformal coating materials, and component placement for accessibility.
- Installation interface that may affect the size and location of mounting holes, connector locations, lead protrusion limitations, part placement, and the placement of brackets and other hardware.
- Testing/fault location requirements that might affect component placement, conductor routing, connector contact assignments, etc.
- Process allowances such as etch factor compensation for conductor widths, spacings, land fabrication, etc. (see Sections 5, 9 and 10).
- Manufacturing limitations such as minimum etched features, minimum plating thickness, printed board shape and size, etc.
- Coating and marking requirements.
- Assembly technology used, such as surface mount, through hole, and mixed.
- Printed board performance class (see 1.6.2).
- Materials selection (see Section 4).
- Producibility of the printed board assembly as it pertains to manufacturing equipment limitations. This includes: Flexibility (Flexural) Requirements
- Electrical/Electronic
- ESD sensitivity considerations.
- Copper density per layer.
- Balanced Construction.
- Partitioning of design for signal integrity, test and ease of design reuse, etc.

Partitioning is performed in the preliminary printed board design phase. It includes trade-off studies, usually including several design concepts that could solve the problem. These design concepts are functionally block diagrammed and, as with any trade-off, a set of advantages and disadvantages is formulated and evaluated by the designer to make his decision on which solution is optimal for this design. It is at this point important to ensure all functional requirements, test connections, and any known growth requirements are being considered. These should flow from the project requirements as documented in the design requirements. The test requirements and growth requirements may not need to be implemented during the electrical design phase, but the interfaces, including printed board wiring, Field Programmable Logic (FPL), and memory assets, should be allocated.

The design partitioning for each concept needs to evaluate what can be implemented on the printed board. The following questions should be answered:

• What are the control requirements?

• What are the memory requirements?

• What are the data path requirements?

• What are the I/O requirements?

It is difficult to convey all the considerations that should be evaluated. The few here have been included to provoke the thought process. Users are encouraged to consult with experienced printed board designers if there is a need for assistance.

3.3 Schematic/Logic Diagram The initial schematic/logic diagram designates the electrical functions and interconnectivity to be provided to the designer for the printed board and its assembly. This schematic should define, when applicable, critical circuit layout areas, shielding requirements, grounding and power distribution requirements, the allocation of test points, and any preassigned input/output connector locations. Schematic information may be generated as hard copy or computer data (manually or automated).

3.4 Density Evaluation A wide variety of materials and processes have been used to create substrates for electronics over the last half century, from traditional printed circuits made from resins (i.e., epoxy), reinforcements (i.e., glass cloth or paper), and metal foil (i.e., copper), to ceramics metallized by various thin and thick film techniques. However, they all share a common attribute in that they route signals through conductors.

There are also limits to how much routing each can accommodate. The factors that define the limits of their wire routing ability as a substrate are:

• Pitch/distance between vias or holes in the substrate.

• Number of wires that can be routed between those vias.

• Number of signal layers required.

In addition, the methods of producing blind and buried vias can facilitate routing by selectively occupying routing channels. Vias that are routed completely through the printed board preclude any use of that space for routing on all conductor layers.

These factors can be combined to create an equation that defines the wire routing ability of a technology. In the past, most components had terminations along the periphery on two or more sides. However area array components are more space conservative and allow coarser I/O pitches to be used (see Figure 3-1).

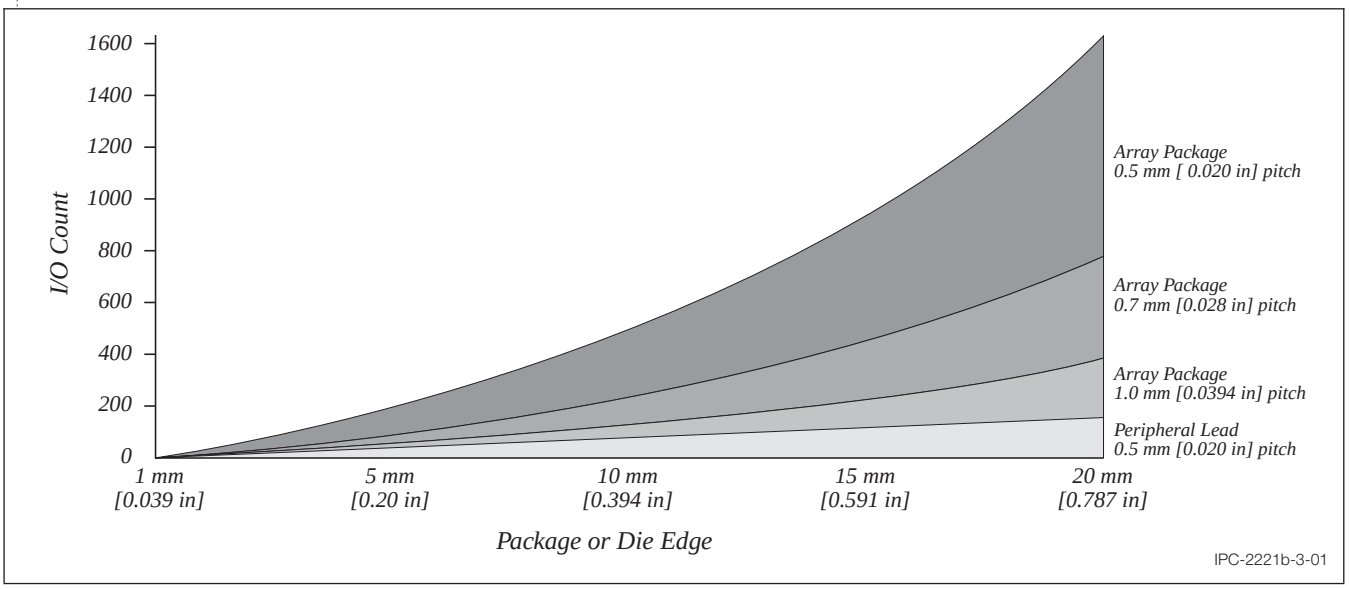


Figure 3-1 Package Size and I/O Count

3.5 Parts List A parts list, or bill of materials (BOM), is a tabulation of parts and materials used in the construction of a printed board assembly. All end item identifiable parts and materials **shall** be identified in the parts list or on the field of the drawing. Excluded are those materials used in the manufacturing process, but may include reference information; i.e., specifications pertinent to the manufacture of the assembly and reference to the schematic/logic diagram.

All mechanical parts appearing on the assembly pictorial **shall** be assigned an item number which **shall** match the item number assigned on the parts list.

Electrical components, such as capacitors, resistors, fuses, ICs, transistors, etc., **shall** be assigned reference designators, (Ex. C5, CR2, F1, R15, U2, etc.). Electrical reference designators **shall** match the assignments given to the same components on the Logic/schematic diagram.

It is advisable to group like items; e.g., resistors, capacitors, ICs, etc., in some sort of ascending or numerical order.

The parts list may be handwritten, manually typed on to a standard format, or computer generated.

3.6 Test Requirement Considerations Normally, prior to starting a design, a testability review meeting should be held with fabrication, assembly, and testing. Testability concerns, such as circuit visibility, density, operation, circuit controllability, partitioning, and special test requirements and specifications are discussed as a part of the test strategy. See Appendix C for an example of a testability design checklist.

During the design testability review meeting, tooling concepts are established, and determinations are made as to the most effective tool-cost versus printed board layout concept conditions. See 3.7.1 for layout recommendations relative to testability.

During the layout process, any printed board changes that impact the test program, or the test tooling, should immediately be reported to the proper individuals for determination as to the best compromise. The testing concept should develop approaches that can check the printed board for problems, and also detect fault locations wherever possible. The test concept and requirements should economically facilitate the detection, isolation, and correction of faults of the design verification, manufacturing, and field support of the printed board assembly life cycle.

3.6.1 Electrical

3.6.1.1 Bare Printed Board Testing When electrical testing is required it **shall** be specified in accordance with IPC-9252 including the assignment of a ''Test Level'' and including any user defined ''AABUS'' (As Agreed Between User and Supplier) test options. It is the responsibility of the user to define test requirements appropriate to the end use of the printed board. The selection of requirements should be carefully considered as these will at least in part determine the relative effectiveness of any test procedure. For example, electrical testing methods optimized for higher productivity may be less capable of detecting certain defects. The user is encouraged to discuss available test options with the supplier so that the appropriate requirements can be developed, which will provide the appropriate level of quality while allowing the greatest freedom in the supplier's use of available tools.

User defined options may include the following:

- Isolation Test Voltage for ''Resistive Testing'' (Maximum rated voltage should be specified; if not specified, it will be 40 volts minimum, which may not be sufficient to detect leakage failures).
- Continuity Test Current for ''Resistive Testing.''
- Horizontal Adjacency (AABUS for Class 3).
- Vertical Layer Adjacency (AABUS for all three Performance Classes).
- Indirect Isolation And Continuity Testing By ''Signature Comparison'' (AABUS for Class 3).
- ''Hi-Pot'' testing of dielectric integrity.
- Impedance testing of specialized circuitry.
- Embedded capacitance and or embedded resistance (test requirements for this technology are not covered by IPC-9252). Refer to IPC-2316 for guidance.

If test requirements are not otherwise defined IPC Performance Class 1, Class 2, and Class 3 **shall** be tested to default IPC-9252 Test Level A, Level B, and Level C respectively.

3.6.1.2 Test Methods The following electrical test methods are available or optional to the supplier in accordance with IPC-9252. Not all test methods have an equal potential for effectiveness. Because of the variations in equipment, training, and practice no method should be considered as ''100-percent'' effective.

a) Resistive Continuity Testing: This type of test measures the resistance of the net under test. If the resistance is lower than the specified threshold, the network under test passes. If resistance is higher than the specified threshold, the network under test fails and an open is reported. Minimum test thresholds are in accordance with IPC-9252. The test current applied **shall not** exceed that allowed for the smallest conductor in that circuit and should be stated on the master drawing. Resistive Continuity Testing may be performed on a fix-grid or a fixtureless moving-probe (flying-probe) or moving grid test system.

b) Resistive Isolation Testing: This type of testing verifies that electrically isolated networks meet the minimum resistive threshold. If the isolation resistance measured is higher than the minimum specified in IPC-9252, the network passes. Faults detected are defined as either shorts or leakages. Resistive Isolation Testing may be performed on a fix-grid or a fixtureless moving-probe (flying-probe) system. However, the use of a moving-probe test system for resistive isolation testing may be considered impractical unless the supplier is permitted to use one of the adjacency sorting protocols to increase productivity the details of which (including adjacency distance) should be developed between user and supplier.

c) Indirect Isolation & Continuity Testing by Signature Comparison: This type of testing indirectly verifies electrical isolation and continuity by measuring and recording electrical properties (such as capacitance, RF, impedance, etc.) of a printed board under test and comparing them to a measured or calculated reference value which is capable of distinguishing between manufacturing and design faults. When faults by the indirect method are verified by the resistive method, they are classified as shorts, leakages, or opens. Otherwise network resistance values are not measured and should not be specified without exception where the intent is to allow the use of indirect testing. Indirect test methods are used with moving probe test systems running proprietary test software.

d) Insulation Resistance Test This test is used to provide a quantifiable resistance value for all of a product's insulation. A Direct Current (DC) test voltage is applied. The voltage and measured current value are used to calculate the resistance of the insulation.

3.6.1.2.1 HiPot Testing A HiPot test (also called a Dielectric Withstanding Voltage Test) verifies that the insulation of a product or component is sufficient to protect the hardware. In a typical HiPot test, high voltage is applied between a product's current-carrying conductors and its metallic chassis. The resulting current that flows through the insulation, known as leakage current, is monitored by the HiPot tester. The theory behind the test is that if a deliberate over-application of test voltage does not cause the insulation to break down, the product will be safe to use under normal operating conditions. Three common high voltage tests include:

- Dielectric breakdown test (IPC-TM-650, Method 2.5.6) – The test voltage is increased until the dielectric fails, or breaks down, allowing too much current to flow. This test is performed on an Acceptable Quality Level (AQL) sample basis by the laminate material supplier. This test allows designers to determine the breakdown voltage of a product's design. This value is often provided in the material supplier's laminate specification sheet.
- Dielectric withstanding voltage (DWV) test (IPC-TM-650, Method 2.5.7) – A standard test voltage is applied (below the established Breakdown Voltage) for a specific length of time to determine any occurrence of flashover, spark over or breakdown. This test is routinely done on a monthly basis (see coupon ''E'' in 12.4.2).
- Dielectric withstanding voltage (IPC-TM-650, Method 2.5.7.2) – thin dielectric layers and planar capacitance layers - The test voltage, voltage ramp rate, hold time at peak voltage, and current threshold are pre-programmed into the HiPot tester. This test allows designers to determine the breakdown voltage of a product's design. This value is often provided in the material supplier's laminate specification sheet.

Note: Capacitance effect within the printed board may affect testing procedures.

The following are design considerations and documention requirements for designs requiring high pot testing:

a. Design Considerations
   1) Inadequate (current) creepage distance between holes (copper migration).
   2) Inadequate clearance distances between conductive geometries in both the horizontal and vertical directions. Consideration should be given to laminate anomalies such as ''eyebrow'' cracks, which may affect the test result.
   3) Solder mask or coating characteristics and thickness.
   4) Dielectric characteristics.

b. Documentation requirements

1) Peak voltage desired. Typically user specified.

2) Specific circuit locations identified, if board testing is required.

3) Voltage ramp rate.

4) Hold time at peak voltage.

5) Sampling plan for testing.

3.6.1.2.2 Impedance Considerations

- Conductor width and spacing is determined by modeling electrical impedance values in conjunction with printed board layer stack-up using a reliable industry accepted impedance calculator. Due to material and fabrication process variations, fabricator calculations will provide more accurate results.
- Should differentiate conductors with impedance requirements from other conductors. As an example, if conductors are routed at 0.15 mm [0.006 in], the conductor width should be increased or decreased by 2.54 µm [100 µin]. This will make it easier for the printed board fabricator to identify which conductors to test.
- Each impedance controlled conductor should be identified with its associated reference plane(s).
- Avoid routing across any empty spaces in the reference layer.
- Testing per IPC-TM-650. Coupons may be specified for evaluation of impedance requirements.

The following are *examples* of sample notes for impedance considerations and are not requirements of this standard:

- *XX. Impedance testing (IPC-TM-650, Method 2.5.5.7)*

  XX.1 Single ended: (Conductor widths [0.0059 in] on Layer X with respect to Layer Y)

  *The printed board **shall** exhibit a characteristic impedance of 52.5 ohms (± 15%) as measured using a Time Domain Reflectometer (TDR) which **shall** be verified by measurement of impedance coupons supplied by the fabricator.*

  XX.2 *Differential pairs: (Conductor widths [0.0059 in] on layer X with respect to Layer Y)*

  *The printed board **shall** exhibit a characteristic impedance of 105 ohms (± 15%) as measured using a Time Domain Reflectometer (TDR) which **shall** be verified by measurement of impedance coupons supplied by the fabricator.*

- *ALL **0.023 in** WIDE CONDUCTORS ON LAYER X ARE IMPEDANCE CONTROLLED (TYPE **XXXXXXX**) TO **XXX** OHMS ± **10%** WITH RESPECT TO REFERENCE PLANE LAYERS Y AND Z. THE PRINTED BOARD MANUFACTURER HAS THE OPTION OF ADJUSTING THE DIELECTRIC MATERIAL THICKNESS AND THE CONDUCTOR WIDTH AS REQUIRED TO MEET THE IMPEDANCE REQUIREMENT. THE ADJUSTED CONDUCTOR WIDTH **SHALL NOT** EXCEED A TOLERANCE OF ± **0.0015 in.** THIS REQUIREMENT TAKES PRECEDENCE OVER OTHER CONDUCTOR WIDTH REQUIREMENTS. THE MANUFACTURER **SHALL** VERIFY IMPEDANCE REQUIREMENTS BY TIME DELAY REFLECTOMETRY (TDR) TEST ON MANUFACTURER SUPPLIED COUPON.*

3.6.1.3 Test Data (Source Data) The fabricator **shall** be provided with CAD Netlist data for use as electrical test source data. When Netlist data cannot be provided or is not available, Level C testing can be performed using CAM (Gerber) data. Certain test methods (e.g., adjacency, capacitance, etc.) require graphical circuitry data which may not be available within the CAM data. In this event, only the product of Gerber netlist extraction created by the supplier's proprietary software will be compatible.

3.6.2 Printed Board Assembly Testability Design of a printed board assembly for testability normally involves systems level testability issues. In most applications, there are system level fault isolation and recovery requirements such as mean time to repair, percent up time, operate through single faults, and maximum time to repair. To meet the contractual requirements, the system design may include testability features, and many times these same features can be used to increase testability at the printed board assembly level. The printed board assembly testability philosophy also needs to be compatible with the overall integrations, testing and maintenance plans for the contract. The factory testers to be used, how integration and test is planned, when printed board assemblies are conformal coated, the depot and field test equipment capabilities and personnel skill level are all factors that should be considered when developing the printed board assembly test strategy. The test philosophy may be different for different phases of the program. For example, the first unit debug philosophy may be much different than the test philosophy for spares when all the systems have already been shipped.

Before the printed board design starts, requirements for the system testability functions should be presented at the conceptual design review. These requirements and any derived requirements should be partitioned down to the various printed board assemblies and documented. The system and program level test criteria and how they are partitioned down to the printed board assembly requirements are beyond the scope of this document.

The two basic types of printed board assembly test are functional test and in-circuit test. Functional testing is used to test the electrical design functionality. Functional testers access the printed board under test through the connector, test points, or bed-of-nails. The printed board is functionally tested by applying pre-determined stimuli (vectors) at the printed board assembly's inputs while monitoring the printed board assembly outputs to ensure that the design responds properly.

In-circuit testing is used to find manufacturing defects in printed board assemblies. In-circuit testers access the printed board under test through the use of a bed-of-nails fixture which makes contact with each node on the printed board assembly. The printed board assembly is tested by exercising all the parts on the printed board individually. In-circuit testing places fewer restrictions on the design. Conformal coated printed board assemblies and many Surface Mount Technology (SMT) and mixed technology printed board assemblies present bed-of-nails physical access problems which may prohibit the use of in-circuit testing. Primary concerns for in-circuit test are that the lands or pins (1) should be on grid (for compatibility with the use of bed-of-nails fixture) and (2) should be accessible from the secondary side (a.k.a. noncomponent or solder side of through-hole technology printed boards) of the printed board assembly.

A Manufacturing Defects Analyzer (MDA) provides a low cost alternative to the traditional in-circuit tester. Like the in-circuit tester, the MDA examines the construction of the printed board assembly for defects. It performs a subset of the types of tests, mainly only tests for shorts and opens faults without power applied to the printed board assembly. For high volume production with highly controlled manufacturing processes (i.e., Statistical Process Control techniques), the MDA may have application as a viable part of a printed board assembly test strategy.

Vectorless Test is another low cost alternative to in-circuit testing. Vectorless Test performs testing for finding manufacturing process-related pin faults for SMT printed boards and does not require programming of test vectors. It is a powered-off measurement technique consisting of three basic types of tests:

a. *Analog Junction Test* – DC current measurement test on unique pin pairs of the printed board assembly using the ESD protection diodes present on most digital and mixed signal device pins.
b. *RF Induction Test* – Magnetic induction is used to test for device faults utilizing the printed board assembly's devices protection diodes. This technique uses chips power and ground pins to make measurements for finding solder opens on device signal paths, broken bond wires, and devices damaged by ESD. Parts incorrectly oriented can also be detected. Fixturing containing magnetic inducers are required for this type of test.
c. *Capacitive Coupling Test* – This technique uses capacitive coupling to test for pin opens and does not rely on internal device circuitry but instead relies on the presence of the metallic lead frame of the device to test the pins. Connectors and sockets, lead frames and correct polarity of capacitors can be tested using the technique.

3.6.3 Boundary Scan Testing As printed board assemblies become more dense with fine pitch devices, physical access to printed board assembly nodes for in-circuit testing may not be possible. The boundary scan standard for integrated circuits (see the IEEE 1149 series of standards) provides the means to perform virtual in-circuit testing to alleviate this problem. Boundary scan architecture is a scan register approach where, at the cost of a few I/O pins and the use of special scan registers in strategic locations throughout the design, the test problem can be simplified to testing of simpler, mostly combinational circuits.

In many applications, the inclusion of scan registers on the inputs and outputs of the printed board assembly allows the printed board to be tested while installed. If the circuit is more complex, additional sets of scan registers can be included in the design to capture intermediate results and apply test vectors to exercise portions of the design.

A full description of the standard access port and boundary scan architecture can be found in the IEEE 1149 series of standards. The full test access port capabilities are not needed to gain significant testability via the scan registers.

The decision to use boundary scan test as part of a test strategy should consider the availability of boundary scan parts and the return on investment for capital equipment and software tools required for implementing this test technique. Boundary scan testing can be conducted using a low cost PC-based tester which requires access to the printed board assembly under test through the edge connector or an existing functional, in-circuit, or hybrid tester that may be adapted to perform boundary scan testing. The printed board interface (e.g., JTAG connector, etc.) can also be used to facilitate on-printed board programming of programmable memory devices.

3.6.4 Functional Test Concern for Printed Board Assemblies There are several concerns for designing the printed board assembly for functional testability. The use of test connectors, problems with initialization and synchronization, long counter chains, self diagnostics, and physical testing are topics which are discussed in detail in the following subsections and are not meant to be tutorials on testability but rather ideas of how to overcome typical functional testing problems.

3.6.4.1 Test Connectors Fault isolation on conformal coated printed boards or most SMT and mixed technology designs can be very difficult because of the lack of access to the circuitry on the printed board.

If strategic signals are brought out to a test connector or an area on the printed board where the signals can be probed (test points), fault isolation may be much improved. This lowers the cost of detection, isolation and correction.

It is also possible to design the circuit so that a test connector can be used to stimulate the circuit (such as taking over a data bus via the test connector) or disable functions on the printed board assembly (such as disabling a free running oscillator and adding single step capability via the test connector).

3.6.4.2 Initialization and Synchronization Some designs or portions of a design do not need any initialization circuitry because the circuit will quickly cycle into its intended function. Unfortunately, it is sometimes very difficult to synchronize the tester with this type of circuit because the tester would need to be programmed to stimulate the circuit until a predetermined signature is found on the outputs of the circuit. This can be difficult to achieve.

With relatively little difference in the design, initialization capability can usually be designed into the circuitry allowing the printed board assembly to be quickly initialized and the circuit and the tester can follow the expected outputs of the printed board assembly.

Free running oscillators also present a problem in testing because of the synchronization problem with the test equipment. These problems can be overcome by (1) adding test circuitry to select a test clock instead of the oscillator; (2) removing the oscillator for test and injecting a test clock; (3) overriding the signal; or (4) designing the clock system so that the clocking can be controlled via a test connector or test points.

3.6.4.3 Long Counter Chains Long counter chains in the design with signals used from many stages of the counter chain present another testability problem. Testability can be very bad if there is no means to preset the counter chain to different values to facilitate testing of the logic that is driven from the high order stages of the counter chain.

Testability is much improved if the counter chain is either broken into smaller counter chains (perhaps no more than 10 stages) which can be individually controlled or if the counter chain can be loaded via the test software. The test software can then verify the operation of the logic that is driven from the counter stages without wasting the simulation and test time that would be required to clock through the complete counter chain.

3.6.4.4 Self Diagnostics Self diagnostics are sometimes imposed either contractually or via derived requirements. Careful consideration should be given to determine how to implement these requirements.

Many times a printed board assembly does not contain functions that lend themselves to self diagnostics at the printed board assembly level but a small group of printed board assemblies, when taken as a unit, do lend themselves to good diagnostics. For example, a complex Fast Fourier Transform (FFT) function may be spread across multiple printed board assemblies. It may be very difficult for any one printed board assembly to self diagnose a problem but it may be very easy to design-in circuitry that self diagnoses the whole FFT function.

The depth of self diagnostics that are needed is usually driven by the line replaceable unit (LRU) which varies with requirements. It may be an integrated circuit or it may be a drawer of electronics depending on the contract, the function of the design, or the system level maintenance philosophy.

For self diagnostics at a printed board assembly level, the printed board assembly is usually put into a test mode and then the printed board assembly applies a known set of test inputs and compares the results with a stored set of expected responses. If the results do not match the expected responses, the printed board assembly signals the test equipment indicating the printed board assembly failed the self-test. There are many variations on this scheme. Some examples are:

- The printed board assembly is placed in a feedback loop with the results checked after a predetermined number of cycles.
- A special test circuit or the Central Processor Unit (CPU) applying the stimuli and comparing the signature of the responses against a known pattern.
- The printed board assembly performing self-checks when idling and then supplying the results to another (or diagnostic) printed board assembly for verification of the responses, etc.

3.6.4.5 Physical Test Concerns Printed board assembly functional test equipment is usually very expensive and requires highly skilled personnel to operate. If printed board assembly testability is poor, the printed board assembly test operation can be very expensive. There are some simple physical considerations that can decrease the debug time and therefore the overall test costs.

The orientation of polarized parts should be consistent so that the operator does not get confused with parts being oriented 180° out of phase with other parts on the printed board assembly. Nonpolarized parts still need to have the pin #1 identified so that the test operator knows which end to probe when guided probe software says to probe a specific pin.

Test connectors are much preferred over test points which require the use of test clips or test hook-up wires. However, test points such as riser leads are preferred over clipping on to the lead of a part. If riser leads are used for temporary testing, such as determining a select-by-test resistor, it is suggested that the risers remain after the installation of the selected component. This allows verification of the selected item without re-fixturing the assembly.

Signals that are not accessible for probing (such as can happen with leadless parts) can greatly increase fault isolation problems. If scan registers are not used, it is recommended that every signal have a land or other test point somewhere on the printed board assembly where the signal can be probed. It is also recommended that lands used for test points be located on grid and placed so that all the probing can be done from the secondary side of the printed board assembly. If it is not feasible to provide capability for probing every signal, then (1) only the strategic signals should have special probing locations and (2) the test vectors need to be increased or other test techniques need to be utilized to assign fault isolation to one component or a small set of components.

Many faults are often due to shorts between the leads of adjacent parts, shorts between a part lead and an external layer conductor on the printed board or shorts between two printed board conductors on the external layers of the printed board. The physical design should consider these normal manufacturing defects and not impair the isolation of the faults due to lack of access or inconvenient access to signals. As with design for in-circuit testability, probe land test points should be on grid to allow automated probing to be used in the future.

Partitioning of the design into functions, perhaps digital separated from analog, is sometimes required for electrical performance. Testing concerns also are helped with physical separation of dissimilar functions. Separation of not just the circuitry but also the test connectors or at least grouping the pins on the connectors can help improve testability. Designs that mix digital design with high performance analog design may require testing on two or more sets of test equipment. Separating the signals will not only help the test fixturing but will help the operator in debugging the printed board assembly.

As with in-circuit test fixturing, functional test fixturing can have a significant cost impact. Normally a standard printed board size or only a few printed board sizes are used for all designs on a program. Similarly one, or at most a few, test fixtures are typically used for a program. Generating test fixtures can be costly and debugging noise problems in the fixtures or tuning the fixtures to the tester can be expensive. If the test fixturing is not adequately engineered, it may not be possible to accurately measure the printed board under test. Typically much effort is expended in generating a few test fixtures and it is expected that the fixtures will be used for all the printed board assembly designs. Therefore the test fixturing restrictions **shall** be considered in the printed board assembly design. The fixturing restraints can be significant. Such as (1) requiring ground and voltage supplies on specific connector pins, (2) limiting which pins can be used for high speed signals, (3) limiting which pins can be used for low noise applications, (4) defining power switching limitations, (5) defining voltage and current limitations on each pin, etc.

3.6.5 In-Circuit Test Concerns for Printed Board Assemblies In-circuit testing is used to find shorts, opens, wrong parts, reversed parts, bad devices, incorrect assembly of printed board assemblies and other manufacturing defects. In-circuit testing is neither meant to find marginal parts nor to verify critical timing parameters or other electrical design functions.

In-circuit testing of digital printed board assemblies can involve a process that is known as backdriving (see IPC-T-50). Backdriving can also cause devices to oscillate and the tester can have insufficient drive to bring a device out of saturation. Backdriving can be performed only for controlled periods of time, or the junction of the device (with the overdriven output) will overheat.

The two main concerns for designing the printed board and printed board assembly for in-circuit testability are design for compatibility with in-circuit test fixturing and electrical design considerations. These topics are discussed in detail in the following subsections.

3.6.5.1 In-Circuit Test Fixtures In-circuit test fixtures are commonly called bed-of-nails fixtures. A bed-of-nails fixture is a device with spring contact probes which contact each node on the printed board under test. The following guidelines should be followed during printed board assembly layout to promote in-circuit testability in bed-of-nails fixtures:

a. The diameter of lands of plated-through holes (PTHs) and vias used as test lands are a function of the hole size (see 9.1.1). The diameter of test lands used specifically for probing should be no smaller than 0.9 mm [0.0354 in]. It is feasible to use 0.6 mm [0.0236 in] diameter test lands on printed boards under 7700 mm^2 [11.935 in^2].

b. Clearances around test probe sites are dependent on assembly processes. Probe sites should maintain a clearance equal to 80% of an adjacent component height with a minimum of 0.6 mm [0.0236 in] and a maximum of 5.0 mm [0.20 in] (see Figure 3-2).

c. Part height on the probe side of the printed board should not exceed 5.7 mm [0.224 in]. Taller parts on this side of the printed board will require cutouts in the test fixture. Test lands should be located 5.0 mm [0.20 in] away from tall components. This allows for test fixture profiling tolerances during test fixture fabrication (see Figure 3-3).

d. No parts or test lands should be located within 3.0 mm [0.118 in] of the printed board edges.

e. All probe areas should be solder coated or covered with a conductive nonoxidizing coating. The test lands should be free of solder mask and markings.

f. Probe the test lands or vias, not the termination/castellations of leadless surface mount parts or the leads of leaded parts (see Figure 3-4). Contact pressure can cause an open circuit or make a cold solder joint appear good.

g. Avoid requiring probing of both sides of the printed board. Use vias, to bring test points to one side, the bottom side (noncomponent or solder side of through-hole technology printed board assemblies) of the printed board. This allows for a reliable and less expensive fixture.

h. Test lands should be on 2.5 mm [0.0984 in] hole centers, if possible, to allow the use of standard probes and a more reliable fixture.

i. Do not rely on edge connector fingers for test lands. Gold plated fingers are easily damaged by test probes.

j. Distribute the test lands evenly over the printed board area. When the test lands are not evenly distributed or when they are concentrated in one area, the results are printed board flexing, probing faults, and vacuum sealing problems.

k. A test land should be provided for all nodes. A node is defined as an electrical connection between two or more components. A test land requires a signal name (node signal name), the x-y position axis in respect to the printed board datum point, and a location (describing which side of the printed board the test land is located). This data is required to build a fixture for SMT and mixed technology printed board assemblies. The quantity of required test lands may be reduced when Boundary Scan test is used.

l. Mixed technology printed board assemblies and pin grid component printed boards provide test access for some nodes at the solder side pins. Pins and vias used at test lands should be identified with node signal name and X-Y position in reference to the printed board datum point. Use solder mount lands of parts and connectors as test points to reduce the number of generated test lands.

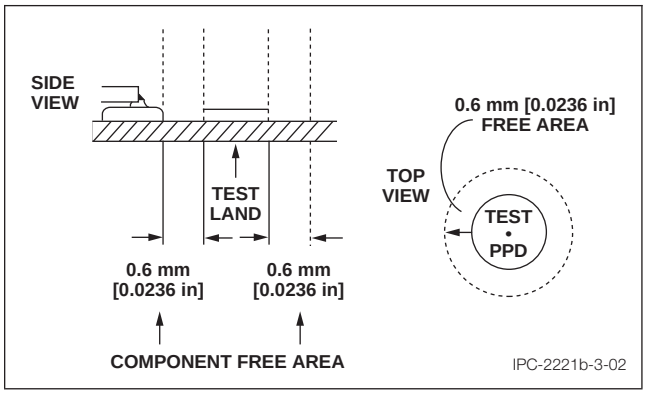


Figure 3-2 Test Land Free Area for Parts and Other Intrusions

Note 1. PPD is short for "Probe Point Diameter"

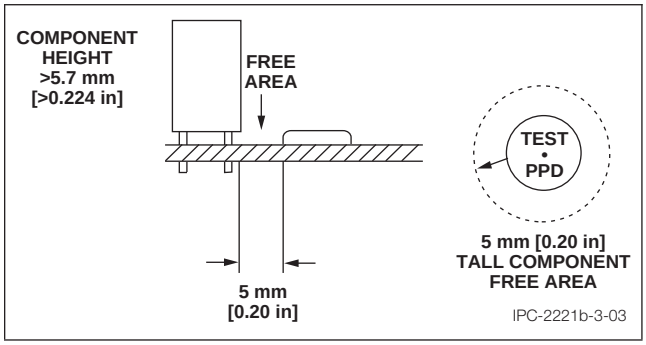


Figure 3-3 Test Land Free Area for Tall Parts

Note 1. PPD is short for "Probe Point Diameter"

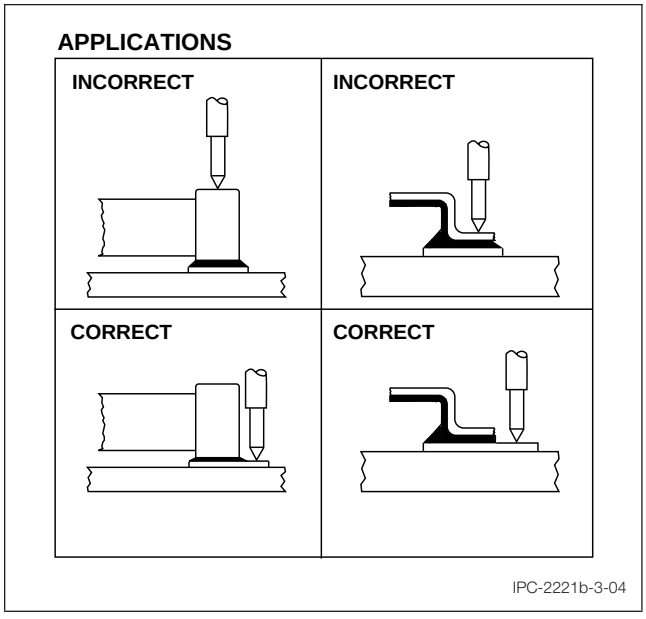


Figure 3-4 Probing Test Lands

3.6.5.2 In-Circuit Test Electrical Considerations The following electrical considerations should be followed during printed board assembly layout to promote in-circuit testability:

a. Do not wire control line pins directly to ground, $V_{cc,}$ or a common resistor. Disabled control lines on a device can make it impossible to use the standard in-circuit library tests. A specialized test with reduced fault coverage and higher program cost is the normal result.

b. A single input vector for tri-stating a device's outputs is preferable for in-circuit testing. Reasons for tri-statable outputs are (1) testers have a limited amount of vectors, (2) the backdrive problems will disappear, and (3) it simplifies the generation of test programs. An example of this which would reduce program cost is tri-statable Programmable Array Logic (PAL) outputs. Use a spare input to a pull-up resistor plus an equation that would enable a normal function in a high state and the device outputs to be tri-stated in a low state.

c. Gate arrays and devices with high pin counts are not testable using an in-circuit tester. Backdrive may not be a problem per pin but the large numbers of pins limit backdrive restrictions. A control line or a single vector to tri-state all device outputs is recommended.

d. Node access and the inability to cover all nodes using standard in-circuit testers is a growing problem. If standard test techniques cannot be applied to detect surface mounted part faults, an alternative method should be developed.

Alternative test strategies **shall** be developed for SMT printed board assemblies with limited nodes. An example of this is a test that will partition the printed board into groups of clustering components. Each group should have control lines (for testability) and test lands to electrically isolate the cluster from the other devices or groups during test.

Another alternative test method for opens, shorts, and correct devices is boundary scan. This built-in-test-circuitry (electronic bed-of-nails) is gaining momentum in the surface mount printed board assembly area. See the IEEE Standard 1149 series of specifications for more information on boundary scan.

3.6.6 Mechanical

3.6.6.1 Uniformity of Connectors Test fixtures are most often designed for automatic or semiautomatic engagement of edge type or on-printed board connectors. Connectors should be positioned to facilitate quick engagement and should be uniform and consistent (standardized) in their relationships to the printed board from one design to another. Similar types of connectors should be keyed, or printed board geometry used, to ensure proper mating, and prevent electrical damage to the circuitry.

3.6.6.2 Uniformity of Power Distribution Arrangement and Signal Levels on Connectors The connector contact position should be uniform for AC and DC power levels, DC common and chassis ground, e.g., contact number 1 is always connected to the same relative circuit power point in each printed board design. Standardizing contact positions will minimize test fixture cost and facilitate diagnostics.

Signals of widely different magnitude should be isolated to minimize crosstalk.

Logic levels should be located in pre-designated connector contacts.

3.7 Layout Evaluation

3.7.1 Printed Board Layout Design The design layout should be such that designated areas are identified by function, e.g., power supply section confined to one area, analog circuits to another section, and logic circuits to another, etc. This will help to minimize crosstalk, simplify bare printed board and assembly test fixture design, and facilitate troubleshooting diagnostics. In addition, the design should:

- Ensure that components have all testable points accessible from the secondary side of the printed board to facilitate probing with single-sided test fixtures.
- Have vias and component holes placed away from printed board edges to allow adequate test fixture clearance.
- Require the printed board be laid out on a grid which matches the design team testing concept.
- Allow provision for isolating parts of the circuit to facilitate testing and diagnostics.
- Test points that will be used for manual testing should be placed for ease of accessability.
- The use of sockets may reduce overall reliability and result in socket related issues such as intermittent circuits, spread socket contacts, etc. Therefore, the potential risk for use of sockets needs to be carefully considered.

• Provide optic targets (fiducials) for surface mount designs to allow the use of optic positioning and visual inspection equipment and methods (see 5.4.3).

Surface mounted components and their patterns require special consideration for test probe access, especially if components are mounted on both sides of the printed board and have very high lead counts.

3.7.1.1 Layout Concepts The printed board layout depicts the physical size and location of all electronic and mechanical components, and the routing of conductors that electrically interconnect the components in sufficient detail to allow the preparation of documentation and artwork.

3.7.2 Feasibility Density Evaluation After approved documents for schematic/logic diagrams, parts lists, and end-product and testing requirements are provided, and before the actual drawing of the layout is begun, a feasibility density evaluation should be made. This should be based on the maximum size of all parts required by the parts list and the total space they and their lands will require on the printed board, exclusive of interconnection conductor routing.

The total printed board geometry required for this mounting and termination of the components should then be compared to the total usable printed board area for this purpose. Reasonable maximum values for this ratio are 70% for Level A, 80% for Level B, and 90% for Level C. Component density values higher than these will be a cause for concern. The lower these values are, the easier it will be to design a cost-effective functional printed board.

Figure 3-5 provides the usable printed board area for the standardized printed board sizes.

Printed Board Size (Fig. 5-1)	Overall Dimensions		Usable Dimensions		Usable Area		
	Height mm [in]	Width mm [in]	Length mm [in]	Width mm [in]	mm^2	Grid Elements 0.5 mm Grid	cm^2
A1	80 [3.15]	60 [2.36]					
B1	170 [6.692]						
C1	260 [10.25]						
D1	350 [13.78]						
A2	80 [3.15]	120 [4.724]					
B2	170 [6.692]						
C2	260 [10.25]						
D2	350 [13.78]						
A3	80 [3.15]	180 [7.087]					
B3	170 [6.692]						
C3	260 [10.25]						
D3	350 [13.78]						
A4	80 [3.15]	240 [9.449]					
B4	170 [6.692]						
C4	260 [10.25]						
D4	350 [13.78]						

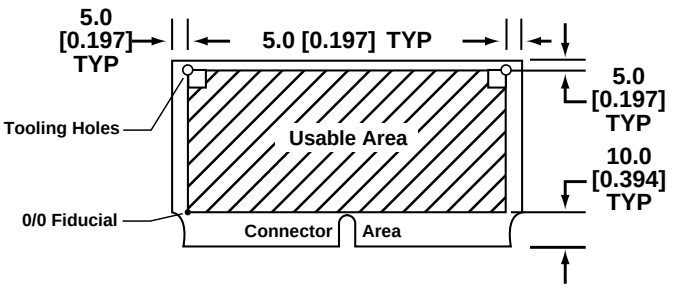


Figure 3-5 Example of Usable Area Calculation, mm [in] (Usable area determination includes clearance allowance for edge printed board connector area, printed board guides, and printed board extractor.)

Table 3-2 gives the area (in 0.5 mm [0.020 in] grid elements) a component will occupy on the printed board for a variety of components. As an example, the 14 lead dual in-line package for through-hole technology occupies a total of 84.0 grid elements. The package outline that encloses the component and land pattern has a grid matrix of 20 x 42 grid elements on 0.5 mm [0.020] centers. The 20 grid elements establish an outline dimension of 10.0 mm [0.394 in] while the 42 grid elements account for 21.0 mm [0.827 in]. This component area would use up a portion of the printed board usable area. The component outline does not include grid elements for conductor routing outside the land area. Total component area compared to total usable area provides the conductor routing availability and thus the density percentage.

Table 3-2 Component Grid Areas

Component Description	Type[1]	Number of Grid Elements[2] 0.5 mm [0.20 in] Grid	
D07 (without stress relief loop)	THT	6 x 24	144
D07 (with stress relief loop)	THT	6 x 28	168
T05	THT	20 x 20	400
T024	THT	10 x 10	100
CK05	THT	6 x 12	72
CM05, 13000pF	THT	20 x 44	880
CM06, 400pF	THT	12 x 26	312
RC07	THT	6 x 20	120
RC20	THT	10 x 26	260
RN60	THT	10 x 30	300
CQFP-10 T090	SMT	16 x 12	192
CQFP-28	SMT	34 x 34	1156
CQFP-144	SMT	68 x 68	4624
3216 (1206)	SMT	4 x 10	40
4564 (1825)	SMT	14 x 12	168
6032	SMT	8 x 18	144
DIP-14	THT	20 x 42	840
DIP-14	SMT	22 x 42	924
DIP-24	SMT	22 x 60	1320
DIP-24L	SMT	26 x 64	1664
SOD87/MLL-41	SMT	6 x 14	84
SOT23	SMT	8 x 8	64
SOT89	SMT	12 x 10	120
SOT143	SMT	8 x 8	64
SQFP 7x7-40	SMT	22 x 22	484
SOIC-20W	SMT	28 x 24	672
SOIC-36X	SMT	48 x 24	1152
TSOP 10x20	SMT	22 x 44	968
SOJ 26/350	SMT	24 x 34	816

[1]THT = Through-Hole Technology, SMT = Surface Mount Technology
[2]Grid area includes physical component outlines and land areas. It does not include space for conductor routing.

An alternative method of feasibility density evaluation expresses printed board density in units of square centimeters per equivalent SOIC. A 16-pin SOIC occupies approximately one cm^2 of printed board area. Figure 3-6 shows a table for determining the SOIC equivalent for a variety of components and the total SOIC equivalents used on the printed board. This number is then divided into the total square centimeters of usable printed board area. Reasonable maximum density values are 0.55 cm^2 per SOIC for Level A, 0.50 for Level B, and 0.45 for Level C. Density values can increase with additional circuit layers. Also, when using surface mount technology, the potential usable printed board area is theoretically doubled.

PRINTED BOARD DENSITY EVALUATION			Date of issue	No. Revised
DESCRIPTION: SOICs per square centimeter				
Comp. Name	**# of comp.**	**or**	**IC equiv**	**Comments**
8 SOIC		.50		
14 SOIC		1.00		
16 SOIC		1.00		
16L SOIC		1.00		
20 SOIC		1.25		
24 SOIC		1.50		
18 PLCC		1.13		
18L PLCC		1.13		
20 PLCC		1.25		
28 PLCC		1.75		
44 PLCC		2.75		
SOT 23		0.19		
SOT 89		0.19		
SOMC 1401		1.00		
SOMC 1601		1.00		
2012 (0805)		0.13		
3216 (1206)		0.13		
3225 (1210)		0.13		
4564 (1812)		0.13		
Others (specify)				
Total IC equivalent _____				
Total Printed Board Area	(X)		=	cm^2 cm^2
Usable Printed Board Area	(X)		=	Usable Printed Board Area Design C~riteria
				☐ Analog / ☐ Digital
				Etch & Spac. /
				PWB & GYD Sz /
	Devel. by	Date	App'd by	Date

IPC-2221b-3-06

Figure 3-6 Printed Board Density Evaluation

4 MATERIALS

4.1 Material Selection A designer of printed boards has several material choices to consider, ranging from standard to highly sophisticated and specialized. When specifying materials, the designer first determines what requirements the printed board needs to meet. These requirements include temperature (soldering and operating), electrical properties, interconnections (soldered components, connectors), structural strength, and circuit density. It should be noted that increased levels of sophistication may lead to increased material and processing costs.

When constructing a composite from materials with different temperature characteristics, the maximum end-use temperature allowable **shall** be limited to that of the lowest rated material.

Other items that may be important in the comparison of various materials include:

- Resin Formula
- Flame Resistance
- Thermal Stability
- Structural Strength
- Electrical Properties
- Flexural Strength
- Maximum Continuous Safe Operating Temperature
- Glass Transition Temperature (T_g)
- Reinforcing Sheet Material
- Nonstandard Sizes and Tolerances
- Machinability or Punchability
- Coefficients of Thermal Expansion (CTE)
- Dimensional Stability
- Overall Thickness Tolerances
- Temperature of Decomposition (T_d)

4.1.1 Material Selection for Structural Strength The first design step in the selection of a laminate is to thoroughly define the service requirements that need to be met, i.e., environment, vibration, ‘‘G’’ force, shock (impact), physical and electrical requirements.

The choice of laminate should be made from standard materials to avoid costly and time consuming proof-out tasks. Several laminates may be candidates, and the choice should be optimized to obtain the best balance of properties.

Materials should be easily available in the form and size required. Special laminate may be costly, and have long lead times. Special laminates should be analyzed against all of the parameters discussed in this section.

Items to be considered are such things as machining, processing, processing costs, and the overall specification of the raw material.

In addition to these parameters, the structural strength of the printed board should be able to withstand the assembly and operational stresses.

4.1.2 Material Selection for Electrical Properties Some of the critical properties to consider are electrical strength, dielectric constant, moisture resistance, and hydrolytic stability. Table 4-1 lists properties of some of the more common systems. Consult the laminate manufacturer utilized by the fabricator for specific values.

4.1.3 Material Selection for Environmental Properties Table 4-1 shows the properties affected by the environment for some of the more common resin systems. The stated values are typical and will vary among different material suppliers. Consult the laminate manufacturer utilized by the fabricator for specific values.

4.2 Dielectric Base Materials (Including Prepregs and Adhesives) Bonding materials described in the following paragraphs **shall** be used to bond layers of copper foil, bare laminate, copper clad laminate or heat-sinking planes to each other.

4.2.1 Preimpregnated Bonding Layer (Prepreg) Prepreg **shall** conform to the types listed in IPC-4101 or UL 746E. In most cases, the prepreg should be of the same resin and reinforcement type as the copper clad laminate. The reinforcement style, nominal resin flow, nominal scaled flow thickness, nominal gel time, and nominal resin content are process parameters normally dictated by the printed board manufacturing process.

Unless design constraints dictate, these values **shall not** be included on master drawings, but **shall** only be specified and used in procurement specifications by the printed board manufacturer.

4.2.2 Adhesives Adhesives used in printed board assemblies are drawn from at least five basic resin types covering a wide range of properties. In addition to adhesion quality or bond strength, criteria for adhesive selection include hardness, CTE, service temperature range, dielectric strength, cure conditions and tendency for outgassing. In some cases structural adhesives may be sufficient for thermal bonding applications, see 4.2.5. Each adhesive type has both strong and weak points.

Selection of a resin system for an adhesive or encapsulant is to be based on the characteristics of the materials being bonded and their compatibility. Special treatments, such as primers or activators, may be required to suitably activate surfaces for bonding. The selection process should also consider the exact purpose of the adhesive bond and its use environment. Fungus inert materials are also a consideration. Not all adhesives are suitable for direct application on or near electronic products due to either their chemical or dielectric properties. Incorrect selection of materials may result in product degradation or failure.

In actual application, most adhesive needs can be addressed by a few carefully selected materials. Storage and shelf life limitations apply to most of these materials.

4.2.2.1 Epoxies Epoxy resin formulations are among the most versatile adhesives for electrical insulating and mechanical bonding applications. They offer a wide range of physical and electrical properties, including adhesive and cohesive strengths, hardness, chemical resistance, thermal conductivity and thermal vacuum stability. They are also available with a wide range of cure methods and times. A thorough review of the material is warranted, based on its intended use. Thermal coefficient of expansion and glass transition temperatures should be considered, in addition to other properties, to preclude problems. Epoxies are available with a variety of modifiers, fillers and reinforcements for specific applications and extended temperature ranges.

4.2.2.2 Silicone Elastomers Silicone elastomers are generally noted for being resilient materials with very good electrical and mechanical properties at ambient and extreme temperatures. Several curing methods are available, including moisture, metallic salts and others. Silicone elastomers which evolve acetic acid during their cure should be avoided in electronic applications. Bond strength, tensile strength, and hardness properties tend to be considerably lower than epoxies. Silicones will swell and dissolve with prolonged exposure to some chemicals. Some of the metallic salts curing silicones will react with TFE and PTFE materials. Conformal coatings other than silicones generally will not adhere to cured silicone materials. Silicones are often used as a cushioning overcoat for articles which will be encased in hard potting compounds later.

A number of high purity grades of silicones are available which offer good thermal vacuum stability. Silicone gels are also available, which offer enhanced properties as encapsulants. These materials generally require physical restraint, such as a potting cup or enclosure to maintain their form, once applied.

4.2.2.3 Acrylics Acrylic resins generally provide rapid cures, good electrical and adhesive properties and hardness. Chemical resistance and thermal vacuum stability tend to be considerably lower than the epoxies. The glass transition temperature of these materials also tends to be low.

4.2.2.4 Polyurethanes Polyurethanes are available in almost as many variations as the epoxies. These materials generally offer toughness, high elasticity, a wide range of hardness, and good adhesion. Some of the urethane compounds are outstanding as vibration and shock damping materials. Moisture and chemical resistance is relatively high, but varies with the individual product. Thermal vacuum stability will also vary by the individual product formulation. Many of the urethanes can be used in a relatively thick application as a local vibration damping compound.

4.2.2.5 Specialized Acrylate-Based Adhesives This category includes the cyanoacrylates (instant cure) and anaerobic adhesives (cure without air). The cyanoacrylates form strong bonds within seconds without catalysts when only a trace amount of moisture is present on a surface. The anaerobic adhesives cure in the absence of oxygen when a peroxide additive can be decomposed by certain transition metal ions. Both adhesive types can give high initial bond strengths which may

Table 4-1 Typical Properties of Common Dielectric Materials[1]

Property	Material						
	Difunctional/ Multifunctional Epoxy (IPC-4101/21)	Epoxy/Multi-functional Epoxy (IPC-4101/24)	Epoxy/Multi-functional Epoxy (IPC-4101/26)	Epoxy Triazine (IPC-4101/29)	Bismaleimide Triazine Epoxy (IPC-4101/30)	Polyimide E-glass (IPC-4101/41)	Polyimide Nonwoven Aramid (IPC-4101/53)[6]
Electric Strength[2] (kV/mm)	47	50	53	47	46	51	51
Moisture Absorption (wt%)	0.17	0.15	0.15	0.1	0.15	0.44	0.6
Dissipation Factor (Loss Tangent) @1 MHz	0.022	0.022	0.021	0.008	0.011	0.012	0.015
Thermal Expansion xy-plane (ppm/°C)	12-16	12-16	11-16	10-14	10-15	12-17	6-9
Thermal Expansion z-axis below T_g[5] (ppm/°C)	50-80	50-55	50-55	_	55-70	40-60	80-90
Glass Transition Temp. T_g (°C) (IPC-4101)	110 - 150	150 - 200	170 - 220	170 - 220	170 - 220	200- 250	220 minimum
Glass Transition Temp. T_g (°C) (DSC)	140	170-175	175 - 180	210	185-200	250 - 260	240
Flexural Modulus (Pa)							
Fill[3]	1.86×10^{10}	1.86×10^{10}	1.93×10^{10}	1.93×10^{10}	2.07×10^{10}	2.69×10^{10}	4.8×10^{8}
Warp[4]	1.20×10^{10}	2.07×10^{10}	2.20×10^{10}	2.20×10^{10}	2.41×10^{10}	2.89×10^{10}	
Tensile Strength (Pa)							
Fill[3]	4.13×10^{10}	4.13×10^{10}	4.13×10^{10}	4.13×10^{10}	3.93×10^{10}	4.82×10^{10}	3.14×10^{7}
Warp[4]	4.82×10^{10}	4.48×10^{10}	5.24×10^{10}	5.24×10^{10}	4.27×10^{10}	5.51×10^{10}	

Note 1. For values of dielectric constant, see Table 6-2.
Note 2. The stated electrical strength values are commonly evaluated under test conditions with a 0.125 mm [0.00492 in] core laminate thickness. These values should not be considered linear for high voltage designs with a minimum dielectric separation, i.e., less than 0.09 mm [0.00354 in].
Note 3. Fill-yarns that are woven in a crosswise direction of the fabric.
Note 4. Warp (cloth)-yarns that are woven in the lengthwise direction of the fabric.
Note 5. Z-axis expansion above T_g can be as much as four times greater. For FR-4 it is 240-390 ppm. Contact supplier for specific values of the other materials.
Note 6. Values for fill and warp do not apply for a random fiber.

be beneficial for wire staking and temporary bonding applications. The instant cure adhesives generally have poor impact resistance and are susceptible to degradation from exposure to moisture and temperatures over 82 °C [179.6 °F]. The anaerobic adhesives have the capability of withstanding higher temperatures but can lose strength with prolonged exposure to chemicals.

4.2.2.6 Other Adhesives Many other types and forms of adhesives are available, including polyesters, polyamides, polyimides, rubber resins, vinyl, hot melts, pressure sensitive, etc. Where they are used is determined by the needs of the design and its performance requirements. Selection of specialized items, such as chip bond adhesives, should be done in conjunction with the using facility, in order to ensure full compatibility of the equipment and process.

4.2.3 Adhesive Films or Sheets Adhesive films or sheets used for bonding heatsinks, stiffeners, etc., or as insulators, are generally in accordance with IPC-4203 or IPC-4101.

Film type adhesives find many uses in laminated structures. The ability to pre-cut a film adhesive to fit given shapes or dimensions is a distinct advantage in the fabrication of some laminated parts. Epoxy based film adhesives provide very good bond strength but require elevated temperature cure. Film adhesives are commonly used to bond printed board heatsinks to printed boards.

Through-hole technology (THT) printed boards and heatsinks may be bonded together with a dry epoxy sheet adhesive to improve heat transfer or resist vibration. These adhesives consist of an epoxy impregnated glass cloth which is cut to the heatsink configuration, assembled between printed board and heatsink, then cured with heat and pressure. The cured adhesive is strong and resists vibration, temperature extremes, and solvents. Thicknesses of 0.1 mm [0.0039 in] should be adequate for most applications. If necessary, specify two sheets.

4.2.4 Electrically Conductive Adhesives This class of adhesives consists, generally, of a conductive filler, such as graphite (carbon) or silver, embedded in a polymeric resin adhesive system, which is loaded into the material to achieve conductivity. Volume resistivity, a measure of the electrically conductive property of the material, may be varied over a range of values consistent with the intended application. This is accomplished by the type of filler used and the loading. Bonding strength of these materials can be compromised by the filler material.

Epoxies, silicone elastomers and urethanes are the resin systems commonly used to formulate conductive adhesives. The strongest bonds are generally achieved with conductive epoxy. Silicone elastomers follow, with urethanes a close third. Cure conditions and filler content have a pronounced effect upon tensile strength of these materials. The choice of conductive adhesive for a particular application should consider the strength of bond, the service temperature, the effect of CTE on the bond and the volume resistivity or conductivity required.

4.2.5 Thermally Conductive/Electrically Insulating Adhesives Thermally conductive adhesives are filled versions of epoxy, silicone, urethane and some acrylic base materials. The filler is normally dried aluminum oxide or magnesium oxide powder.

4.2.5.1 Epoxies The epoxies offer the greatest bond strength and best solvent resistance, along with good thermal conductivity and electrical resistance. As with most two part systems, the choice of catalyst has an impact on cure conditions and ultimately could affect the glass transition temperature, since it is somewhat dependent upon cure conditions.

4.2.5.2 Silicone Elastomers The silicone elastomers are characterized by relatively low bond strengths and less rigidity (lower hardness) than epoxies. They are less resistant to solvent attack than epoxy and are two part systems with other variable properties dependent upon formulation. Thermal conductivity and electrical resistance properties are good.

Silicone elastomers may be obtained as humidity curing or heat curing, the latter offering accelerated cure with applied heat. They cure well in contact with most materials except butyl and chlorinated rubbers, some RTV silicone elastomers and residues of some curing agents. Some bonding applications may require a primer.

4.2.5.3 Urethanes Urethanes can be varied through a wide range of hardness, tensile and electrical properties by varying the proportions of curing agent to resin. Consistency can be varied from a soft, rubbery state to a hard, rigid condition by this method. The latitude for formulation optimization over a range of application conditions is an advantage offered by the filled urethanes.

The urethanes are characterized by relatively low bond strengths and less rigidity (lower hardness) than epoxies. They are less resistant to solvent attack than epoxy; are two part systems with variable other properties dependent upon formulation. Thermal conductivity and electrical resistance properties are good.

4.2.5.4 Use of Structural Adhesives as Thermal Adhesives In design circumstances where thermal conduction properties are not critical, the use of structural adhesives (see 4.2.2) in place of thermal adhesives may be acceptable as determined by thermal analysis and may be a more cost effective alternative.

4.3 Laminate Materials Laminate materials **shall** be selected from material listed in IPC-4101, IPC-4103 or IPC-4202, as applicable.

When the Underwriters Laboratories Inc. (UL) recognized component mark is required, the designer should ensure that the specified laminate is certified to the required flammability rating. Typically FR-4 materials are ''94 V-0'' certified, where ''94'' refers to the specification UL-94, the letter(s) refers to the test performed and the number refers to the results grade. Other materials such as some polyimides may have ''94 HB''; some high frequency materials have no rating. The flammability rating of the material can typically be found on the laminate's datasheet which can usually be found on the manufacturer's web site.

The fabricator of the printed board should also have their product, the combination of that material and their fabrication processes, be UL certified to be able to mark the printed board with the flammability rating. Constructions using more than one laminate type, such as rigid-flex or hybrids, which combine epoxy fiberglass with polyimide or PTFE, require that the fabricator be certified for that combination even if they are certified for each individually.

The printed board design **shall** be such that internal temperature rise due to current flow in the conductor, when added to all other sources of heat at the conductor/laminate interface, will not result in an operating temperature in excess of that specified for the laminate material or maximum sustained operating temperature of the assembly.

Since heat dissipated by parts mounted on the printed boards will contribute local heating effects, the material selection **shall** take this factor, plus the equipment's general internal rise temperature, plus the specified operating ambient temperature for the equipment into account for maximum operating temperature.

Hot spot temperatures **shall not** exceed the temperatures specified for the laminate material selected. See IPC-2222 for maximum operating temperature specified for laminate materials. Materials used (copper-clad, prepreg, copper foil, heatsink, etc.) **shall** be specified on the master drawing.

4.3.1 High T_g Laminates High temperature laminates include those made from resins, and blends of resins, such as Epoxy, Cyanate Ester, Bismaleimide-Triazine, Modified Thermoplastics, and Polyimide. High temperature laminates offer the advantages of increased chemical resistance and thermal stability. They are commonly used to improve the reliability of a device where extremes of thermal cycles and temperatures are expected during assembly or use. Disadvantages may include the need for specialized processing and/or higher material cost.

4.3.2 Color Pigmentation Natural colored stock is preferred, because whenever a pigment is added to change a color, the possibility exists for the pigment to retard the ability of the impregnating resin to completely wet each and every glass fiber. Without complete wetting, moisture can be trapped.

Colored stock should not be used because the material usually costs more. Production delays may also be incurred because of lack of availability of the colored stock. If colored stock is required, it **shall** be specified on the procurement documentation.

4.3.3 Dielectric Thickness/Spacing The minimum dielectric thickness/spacing **should** be specified on the master drawing. When raw materials are specified on the master drawing, classes and tolerances **shall** be selected compatible with end item dielectric thickness requirements. Recognize that when material is called out as nominal thicknesses, such as 0.1 mm [0.0039 in.] IPC-4101 Class M core for example, tolerance or process variation can take the thickness below the minimum, which is 87 µm [3,425 µin].

4.3.4 Thermally Conductive Laminates Several composite laminates have been developed to increase heat dissipation. These laminates should be selected from IPC-4101. If the laminate requirements are not in the IPC specifications, the requirements **shall** be as specified on the master drawing and AABUS.

4.3.5 Minimum Base Material Thickness for PC Card Form Factors The minimum base material thickness associated with PC card form factor printed boards is generally much thinner than conventional printed board technology, with a single ply of dielectric material between conductive layers. Copper cladding used with these materials may require a low profile foil to ensure the insulating properties of clad base materials. This can be implemented by specificying IPC-4562 with foil profile type "L."

4.4 Conductive Materials The primary function of metallic coatings is to contribute to the formation of the conductive pattern. Beyond this primary function, specific platings offer such additional benefits as corrosion prevention, improved long term solderability, wear resistance, and others.

The thickness and integrity requirements for metallic platings and coatings on as-produced printed boards **shall** be in accordance with the requirements of Table 4-2 through Table 4-5 for the appropriate class of equipment (see also IPC-6012, IPC-6013, IPC-6018, etc.). Unless otherwise specified on the master drawing, metallic platings and coatings **shall** meet the requirements specified in 4.4.1 through 4.4.11. Attention should be paid to the effects of dissimilar metals in areas such as connectors, sockets, and other interfaces. The result of a poor material selection could be a reduction in function, either mechanical or electrical. Table 4-6 provides guidance on these metallic platings and coatings for use in lead-free soldering environments and should be tempered by evaluation of each individual application.

Table 4-2 Final Finish and Coating Requirements

Code	Finish	Thickness	Applicable Acceptability Specification	Marking Code[1]
S	Solder Coating over Bare Copper	Coverage & Solderable[2]	J-STD-003 J-STD-006	b0
b1	Lead-Free Solder Coating over Bare Copper	Coverage & Solderable[2]	J-STD-003 J-STD-006	b1
T	Electrodeposited Tin-Lead (fused) - minimum	Coverage & Solderable	J-STD-003 J-STD-006	b3
X	Either Type S or T	As indicated by code		
TLU	Electrodeposited Tin-Lead Unfused - minimum	8.0 µm [315 µin]	J-STD-003 J-STD-006	b3
G	Gold for edge printed board connectors and areas not to be soldered - minimum	Class 1 and Class 2 0.8 µm [31.5 µin]	None	b4
		Class 3 1.25 µm [49.21 µin]		
GS	Gold Electroplate on areas to be soldered - maximum[3]	0.45 µm [17.72 µin]	None	b4
GWB-1	Gold Electroplate for areas to be wire bonded (ultrasonic) - minimum	0.05 µm [1.97 µin]	None	b4
	Electrolytic nickel under gold for areas to be wire bonded (ultrasonic) - minimum	3 µm [118 µin]	None	b4
GWB-2	Gold Electroplate for areas to be wire bonded (thermosonic) - minimum	Class 1 and Class 2 0.3 µm [11.8 µin]	None	b4
		Class 3 0.8 µm [31.5 µin]		
	Electrolytic nickel under gold for areas to be wire bonded (thermosonic) - minimum	3 µm [118 µin]	None	b4
N	Nickel - Electroplate for edge printed board connectors - minimum	Class 1 2.0 µm [78.7 µin]	None	N/A
		Class 2 and Class 3 2.5 µm [98.4 µin]		
NB	Nickel-Electroplate as a barrier[4] - minimum	1.3 µm [51.2 µin]	None	N/A
OSP	Organic Solderability Preservative	Solderable[5]	None	b6
HT OSP	High Temperature OSP	Solderable[5]	None	b6
ENIG	Electroless Nickel - minimum	3 µm [118 µin]	IPC-4552	b4
	Immersion Gold - minimum	0.05 µm [1.97 µin][6]		b4

Code	Finish	Thickness	Applicable Acceptability Specification	Marking Code[1]
ENEPIG	Electroless Nickel - minimum	3 µm [118 µin]	IPC-4552	b4
	Electroless Palladium - minimum	0.05 µm [2 µin]	None	N/A
	Immersion Gold - minimum	Coverage and Solderable[6]	None	b4
DIG	Direct Immersion Gold (Solderable Surface)	Solderable[6]	None	b4
IS	Immersion Silver	Solderable[7]	IPC-4553	b2
IT	Immersion Tin	Solderable[8]	IPC-4554	b3
C	Bare Copper	AABUS	AABUS	N/A

Note 1. These marking and labeling codes represent the codes for surface finish categories established in IPC/JEDEC-J-STD-609.
Note 2. No finish thickness requirement is needed to be specified on drawing. See also 4.4.10.1.
Note 3. Industry investigations have shown that a gold-tin intermetallic phase forms under normal soldering process parameters when the weight percent of gold in the solder joint reaches the 3-4% range. Refer to IPC-J-STD-001 and IPC-HDBK-001 for further information on gold removal to prevent the formation of brittle solder joints resulting from high concentrations of gold dissolving into the solder joint.
Note 4. Nickel plating used under the tin-lead or solder coating for high temperature operating environments act as a barrier to prevent the formation of copper-tin compounds.
Note 5. See 4.4.7.
Note 6. See 4.4.4.1 through 4.4.4.3.
Note 7. See 4.4.5.
Note 8. See 4.4.6.

Table 4-3 Surface and Hole Copper Plating Minimum Requirements for Buried Vias >2 Layers, Through-Holes, and Blind Vias[1]

	Class 1	Class 2	Class 3
Copper - average[2]	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
Thin areas	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
Wrap3	AABUS	5 µm [197 µin]	12 µm [472 µin]

Note 1. Does not apply to microvias (see 1.5.1).
Note 2. Copper plating thickness **shall** be continuous and extend or wrap from hole walls onto outer surfaces. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.
Note 3. Wrap copper plating for filled PTHs and vias **shall** be in accordance with IPC-6012.

Table 4-4 Surface and Hole Copper Plating Minimum Requirements for Microvias (Blind and Buried)[1]

Copper - average[2]	12 µm [472 µin]	12 µm [472 µin]	12 µm [472 µin]
Thin areas	10 µm [394 µin]	10 µm [394 µin]	10 µm [394 µin]
Wrap[3]	AABUS	5 µm [197 µin]	6 µm [236 µin]

Note 1. See 1.5.1 for definition of microvia.
Note 2. Copper plating thickness **shall** be continuous and wrap from hole walls onto outer surfaces. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.
Note 3. Wrap copper plating for filled microvias **shall** be in accordance with IPC-6012.

Table 4-5 Surface and Hole Copper Plating Minimum Requirements for Buried Via Cores (2 Layers)

Copper - average[1]	13 µm [512 µin]	15 µm [592 µin]	15 µm [592 µin]
Thin areas	11 µm [433 µin]	13 µm [512 µin]	13 µm [512 µin]
Wrap[2]	AABUS	5 µm [197 µin]	7 µm [276 µin]

Note 1. Copper plating (1.3.4.2) thickness **shall** be continuous and extend or wrap from hole walls onto outer surfaces. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.
Note 2. Wrap copper plating for filled buried via cores **shall** be in accordance with IPC-6012.

Table 4-6 Surface Finishes

Application	Lead-Free Hot Air Solder Level	Organic Solderability Preservative	Electroless Nickel/ Immersion Gold	Electroless Nickel/ Electroless Palladium/ Immersion Gold	Electroless Nickel/ Immersion Palladium/ Immersion Gold	Electroless Nickel/ Electroless Palladium/ Electroless Gold[1]	Electrolytic Nickel/ Electrolytic Gold[1]	Electroless Nickel/ Immersion Gold/ Electroless Gold[1]	Immersion Tin	Immersion Silver
Finish Code	LF-HASL	OSP	ENIG	ENEPIG	ENIPIG	ENEPEG	Ni/Au	ENIG/EG	ISn	IAg
Soldering	◐	◐	●	●	●	●	◐	◐	◐	●
Gold Embrittlement	●	●	●	●	●	◐	◐	◐	●	●
Switch Contacts	○	○	●	●	●	●	●	●	○	◐
Wire Bonding	○	○	●	●	●	●	●	●	○	○
Press Fit	●	○	●	●	●	●	●	●	●	◐
Compliant Pin	●	○	●	●	●	●	●	●	◐	◐
Edge Board Connector	○	○	◐	◐	◐	●	●	◐	○	○
Shelf Life (1 year)	◐	●	●	●	●	●	●	●	◐	◐
Oxidation Resistance	●	○	●	●	●	●	●	●	◐	◐
Solderable After Multiple Reflow Cycles	●	●	●	●	●	●	●	●	○	●
Coplanarity	○	●	●	●	●	●	●	●	●	●
Radio Frequency (RF)	◐	●	◐	◐	◐	◐	◐	◐	●	●
Special Packaging[2]	●	●	●	●	●	●	●	◐	●	●

Note 1. Embrittlement becomes a concern when the gold thickness is in excess of 0.45 µm [17.72 µin]. Embrittlement is a function of gold thickness and not of gold type.
Note 2. Refer to IPC-1601.

●= Preferred ◐ = Functional ○ = Not Recommended

4.4.1 Electroless Copper Plating Electroless copper is deposited on the surface and through holes of the printed board as a result of processing the drilled panel through a series of chemical solutions. Typically, this is the first step in the plating process and is usually 0.6 to 2.5 µm [24 to 98.4 µin] thick. Electroless copper can also be used to fully build the required copper thickness, which is referred to as additive plating.

4.4.2 Semiconductive Coatings Semiconductive coatings for direct metallization are used as a conductive starter coating prior to electrolytic copper plating and are applied to the hole wall. The coating should be of sufficient quality for subsequent metallic deposition and **shall** be non-migrating. This process is typically fabricator dependent and is not specified on the master drawing. Palladium and tin are commonly used materials. A thin layer is deposited on exposed surfaces, especially inside drilled holes. This provides a surface for auto-catalyzing the electroless copper deposition.

4.4.3 Electrolytic Copper Plating Electrolytic copper can be deposited from several different electrolytes, including copper fluoroborate, copper cyanide, copper sulfate, and copper pyrophosphate. Copper sulfate and copper pyrophosphate are the most commonly used electrolytes for building the copper deposition on the surface and through the holes to the required thickness. This type of plating usually produces the final copper thickness requirement.

4.4.4 Gold Plating A variety of gold platings are available for depositions on printed boards. These may be electrolytic, electroless, or immersion deposits. The electrolytic deposition may come in 24k soft gold, 23+k hard gold (hardening uses trace amounts of cobalt, nickel, or iron which are co-deposited with the gold), or the plating may be a lower karat alloy (14 - 20k) for some applications. Gold plating serves several purposes:

- To act as a self lubricating and tarnish resistant contact for edge printed board connectors (see Table 4-2). Hard electrolytic gold plating is most often used for this application.
- To prevent oxidation of underlying plating such as nickel and electroless nickel so as to enhance solderability and extend storage life. Electrolytic, immersion and electroless gold are most often used for this purpose (see Table 4-2 for thickness).
- To provide a wire bonding surface. This application employs a soft 24k electrolytic gold, see Table 4-2 for thickness.
- To provide an electrically conductive surface on printed boards when electrically conductive adhesives are used. A minimum thickness of 0.25 µm [9.84 µin] is recommended.
- To act as an etch resist during printed board fabrication, a minimum thickness of 0.13 µm [5.12 µin] is recommended.

Electrolytically deposited gold is often specified as required to meet ASTM-B-488 with the type and grade selected to satisfy the different applications. A low-stress nickel or electroless nickel **shall** be used between the gold overplating and the basis metal when gold finish is to be used for electrical or wire bonding.

Table 4-7 will help clarify some of the uses for the various alloys.

Table 4-7 Gold Plating Uses

Minimum Purity	Knoop Hardness	Contacts	Wire Bonding	Soldering
99.0	130-200	S	C*	C**
99.0	90 max	NR	S	C**

S - Suitable use NR - Not recommended C - Conditional use

* May be used, but will depend on type of wire bonding being used. Run Test prior to wire bonding.

** More than 0.45 µm [17.72 µin] gold on printed boards or leads may cause embrittled solder joints.

4.4.4.1 Electroless Nickel/Immersion Gold (ENIG) ENIG (Electroless Nickel/Immersion Gold) is widely used as a surface finish for high density SMT designs. The surface is coplanar and is compatible with eutectic and lead-free solders. It is widely considered an ideal contacting surface. It is also aluminum wire bondable and its shelf life can exceed 12 months.

The thickness of the deposit **shall** comply with IPC-4552 which specifies Ni between 3 - 6 µm [118 - 236 µin] and a gold thickness of 0.05 µm [1.97 µin] minimum. Attempting to put more than 0.125 µm [4.92 µin] of gold using the ENIG process could result in corrosion and loss of solderability of the underlying Ni and give rise to the phenomenon of ‘‘Black Pad.’’ Black pad is a deterioration of the pad surface finish. See IPC-4552 for a complete discussion.

The bare printed board requirements for deposit thickness of the ENIG should be verified using X-Ray Fluorescence (XRF), or similar, measurement. Class 1 and Class 2 products require, as a minimum, five measurements per lot. Class 3 product measurements are AABUS, and the procurement documentation **shall** specify the minimum frequency of thickness verification. For consistency, all measured pad sizes **shall** have an area approximately 1.5 x 1.5 mm [0.060 x 0.060 in]. The advantages and limitations of ENIG are outlined in Table 4-8.

Table 4-8 ENIG Surface Finish Advantages and Disadvantages

Advantages	Limitations
Uniform coplanar surface	Moderately higher cost to OSP or HASL
Excellent wettability, with eutectic and lead-free solder	Multi-step process
Multiple lead-free reflow cycles	Requires good process control
Ideal contacting surface	Poor process control may lead to Black Pad
Aluminum wire bondable	Not recommended for gold wire bonding
Shelf-Life - capable of J-STD-003 Category 3 durability	Limited re-workability at the printed board level
Improved PTH reliability	Solder mask **shall** be fully cured before ENIG plating
Nickel barrier reduces copper dissolution during lead-free solder assembly and/or rework	

Note: In spite of ENIG's potential for ''black pad'' or nickel corrosion, it remains a widely used surface finish, particularly for lead-free soldering. Nickel corrosion occurs during the gold deposition step. It only occurs on a compromised Ni deposit coupled with extended dwell in an aggressive gold bath, Focus on ENIG pre-treatment and control of the Ni bath will produce the desired nickel deposit that is not susceptible to corrosion. Limiting the gold thickness and hence dwell time in the gold deposition step has come a long way in eliminating the defect.

4.4.4.2 Electroless Nickel/Immersion Gold/Electroless Gold (ENIG/EG) The finish is used for gold wire bonding and in compression connections. Some gold wire bonding requires a thicker gold than ENIG or ENEPIG can supply. The immersion gold serves as an initiator for electroless gold deposition, as electroless gold does not initiate directly on electroless nickel. The surface is coplanar and has excellent shelf life, in excess of 12 months.

The thickness of the deposit is designed to meet the requirements of the intended use. For gold wire bonding, the minimum thickness per Table 4-2 would be sufficient to ensure proper bonding and shelf life stability. Thicker gold in the order of 1.0 µm [40 µin] may be needed for compression connections.

ENIG/EG is not ideal for soldering, as the thicker gold layer may embrittle the solder joint, depending on the volume of solder used in the joint.

The bare printed board requirements for deposit thickness of the nickel and gold should be verified with an appropriate instrument, such as, X-Ray Fluorescence (XRF) Spectrometry.

The advantages and limitations of ENIG/EG are outlined in Table 4-9.

Table 4-9 ENIG/EG Surface Finish Advantages and Limitations

Advantages	Limitations
Uniform coplanar surface	Limited applicability for soldering
Gold wire bondable	Multi-step process
Compression connection surface	More stringent process control of electroless gold required
Improved PTH reliability	Moderately higher cost to OSP or HASL
Shelf-Life - capable of J-STD-003 Category 3 durability	Limited re-workability at the bare printed board level
No copper sidewalls, No overhang or slivers, pad completely encapsulated	

4.4.4.3 Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG) ENEPIG is a very versatile surface finish with a wide range of applications. It has gained popularity as a surface finish for high density SMT designs. The surface is coplanar and is compatible with eutectic and lead-free solders. ENEPIG forms a very robust solder joint with copper bearing lead-free solders, such as, SAC alloys. It is a surface finish that is both aluminum and gold wire bondable with a shelf life that can exceed 12 months. ENEPIG is suitable to replace multiple finishes used for soldering, wire bonding and/or contact surfaces on the same printed board.

Most users specify nickel thickness between 3 - 6 µm [118 - 236 µin], palladium thickness in the range of 0.05 - 1.0 µm [1.97 - 40.0 µin] and immersion gold layer **shall** have coverage and be solderable (Common gold plating results in a thickness from 0.025 to 0.1 µm [0.984 - 4.0 µin]). If the finish is going to be used for both soldering and wire bonding, then, the thinner palladium thickness (0.1 µm [4.0 µin]) is recommended. If the finish will not be used for soldering, a higher palladium thickness may be specified. As of the publication to this revision of IPC-2221, the IPC-4556 specification for ENEPIG is under development.

The bare printed board requirements for deposit thickness of the nickel and palladium should be verified with an appropriate instrument, such as X-Ray Fluorescence (XRF) Spectrometry. For consistent data, all measured land sizes should have an area approximately 1.5 x 1.5 mm [0.060 x 0.060 in]. Class 1 and Class 2 products require, as a minimum, five measurements per lot. Class 3 product measurements are AABUS. It is, therefore, recommended that an inspection plan be established for the quantity and extent of XRF measurements for Class 3 product. A pull test may be desirable for some wire bond applications. A custom coupon may be utilized.

The advantages and limitations of ENEPIG are outlined in Table 4-10.

Table 4-10 ENEPIG Surface Finish Advantages and Disadvantages

Advantages	Limitations
Uniform coplanar surface	Moderately higher cost to OSP or HASL
Excellent wettability, with eutectic and lead-free solder	Multi-step process
Multiple lead-free reflow cycles	Requires good process control
Ideal contacting surface	Limited re-workability at the bare printed board level
Shelf-Life - capable of J-STD-003 Category 3 durability	Solder mask **shall** be fully cured before ENEPIG plating.
Aluminum and gold wire bondable	Difficult to build thicker gold finishes over palladium
Improved PTH reliability	High palladium thicknesses combined with solders containing lead have the potential of generating embrittled solder joints
No probability of ‘‘Black Pad’’	
Alleviates copper dissolution from hole walls	

4.4.5 Immersion Silver Immersion silver is a viable solderable surface finish for all categories of printed boards. The surface is coplanar and is compatible with eutectic and lead-free solders. It may be the preferred finish for very high frequency RF applications because it avoids the skin effect problem that may arise with nickel-gold finishes. The immersion silver coating consists of pure silver and a small amount of organic additives. At assembly, the silver is dissolved in the solder and a Cu/Sn intermetallic (IMC) is formed.

As this surface finish has established itself in the marketplace, its advantages and weaknesses have become better understood. Instances of interfacial voiding reported by early users have been resolved. Immersion silver is susceptible to creep corrosion in humid environments that contain sulfur compounds. Solder mask defined lands are more susceptible to creep corrosion, as compared to pattern defined lands.

The IPC immersion silver specification, IPC-4553, specifies the minimum thickness.

Appropriate packaging and storage of immersion silver finishes is important to preserve solderability. See IPC-4553.

The advantages and limitations of Immersion Silver Surface Finish are outline in Table 4-11.

Table 4-11 Immersion Silver Surface Finish Advantages and Disadvantages

Advantages	Limitations
Uniform coplanar surface	Limited re-workability at the bare printed board level
Excellent wettability, with eutectic and lead-free solder	Solder mask **shall** be fully cured before Immersion silver plating
Low loss finish compatible with RF design requirements	Reduced Shelf Life - in environments containing sulfur compounds or chlorides
	Excessive thickness of IAg combined with lead-free silver bearing solder, has the potential to create an embrittled solder joint
	No Nickel barrier allows copper dissolution during lead-free solder assembly and/or rework

4.4.6 Immersion Tin Immersion tin is a viable solderable surface finish for all categories of printed boards. The surface is coplanar and is compatible with eutectic and lead-free solders. It has been used for very high frequency RF applications because it avoids the skin effect problem that may arise with nickel-gold finishes.

The immersion tin coating consists of pure tin, some formulations contain small quantities of silver for whisker mitigation and a small amount of organic additives. At assembly, the deposit is dissolved in the solder and a Cu/Sn IMC is formed.

IPC-4554 covers this surface finish and it is the one finish currently that has been broken into 3 categories of coating durability - this is a function of copper migration through the deposit and the number of thermal cycles in assembly the deposit

will see. Thicknesses should be specified as a function of coating durability categories, in accordance with IPC-J-STD-003, and may be found in IPC-4554. It is imperative that the correct thickness of tin, devoid of copper, be specified for a particular assembly process. Failure to do so, or receiving product that does not meet the specified requirements, will result in solderability defects. The same 1.5 x 1.5 mm [0.060 x 0.060 in] pad size is used for XRF measurements, as this is the standard pad size for all surface finish measurements.

Appropriate packaging and storage of immersion tin finishes is important to preserve solderability. See IPC-4554 and IPC-1601. Unlike other finishes, heat is a key driver in the degradation of performance of this finish. Heat facilitates the migration of copper through the tin finish to the surface, resulting in oxidation and loss of solderability.

The advantages and limitations of Immersion Tin Surface Finish are outlined in Table 4-12.

Table 4-12 Immersion Tin Surface Finish Advantages and Disadvantages

Advantages	Limitations
Uniform coplanar surface	Rapid diffusion of copper through the deposit can impact shelf life - specify coating durability
Forms CuSn IMC's - predictable solder joints	Deposit is "dirty" requiring special cleaning post plating
Easy to measure by XRF	Deposit is soft and mars easily
Low loss finish compatible with RF design requirements	Very aggressive chemistry on solder masks, especially around annular rings
Excellent wettability with eutectic and lead-free solder	Tin whiskers have been reported in some instances - some chemistries offer mitigation strategies (i.e., silver)
	No Nickel barrier allows copper dissolution during lead-free solder assembly and/or rework
	Limited re-workability at the bare printed board level
	Not suitable as a surface finish for either aluminum or gold wire bonding due to the instability and metallurgical incompatibility of the deposit

4.4.7 Organic Solderability Preservative (OSP) OSP is a general term that describes a variety of water based surface treatments containing organic compounds that are designed to serve the same function. They coat the copper surface by forming an organo-metallic complex, whose thickness and chemical composition may range from a molecular monolayer, to complex films with thicknesses up to 0.5 µm [19.7 µin]. OSPs are copper surface specific and are often designed specifically to minimize film formation on gold or other surfaces. The coatings protect the underlying copper from oxidation, thus preserving its solderability.

Some examples of classes of organic compounds used in OSPs are benzotriazoles, imidazoles and benzimidazoles. The ability of a particular OSP to withstand thermal excursions at assembly can be affected by a variety of formulation factors including the choice of organic compound. The simpler types may only withstand a single eutectic thermal excursion, while the more sophisticated ones can withstand multiple thermal excursions even at lead-free soldering temperatures, with or without a nitrogen atmosphere.

When selecting OSP as a surface finish, it is advisable to work with the assembler to confirm that the assembly conditions (for example, number and type of reflow cycles, in-process hold times) are compatible. Some designs are not suitable for OSP. Fabricators often process a single OSP proprietary product, so specifying an OSP may limit the choice of suppliers.

If the paste print screen openings are smaller than the land, there may be exposed copper after assembly, because OSP finishes provide only very limited solder spread.

During assembly, the OSP coating is removed when it comes in contact with soldering flux. The intermetallic formed at the solder joint/land interface is a Cu/Sn compound. The OSP coating, itself, does not become part of the solder joint.

Shelf life of OSP coated printed boards may be as high as 12 months, but will vary depending on the type of OSP, the packaging and storage conditions and the application/assembly process conditions. Printed boards that have exceeded their shelf life may become oxidized which will then require rework by stripping and recoating.

The advantages and limitations of OSP are outlined in Table 4-13.

4.4.8 Nickel Plating Nickel plating serves a dual function in contact plating: 1) It provides an anvil effect under the gold providing an essential extra hardness to the gold; 2) It is an effective barrier layer (when its thickness exceeds 2.5 µm [98.4 µin]) which prevents the diffusion of copper into gold. This diffusion process can result in a room temperature alloying of the gold, degrading the electrical and corrosion resistance characteristics of the contact.

Table 4-13 OSP Surface Finish Advantages and Limitations

Advantages	Limitations
Uniform coplanar surface	May require an aggressive flux
Some OSPs do not deposit on gold	Boards with OSP coating requires careful handling
Reworkable, aqueous process	Not easy to inspect or measure
Controllable, automated process	Exposed copper areas may be vulnerable to corrosion
No process thermal shock during application	Not a suitable contact surface
Preferentially coats copper	Soldering of Class 3 holes with aspect ratios greater than 10:1 are not achieveable
Consistent compliant pin insertion and rework	May have limited in-process hold times
Least expensive of all final finishes	As there is no Nickel barrier, copper dissolution may occur during lead-free solder assembly and/or rework
	OSPs may be damaged by baking prior to soldering

All electrolytically deposited nickel plating **shall** be low-stress and conform to AMS-QQ-N-290, Class 2, except that the thickness **shall** be as specified in Table 4-2.

Reasons for using a nickel underplate include:

- *Diffusion Barrier* – To inhibit diffusion of copper from the basis metal (and of zinc from brass) to the surface of the precious metal plating, or to inhibit interdiffusion between the basis metal and the gold top coat (for example, silver and copper), which might produce a weak alloy or intermetallic compound at the interface.
- *Levelling Layer* – To produce a smoother surface than the basis metal in order to ensure a lower porosity gold top plate (for example, levelling nickel over a rough substrate).
- *Pore Corrosion Inhibitor* – A nickel underplate under the gold top coat will form passive oxides at the base of pores in humid air, provided the environment does not contain significant amounts of acidic pollutants (such as SO_2 or HCI).
- *Tarnish Creepage Inhibitor for Gold* – Non-copper base metals will inhibit creepage of copper tarnish films over the gold—where the tarnish originates from pores and bare copper edges.
- *Load-Bearing Underlayer for Contacting Surfaces* – A hard nickel underplate can serve as a load-bearing foundation for the gold top coat to prevent cracking of hard golds and reduce the wear of the precious metal during sliding of the contacting surfaces. For all these purposes, the nickel underplating should be intact (that is, not cracked) and should have sufficient thickness to achieve the particular function for which it was intended. As a general rule, the minimum thickness should be 1.2 µm [47.2 µin], preferably greater. For some levelling purposes, a far greater thickness may be required.

4.4.9 Tin/Lead Plating Tin/Lead Plating is applied in the subtractive fabrication process to provide a copper etch resist and a solderable coating, when required. Typical thickness sufficient for etch resist on 2 oz. copper is 8.0 µm [315 µin], but it is a fabrication process parameter, not a design requirement. The electrodeposit is generally fused by one of several techniques (hot oil immersion, infrared exposure, exposure to hot vapors or inert liquids). The fusing operation results in the formation of a true alloy on the surface and in the through holes of the printed board. Fusing is required unless the unfused option is selected to maintain flatness. It also promotes improved long-term solderability.

Tin lead plating does not apply to buried PTHs which are internal to the printed board and do not extend to the surface.

Tin-lead plating **shall** meet the composition requirements of ASTM-B-579.

4.4.9.1 Tin Plating Tin Plating is applied in the subtractive fabrication process to provide a copper etch resist.

4.4.10 Solder Coating Solder coating is generally applied by immersing the printed board into molten solder and removing the excess by blowing hot, pressurized air, fluid or vapors over the surface of the printed board in a specially designed machine.

Solder coating does not apply to buried or tented PTHs which are internal to the printed board and do not extend to the surface.

Unless otherwise specified on the master drawing, the solder used for solder coating **shall** be in accordance with J-STD-006. Solder coating thickness may be specified for particular applications. The performance of solder coating is evaluated, not by a mechanical thickness measurement, but by the ability of the printed board to pass solderability testing per J-STD-003 (see Table 4-2). The user has the responsibility to determine if steam aging, prior to solderability testing, is required.

4.4.10.1 Hot Air Solder Leveling (HASL) The current surface finish of long standing is hot air solder leveling (HASL). In this process, the finished circuit board is dipped either vertically or horizontally into a molten solder bath and the excess solder is blown away and leveled with hot air, giving the process its name. The HASL process is the first soldering stress that the printed board experiences. Some material combinations may be prone to delamination or reduced product life cycle due to multiple thermal excursions.

When done properly, the HASL finish process generates visual assurance of solderability. The quality of the product regarding solderability can be confirmed using an approved test method as specified in IPC-J-STD-003. Any evidence of nonwetting or dewetting is immediately apparent as the printed board exits the process.

HASL finish has good solderability and has limited shelf life. It can withstand multiple thermal excursions for double sided assembly. HASL processes, however, are considered to have a degree of difficulty in their control. This, coupled with pad sizes and geometries placing additional challenges on such processes, places the creation of a practical minimum thickness outside the scope of this design standard.

4.4.10.1.1 Tin Lead HASL Although the tin lead surface finish was the main solution for printed boards, one concern with the HASL process is coating thickness uniformity. Often in the process, the solder thickness varies widely from 0.75 - 35 µm [29.5 - 1,378 µin]. Thinner solder finishes, such as <1.2 mm [0.0472 in], reduce shelf life due to formation of intermetallics. As a result, acceptance criteria for the solderability of printed boards should include or be entirely based on functional testing of sample boards or coupons.

The wide variation seen in solder thickness in HASL affects the coplanarity of solder termination on the printed board and hence the coplanarity of SMT components, and uniform solder paste stencil contact.

The increase in the use of thin printed boards (< 0.5 mm [0.0197 in] in thickness) may preclude the use of HASL because of warping of the printed boards during processing.

4.4.10.1.2 Lead-free HASL The lead-free hot air solder leveling process can provide both quality and reliability of the surface finish in providing long shelf life solderability. Like most of lead-free technology, the process for lead-free HASL is maturing as more printed board fabrication facilities implement its use.

The most likely candidates for lead-free HASL are Sn-Cu eutectic (227 °C [441 °F] melting point), or Sn-Ag-Cu eutectic (217 °C [423 °F] melting point). The Sn-Ag-Cu alloy has a lower melting point, but the tin-copper is lowest cost. The Sn-Cu solder pool is easy to manage and recycle, because there are only two constituents. The solder bath is not too aggressive, has low copper dissolution, and is relatively tolerant of common impurities. In contrast, the Sn-Ag-Cu has a much higher copper dissolution rate.

Some proprietary formulas have application for specific uses, such as, carbon paste.

Lead-free HASL finishes are more expensive because tin and silver cost more than lead. The finish is smooth and bright and less domed than eutectic tin/lead HASL (see Figure 4-1).

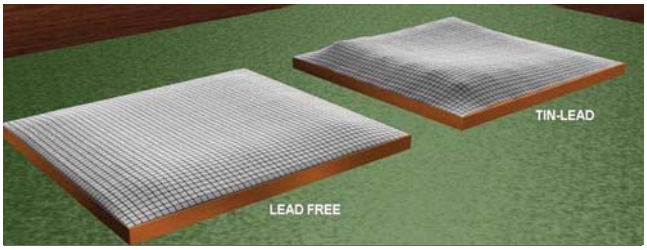


Figure 4-1 HASL Surface Topology Comparison

4.4.11 Other Metallic Coatings for Edge Printed Board Contacts In addition to the coatings cited previously, there are several other options that the designer may want to consider:

- Rhodium – a low resistance contact coating for flush circuits, switches or where a high number of insertions is expected. Expense has precluded its general use.
- Tin/Nickel Alloy – an abrasion resistant coating.
- Palladium/Nickel Alloy – a low resistance contact coating. May be particularly useful for flush circuits.

4.4.12 Metallic Foil/Film

4.4.12.1 Copper Foil There are two types of copper foil available: (W) – wrought (or rolled), and (ED) – electrodeposited. There are also several copper foil grades. For rigid printed boards, electrodeposited copper foil is generally used. For flexible printed boards, wrought foil is generally used. Whichever type is used, the copper foil **shall** conform to the requirements of IPC-4562.

The thickness of starting copper conductors **shall** be as defined in Table 4-14 for the appropriate class of equipment (a reduction in copper thickness of inner layers may be expected after processing). See Appendix A of IPC-4562 for details of foil properties.

Thinner foils are generally used by the printed board manufacturer for ''fine line'' designs to reduce the amount of undercutting of circuit conductors that occurs during the etch operation and meet the requirements of flip chip and chip scale packages. The final after-plating copper thickness is nominally 25.0 - 35.0 µm [984.0 - 1,378 µin] greater than the base foil. For multilayer constructions, the copper thickness should be specified for each layer of the printed board.

If thinner foils are specified and greater after-process copper thicknesses are required, the following should be kept in mind. Using thinner copper foil means that more copper plating is required to reach the final requirement. Thus there will also be more plating in the holes, which means that the vendor should start out with larger hole diameters. This in turn will decrease the annular ring and increase the chance of hole breakout if a larger size land is not used. If larger land sizes cannot be used, the greater copper thickness requirement should be reconsidered or met by other means such as increasing the width of conductors.

4.4.12.2 Copper Film Copper film **shall** be in accordance with Table 4-14.

Table 4-14 Copper Foil/Film Requirements[1]

Copper Type	Class 1-3
Minimum Starting Copper Foil - external	1/8 oz/ft^2 (5 µm) [197 µin]
Minimum Starting[2] Copper Foil - internal	1/4 oz/ft^2 (9 µm) [354 µin]
Starting Copper Film (semi-additive)	5 µm [197 µin]
Final Copper Film (fully-additive)	15-20 µm [591-787 µin]

1. All dimensional values are nominal and derived from weight measurements.
2. 1/8 oz/ft^2 (5 µm) [197 µin] may be used for buried via applications.

It should be noted that the minimum material properties for electrodeposited copper foils given in IPC-4562 are inadequate for many printed board designs and applications. This is particularly the case for IPC-4562/1 (CV-E1), IPC-4562/2 (CV-E2), and IPC-4562/3 (CV-E3). While the vast majority of foil product sold under these slash sheet specifications far exceed the minimum property values, some product sold barely meets these specifications. Thus, it is prudent to obtain actual material properties for critical product.

4.4.12.2.1 Resin Coated Copper Foil Metal foils coated with a resin or composite of resins on one side which are used for the fabrication of printed boards. Coated copper foils when used **shall** be as specified in IPC-4563.

4.4.12.2.1.1 Copper Foil With Single Layers of Resin Copper foil with a single coating of thermosetting resin can be used to improve the surface uniformity, flatness, and chemical resistance of the outer dielectric layers of a printed board.

4.4.11.2.1.2 Copper Foil With Two Layers of Resin Copper foil with two layers of thermosetting resin coated onto one side, such that the layer against the foil is cured to a ''C'' stage to provide a fixed minimum dielectric thickness and the outer layer of resin partially cured to a ''B'' stage to provide an adhesive layer, can be used to provide a very thin, flat, dielectric layer between conductors. One layer of resin with a gradient of cure, with the extent of cure being highest against the copper, can be used to simulate the two layer resin coated product. The dielectric and mechanical characteristics of the resin layer between the conductors will be consistent with those of the cured resin. These dielectric layers, produced without reinforcement, are commonly used to facilitate production of high density micro via layers by laser and plasma ablation techniques.

4.4.12.3 Other Foils/Film When other foils or films (nickel, aluminum, etc.) are used, their characteristics **shall** be specified on the master drawing.

4.4.12.4 Metal Core Substrates Substrates for metal core printed boards **shall** be in accordance with Table 4-15.

Table 4-15 Metal Core Substrates

Material	Specification	Alloy
Aluminum	SAE-AMS-QQ-A-250	As specified on master drawing
Steel	QQ-S-635	As specified on master drawing
Copper	ASTM B-152 / IPC-4562	As specified on master drawing
Copper-Invar-Copper Copper-Moly-Copper	IPC-CF-152	As specified on master drawing
Other	User defined	As specified on master drawing

4.5 Electronic Component Materials The following subsections provide a generic overview of embedded passive device materials, including resistors, capacitors and inductors. For more detailed guidance on the incorporation of embedded components in printed boards, see IPC-2316.

4.5.1 Embedded (Buried) Resistors Incorporating embedded resistance technology is considerably more expensive than standard multilayer printed board fabrication. This is due to the special material copper foil purchasing, additional imaging and etching, and resistance (ohm) value verification.

One of the main printed board attributes that requires embedded resistance technology is the availability of component real estate. Some high-density designs do not permit discrete resistors. In these cases, buried resistors are viable because they are considerably smaller and when buried allow surface mount components or surface circuitry to pass over them.

An annular resistor is a polymer resistor that can be formed in the empty annulus or ''antipad'' which surrounds each via hole which passes through the plane or circuit layer. The annular design allows the resistor to be screened with a minimum number of factors which will affect the final resistor value. The primary use of this type of resistor is to replace pull up or pull down resistors that have an acceptable tolerance of 10% or greater. This resistor may be produced much less expensively than a surface resistor and does not require any room on the printed board surface. The larger resistor tolerance and limited number of resistor types that can be replaced are the primary design limitations.

4.5.2 Embedded (Buried) Capacitors Distributed capacitance is a design feature which places the power (VCC - voltage common carrier) and ground plane directly facing and in close proximity to each other. A separation of the two planes by 0.1 mm [0.0039 in] or less will produce a ''sandwich'' that will provide a low inductance, high capacitance connection to the active devices on the printed board. This fast switching, low current bypass is most useful in high speed digital applications in which the desire to remove surface capacitors or EMI are key considerations. In most designs two power/ground sandwiches are used to replace the existing power and ground plane layers presently in the printed board. In many cases the bypass capacitors 0.1 µF and smaller may be removed from the printed board.

Because of the construction of PC card form factors, minor natural capacitance will be achieved with these types of printed board constructions. Buried discrete technologies are available and can be applied.

4.5.3 Embedded (Buried Inductors) Embedded inductors are typically fabricated by imaging the copper on one or more layers within the printed board in spiral patterns. Inductors are also made by applying a ferromagnetic material above, below or between the spiral conductor patterns.

At the time of publication of this revision to IPC-2221, there were no known commercially available embedded inductance materials.

4.6 Organic Protective Coatings

4.6.1 Solder Mask Coatings Coatings and markings **shall** be compatible with each other and with all other parts and materials used in the printed board, and the printed board assembly process, including the printed board preparation/cleaning required prior to their application. IPC-SM-840 assigns determination of this compatibility to the printed board fabricator and assembler.

The use of solder mask coatings **shall** be in accordance with the requirements of IPC-SM-840. When required, Class 3 printed boards **shall** use IPC-SM-840, Class H or FH solder mask. When Underwriters Laboratories (UL) requirements are imposed, the coatings used **shall** be approved by UL for use by the printed board manufacturer's process.

When solder mask is used as an electrical insulator the dielectric properties of the coating **shall** be sufficient to maintain electrical integrity. There **shall** be no solder mask in areas of the printed board that make contact with the printed board guides.

If the application or design mandates, the minimum and/or maximum solder mask thickness **shall** be specified on the Master Drawing. The minimum thickness specification is required to meet insulation resistance requirements and **shall** be calculated from solder mask material specifications. The maximum thickness specification is required for component assembly process issues, such as solder paste applications.

Solder mask coating adhesion to melting metal surfaces (solder coating, tin/lead plating, etc.) cannot be assured, as printed boards are subjected to temperatures that cause redistribution of the melting metals. When solder mask coating is required over melting metal surfaces, the maximum recommended conductor width, where the coating completely covers the conductor, **shall** be 1.3 mm [0.0512 in].

When conductors of melting metal have a width larger than 1.3 mm [0.0512 in], the design of the conductor **shall** provide a relief through the metal to the base laminate substrate. The relief should be at least 0.625 mm^2 [0.001 in^2] in size and located on a grid no greater than 6.35 mm [0.25 in]. When conductor areas of melting metal are to be left uncovered, the design for all class printed board **shall** provide that the solder mask **shall not** overlap the melting metal by more than 1.0 mm [0.0394 in].

Design requirements may dictate that via holes are protected from access by processing solutions during soldering, cleaning, etc.

The occurrence of solder balls at the assembly level may be related to the surface finish of the solder mask, e.g., matte, glossy, etc.

Additional design guidance and coverage of application processes for solder mask are described in IPC-HDBK-840.

4.6.1.1 Mask Adhesion and Coverage Adhesion between solder mask and laminate and between solder mask and conductor **shall** be complete for the total coverage area. Oxide treatment, double-treated copper, protective chemical treatment, or other adhesion promoter may be used. The use of an adhesion promoter may need user approval.

When circuit designs include unrelieved copper areas greater than 625 mm^2 [0.9688 in^2], the use of a mask adhesion promoter is advisable.

When polymer coatings are required over nonmelting metals, such as copper, the design should provide that conductors not covered by the mask **shall** be protected from oxidation, unless otherwise specified.

4.6.1.2 Mask Clearances and Dams Mask clearances and dams should be in accordance with Table 4-16. Clear areas may have to be provided for assembly fiducials.

Table 4-16 Typical Minimum Solder Mask Clearances and Dams

Mask Type	Clearance	Dam
Liquid Screenable	0.25 mm [0.010 in]	0.25 mm [0.010 in]
Photoimageable Dry Film ≤0.0635 mm [≤0.0025 in]	0.051 mm [0.002 in]	0.127 mm [0.005 in]
Photoimageable Dry Film 0.066 - 0.1 mm [0.0026 - 0.0039 in]	0.051 mm [0.002 in]	0.25 mm [0.010 in]
LPI	0.051 mm [0.002 in]	0.1 mm [0.0039 in]

Data files usually will contain openings equal to the lands. This will allow the printed board fabricators to adjust the clearance to meet his process capabilities while meeting minimum design clearance requirements specified on the master drawing.

Solder mask-to-land relationship **shall** meet the registration requirements stated on the master drawing.

4.6.2 Conformal Coatings When conformal coating is required, it **shall** meet the requirements of IPC-CC-830 and **shall** be specified on the master drawing or master assembly drawing. When UL requirements are imposed, the coatings **shall** be approved by UL for use by the printed board manufacturer. The designer should be cognizant of compatability issues. Conformal coating is an electrical insulation material which conforms to the shape of the circuit printed board and its components. It is applied for the purpose of improving surface dielectric properties and protecting against the effects in a severe environment.

Unless otherwise specified on the drawing/documentation, conformal coating is not required on surfaces or in areas that have no electrical conductors. Conformal coating **shall not** be applied on printed board surfaces that interface with card guides or printed board mounting hardware. Conformal coating need not be present on printed board edges (i.e., the vertical surface) unless otherwise specified on the drawing/documentation.

4.6.2.1 Conformal Coating Types and Thickness Conformal coating may be any one of the types indicated. The thickness of the conformal coating **shall** be in accordance with Table 4-17 for the type specified, when measured on a flat unencumbered surface:

Table 4-17 Conformal Coating Types and Thickness Range

Conformal Coating Type	Thickness Range
Type AR - Acrylic Resin	0.03 - 0.13 mm [0.00118 - 0.00512 in]
Type ER - Epoxy Resin	0.03 - 0.13 mm [0.00118 - 0.00512 in]
Type UR - Urethane Resin	0.03 - 0.13 mm [0.00118 - 0.00512 in]
Type SR - Silicone Resin	0.05 - 0.21 mm [0.00197 - 0.00828 in]
Type XY - Paraxylylene Resin	0.01 - 0.05 mm [0.000394 - 0.00197 in]

There are three primary chemical categories in use for conformal coating materials: silicone elastomers, organics, and parylene. All three types provide various levels of protection from solvents, moisture, corrosion, arcing, and other environmental factors that can jeopardize the circuit's operational performance (see Table 4-18). Many surface mount technologies cannot perform adequately without the use of a conformal coating due to the tight spacing of leads and conductors.

Conformal coatings may be used in greater thicknesses as shock and vibration dampening agents. This type of application brings with it the risk of mechanical stress to glass and ceramic sealed parts during cold temperature excursions, which may require the use of buffer materials. Heavy build up of conformal coatings under DIPs may also result in mechanical stress of soldered connections during thermal cycling, unless precautions are taken.

Conformal coatings, in particular Type UR, are sometimes used to help mitigate tin whiskers as a means of reducing the potential for an electrical short circuit. However, when used for this purpose, it is recommended that a second method of tin whisker mitigation be used since tin whiskers can grow under the coating or may penetrate the coating, depending on its thickness. See IPC/JEDEC-JP002 for additional information.

Table 4-18 Conformal Coating Functionality

Type	Advantages	Disadvantages
Silicone elastomers	Resistant to extreme temperature cycling. Good intermittent solvent splash resistance. Low modulus, easily removed, flexible. Works well over most solder resists and no clean fluxes. Easily reworked.	Low mechanical abrasion resistance. Half the dielectric strength of organics. Can impair solderability after coating.
Organics	High dielectric strength. Excellent mechanical abrasion resistance. Excellent solvent resistance. Excellent moisture resistance.	Can only be used to 125 °C [257 °F]. Difficulty of rework varies. Coefficient of thermal expansion needs to be matched. Required compatibility check with solder resist. Required compatibility check with flux chemistry.
Parylene	Extremely high dielectric strength. Excellent conformability around parts. Excellent penetration of polymer. Excellent moisture/chemical resistance.	High raw material cost. Applied in a vacuum chamber (batch process). Masking seals must be air-tight. Thin film leakage difficult to visually detect.

4.6.3 Tarnish Protective Coatings Protective coatings may be applied to bare copper on the unassembled printed board in order to maintain solderability or appearance for extended periods. These coatings may be dispersed during the soldering operation or may require a separate removal process prior to the soldering operation. The coating requirement **shall** be designated on the master drawing.

4.7 Marking and Legends When specified on the master drawings, printed boards and assemblies **shall** be marked with their full identification by appropriate nonconductive inks, labels, etched characters, or other methods. Marking should be used to provide reference designators, part or serial numbers, revision level, orientation or polarization symbols, bar codes, electrostatic discharge (ESD) status, etc.

The marking locations should be such to avoid placing information under components, in hidden locations after assembly or installation, or on conductive surfaces. Marking should not be placed on surfaces covered with melting metals or opaque coatings. Etched markings may affect electrical characteristics such as capacitance.

Whenever practical, fixed format information such as part number, revision level, layer number, and orientation symbols should be incorporated on the artwork master and be considered during printed board layout. Coupons should include this same information. Variable format information, such as serial numbers, fabricator information, date codes, etc., should be placed in an appropriate area utilizing permanent nonconductive, nonnutrient, and high contrast inks, labels, laser scribes, or other means with sufficient durability to survive assembly and cleaning.

Markings **shall** be of sufficient size, clarity, and location to allow legibility during the processing, inspection, storage, installation, and field repair of a printed board or assembly. Typically, for a silk screening application process, the minimum character height would be 1.5 mm [0.0591 in] with a minimum line width of 0.30 mm [0.012 in]. Typically, for an ink-jet character screening process, the minimum character height would be 1.1 mm [0.045 in] with a minimum line width of 0.15 mm [0.006 in].

Every attempt should be made to provide enough space for the marking and it is recommended that space be reserved when component placement is determined per 8.1. Avoid the use of marking inks in close proximity to surfaces that need to be solderable as the resin systems used in these inks may impair solderability.

Liquid screened markings require clearances that are typically 0.4 - 0.5 mm [0.016 - 0.020 in] from solderable surfaces. Ink jet screened markings require clearances that are typically 0.127 - 0.20 mm [0.005 - 0.008 in] from solderable surfaces. Caution should be used when calling for liquid screened markings as their legibility is affected by high surface irregularities.

ESD or Underwriters Laboratories requirements may include special marking considerations which **shall** become a part of the master drawing.

The marking(s) specified in J-STD-609 and/or J-STD-075 **shall** be provided, as applicable.

4.7.1 ESD Considerations Circuit card assemblies which contain electrostatic discharge sensitive devices **shall** be marked in accordance with the ESD Control Program Plan requirements of ANSI/ESD-S20.20 using appropriate ESD symbols, etc in accordance with a recognized marking standard such as RS-471, etc.

The marking **shall** be etched or applied by the use of a permanent ink or a permanent label which will withstand assembly processing and remain visible just prior to removal of the assembly for maintenance. Additional markings, if required, **shall** be specified on the assembly drawing.

5 MECHANICAL/PHYSICAL PROPERTIES

5.1 Fabrication Considerations Table 5-1 lists some fabrication assumptions and considerations.

5.1.1 Bare Printed Board Fabrication Due to the equipment involved in printed board fabrication, there are certain limits that should be taken into account in order to maximize manufacturability and, thereby, minimize costs. In addition, human factors such as strength and reach and control, preclude the use of full-size sheets in most printed board manufacturing facilities.

5.2 Product/Printed Board Configuration The physical parameters of the printed board should be consistent with the mechanical requirements of the electronic system. Tolerances, as defined in Section 3 and Section 5, should be optimized to provide the best fit between the printed board size, shape, and thickness and mechanical hardware used to mount the product.

Table 5-1 Fabrication Assumptions and Considerations

Fabrication Design Assumptions	Impacts
Maximization of Land to Hole Size Difference (See 9.1.1 of IPC-2221)	*Benefit* – Provides sufficient land area to prevent breakout, i.e., hole intersecting edge of land (insufficient annular ring) *Drawback* – Large lands may interfere with minimum spacing
Filleting (Teardrop) at Connection of Conductor with Land	*Benefit* – Provides additional area to prevent breakout *Benefit* – May improve reliability by preventing cracking at land to conductor boundary in vibration or thermal cycling *Drawback* – May interfere with minimum space requirements
Printed Board Thickness: 0.8 mm - 2.4 mm [0.031 in - 0.0945 in] typical (over copper)	*Drawback* – Thinner printed boards tend to bow & require extra handling with through-hole technology components *Drawback* – Some through-hole components may not have long enough leads for thicker printed boards *Drawback* – Thicker printed boards with higher layer counts have lower yield because of the layer registration
Minimization of Aspect Ratio (See 9.2.2.1 of IPC-2222)	*Benefit* – Smaller ratios result in more uniform plating in hole, easier cleaning of holes and less drill wander *Benefit* – Larger holes are less susceptible to barrel cracking
Symmetrical Layer Stack-up	*Comments* – Top half should be a mirror image of bottom half to achieve a balanced construction. This includes copper thickness, dielectric thickness, and material *Drawback* – Asymmetrical printed boards tend to warp
Printed Board Size	*Comments* – Panel utilization determines cost. Assembly palletization requirements should also be taken into consideration (small or odd-shaped printed boards may require an assembly pallet)
Conductor Spacing	*Drawback* – Etchant fluid does not circulate efficiently in narrow spaces resulting in incomplete metal removal *Comments* – Plated layers generally require more spacing than print and etch layers. Heavier copper requires proportionally more spacing
Circuit Feature (Conductor Width)	*Comments* – Long, narrow width conductors are more susceptible to breakage and damage during etching and subsequent handling. The normal tolerance associated with etching the circuit becomes a greater percentage of the finished width, making controlled impedance to a specified tolerance more difficult as line widths narrow. Heavier copper requires proportionally wider conductors

Substrates for use in PC card form factors **shall** fit one of the three types as shown in Table 5-2.

Table 5-2 PC Card Form Factor Substrate Dimensions

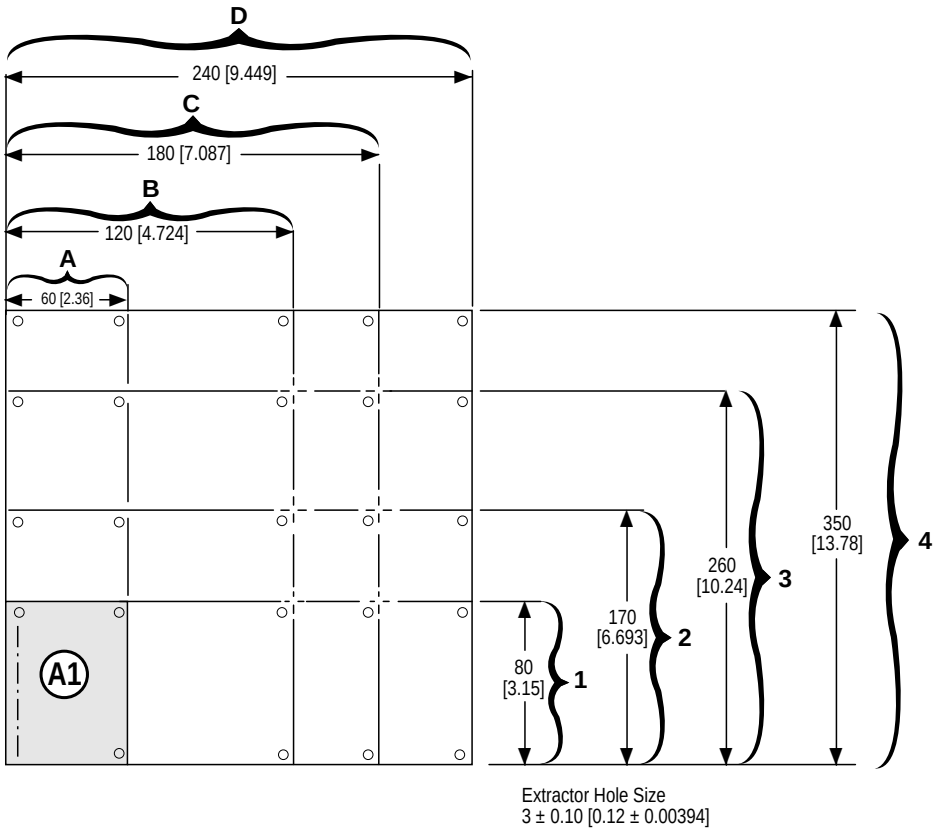
Form Factor Type	Length (±20 µm [787 µin])	Width (±10 µm [394 µin])	Interconnect Area[1] (±5 µm [197 µin])	Substrate Area[1] (±10 µm [394 µin])
Type I	85.6 mm [3.37 in]	54.0 mm [2.13 in]	4.19 mm [0.165 in]	4.19 mm [0.165 in]
Type II	85.6 mm [3.37 in]	54.0 mm [2.13 in]	4.19 mm [0.165 in]	6.35 mm [0.25 in] maximum
Type III	85.6 mm [3.37 in]	54.0 mm [2.13 in]	4.19 mm [0.165 in]	10.0 mm [0.394 in]

Note 1. Interconnect area and substrate area thickness are specified from the substrate center line to either the top or bottom surface.

5.2.1 Printed Board Type The decision for printed board type (single-sided, double-sided, multilayer, metal core, etc.) should be made prior to starting layout procedures and be based on assembly performance requirements, heat dissipation, mechanical rigidity requirements, electrical performance (shielding, impedance matching, etc.) and anticipated circuit density (see 3.6.2).

5.2.2 Printed Board Size Printed boards should be of uniform size whenever possible to facilitate bare printed board and assembly test fixturing, and minimize the number of fixtures required. An example of printed board standardization is shown in Figure 5-1. The printed board size should also be compatible with standard manufacturing panel sizes in order to achieve lowest cost and maximum number of printed boards per panel. This will also help facilitate bare printed board testing (see IPC-D-322).

Board No.	Printed Board Size ± 0.4 [0.016]
A1	60 x 80 [2.36 x 3.15]
A2	60 x 170 [2.36 x 6.693]
A3	60 x 260 [2.36 x 10.24]
A4	60 x 350 [2.36 x 13.78]
B1	120 x 80 [4.724 x 3.15]
B2	120 x 170 [4.724 x 6.693]
B3	120 x 260 [4.724 x 10.24]
B4	120 x 350 [4.724 x 13.78]
C1	180 x 80 [7.087 x 3.15]
C2	180 x 170 [7.087 x 6.693]
C3	180 x 260 [7.087 x10.24]
C4	180 x 350 [7.087 x 13.78]
D1	240 x 80 [9.449 x 3.15]
D2	240 x 170 [9.449 x 6.693]
D3	240 x 260 [9.449 x 10.24]
D4	240 x 350 [9.449 x 13.78] [Not recommended for Best Panel Utilization]



IPC-2221b-5-01

Figure 5-1 Example of Printed Board Size Standardization, mm [in]

5.2.3 Printed Board Geometries (Size and Shape)

5.2.3.1 Material Size The largest size for a printed board fabrication panel is a function of the economic use of sheet laminate common to the marketplace (see IPC-D-322).

The use of a panel size smaller than the largest sub-multiple of the full-size sheet is recommended. One common panel size is 460 x 610 mm [18.110 x 24.02 in]. Secondary standard panel sizes should be sub-multiples of the full-size sheet.

It is recommended that the designer be aware of the board manufacturer's process panel size in order to optimize the printed board-to-panel yield, and cost relationships. The use of the larger panel sizes is typically the most effective from a labor cost per unit area of end-product printed board processed. However, the use of large panels may pose difficulties in achieving fine lines and feature positional accuracy due to an increase in base material movement.

In taking into account the design of a PC card form factor printed board, it has been demonstrated that it is more economical to process thin printed boards with smaller panel sizes due to smaller circuit design features.

5.2.4 Bow and Twist Proper printed board design, with respect to balanced circuitry construction distribution and component placement, is important to minimize the degree of bow and twist of the printed board. Additionally, the cross-sectional layout, which includes core thicknesses, dielectric thicknesses, inner layer planes, and individual copper layer thicknesses, should be kept as symmetrical as possible about the center of the printed board.

Unless otherwise specified on the master drawing, the maximum bow and twist **shall** be 0.75% for printed board that use surface mount components and 1.5% for all other printed board technologies. Panels that contain multiple printed boards to be assembled on the panel and later separated **shall** also meet these bow and twist requirements.

If symmetrical construction and tighter tolerances are not sufficient to meet critical assembly or performance requirements, stiffeners or other support hardware may be necessary.

Values are measured per IPC-TM-650, Method 2.4.22.

5.2.4.1 Bow and Twist for PC Card Form Factor Printed Boards Assembly handling fixtures are usually used for PC card form factor printed boards. Solid copper rails, as part of the circuit design, are necessary for providing rigidity to the panel, but have ''memory'' and can affect bow and twist of the panel. However, the effect of bow and twist is minimized for these thin printed boards. Bow and twist may be decreased by using solid copper on external frame areas and copper dots on internal frame areas. Bow and twist can affect the final assembly by torquing devices and placing strain on the connections, thus it should be accounted for in design considerations. Position of ground and power planes should be symmetrically located to help prevent warpage during assembly or use. Partial ground and power areas should be designed for symmetric construction as well.

5.2.5 Structural Strength The wide variety of materials and resins available places a serious analytical responsibility on the designer when structural properties are important. The structural properties of laminates are influenced by environmental conditions that vary with the lay-up and composition of the base materials. Physical and electrical properties vary widely over temperature and loading ranges. The ultimate properties of printed board materials are of marginal use to the designer trying to employ the printed board as a structural member. The concern to meet electrical performance requirements, which are impacted by deformation and elongation of the printed board, should consider lower values of ultimate material strength than those listed in the technical literature for determining structural needs.

5.2.6 Composite (Constraining-Core) Printed Boards When structural, thermal, or electrical requirements dictate the use of a constraining-core printed board, the physical performance properties **shall** be evaluated using similar conformance specimen to those designed for standard rigid printed board. The coupons for the constraining-core board **shall** include the core material.

Whether for thermal or constraining characteristics, the printed board configuration may be symmetrical or asymmetrical. There are some advantages in an asymmetrical design in that the electrical properties or functions are separated from the mechanical or heat dissipation functions (see Figure 5-2).

The drawback of the asymmetrical design is that due to the differences of the coefficient of thermal expansion of the printed board and the core material, the completed printed board may distort during assembly soldering/reflow operations or while in system use due to temperature change. Some compensation can be achieved by having an additional copper plane added to the back of the interconnection product. The extra copper plane increases the expansion coefficient slightly, but a positive effect is that it enhances thermal conductivity.

A more desirable construction may be that of the symmetrical cored printed board (see Figure 5-3A and 5-3B). Figure 5-3A shows the two restraining cores laminated into the multilayer printed board where they serve as part of the electrical function, in this case, power and ground. The center core construction as shown in Figure 5-3B has a single thicker restraining core which usually has only the thermal plane and restraining function. To achieve restraint in the usable range, the combined thickness of the copper-Invar-copper in the multilayer printed board should be approximately 25% of the printed board thickness. The two-restraining-core printed board is more often used because the core layers may be imaged, etched and connected to the PTH; the thicker center core needs to be machined. Better thermal cycle survival is exhibited by the two-restraining-core printed board.

A special constraining-core printed board may be made by bonding a multilayer printed board to each side of a thick constraining metal core after the printed boards have been completed. A more complex variation may also be fabricated wherein the constraining metal core is laminated between two partially completed multilayer boards. The composite printed board is then sequentially drilled, plated and etched to form plated-through hole connections between the two printed boards. Coupons should be provided to test the integrity of the composite structure.

Metal core printed boards add significantly to the thermal mass of the assembly. This may force the preheating and soldering process to be operated at abnormally high limits. These designs should be thoroughly evaluated under assembly conditions prior to manufacture. Laminate ruptures and discoloration and grainy or textured solder are typical effects that have been observed.

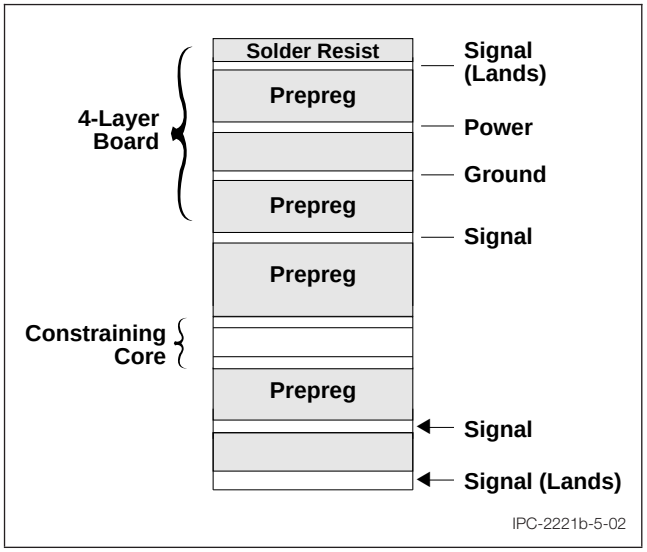


Figure 5-2 Typical Asymmetrical Constraining-Core Configuration

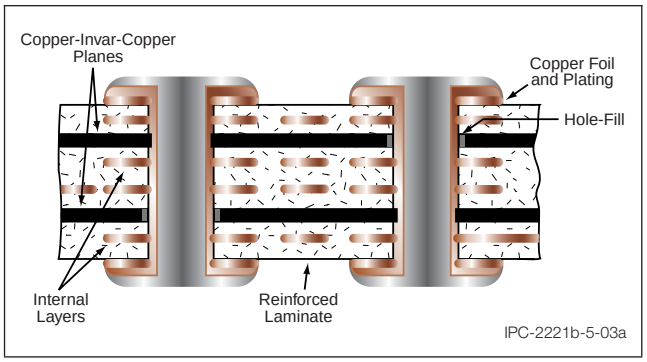


Figure 5-3A Multilayer Metal Core Printed Board with Two Symmetrical Copper-Invar-Copper Constraining Cores (when the Copper-Invar-Copper planes are connected to the plated-through hole, use thermal relief per Figure 9-4)

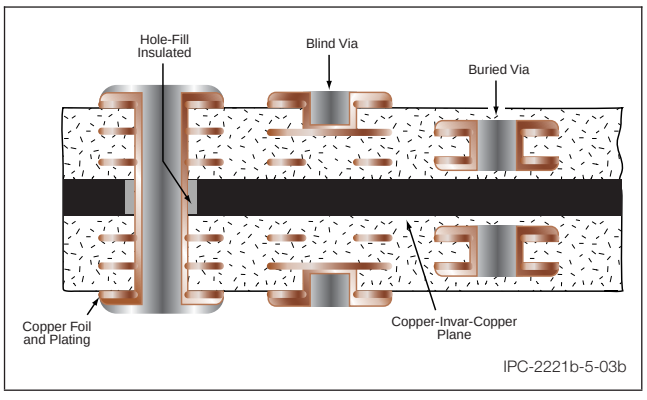


Figure 5-3B Symmetrical Constraining Core Printed Board with a Copper-Invar-Copper Center Core

5.2.7 Vibration Design The design of printed boards that will be subjected to vibration while in service requires that special consideration be given to the printed board prior to printed board layout. The effect on the printed board assembly caused by the vibration can seriously reduce the reliability of the assembly. The interrelationship between the unit, printed board assemblies, their mounting and the environmental

conditions make necessary the need for a vibration analysis of the complete system very early in the design. The effect from vibration on any item within a unit can make the vibration analysis very complex.

Vibration analysis should be done on each piece of electronic hardware which contains printed board assemblies. The complexity of the analysis should depend on the vibration level to which the hardware will be subjected in service. The design of the printed boards will depend on the level of vibration transmitted to the printed board. Particular attention should be given to printed boards subjected to random vibration.

The following criteria should be used as guidelines for determining if the level of vibration to which the printed boards will be subjected is a level which would require complex vibration analysis of the printed board:

- The random spectral density is at, or above, $0.1G^2$/Hz in the frequency range of 80 to 500 hertz or an unsupported printed board distance of greater than 76.2 mm [3.0 in].
- A sinusoidal vibration level at, or above, 3 Gs at a frequency of 80 to 500 Hz.
- The printed board assembly will be subjected to Reliability Development Growth Testing (RDGT) at a spectral density at, or above, 0.07 G^2/Hz for more than 100 hours in conjunction with temperature cycling.

The following guidelines should be observed during the design of boards to eliminate vibration induced failures of the printed board assemblies:

- The printed board deflection, from vibration, should be kept below 80 µm [3,150 µin] per mm of printed board length (or width) to avoid lead failure on multiple lead devices.
- Positive support of all components with a weight of more than 5.0 gm per lead should be considered when the printed board will be subjected to vibration (see 5.3.2).
- Printed board stiffeners and/or metal cores should be considered to reduce the printed board deflection.
- Cushioned mounting of relays should be considered for their usage in high level vibration environments.
- Vibration isolators should be considered for mounting of units whenever practical.
- The mounting height of freestanding components should be kept to a minimum.
- Nonaxial leaded components should be side-mounted.

Because of the interrelationship of the many components that make up a system, the use of the above guidelines does not ensure the success of a unit subjected to a vibration test. A vibration test of a unit is the only way to ensure that a unit will be reliable in service.

5.3 Assembly Requirements

5.3.1 Mechanical Hardware Attachment The printed board **shall** be designed in such a manner that mechanical hardware can be easily attached, either prior to the main component mounting effort, or subsequently. Sufficient physical and electrical clearance should be provided for all mechanical hardware that requires electrical isolation. In general, mounting hardware should protrude no more than 6.4 mm [0.252 in] below the printed board surface to allow sufficient clearances for assembly equipment and solder nozzles.

5.3.2 Part Support All parts weighing 5.0 gm, or more, per lead **shall** be supported by specified means (see 8.1.9), which will help ensure that their soldered joints and leads are not relied upon for mechanical strength.

The reliability of printed boards that will be subject to shock and vibration in service require consideration of the following criteria:

- The worst-case levels of shock and vibration environment for the entire structure in which the printed board assembly resides, and the ultimate level of this environment that is actually transmitted to the components on the printed board. (Particular attention should be given to equipment that will be subjected to random vibration.)
- The method of mounting the printed board in the equipment to reduce the effects of the shock and vibration environment, specifically the number of printed board mounting supports, their interval, and their complexity.
- The attention given to the mechanical design of the printed board, specifically its size, shape, type of material, material thickness, and the degree of resistance to bowing and flexing that the design provides.
- The shape, mass and location of the components mounted on the printed board.
- The component lead wire stress relief design as provided by its package, lead spacing, lead bending, or a combination of these, plus the addition of restraining devices.

• The attention paid to workmanship during printed board assembly, so as to ensure that component leads are properly bent, not nicked, and that the components are installed in a manner that tends to minimize component movement.

• Conformal coating may also be used to reduce the effect of shock and vibration on the printed board assembly (see 4.5.2).

Where circuit design permits, the selection of components to be mounted on printed boards subjected to severe shock and vibration should favor the use of components that are lightweight, have low profiles and inherent strain-relief provisions. Where discrete components are to be used, preference should be given to surface mount and/or axially-leaded types that present a relatively low profile that can be mounted and easily clamped or bonded in intimate contact with the printed board surface.

The use of irregularly-shaped components, especially those having a large mass and a high center of gravity, should be avoided where practical. If their use cannot be avoided, they should be located toward the outer perimeter of the board, or where hardware or mounting reduces flexing. Depending on the severity of this problem, the use of mechanical clamping, adhesive bonding, or embedding may be required.

5.3.3 Assembly and Test Consideration, similar to that mentioned above for printed board fabrication, **shall** be given to printed board assembly and test equipment utilization in order to improve manufacturing yields and to minimize end-product costs. Table 5-3 provides limits associated with the use of typical printed board assembly equipment.

Table 5-3 Typical Assembly Equipment Limits

Operation	Panel Size
Component Placement	450 mm x 450 mm [17.72 in x 17.72 in]
Wave Solder	400 mm x Open [15.75 in x Open]
In-Circuit Test*	400 mm x 400 mm [15.75 in x 15.75 in]
Reflow	450 mm x 610 mm [17.72 in x 24.02 in]
Cleaning	450 mm x 450 mm [17.72 in x 17.72 in]
Stencil	450 mm x 450 mm [17.72 in x 17.72 in]

Note 1. Maximum size also determined by the number of electrical nodes to be tested,

5.3.4 Tooling Rails for PC Card Form Factor Printed Boards Expendable tooling rails for assembly processes should be solid copper to add stability to the printed board or array. Maximize copper fill to add dimensional stability to the printed board.

5.4 Dimensioning Systems

5.4.1 Dimensions and Tolerances Historically, printed board designs have used bilateral tolerances for size and position, which is acceptable. However, the use of Geometric Dimensioning and Tolerancing (GDAT) per IPC-2615, has many advantages over bilateral tolerancing:

• It allows at least 57% more tolerance area with true positioning than with bilateral tolerancing (see Figure 5-4).

• It provides for maximum producibility while assuring the mechanical function of the printed board. It allows ‘‘bonus’’ or extra tolerances when the maximum/least material concept is used.

• It ensures that design requirements, as they relate to fit and function, are specifically stated and carried out. This is particularly significant when automated assembly techniques are to be used.

• It ensures interchangeability of mating parts.

• It provides uniformity and convenience in drawing delineation and interpretation, thus reducing controversy and guesswork.

For these reasons, the use of geometric dimensioning and tolerancing is encouraged.

5.4.2 Component and Feature Location Component and feature locations may be defined by the use of a grid system or the use of a gridless system. It is up to the printed board designer to predetermine what the manufacturing and testing requirements of a printed board are and then to choose which grid to use to place parts and when to use a gridless system to layout a printed board.

5.4.2.1 Grid Systems Grid systems are described in IPC-1902/IEC 60097. Grid systems are used to locate components, PTHs, conductor patterns, and other features of the printed board and its assembly so they need not be individually dimensioned. When printed board features are required to be off grid, they may be individually dimensioned and toleranced on the master drawing.

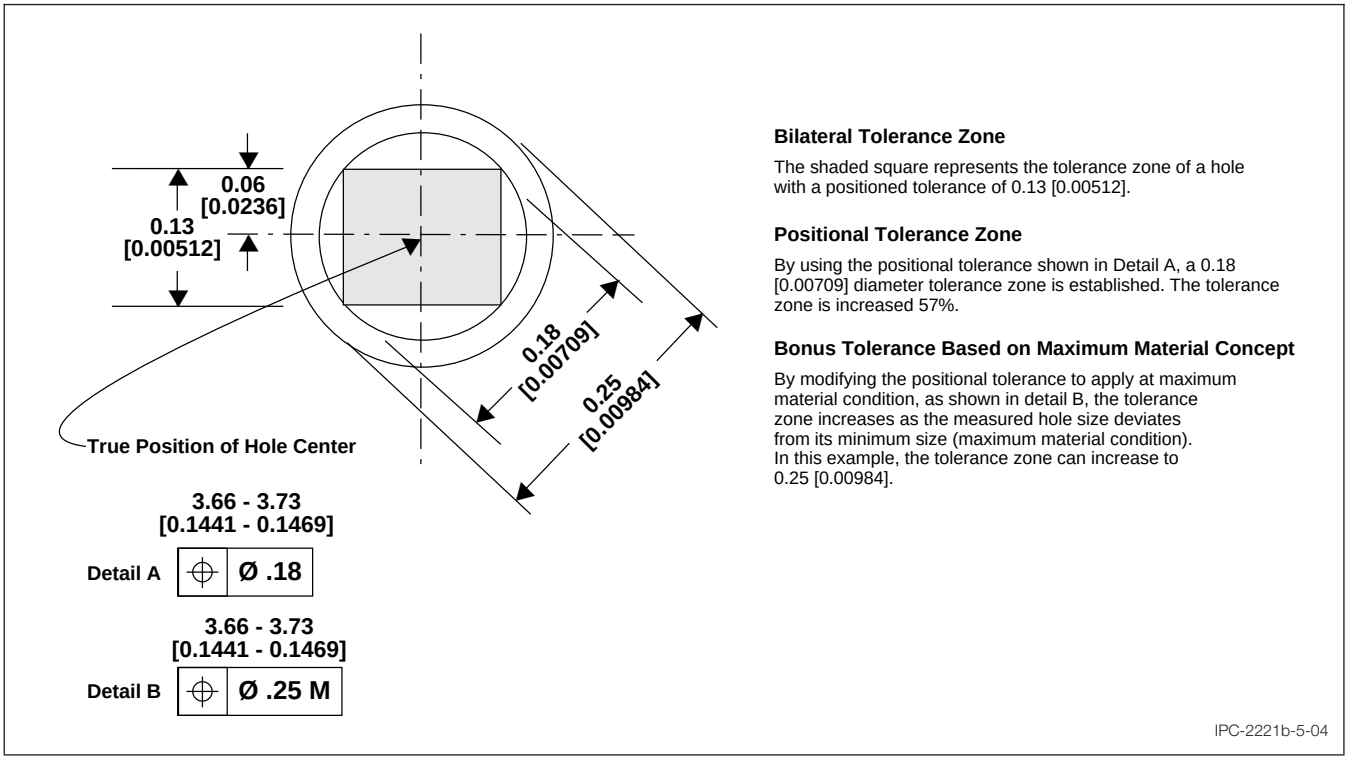


Figure 5-4 Advantages of Positional Tolerance Over Bilateral Tolerance, mm [in]

Grid systems are always basic and have no tolerance, and therefore all features located on a grid **shall** be toleranced on the master drawing. Grid systems **shall** be located with respect to a minimum of two datums. The selected grid increment or the use of electronic media **shall** be specified on the master drawing. Either the selected grid or the electronic media establishes the component terminal location for through-hole components or the component center location for surface mount components.

There are occasions when a particular grid is often used: for example, for a pre-determined test fixture that uses test points etched on a surface of a printed board. Typical grid increments are multiples of 0.5 mm [0.020 in] for through-hole components or 50 µm [1,967 µin] for surface mount components.

5.4.2.2 Gridless Systems Electronic media generated by CAD systems use autorouters that are considered ''gridless.'' Although this is a misnomer - a gridless router may actually use a very small grid (i.e., 2.54 µm [100 µin]), the practicality is that the CAD software is used to ensure the conductors are routed per set design rules and the data files from the CAD system allow a fabrication vendor to produce a printed board to meet the rules described by those files and the accompanying drawing notes and details. Designs where a gridless router is used may preclude some traditional test methodologies (i.e., bed-of-nails tester). With today's large variety of package sizes for SMT parts and having to put more parts on smaller printed boards, having to use a specific grid is no longer practical. Automatic placement equipment uses electronic data to determine where to place components. The use of electronic media precludes the necessity for dimensioning components, PTHs, conductor patterns and other features of the printed board.

5.4.3 Datum Features Datums are theoretically exact points, axes, and planes. These elements exist within a framework of three mutually perpendicular intersecting planes known as the datum reference frame. Datum features are chosen to position the printed board in relation to the datum reference frame (see Figure 5-5).

There are some cases where a single datum reference is sufficient, however in most cases all three datums are referenced.

Typically the secondary side of the printed board is identified with the primary datum. The other two datum planes or axes are usually identified using adjacent unsupported holes. Alternatively, etched features or the printed board edges may be used.

The choice of features to be used for datums depends on what design elements are intended to be controlled. Printed board edge datums may be used when they represent a major function of the printed board. Datum features **shall** be identified on the master drawing by means of symbols per IPC-2615. Datum features should be functional features of the printed board

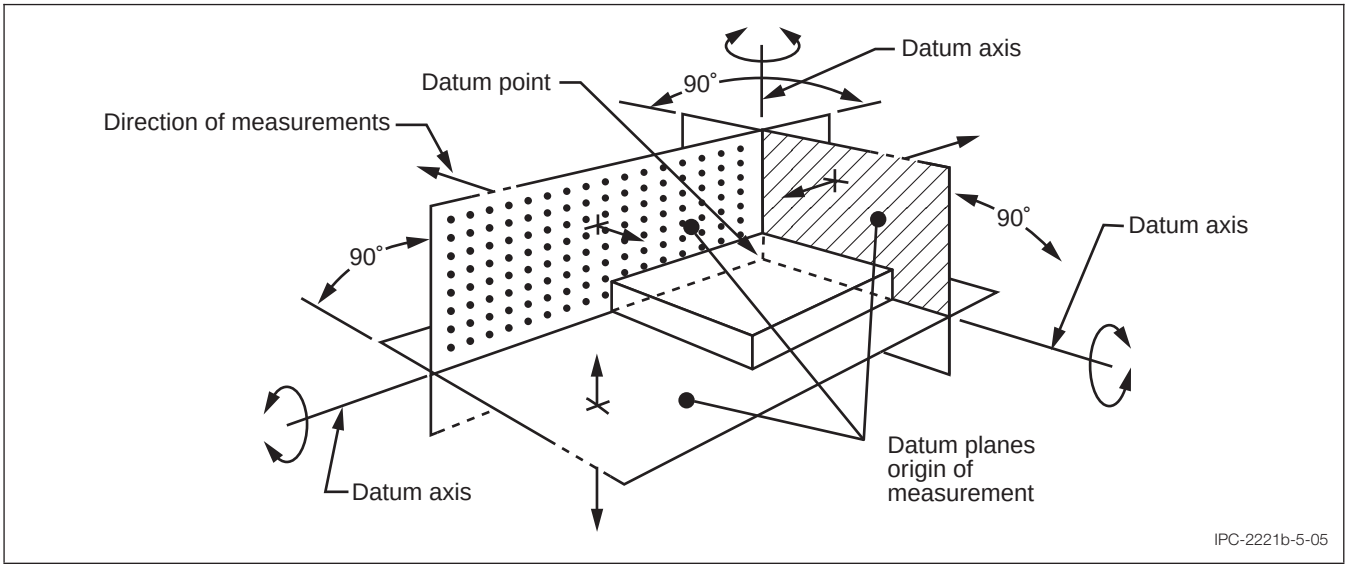


Figure 5-5 Datum Reference Frame

and should relate to mating parts such as mounting holes. All datum features should be located within the printed board profile. The second datum feature typically becomes the coordinate zero for measurements. It is preferred that this be located within the printed board.

Note: When printed boards are very dense with circuitry or are very small, there may be no room to have the tooling features located on the printed board. In these instances the zero-zero origin is off the printed board and a secondary location is identified for visual orientation. Often times marking ink provides this function.

With the use of electronic data, all holes, conductors and features are viable elements to allow for fabrication and inspection. However, for any feature not dimensioned digitally within the database, it is necessary to delineate dimensions to the design not in electronic format. Some of these characteristics are as follows:

a) *PTH Patterns* – The plated through-hole pattern (see Figure 5-6) is generally accomplished during the first drilling operation. It can be dimensioned as a basic dimension with each hole toleranced to a basic grid location. The hole location tolerance is specified either in the hole list or is best defined by a note on the master drawing.

b) *Unsupported Through-Hole Patterns* – Nonplated through-hole patterns, especially tooling and mounting holes (see Figure 5-7), are generally drilled during the primary drilling operation. They should be explicitly dimensioned and toleranced, even if they occur on grid, when they are critical to printed boards mounting functionality or the tooling features. Two of these may be identified as datum features for the secondary and tertiary datums.

   Tooling holes are features of the printed board or the printed board panel. They are features in the form of a hole that may also be used by printed board manufacturers to optimize the tolerance conditions between pins on the tooling fixture and the holes or slots in the printed board. Fabrication tooling holes are usually determined by the printed board manufacturer, although it is a good plan to interface with the assembler since they also use tooling features as part of the assembly panel.

c) *Conductor Patterns* – The conductor pattern does not need a separate datum reference, provided a minimum annular ring is specified. Minimum annular ring is a common way to tolerance the conductor pattern location with respect to the plated through-hole pattern. For some designs, particularly where automated assembly of fine pitch and/or high lead count devices is used, additional accuracy may be required. In these cases, a feature location tolerance may be required and **shall** appear on the master drawing. Alternately, fiducials restricted to component features may be required. These would be toleranced with respect to the assembly tooling requirements (see Figure 5-8).

   The fiducial size, shape and quantity may depend on the type of equipment used in the assembly process and the lead pitch and count. Figure 5-11 shows the Surface Mount Equipment Manufacturers Association (SMEMA) recommended fiducial design.

   Another method to locate and tolerance conductor patterns is by dimensioning to the centerline of a conductor. A critical area such as edge printed board contacts could be dimensioned as in Figure 5-13. Tolerances used for edge contacts and keying lots **shall** be such that the keying slot does not cut into or damage the contact finger. Dimensioning to the edge of a conductor is not recommended.

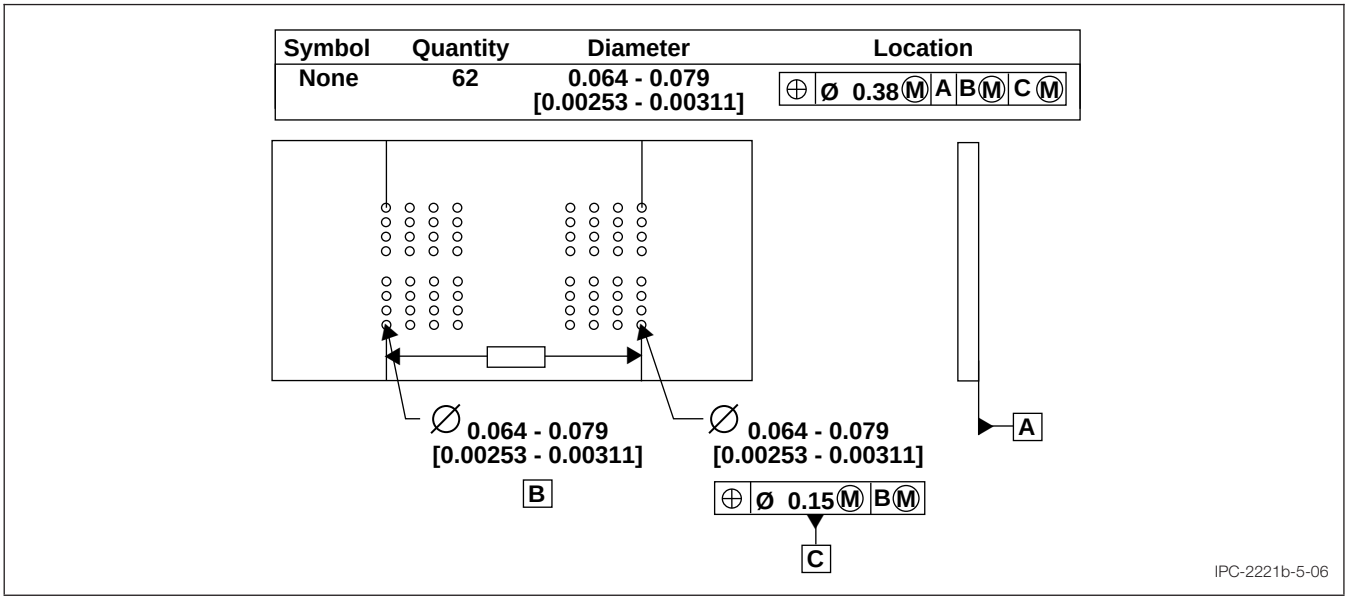


Figure 5-6 Example of Location of a Pattern of PTHs, mm [in]

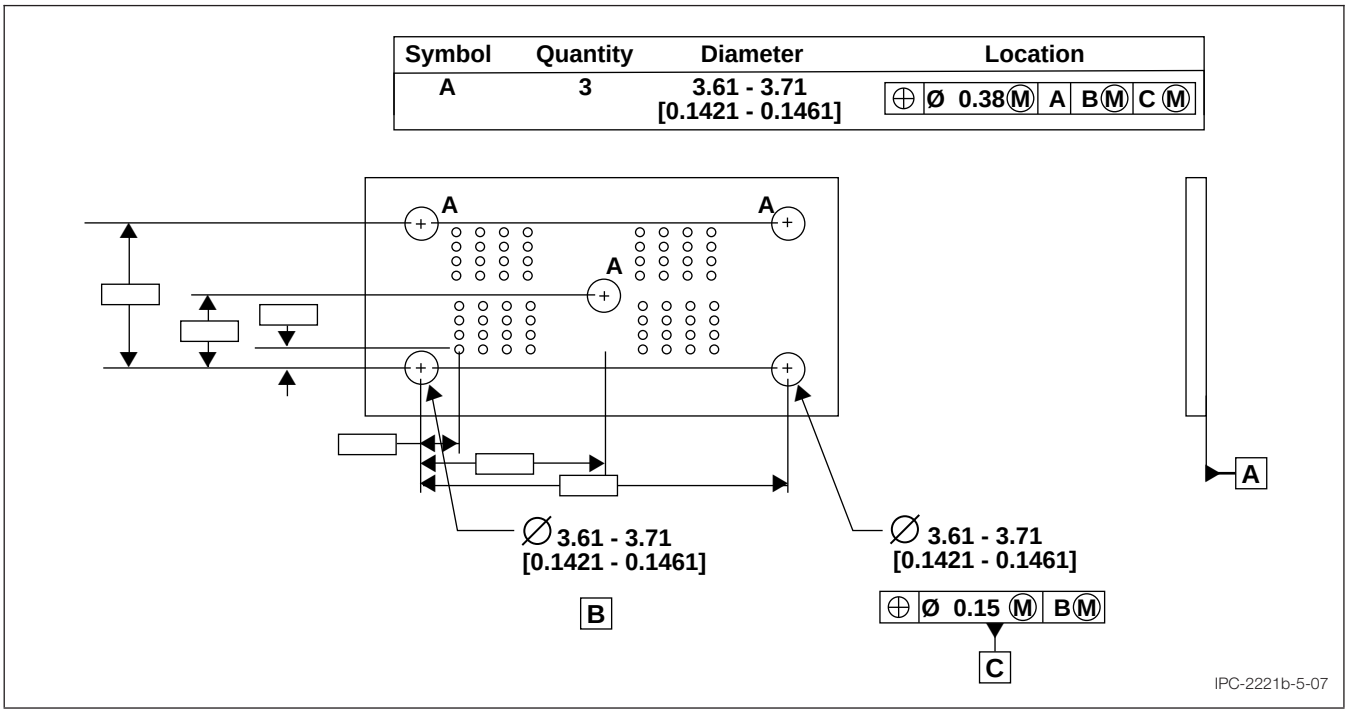


Figure 5-7 Example of a Pattern of Tooling/Mounting Holes, mm [in]

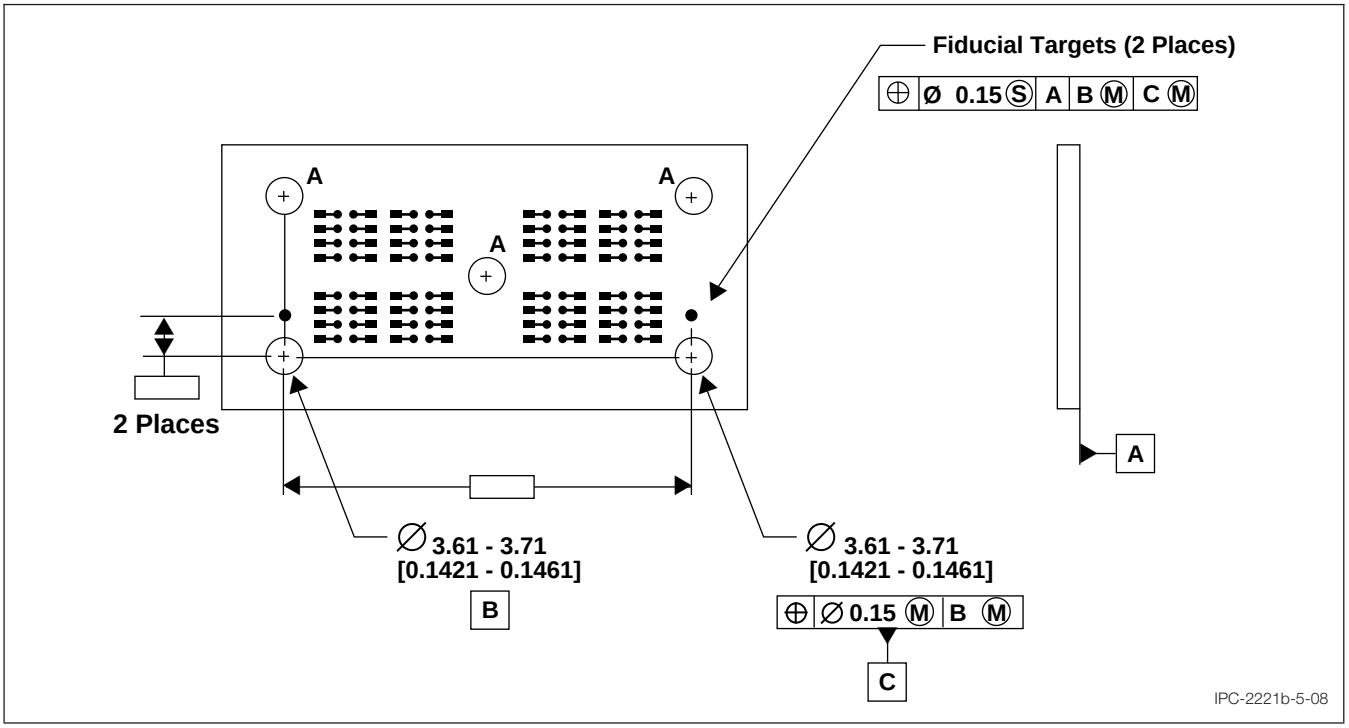


Figure 5-8 Example of Location of a Conductor Pattern Using Fiducials, mm [in]

Figure 5-10 shows how Figure 5-6 through 5-9 can be assembled into one drawing.

d) *Printed Board Profile* – The printed board profile, including cutouts and notches (see Figures 5-9 and 5-12), requires a minimum of one datum reference. The use of three datum references and maximum material condition modifiers, as shown in Figure 5-9, maximizes allowable tolerances and allows the use of hard tool gauging, which is particularly useful in high volume production situations.

e) *Solder Mask Coatings* – The solder mask coating pattern may be located by specifying a minimum land clearance or targets may be provided which serve the same function as fiducials for conductive patterns. A minimum land clearance serves the same purpose as a minimum annular ring requirement in that it tolerances the solder mask pattern location with respect to the conductor pattern.

5.4.3.1 Datum Features for Palletization Palletization or assembly arrays are a common process for facilitating test and assembly of printed boards. A datum system is required for the pallet or array as well as each individual printed board. It is important to relate the individual printed board datum system to the pallet or array datum system (see Figure 5-12).

5.5 Printed Board Thickness Tolerance The overall thickness and tolerance **shall** be specified on the drawing. See IPC-2222 for more information on printed board thickness tolerance.

5.6 Panelization At the fabrication level, panelization is the process of placing one or more printed board images on the same piece of material. This may also include the addition of test coupons to a single printed board on a panel. Multiple printed board imaging provides a cost advantage for maximizing the utilization of the materials. Most of the fabrication processes and costs are realized at the panel level before the individual printed boards are excised. By fabricating two or more printed boards on a panel, the fabrication costs prior to routing can be amortized to each printed board in the panel. It might not always be a good fit for complex printed boards. Great care should be taken in deciding to panelize a printed board.

5.7 Palletization Palletization facilitates the assembly of one or more printed boards as if they were a single large printed board. This allows for less material handling and provides panel edges that can protect the printed boards through assembly and test. The pallets may not need to be broken apart until ready to go into the next higher assembly level. Palletization works well for small printed boards, or printed boards with unique edges. For example, breakaway edges can turn a round printed board into a square shape for ease of handling through assembly equipment, the edges being broken, cut, or nibbled off, after assembly to reveal the finished round shape.

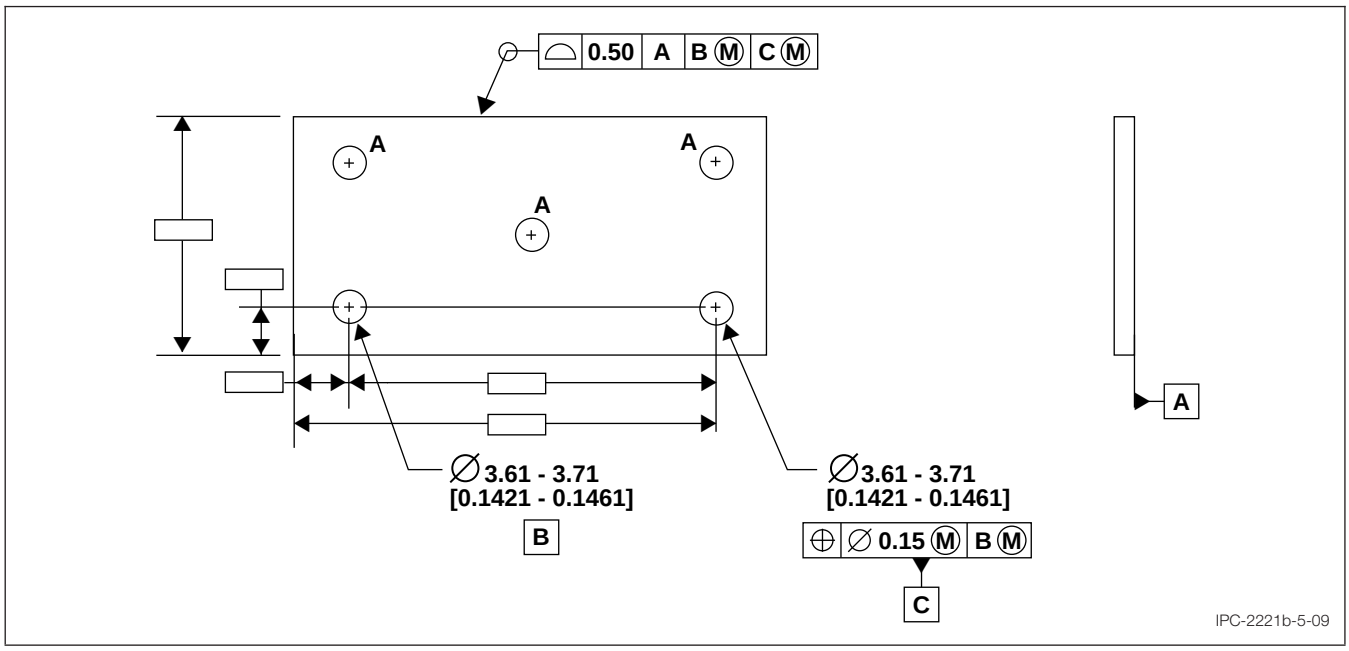


Figure 5-9 Example of Printed Board Profile Location and Tolerance, mm [in]

Symbol	Quantity	Diameter	Location
A	3	3.61 - 3.71 [0.1421 - 0.1461]	Ø 0.38 M A B M C M
None	64	3.64 - 3.79 [0.1433 - 0.1492]	Ø 0.15 M A B M C M

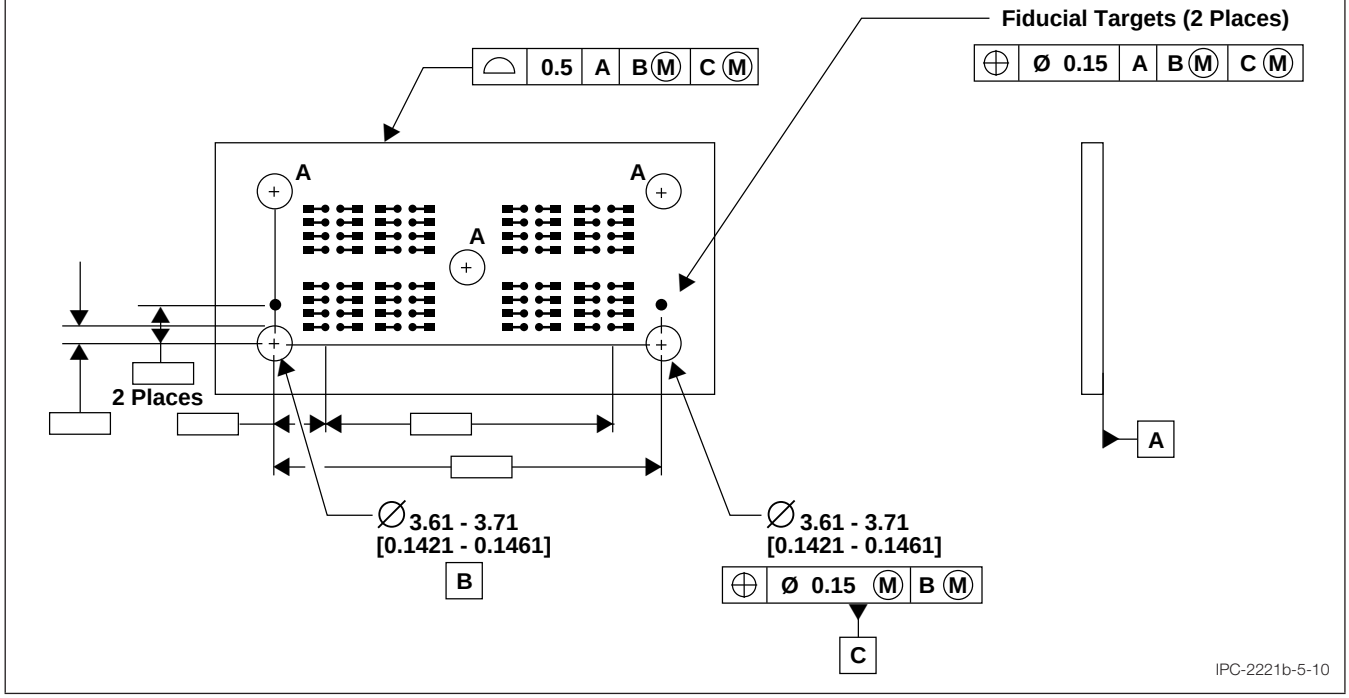


Figure 5-10 Example of a Printed Board Drawing Utilizing Geometric Dimensioning and Tolerancing, mm [in]

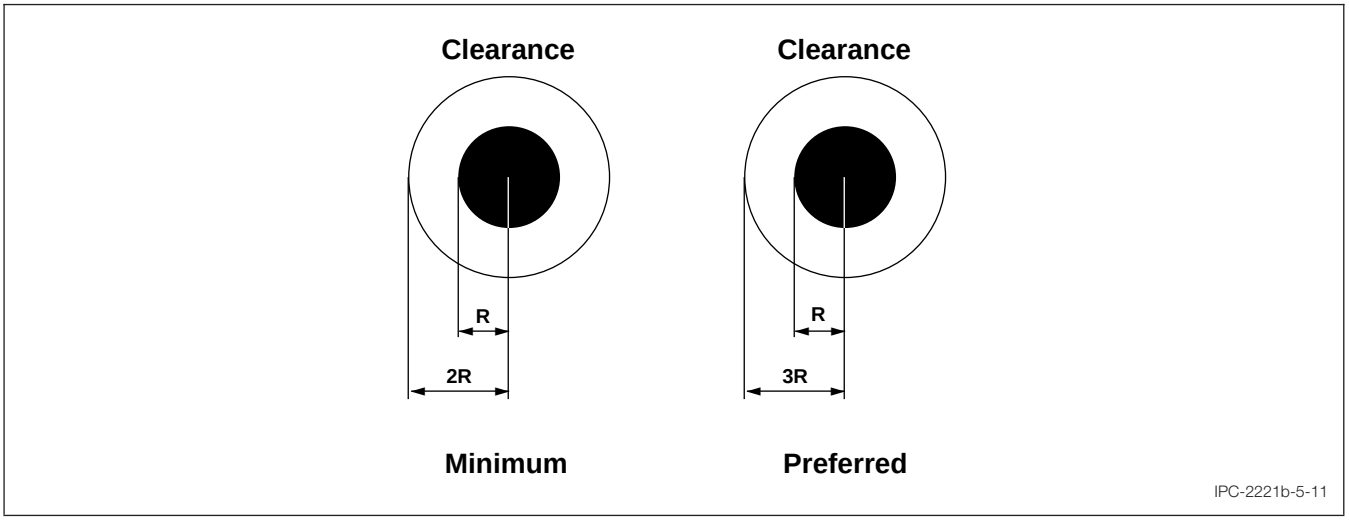


Figure 5-11 Fiducial Clearance Requirements

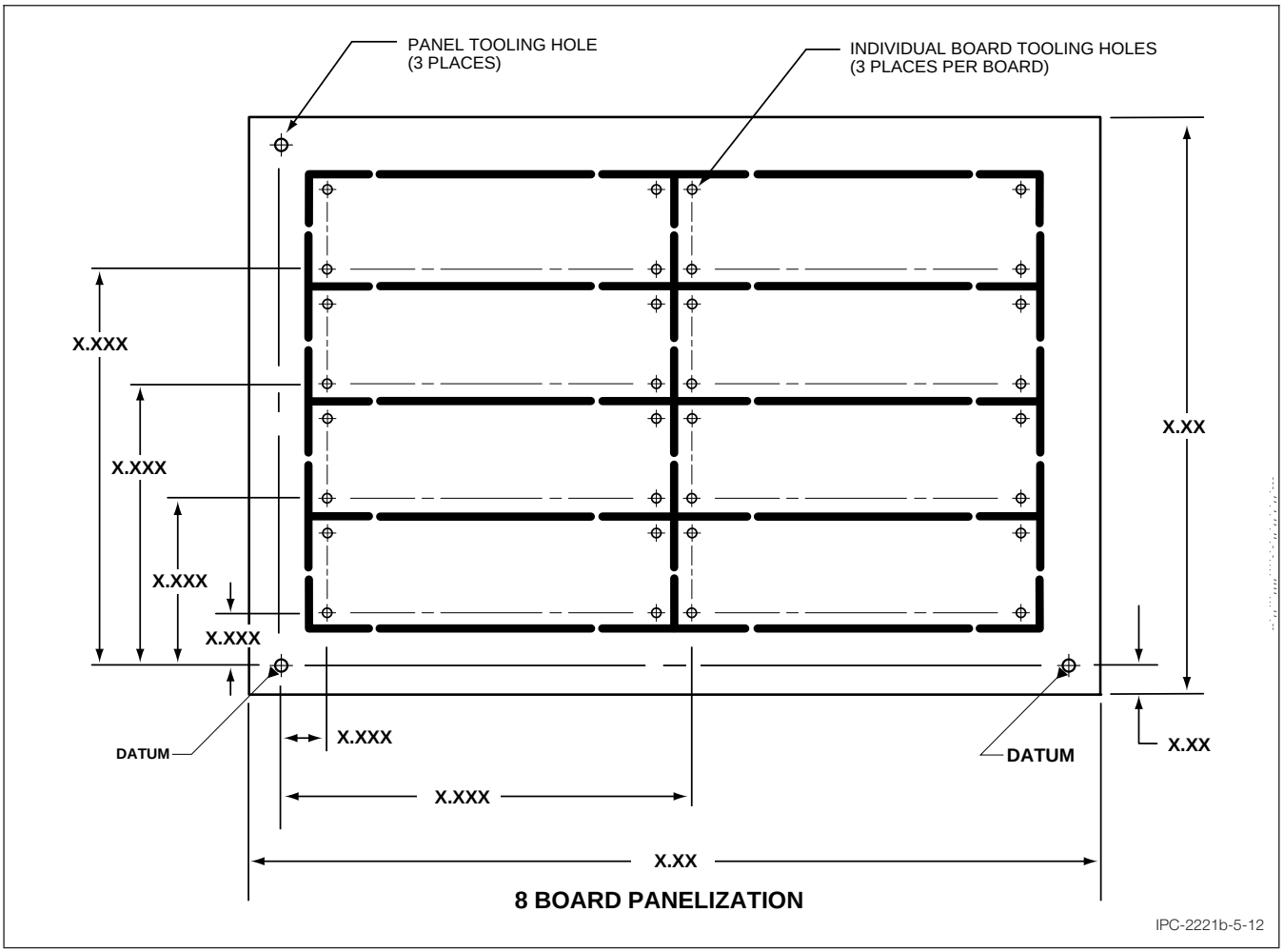


Figure 5-12 Printed Board Panelization/Palletization, mm

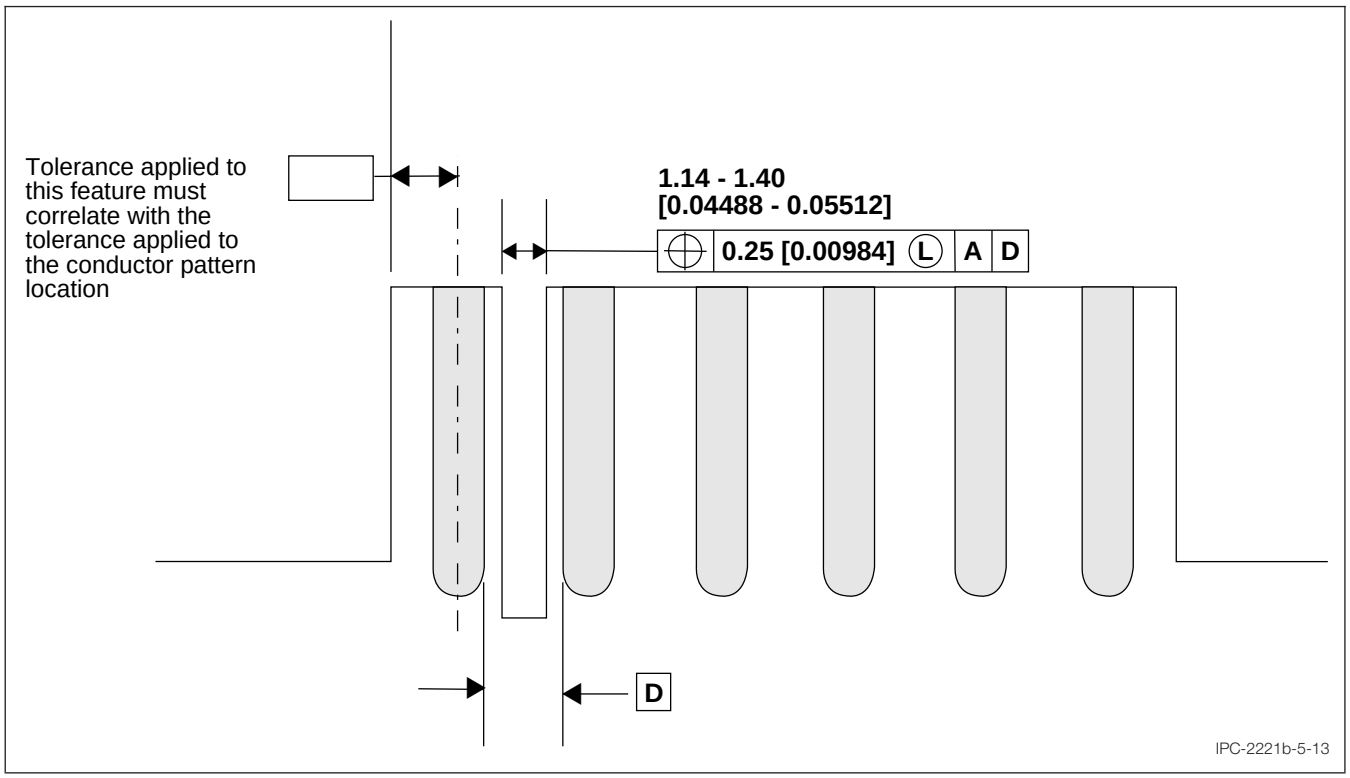


Figure 5-13 Example of Connector Key Slot Location and Tolerance, mm [in]

Palletization may also be used to provide a removable portion of rigid material on a single printed board as a framework for that printed board. This process is particularly valuable during the soldering, assembly and test procedures for rigid flex, or odd shaped printed boards. These pallet edges maintain a fixed dimension between various features on the printed board so that they can be accessed by automated equipment. It may also help prevent the flexible portion of the printed board from dipping into a solder bath.

Excising palletized printed boards can be done in a variety of ways. Some designers provide score lines that can be snapped apart (see IPC-2222 for scoring parameters). Others provide tabs that can be broken, cut, routed, or ''nibbled'' away. Often the tabs will have mouse bites to facilitate removal. In some instances the printed board(s) is (are) completely routed from the pallet after assembly. The method of excising and the location of breakaway tabs should be considered with the final assembly in mind. Sometimes the breakaway tabs can leave a little material that might not be completely flush with the printed board edge and might cause clearance problems in some applications. The location of the mousebite or score in relationship to the actual printed board edge will affect the resultant smoothness of that edge.

Another consideration is the type, style or orientation of parts near the breakaway tabs. When excising printed boards, a fixture should be utilized to minimize mechanical stress. For instance, components such as BGAs and ceramic capacitors might need to be supported to reduce stress during printed board separation. Caution should be given to routing debris that can collect beneath components and may require subsequent cleaning.

Printed board assemblies which contain electrostatic discharge sensitive devices **shall** be handled in accordance with IPC J-STD-001.

6 ELECTRICAL PROPERTIES

6.1 Electrical Considerations

6.1.1 Electrical Performance When printed board assemblies are to be conformal coated, they **shall** be constructed, adequately masked, or otherwise protected in such a manner that application of the conformal coating does not degrade the electrical performance of the assembly. High speed circuit designs should consider the recommendations of IPC-2251.

6.1.2 Power Distribution Considerations A predominately important factor that should be considered in the design of a printed board is power distribution. The grounding scheme can be used as a part of the distribution system. It provides not only a DC power return, but also an AC reference plane for high-speed signals to be referenced. The following items should be taken into consideration:

- Maintain a lower radio-frequency (RF) impedance throughout the DC power distribution. An improperly designed power/ground scheme can result in RF emissions. This results from radiated field gradients developed across the uneven board impedance and its inability of decoupling capacitors to efficiently reduce the printed board's EMI.
- Decouple the power distribution at the printed board connector using adequate decoupling capacitance. Distribute adequate individual power/ground decoupling capacitors evenly throughout logic device printed board areas. Minimize the impedance and radiation loop of the coupling capacitor by keeping capacitor leads as short as possible, and locating them adjacent to the critical circuit.

A good technique for the distribution of power and grounds in a multilayer printed board is to use planes. When utilizing planes for power and ground distribution, it is recommended that the incoming power and ground signals terminate at the input decoupling network, prior to connecting to the respective internal planes. If external power busses are required, commercially available bussing schemes may be employed as defined in 8.2.13. When using power conductors, as shown in Figure 6-1, power conductors should be run as close as possible to ground conductors. Both power and ground conductors **shall** be maintained as wide as possible. The power and ground planes virtually become one plane at high frequencies, and should, therefore, be kept next to each other.

Figure 6-1A shows a poor layout, giving high inductance and few adjacent signal return paths; this leads to crosstalk.

Figure 6-1B is a better layout and reduces power distribution, logic-return impedances, conductor crosstalk and printed board radiation.

The best layout is shown in Figure 6-1C, which has further EMI problem reductions.

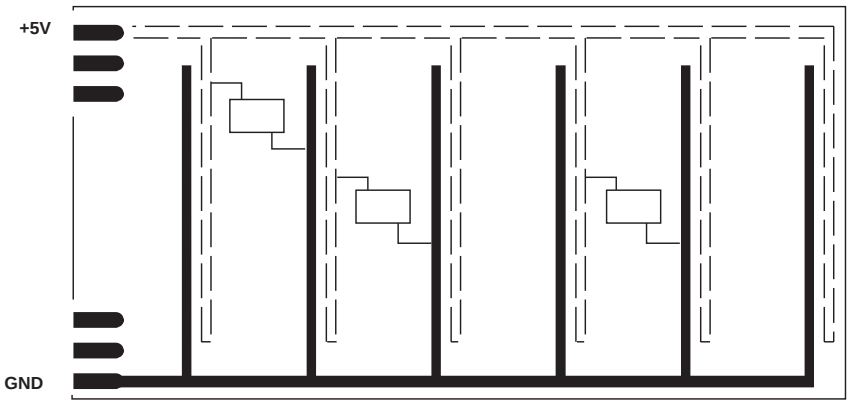
In digital power distribution schemes, the grounding and power should be designed first, not last, as is typically done with some analog circuits. All interfacing, including power, should be routed to a single reference edge, or area. Opposing end interconnections should be avoided. When unavoidable, care should be taken to route the power and ground away from active circuits (see Figure 6-2). At the interconnection reference edge, all ground structures should be made as heavy as possible.

The shortest possible conductor length should be used between devices. The printed board should be separated into areas for high, medium, and low frequency circuits (see Figure 6-3).

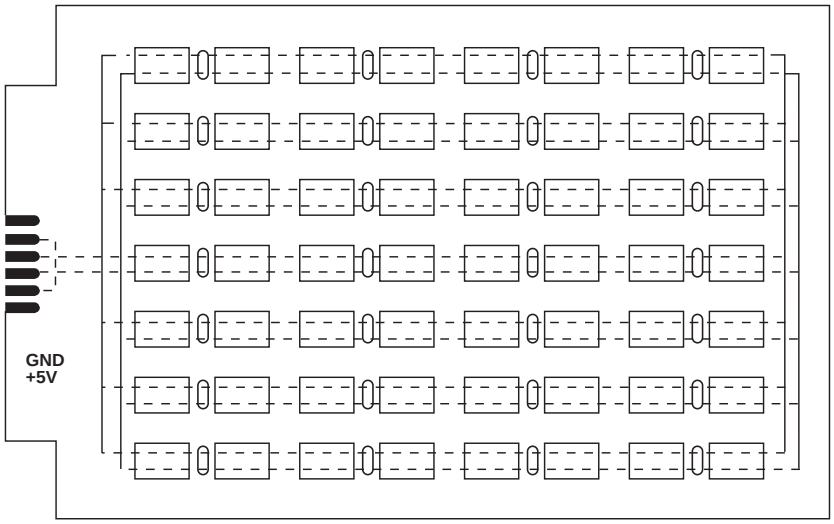
6.1.3 Circuit Type Considerations The following guidelines should be considered when designing printed board assemblies:

- Always determine correct polarity of the component, where applicable
- Transistor emitter/base and collector should be properly identified (ground transistor case where applicable)
- Keep lead length as short as possible, and determine capacitive coupling problems between certain components
- If different grounds are used, keep grounding busses or planes as far away from each other as possible
- As opposed to digital signals, analog design should have signal conductors considered first, and ground planes or ground conductor connections considered last
- Keep heat-sensitive and heat-radiating components as far apart as possible (incorporate heatsinks whenever necessary)

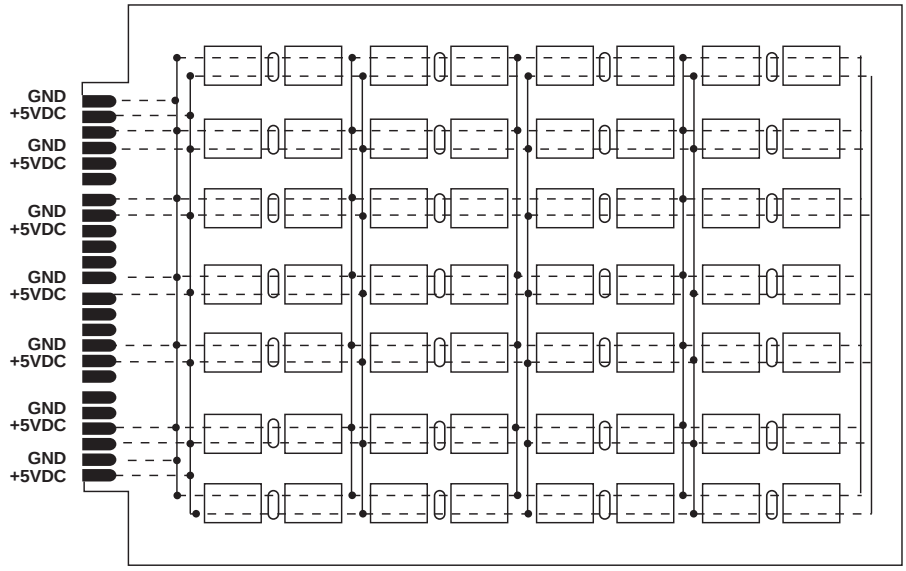
6.1.3.1 Digital Circuits Digital circuits are composed of electronic components that can provide state information (1 or 0), as a function of the performance of the overall circuit. Normally, logic integrated circuits are used to perform this function; however, discrete components may also be used sometimes to provide digital responses.



A. Poor layout



B. Acceptable layout



C. Preferred layout

= Integrated Circuit

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Figure 6-1 Voltage/Ground Distribution Concepts

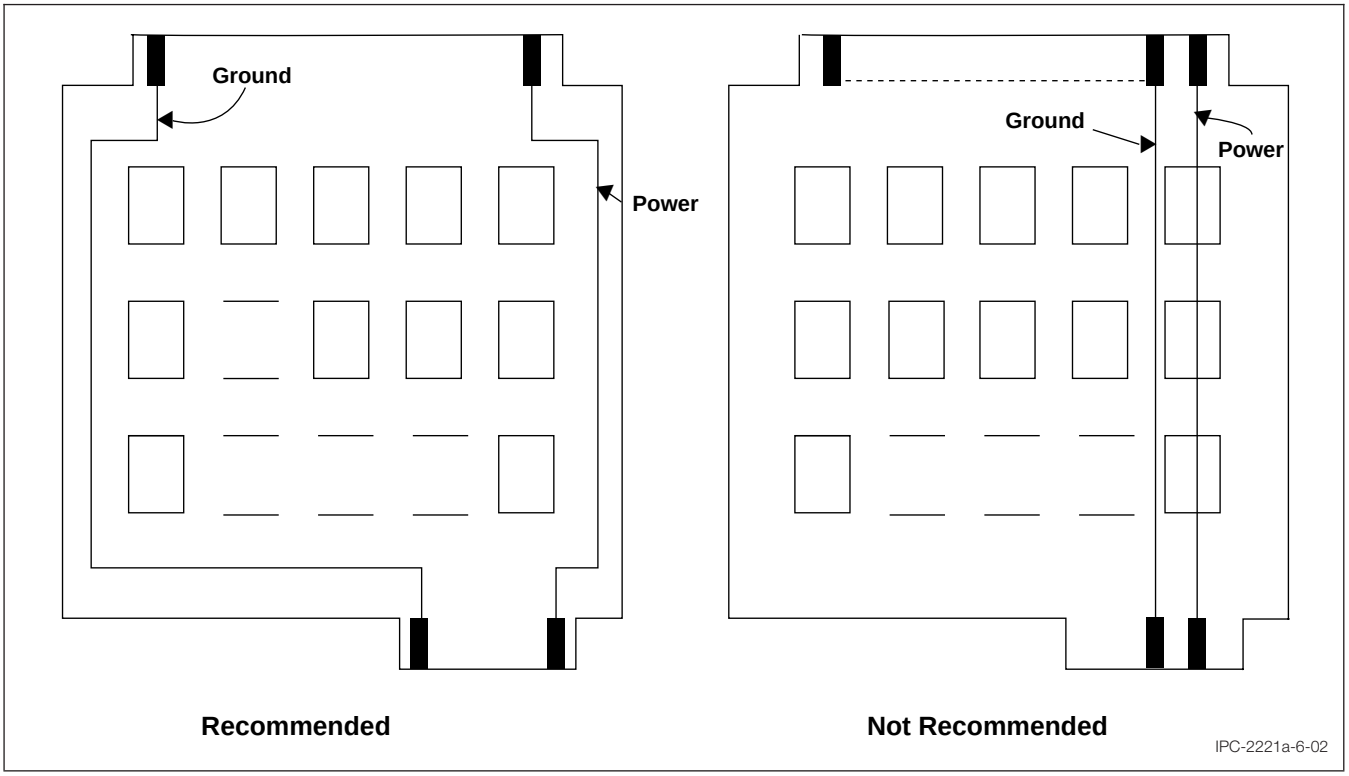


Figure 6-2 Single Reference Edge Routing

Integrated circuit devices use a variety of logic families. Each family has its own parameters regarding the speed of the digital transmission, as well as the temperature rise characteristics necessary to provide the performance. In general, a single printed board usually uses the same logic family in order to facilitate a single set of design rules for conductor length for signal driving restrictions. Some of the more common logic families are:

TTL – Transistor Transistor Logic
MOS – Metal Oxide Semiconductor Logic
CMOS – Complimentary Metal Oxide Semiconductor Logic
ECL – Emitter Coupled Logic
GaAs – Gallium Arsenide Logic

In certain high-speed applications, specific conductor routing rules may apply. A typical example is serial routing between signal source, loads and terminators. Rating branches (stubs) may also have specified criteria.

Digital signals can be roughly placed in four classes of criticality. These classes are:

a) *Noncritical Signals* – Those which are not sensitive to coupling between them. Examples are between lines of a data bus or between the lines of an address bus where they are sampled long after they are settled.

b) *Semi-Critical Signals* – Those where coupling is kept low enough to avoid false triggering, such as reset lines and level triggering strobe lines.

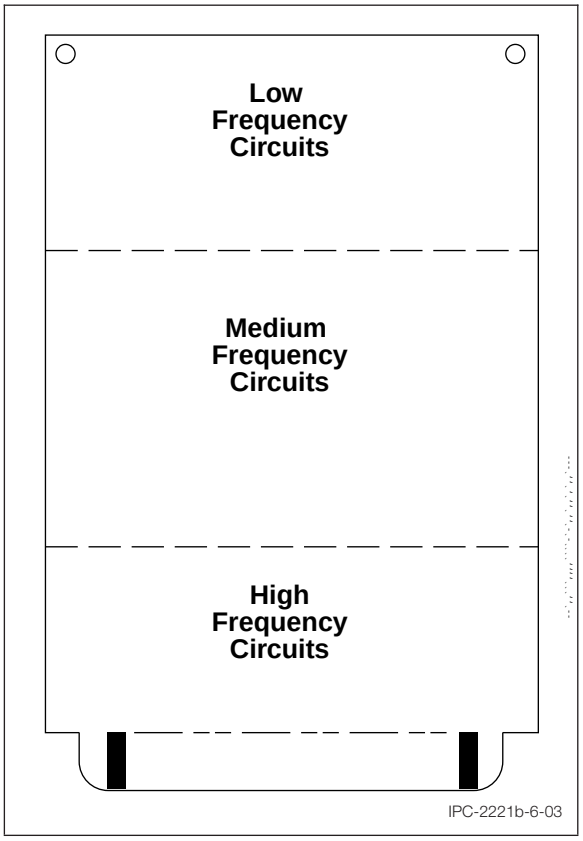


Figure 6-3 Circuit Distribution

c) *Critical Signals* – Those with waveforms that are required be monotonic through the voltage thresholds of the receiving device. These are normally clocking signals and any glitch while the wave form is in transition may cause a double clocking of the circuit. A noncritical signal has a waveform that need not be monotonous and may even make multiple transitions between the voltage thresholds before it settles. Obviously it needs to settle before the receiving device acts upon the data, e.g., the data input to a flip-flop may be a noncritical but the clock signal is most probably a critical signal. Asynchronous signals, although they may (or may not) be noncritical signals, should not be mixed with critical signals since there is a real possibility of the asynchronous signals inducing noise on the critical signals during the clock transitions. Clock signals that do not have a common master frequency should also not be routed together for similar reasons.

d) Super-Critical Signals – Those in applications such as clocks or strobes for A/D and D/A converters, signals in Phase Locked Loops, etc. In these types of applications phase lock jitters and crosstalk, causing errors, noise and timing jitters, will show up in the application's output performance. It is only a question of the amount of disturbance within the required performance specification. This class of signal is essentially the same as an analog coupling situation. In other words, it is completely linear (the total noise is the sum of the individual noise elements; no averaging or canceling out can be assumed).

6.1.3.2 Analog Circuits Analog circuits are usually made from integrated circuits and discrete devices. Standard discrete components (resistors, capacitors, diodes, transistors, etc.), as well as power transformers, relays, coils and chokes, are usually the types of discrete devices used for analog circuits.

6.2 Conductive Material Requirements The minimum width and thickness of conductors on the finished printed board **shall** be determined primarily on the basis of the current-carrying capacity required, and the maximum permissible conductor temperature rise, which is dependent upon cross-sectional area and other factors such as printed board thickness and material, the amount and adjacency of copper in the printed board, and the environment in which the printed board will operate. The minimum conductor width and thickness should be in accordance with the universal charts provided in IPC-2152 that are recommended for sizing of all conductors, both internal and external. IPC-2152 contains additional conductor sizing charts that are based on test data from specific materials and copper thicknesses evaluated in both air and vacuum environments which provide further insight into conductor temperature rise from an applied current.

For internal layers, the conductor thickness is the copper foil thickness of the base laminate unless blind/buried vias are used in which case the copper foil thickness includes copper process plating. For external layers, the conductor thickness also includes the thickness of plated copper deposited during the PTH formation process, but should not include the thickness of solder coating, tin-lead plating, or secondary platings. It should be noted that the foil thickness specified by the standard drawing noted for the preferred printed board materials are nominal thickness values which can generally vary by as much as ± 10%. For external layers, the total copper thickness will also vary due to processing prior to plating which may reduce the thickness of base copper. Furthermore, since the thickness of plated copper is controlled by the requirement for the thickness of copper required in the barrel of the PTH, the associated amount of copper on the external layers may not be the same thickness as the plating in the barrels of the PTHs (see 10.1.1). Therefore, if conductor thickness is critical, a minimum finished printed board conductor thickness should be specified on the master drawing.

For ease of manufacture and durability in usage, these parameters should be optimized while maintaining the minimum recommended spacing requirements. To maintain finished conductor widths, as on the master drawing, conductor widths on the production master may require compensation for process allowances as defined in Section 10.

6.3 Electrical Clearance Spacing between conductors on individual layers should be maximized whenever possible. The minimum spacing between conductors, between conductive patterns, and between conductive materials (such as conductive markings or mounting hardware) and conductors **shall** be in accordance with Table 6-1, and defined on the master drawing.

Layer to layer conductive spaces (z-axis) should be in accordance with Table 6-1. Z-axis minimum spacing requirements may be reduced with appropriate qualification.

Note: The designer should be aware that the profile roughness of the copper foil determines the minimum dielectric distance between opposing copper points within a thin core laminate. See also IPC-4101 for tolerances by class and thickness of core; IPC-4562 for surface roughness of copper foil types; and IPC-6012 for the method to determine minimum dielectric thickness. Designers should be careful not to use minimum dielectric spacing values to determine overall printed board thickness.

See Section 10 for additional information on process allowances affecting electrical clearance.

When mixed voltages appear on the same printed board and they require separate electrical testing, the specific areas **shall** be identified on the master drawing or appropriate test specification. When employing high voltages and especially AC and pulsed voltages greater than 200 volts potential, the dielectric constant and capacitive division effect of the material **shall** be considered in conjunction with the recommended spacing.

For voltages greater than 500V, the (per volt) table values **shall** be added to the 500V values. For example, the electrical spacing for a Type B1 printed board with 600V is calculated as:

600V - 500V = 100V
0.25 mm [0.00984 in] + (100V x 0.0025 mm)
= 0.50 mm [0.0197 in] clearance

When, due to the criticality of the design, the use of other conductor spacings is being considered, the conductor spacing on individual layers (same plane) **shall** be made larger than the minimum spacing required by Table 6-1 whenever possible. Printed board layout should be planned to allow for the maximum spacing between external layer conductive areas associated with high impedance or high voltage circuits. This will minimize electrical leakage problems resulting from condensed moisture or high humidity. Complete reliance on coatings to maintain high surface resistance between conductors **shall** be avoided.

6.3.1 B1-Internal Conductors Internal conductor-to-conductor, and conductor-to-PTH electrical clearance requirements at any elevation (see Table 6-1).

6.3.2 B2-External Conductors, Uncoated, Sea Level to 3050 m [10,007 feet] Electrical clearance requirements for uncoated external conductors are significantly greater than for conductors that will be protected from external contaminants with conformal coating. If the assembled end product is not intended to be conformally coated, the bare printed board conductor spacing **shall** require the spacing specified in this category for applications from sea level to an elevation of 3050 m [10,007 feet] (see Table 6-1).

6.3.3 B3-External Conductors, Uncoated, Over 3050 m [10,007 feet] External conductors on uncoated bare printed board applications over 3050 m [10,007 feet] require even greater electrical spacings than those identified in category B2 (see Table 6-1).

Table 6-1 Electrical Conductor Spacing

Voltage Between Conductors (DC or AC Peaks)	Minimum Spacing						
	Bare Printed Board				Assembly		
	B1[1]	B2	B3	B4	A5	A6	A7
0-15	0.05 mm [0.002 in]	0.1 mm [0.004 in]	0.1 mm [0.004 in]	0.05 mm [0.002 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]
16-30	0.05 mm [0.002 in]	0.1 mm [0.004 in]	0.1 mm [0.004 in]	0.05 mm [0.002 in]	0.13 mm [0.00512 in]	0.25 mm [0.00984 in]	0.13 mm [0.00512 in]
31-50	0.1 mm [0.004 in]	0.64 mm [0.025 in]	0.64 mm [0.025 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.4 mm [0.016 in]	0.13 mm [0.00512 in]
51-100	0.1 mm [0.004 in]	0.64 mm [0.025 in]	1.5 mm [0.0591 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.5 mm [0.020 in]	0.13 mm [0.00512 in]
101-150	0.2 mm [0.0079 in]	0.64 mm [0.025 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
151-170	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
171-250	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	6.4 mm [0.252 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
251-300	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	12.5 mm [0.4921 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]
301-500	0.25 mm [0.00984 in]	2.5 mm [0.0984 in]	12.5 mm [0.4921 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]	1.5 mm [0.0591 in]	0.8 mm [0.031 in]
≥500 See para. 6.3 For calc.	0.0025 mm/ volt	0.005 mm/ volt	0.025 mm/ volt	0.00305 mm/ volt	0.00305 mm/ volt	0.00305 mm/ volt	0.00305 mm/ volt

Note 1. These values presume woven fiberglass coated with epoxy-based resin systems; other sytems may have different values.

6.3.4 B4-External Conductors, with Permanent Polymer Coating (Any Elevation) When the final assembled printed board will not be conformally coated, a permanent polymer coating over the conductors on the bare printed board will allow for conductor spacings less than that of the uncoated printed boards defined by category B2 and B3. The assembly electrical clearances of lands and leads that are not conformally coated require the electrical clearance requirements stated in category A6 (see Table 6-1). This configuration is not applicable for any application requiring protection from harsh, humid, contaminated environments.

Typical applications are computers, office equipment, and communication equipment, bare printed boards operating in controlled environments in which the bare printed boards have a permanent polymer coating on both sides. After they are assembled and soldered the printed boards are not conformal coated, leaving the solder joint and soldered land uncoated.

Note: All conductors, except for soldering lands, **shall** be completely coated in order to ensure the electrical clearance requirements in this category for coated conductors.

6.3.5 A5-External Conductors, with Conformal Coating over Assembly (Any Elevation) External conductors that are intended to be conformal coated in the final assembled configuration, for applications at any elevation, will require the electrical clearances specified in this category.

Typical applications are military products where the entire final assembly will be conformal coated. Permanent polymer coatings are not normally used, except for possible use as a solder mask. However, the compatibility of polymer coating and conformal coating should be considered, if used in combination.

6.3.6 A6-External Component Lead/Termination, Uncoated, Sea Level to 3050 m [10,007 feet] External component leads and terminations, that are not conformal coated, require electrical clearances stated in this category.

Typical applications are as previously stated in category B4. The B4/A6 combination is most commonly used in commercial, nonharsh environment applications in order to obtain the benefit of high conductor density protected with permanent polymer coating (also solder mask), or where the accessibility to components for rework and repair is not required.

6.3.7 A7-External Component Lead/Termination, with Conformal Coating (Any Elevation) As in exposed conductors versus coated conductors on bare printed board, the electrical clearances used on coated component leads and terminations are less than for uncoated leads and terminations.

6.4 Impedance Controls Multilayer printed boards are ideally suited for providing interconnection wiring that is specifically designed to provide desired levels of impedance and capacitance control. Techniques commonly referred to as ‘‘stripline,‘‘ or ‘‘embedded microstrip,‘‘ are particularly suited for impedance and capacitance requirements. Figure 6-5 shows four of the basic types of transmission line constructions. These are:

a) *Microstrip* – A rectangular conductor placed at the interface between two dissimilar dielectrics (usually air and usually FR-4) whose main current return path (usually a solid copper plane) is on the opposite side of the high εr material. Three sides of the conductor contact the low-εr materials (εr = 1), and one side of the conductor contacts the high-εr material (εr>1).

b) *Embedded Microstrip* – Similar to Microstrip except that the conductor is completely embedded in the higher-εr materials.

c) *Symmetric Stripline* – A rectangular conductor surrounded completely by a homogeneous dielectric medium and located symmetrically between two reference planes.

d) *Dual (Asymmetric) Stripline* – Similar to Stripline except that one or more conductor layers are asymmetrically located between the two reference planes.

The design of such multilayer printed boards should take into consideration the guidelines of IPC-2251 and IPC-2141.

6.4.1 Microstrip Flat conductors are the geometry normally found on a printed board as manufactured by the copper plating and etching processes (see Figure 6-4A). The capacitance is influenced most strongly by the region between the signal line and adjacent ground (or power) planes. Inductance is a function of the ''loop'' formed by the frequency of operation (i.e., skin effect) and the distance to the reference plane for microstrips and striplines, and the length of the conductor.

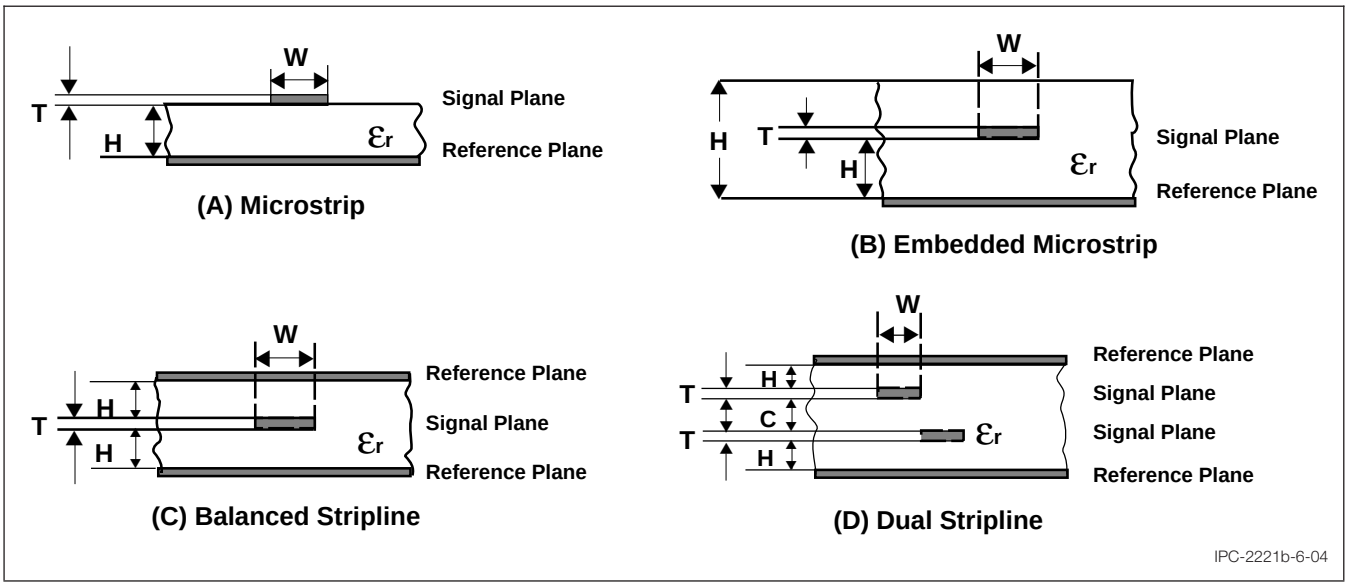


Figure 6-4 Transmission Line Printed Board Construction

The following equations give the impedance (Z_0) propagation delay (T_{pd}), and intrinsic line capacitance (C_0) for microstrip circuitry.

$$Z_0 = \frac{87}{\sqrt{\varepsilon r + 1.41}} \ln\left[\frac{5.98h}{0.8w + t}\right] \quad \text{in ohms}$$

$$T_{pd} = \frac{\sqrt{\varepsilon r}}{c} \quad \text{in psec/inch}$$

$$C_0 = \frac{T_{pd}}{Z_0} \quad \text{in pF/inch}$$

$$\text{For } \frac{w}{h} < 1$$

where:

c = Speed of light in vacuum (3.0×10^8 m/s)
h = Dielectric thickness, inches
w = Line width, inches
t = Line thickness, inches
εr = Relative permittivity (dielectric constant) of substrate (see Table 6-2)

The radiated electromagnetic interference (EMI) signal from the lines will be a function of the line impedance, the length of the signal line and the incident waveform characteristics. This may be an important consideration in some high speed circuitry. In addition, crosstalk between adjacent circuits will depend directly upon circuit spacing, the distance to the reference planes, length of parallelism between conductors, and signal rise time (see IPC-2251).

6.4.2 Embedded Microstrip The embedded microstrip has the same conductor geometry as the uncoated microstrip discussed above. However, the effective dielectric constant is different because the conductor is fully enclosed by the dielectric material (see Figure 6-4B). The equations for embedded microstrip lines are the same as in the section on [uncoated] microstrip, with a modified effective dielectric constant. If the dielectric thickness above the conductor is 2.54 µm [100 µin] or more, then the effective dielectric constant can be determined using the criteria in IPC-2251. For very thin dielectric coatings (less than is 2.54 µm [100 µin]), the effective dielectric constant will be between that for air and the bulk dielectric constant (see Table 6-2).

Table 6-2 Typical Relative Bulk Dielectric Constant of Printed Board Material

DESIGNATOR					Resin Ref. Code	Material Reinforcement/Resin	Dielectric Constant
NEMA[2]	IPC Specification			Military[3]			Er value[4]
	4202	4101	4103	S-13949			
G-10		/20		/3	GEN	Woven E Glass/Epoxy	4.6 - 5.4
G-11		/22		/2	GB	Woven E Glass/Epoxy	4.5 - 5.4
FR-4[5]		/24		/4	GF GFN GFK	Woven E Glass/Epoxy	4.2 - 4.9
FR-5		/23		/5	GH	Woven E Glass/Epoxy	4.2 - 4.9
GPY		/42		/10	GI GIJ	Woven E Glass/Polyimide	4.0 - 4.7
		/50		/15	AF	Woven Aramid/Modified Epoxy	3.8 - 4.5
		/55		/22	BF	Non-Woven Aramid/Epoxy	3.8 - 4.5
		/53		/31	BI	Non-Woven Aramid/Polyimide	3.6 - 4.4
		/60		/19	QIL	Woven Quartz/Polyimide	3.0 - 3.8
		/30		/24	GM GFT	Woven E Glass/Triazine/BT	3.6 - 4.2
		/71		/29	GC	Woven E Glass/Cyanate Ester	4.0 - 4.7
			4103/03	/6	GP	Non-Woven Glass/PTFE	2.15 - 2.35
			4103/04	/7	GR	Non-Woven Glass/PTFE	2.15 - 2.35
			4103/01	/8	GT	Woven Glass/PTFE	2.45 - 2.65
			4103/02	/9	GX	Woven Glass/PTFE	2.4 - 2.6
			4103/05	/14	GY	Woven Glass/PTFE	2.15 - 2.35
	/1[6]					Non-Supported Polyimide	3.2 - 3.6

Note 1. Dielectric values will vary approximately within the range given, depending on the reinforcement/resin ratio. Generally thin laminates tend toward the lower values.

Note 2. National Electrical Manufacturers Association. Several NEMA grades, such as the paper/paper composite based products XPC, FR-1, FR-2, CEM, etc. has been omitted from this table. See IPC-4101 for complete cross-reference and properties of these grades.

Note 3. MIL-S-13949 is canceled and listed for reference only.

Note 4. Permittivity @ 1 MHz maximum. (Laminate or prepreg as laminated)

Note 5. Multiple slash sheet designations exist within IPC-4101 for the FR-4 classification. See IPC-4101 /21, /25, /26, /82 for specific differences of resin formulations and T_g valves.

Note 6. Polyimide flexible film is listed for comparison to reinforced materials; additional properties of flexible films with coatings and cladding can be found in IPC-4203 and IPC-4204 respectfully. See also IPC-2223 for applications.

6.4.3 Stripline Properties A stripline is a thin, narrow conductor embedded between two AC reference planes (Figure 6-4C). Since all electric and magnetic field lines are contained between the planes, the stripline configuration has the advantage that EMI will be suppressed except for lines near the edges of the printed board. Crosstalk between circuits will also be reduced (compared to the microstrip case) because of the closer electrical coupling of each circuit to ground. Because of the presence of reference planes on both sides of a stripline circuit, the capacitance of the line is increased and the impedance is decreased from the microstrip case.

Stripline impedance (Z_0) and intrinsic line capacitance (C_0) parameters are presented below for flat-conductor geometries. The equations assume that the circuit layer is placed midway between the planes.

$$Z_0 = \frac{60 \ln\left[\frac{1.9\,(2H + T)}{(0.8W + T)}\right]}{\sqrt{\varepsilon r}} \quad \text{in ohms}$$

$$C_0 = \frac{1.41\,(\varepsilon r)}{\ln\left[\frac{3.81H}{(0.8W + T)}\right]} \quad \text{in pF/in}$$

$$\text{For } \frac{W}{H} < 2$$

where:

H = Distance between line and one ground plane
T = Line thickness inches
W = Line width inches
εr = Relative permittivity of substrate
pF = Picofarads

6.4.4 Asymmetric Stripline Properties When a layer of circuitry is placed between two reference planes, but is not centered between them, the stripline equations **shall** be modified. This is to account for the increased coupling between the circuit and the nearest plane, since this is more significant than the weakened coupling to the distant plane. When the circuit is placed approximately in the middle third of the interplane region, the error caused by assuming the circuit to be centered will be quite small.

One example of an unbalanced stackup is the dual stripline configuration. A dual-strip transmission line closely approximates a stripline except that there are two signal planes between the power planes. The circuits on one layer are generally orthogonal to those on the other to keep parallelism and crosstalk between layers to a minimum.

Dual stripline impedance (Z_0) and intrinsic line capacitance (C_0) parameters are:

$$Z_0 = \frac{80 \ln\left[\frac{1.9\,(2H + T)}{(0.8W + T}\right] \bullet \left[1 - \frac{H}{4\,(H + C + T)}\right]}{\sqrt{\varepsilon r}} \quad \text{in ohms}$$

$$C_0 = \frac{2.82\,(\varepsilon r)}{\left[\frac{2H - T}{(0.268W + 0.335T)}\right]} \quad \text{in pF/in}$$

where:

H = Height above power plane
C = Signal plane separation
T = Line thickness, inches
W = Line width, inches
pF = Picofarads

This stackup is shown in Figure 6-4D. As with stripline, EMI will be completely shielded except for signal lines near the edges of the printed board.

The above equations can be adapted to determine Z_0 or C_0 for asymmetric stripline circuits that are not dual stripline. Plane sequences for a four-layer printed board should be as described in Figure 6-4D. For printed boards with more than four layers, the sequence should be arranged so that the signal layers are symmetrical about the reference planes. This may be accomplished several ways provided that any adjacent signal layers, not separated by a plane should have their key axes running perpendicular to each other. For a 6-layer printed board, the sequence might be as shown in Table 6-3.

Table 6-3 Example Plane Sequences for a Six Layer Printed Board

A	B
Signal #1	Signal #1
Plane #1	Signal #2
Signal #2	Plane #1
Signal #3	Plane #2
Plane #2	Signal #3
Signal #4	Signal #4

''A'' is the desired configuration in Table 6-3 since the impedance is well matched through the entire stack-up. ''B'' is a less desirable configuration since signals 1 and 4 will be further away from the return path (reference plane) than signals 2 and 3.

Special attention is required in the design of specific circuit characteristics where attention should be given to total conductor lengths, both short and long conductor runs, as well as total interconnection routing.

DC power and ground planes also function as AC reference planes. Power and ground connector pins should be evenly distributed along the edge of the printed board for AC reference.

As a general rule, the reference planes of a multilayer printed board design should not be segmented. Limited plane segmentation, in which the segmented plane is supported by an elevated plane to an adjacent signal layer, and supported by PTHs on approximately 2.54 mm [0.1 in] centers on both sides, may be used to ''bury'' a special high frequency signal within the planes to create a ''coaxial type'' line within the printed board. Spacing of the holes is dependent on frequency of the signal.

6.4.5 Capacitance Considerations Figure 6-5 and Figure 6-6 show the intrinsic line capacitance/per unit length, of copper, for microstrip and stripline, respectively. These charts provide capacitance in pF/ft for 1 oz. copper conductors with various dielectric thicknesses to the ground or power reference plane. Figure 6-6 for stripline is based upon symmetry with the conductor centered between the reference planes.

The capacitance associated with single crossover (see Figure 6-7) is very small and is typically a fraction of a picofarad. As the number of crossovers per unit length increases, the intrinsic capacitance of the transmission line also increases. The crossover lumped capacitance adds to the intrinsic line capacitance. Crossover capacitance (C_c) may be approximated by:

$$C_c = X\varepsilon_r(l + 0.8h)\ \frac{(W + 0.8h)}{h}\ \text{in pF}$$

provided that $l \geq 0.5h$

$$W \geq 0.5h$$

where:

X = 0.0089 if h, l and W are in mm, 0.225 if h, l and W are in inches
εr = relative permittivity
h = dielectric thickness between crossovers
l = length
W = Width

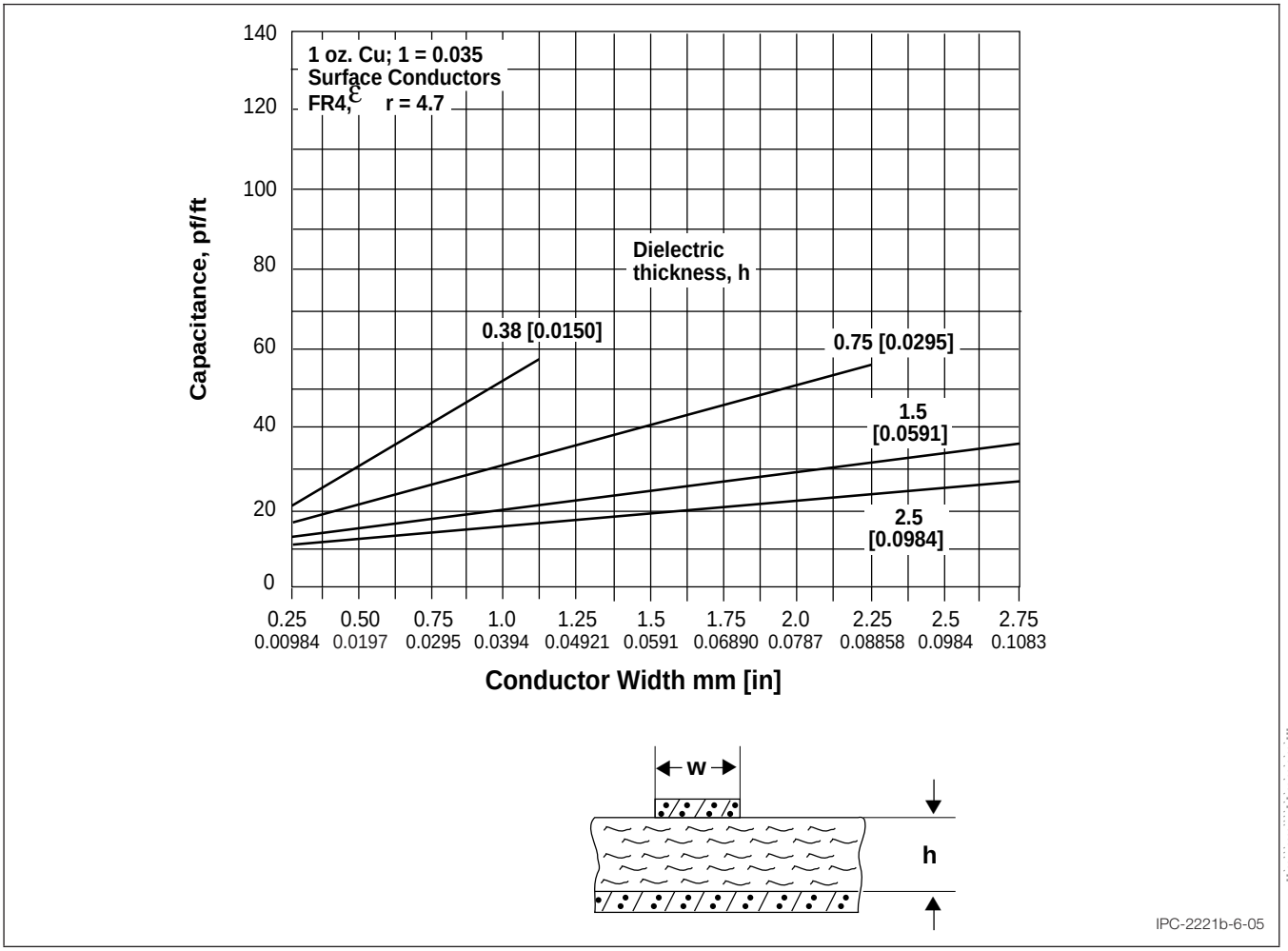


Figure 6-5 Capacitance vs. Conductor Width and Dielectric Thickness for Microstrip Lines, mm [in]

6.4.6 Inductance Considerations Inductance is the property of a conductor that allows it to store energy in a magnetic field induced by a current flowing through that conductor. When this current has high frequency components, the self-inductance of the leads and conductors become significant, leading to transient or switching noise. These transients are related to the inductance of a power/ground loop and the circuit should be designed to reduce this inductance as much as possible.

A common technique to reduce this switching noise is the use of decoupling capacitors that serve to provide the current from a point closer to the IC gate than the power supply. Even when these capacitors are designed into the circuit, the positioning of the capacitor is important. If the capacitor leads are too long, the self inductance becomes too high leading to switching noise. Decoupling on the printed boards is normally achieved with discrete capacitors that can be closely positioned to the IC. In higher I/O packages, a trend has begun which places the decoupling capacitor inside of the package. This has the double advantage of not using real estate for the capacitor location and reducing the size of the capacitor interconnections.

Another consideration is the use of smaller diameter via holes and their associated land sizes. A change from 0.5 - 0.3 mm [0.020 - 0.012 in] vias will reduce parasitic inductance in the circuit. Smaller diameter vias will improve it even more.

Closely spaced adjacent power and ground planes are also being utilized to provide high frequency decoupling capacitance. This also decreases the real estate required for decoupling capacitors.

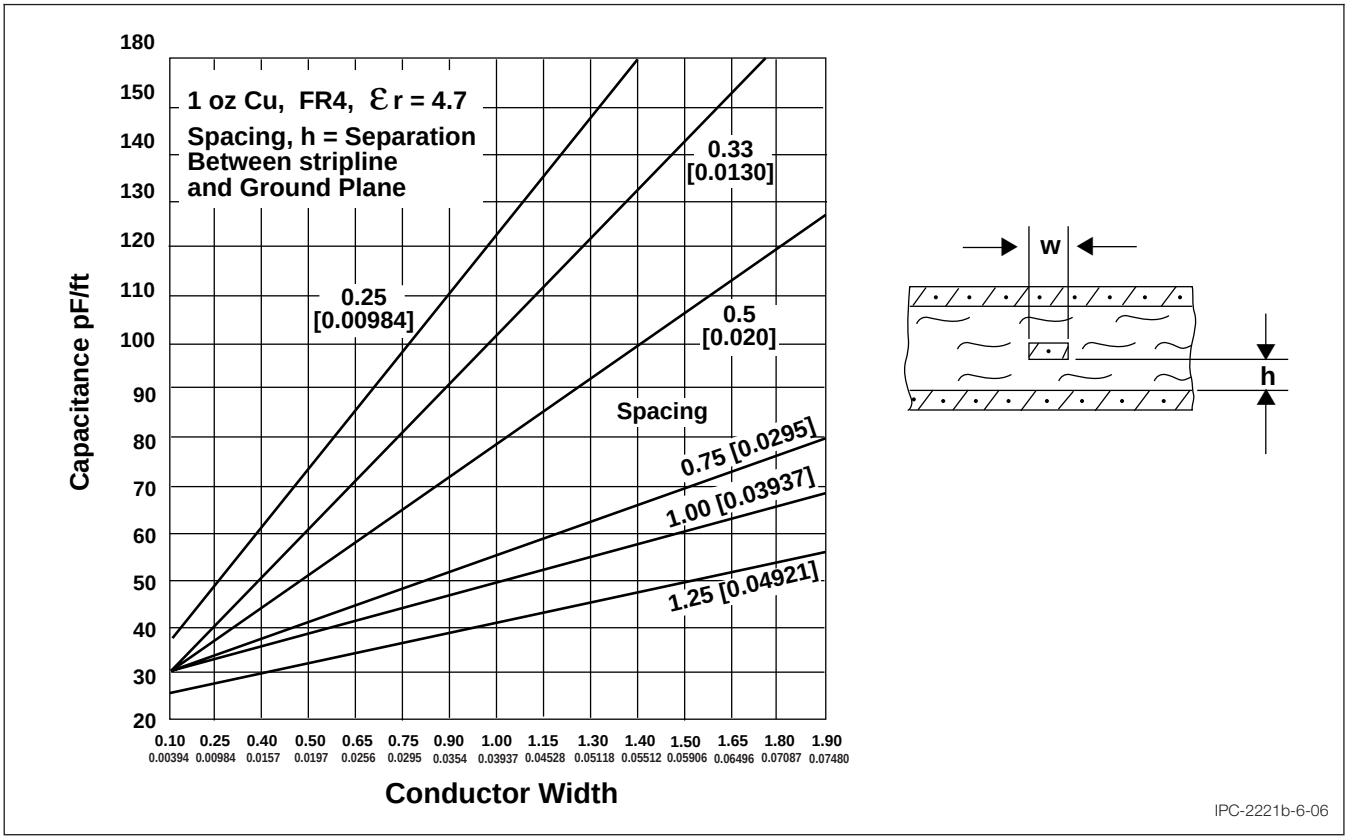


Figure 6-6 Capacitance vs. Conductor Width and Spacing for Striplines, mm [in]

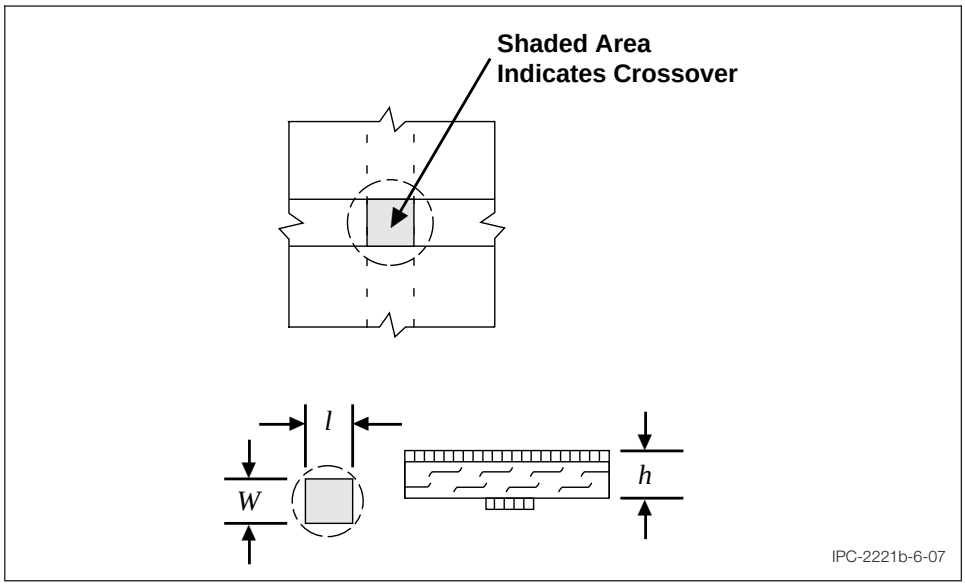


Figure 6-7 Single Conductor Crossover

7 THERMAL MANAGEMENT

This section is intended as an outline for temperature control and heat dissipation. This material, coupled with appropriate thermal analysis can result in greatly reduced thermal stresses and improved reliability of the components, solder attachment and the printed board.

The primary objective of thermal management is to ensure that all circuit components, especially the integrated circuits, are maintained within both their functional and maximum allowable limits. The functional temperature limits provide the ambient temperature range of the component package (case), within which the electronic circuits can be allowed to properly perform.

The cooling technique to be used in the printed board assembly application should be known in order to ensure the proper printed board assembly design. For commercial applications, direct-air cooling (i.e., where cooling air contacts the printed board assembly) may be used.

For rugged and hostile environmental usage, indirect cooling is most often used to cool the printed board assembly. In this application, the assembly is mounted to the structure, that is air or liquid cooled, and the components are cooled by conduction to a heat-exchange surface. These designs should use appropriate metal heatsinks on the printed board assembly. Appropriate component mounting and bonding may be required. To ensure adequate design, thermal dissipation maps should be provided to aid analysis and thermal design of the printed board assembly.

When power densities of a few watts/square inch are confined in the PC card form factor, properly defining ‘‘hot spots,‘‘ thermal paths and cooling technique is essential. A combination of natural and artificial cooling methods may be necessary to maintain a proper steady state operating environment.

7.1 Cooling Mechanisms The dissipation of the heat generated within electronic equipment results from the interaction of the three basic modes of heat transfer: conduction, radiation and convection. These heat transfer modes can, and often do, act simultaneously. Thus, any thermal management approach should attempt to maximize their natural interaction.

7.1.1 Conduction The first mode of heat transfer to be encountered is conduction. Conduction takes place to a varying degree through all materials. The conduction of heat through a material is directly proportional to the thermal conductivity constant (K) of the material, the cross sectional area of the conductive path and the temperature difference across the material. Conduction is inversely proportional to the length of the path and the thickness of the material (see Table 7-1).

Table 7-1 Effects of Material Type on Construction

Material	Thermal Conductivity (K)	
	Watts/m °C	Gram-Calorie/cm °C • s
Still Air	0.0276	0.000066
Epoxy	0.200	0.00047
Thermally Conductive Epoxy	0.787	0.0019
Aluminum Alloy 1100	222	0.530
Aluminum Alloy 3003	192	0.459
Aluminium Alloy 5052	139	0.331
Alumimum Alloy 6061	172	0.410
Aluminum Alloy 6063	192	0.459
Copper	401	0.464
Steel Low Carbon	46.9	0.112

7.1.2 Radiation Thermal radiation is the transfer of heat by electromagnetic radiation, primarily in the infrared (IR) wavelengths. It is the only means of heat transfer between bodies that are separated by a vacuum, as in space environments.

Heat transfer by radiation is a function of the surface of the ‘‘hot’’ body with respect to its emissivity, its effective surface area and the differential to the fourth power of the absolute temperatures involved.

The emissivity is a derating factor for surfaces that are not ‘‘black bodies.‘‘ It is defined as the ratio of emissive power of a given body to that of a black body, for which emissivity is unity (1.0). The optical color of a body has little to do with it being a ‘‘thermal black body.‘‘ The emissivity of anodized aluminum is the same if it is black, red or blue. However, surface finish is important. A matte or dull surface will be more radiant than a bright or glossy surface (see Table 7-2).

Table 7-2 Emissivity Ratings for Certain Materials

Material and Finish	Emissivity
Aluminum Sheet - Polished	0.040
Aluminum Sheet - Rough	0.055
Anodized Aluminum - any color	0.80
Brass - Commercial	0.040
Copper - Commercial	0.030
Copper - Machined	0.072
Steel - Rolled Sheet	0.55
Steel - Oxided	0.667
Nickel Plate - Dull Finish	0.11
Silver	0.022
Tin	0.043
Oil Paints - Any Color	0.92-0.96
Lacquer - Any Color	0.80-0.95

Devices, components, etc. close to one another will absorb each other's radiant energy. If radiation is to be the principal means of heat transfer, ''hot'' spots should be kept clear of each other.

7.1.3 Convection The convection heat transfer mode is the most complex. It involves the transfer of heat by the mixing of fluids, usually air.

The rate of heat flow by convection from a body to a fluid is a function of the surface area of the body, the temperature differential, the velocity of the fluid and certain properties of the fluid.

The contact of any fluid with a hotter surface reduces the density of the fluid and causes it to rise. The circulation resulting from this phenomenon is known as ''free'' or ''natural'' convection. The air flow can be induced in this manner or by some external artificial device, such as a fan or blower. Heat transfer by forced convection can be as much as ten times more effective than natural convection.

7.1.4 Altitude Effects Convection and radiation are the principal means by which heat is transferred to the ambient air. At sea level, approximately 70% of the heat dissipated from electronic equipment might be through convection and 30% by radiation. As air becomes less dense, convective effects decrease. At 5200 m [17060.37 ft], the heat dissipated by convection may be less than half that of radiation. This needs to be considered when designing for airborne applications.

7.2 Heat Dissipation Considerations Design of multilayer printed boards to remove heat from a high thermal radiating printed board assembly should consider the use of:

- Heatsinking external planes (usually copper or aluminum)
- Heatsinking internal planes
- Special heatsink fixtures
- Connection to frame techniques
- Liquid coolants and heatsink formation
- Heat pipes
- Heatsinking constraining substrates

7.2.1 Printed Board Housings For thermal purposes a housing can be considered to be either the ''enclosed'' type, in which the inside of the housing is completely separated from the outside ambient environment, or the ''ventilated'' type, in which the inside air is supplied from the host environment and returned to it in a heated condition.

7.2.1.1 Enclosed Housing Heat from the ''enclosed'' printed board is dissipated indirectly. In other words, the internal heat must first be transferred to the external cooling surfaces of the printed board housing through the use of internal conduction, natural convection and radiation and subsequent conduction through the walls of the housing with the heat dissipated from the housing through natural convection and radiation into the host environment.

The following is a list of practices which will aid in the transfer of heat in an enclosed housing:

a) Maximize the use of ground, power or case ground planes on every layer of the printed board. Mount ''hot'' devices over large sections of plane whenever possible. Devices should be mounted as near the printed board as possible and use thermal transfer creams or adhesives whenever necessary. Thermal vias connecting planes of common electrical potential will help conduct best to all the planes. Vias under hot devices will be especially helpful. Fill of vias with solder or other type of protection is recommended to avoid solder depletion and/or contamination traps. The positioning of thermal vias is relevant to these issues.

b) Thermally connect planes to the housing rails whenever possible. The use of thermal transfer creams on the rails can be beneficial. Many vias along the printed board edges which contact the rails will help to conduct heat away from inner planes.

c) Mount ''hot'' devices near the edge of the printed board to minimize the thermal conductivity path. Have ''hot'' devices contact the inside of the large surface of the housing, either directly or through a metal transfer plate. Use creams when needed.

d) Mount ''hot'' devices away from each other to maximize thermal radiation.

e) Printed board housing to be fabricated from materials with high thermal conductivity and high thermal emissivity. Materials should be thermally black with a rough finish.

f) If the printed board's host environment has an internal fan, have the receiving port for the printed board mounted in the path of the air movement. If possible, the housing should be parallel to the air movement. This will promote convective transfer away from the housing and into the host environment.

g) If the printed board's host environment does not have an internal cooling fan and heat is being transferred to both walls of the printed board housing, mount the receiving port so the printed board is parallel to gravity. If the heat is primarily transferred to one wall of the housing, mount perpendicular to gravity with that wall facing up.

h) If all else fails and analysis shows that enough heat cannot be successfully removed, look carefully at designing the printed board to use polyimide or some other material with a high T_g and a more stable Z axis and design the circuit with high heat capable components.

7.2.1.2 Ventilated Housing In the case of a ''ventilated'' printed board housing the ambient cooling air can be introduced into the printed board by means of natural ventilation or forced convection. In this manner, the heat generated within the enclosure is dissipated to the host environment by the heating of the cooling air as it passes from the housing.

The following is a list of practices which will aid in the transfer of heat in a ventilated housing:

a) Apply all the practices listed above for an enclosed housing. These concepts of transfer by radiation and conduction will apply equally well in a convective environment.

b) In cases where heat densities are greater in the printed board environment than the host environment, openings or vents, near the ''hot'' spots, may be considered in the printed board housing. This will allow for natural convection of heat. It is recommended to position as many vents as possible without weakening the housing.

c) When possible mount the printed board receiving port (in the host device) so the printed board housing has its hot, vented surface perpendicular to gravity and facing up. Try to mount the port so the hot side is not immediately adjacent to other heat generators.

d) When forced cooling air is available and can be directed against the hot surface of the printed board housing, position the vents in the housing to help direct air in one end, across the devices and out the other end.

7.2.2 Individual Component Heat Dissipation Heatsinking of individual components can use a variety of different techniques. Section 8.1.10 provides information on some of the heatsinking devices that come with individual components requiring specific heat dissipation. In addition, consideration should be given to:

• Heatsink mounting (hardware or soldering)

• Thermal transfer adhesives, paste, or other materials

• Solder temperature requirements

• Cleaning requirements under heatsinks

7.2.3 Thermal Management Considerations for Printed Board Heatsinks The following factors should be addressed while the printed board components are being placed:

a) Method of heatsink mounting (e.g., adhesive bond, rivet, screw, etc.) to printed board.

b) Thickness of heatsink and printed board assembly to allow adequate component lead protrusion.

c) Automatic component insertion clearances (see Figure 7-1).

d) Heatsink material and material properties.

e) Heatsink finish (e.g., anodize, chemical film, etc.).

f) Component mounting methods (e.g., spacers, screw, bonding, etc.).

g) Heat transfer path and rate of heat transfer.

h) Producibility (e.g., method of assembly, method of cleaning, etc.).

i) Dielectric material required between the heatsink and any circuitry that may be designed on the heatsink mounting surface of the printed board.

j) Edge clearance to any exposed circuitry (i.e., component lands and circuit runs). Tooling hole location and size.

k) Heatsink shape as it relates to the structure of heatsink/printed board assembly.

l) The heatsink should fully support the component. Do not allow the component the opportunity to tip during assembly or soldering.

Heatsinks **shall** be designed to avoid the occurrence of moisture traps and to allow access for post-soldering cleaning. This can be accomplished by providing accessible slots in the heatsink instead of round clearance holes under TO-204-AA, TO-213-AA, and similar packages with leads which extend through the heatsink and are soldered into the board.

Through hole printed board assembly heatsinks generally are of a ladder configuration when standard component package types (i.e., DIPs and axial-leaded components) can be used. The ladder heatsink type is preferred due to its relative simplicity in design and fabrication. Figure 7-1 provides standard clearances between heatsink and components that are necessary to facilitate automatic component insertion.

Certain printed board assemblies (e.g., power supplies and other analog designs in particular) utilize many different component types. The circuit function for these analog circuits may be very dependent upon component placement. For analog designs, heatsinks sometimes cannot be designed in a ladder type configuration, however they should be designed with producibility in mind. Minimizing the number of unique cutout shapes required, and the number of areas where the heatsink thickness will change (requiring milling or lamination) will enhance heatsink producibility. When machined heatsinks are used efforts should be made to utilize as large a radius as possible in corners to enhance producibility (e.g., a 3.0 mm [0.118 in] radius can cost substantially more to fabricate than a 6.0 mm [0.236 in] radius). In all cases, analog heatsink designs that can't use ladders should be designed in parallel with the printed board (as opposed to after completion of artwork) and should be reviewed for producibility in both the metal fabrication and printed board assembly areas. PTH relief in the heat sink should be 2.5 mm [0.0984 in] larger than the hole, which includes electrical clearance and misregistration tolerance.

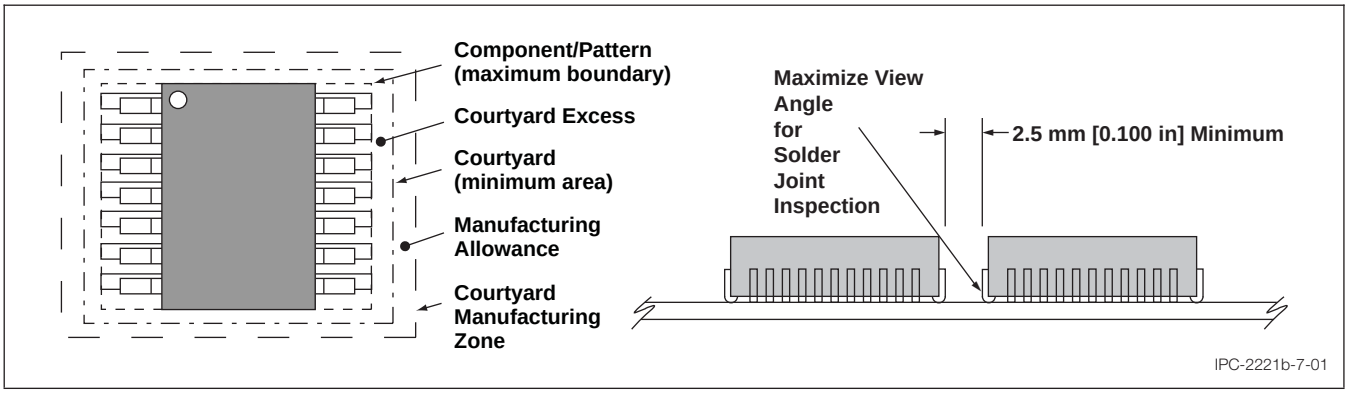


Figure 7-1 Component Clearance Requirements for Automatic Component Insertion

7.2.4 Assembly of Heatsinks to Printed Boards Assembly of heatsinks to printed boards may be accomplished as listed below (in order of manufacturing preference). If the printed board and the heatsink are purchased as an assembly, the manufacturer may have other preferences. Table 7-3 shows the preferences.

Details of these assembly methods are as follows:

a) *Mechanical Fasteners* – Riveting is the preferred fastening method, but care should be taken in rivet selection (solid or tubular), and rivet installation, to obviate laminate damage. Screws should be used if the unit is expected to be disassembled. Closer contact may be necessary to resist vibration or improve heat transfer. Use of adhesives along with mechanical fasteners can promote warpage but may help in a vibration environment. Dry film epoxy adhesives are preferred over liquids as the bond line thickness and squeeze-out is easy to control. Bonding temperatures should be as low as possible to minimize warpage.

b) *Film Type Adhesives* – Sheet adhesive is die or mechanically cut to fit the outline of the heatsink. The associated cure cycles and warpage of the heatsink/printed board assembly are problems that affect producibility. See 4.2.3 for film type adhesives.

c) *Liquid Adhesives* – Liquid adhesive is a producibility concern because of the difficulty in application, associated cure cycle and warpage of the heatsink/board assembly. The recommended structural adhesives listed in 4.2.2 are well suited for the heatsink bonding application.

Specification of adhesive thickness involves a trade-off between contact area (bond line) and producibility. Bond line may be reduced by process variables (e.g., surface finish or cleanliness), material warpage, and surface protrusions (especially surface runs of 2 oz. copper). More adhesive may improve contact, but excess can flow from under the heatsink and contaminate lands and PTHs. In many cases, a 75% (of the heatsink) bond is sufficient, but care should be taken to avoid moisture or flux entrapment that cannot be cleaned. Adhesive bonding will raise the vibration natural frequency of the printed board assembly above that which can be obtained by mechanical fasteners alone. Heat transfer may also be improved when adhesive bonding is used.

Table 7-3 Printed Board Heatsink Assembly Preferences

Method	Major Advantages	Major Disadvantages	Considerations
Rivets	Fastest, no cure cycle or adhesive application	Board area and holes needed for rivets	Use standard rivet sizes
Screws	Allows disassembly	Requires washers and nuts, board area and holes	Use standard hardware
Film Adhesive	No wasted space, potentially improved heat transfer, higher vibration natural frequency. Increased insulation	Cure time and possible warpage	Low cure temperature will minimize warpage
Liquid Adhesive	No wasted space, potentially improved heat transfer, higher vibration natural frequency	Producibility concern as well as cure time and warpage concern	Low cure temperature will minimize warpage

7.2.5 Special Design Considerations for SMT Printed Board Heatsinks Surface mount heatsinks can dramatically affect the CTE of the surface mount assembly. The reliability of surface mount component solder joints may be compromised if a high CTE material is used, but depends upon the service environment of the surface mount assembly. Laboratory environments which do not subject the surface mount assembly to significant temperature changes may allow heatsink materials such as 1100 series aluminum to be used. Most environments require the use of low CTE heatsink materials to provide long solder joint life.

Heatsinks used in surface mount applications are either built within the printed board (typically copper-Invar-copper layers laminated in the printed board) or are a solid plate that has a surface mount printed board bonded to one or both sides.

Bonding of the heatsink to two printed boards requires a compliant sheet adhesive to decouple the difference in CTE of the heatsink and printed board and serve as a vibration damping and heat transfer material. A solid sheet adhesive provides an inspectable material that allows the assembler to check for pin holes that might allow electrical connection between the heatsink and the printed board. Designing vias under a heat sink should be avoided. Most adhesive systems use pressure during the cure cycle which will allow the adhesive to (cold) flow away from the via. This can generate a short between the via and the heat sink.

Silicone sheet adhesives have been very effective in bonding printed boards to a solid heatsink. The bonding integrity of silicone sheet adhesives is dependent upon the proper application of a primer to the surfaces to be bonded. Care should be taken to prevent silicone contamination of surfaces which are to be soldered and/or conformal coated. See 4.2.2 for silicone sheet adhesives. To minimize warpage of the final bonded assembly, and thermal and mechanical stress on the assembled components during the adhesive cure process, a low temperature curing silicone adhesive should be chosen. Components

subject to damage should be so noted on the drawing and protection during assembly required. It may be necessary to assemble some components by hand after the bonding process is complete.

7.3 Heat Transfer Techniques

7.3.1 Coefficient of Thermal Expansion (CTE) Characteristics For applications with surface mount components, the CTE of the interconnecting structure becomes an important consideration. Table 7-4 establishes calculated reliability figures of merit related to the differences in the X and Y expansion characteristics of the component and the substrates, the distance from the solder joint to the neutral point (zero strain point), and the solder joint height. This factor is related to the total strain per cycle of the solder joint. It is important to minimize the relative differences in the CTE of the component and printed board assembly. Typical ceramic substrates have a CTE from 5 to 7 ppm/°C. Figure 7-2 provides examples of the CTE for some materials used by themselves (polyimide, glass or epoxy glass) and some constraining substrate materials used in conjunction with the printed board dielectric materials.

Table 7-4 Comparative Reliability Matrix Component Lead/Termination Attachment

Cyclic Services Environment [°C]	Design Life [Years]								
	5			10			20		
	Cyclic Frequency [Cycles/Day]								
	0.1	1	10	0.1	1	10	0.1	1	10
	Mean Cyclic Life Frequency [Cycles/Day]								
	183	1825	18,250	365	3650	36,500	730	7300	73,000
	Relative Reliability Index, R [ppm/°C]								
+20 to +40	2200	790	360	1600	580	270	1150	420	200
+20 to +80	670	240	110	490	170	79	350	130	58
-40 to +40[1]	600	230	110	440	170	83	330	130	62
-40 to 80[1]	370	140	65	270	100	48	200	75	36

(1) These environments straddle the transition region from stress-driven (<20 °C) to strain/creep-driven (>+20 °C); for such environments it has been shown that fatigue occurs significantly earlier by a mechanism different from that underlying this reliability matrix and it should be assumed that the R-values for these environments are optimistic.

7.3.2 Thermal Transfer Components, which for thermal reasons require extensive surface contact with the printed board or with a heatsink mounted on the printed board, **shall** be compatible with or protected from processing solutions at the conductive interface.

Some thermal transfer mediums **shall** be assembled in such a fashion as to not be damaged by subsequent assembly operations (i.e., thermal grease, boron nitride, may be damaged or removed by processing operations). Entrapment of processing solutions **shall** be avoided.

7.3.3 Thermal Matching A primary thermal concern with through-hole mounted glass components and with ceramic surface-mounted components is the thermal expansion mismatch between the component and the printed board. This mismatch may result in fractured solder joint interconnections if the assembly is subjected to thermal shock, thermal cycling, power cycling and high operating temperatures.

The number of fatigue cycles before solder joint failure is dependent on, but not limited to, the thermal expansion mismatch between the component and the printed board, the temperature excursion over which the assembly is expected to operate, the solder joint size, the size of the component, and the power cycling that may cause an undesirable thermal expansion mismatch if a significant temperature difference exists between the component and the printed board.

7.4 Thermal Design Reliability Design life can be verified through comparative testing intended to simulate the service environment. Table 7-4 represents an example of design verification of surface mounted devices for three service environments: 0.1 cycles per day, 1 cycle per day, and 10 cycles per day. The service environments shown represent four categories of different temperature ranges. The table establishes a relative reliability index (ppm/°C) for the design depending on a desired equipment life of 5, 10, or 20 years. This reliability index (R) is a factor that may be used in considering if the assembly will survive in the environment for the expected life.

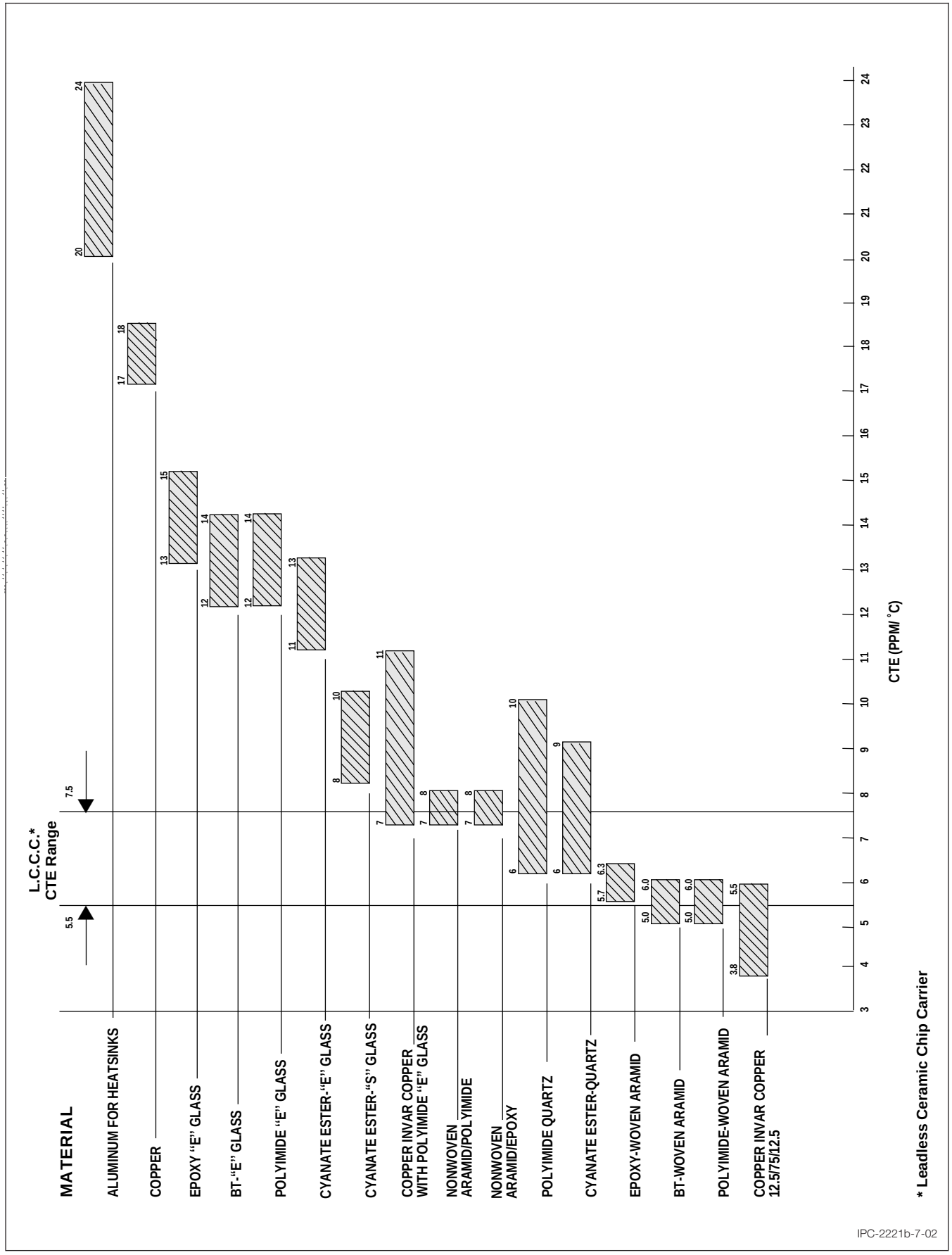


Figure 7-2 Relative Coefficient of Thermal Expansion (CTE) Comparison

$$R = \Delta\gamma/\Delta T \cong L_D\ \Delta\alpha/h[\ (ppm/°C)\ ]$$

where:

$\Delta\gamma$ = total solder joint strain (ppm)

ΔT = cyclic temperature swing (°C)

L_D = half the maximum distance between solder joint centers on any component, corner to corner or end to end (mm)
$\Delta\alpha$ = the absolute difference in coefficients of thermal expansion of substrate and component, (ppm/°C)

h = solder joint height (mm)

The longer the life or the more severe the requirements, the lower the number in the matrix becomes. A reliability index roughly gives the maximum cyclic strain that will result in a mean fatigue life just equal to the expected design life. The matrix is primarily meant for leadless components; for leaded components, some underlying relationships are different which, while not changing the indicated trends, will change the matrix quantitatively. Only mean cyclic life is represented, indicating when half the components are expected to fail, not when the first component in a system fails. The statistical distribution of the solder joint fatigue failure **shall** be included in a reliability assessment.

In the case of through-hole mounted glass components, it is often sufficient to provide stress-relief bends in the component's leads (see 8.1.14). With surface-mount components, the number of fatigue cycles can be increased by reducing the thermal expansion mismatch, reducing the temperature gradient, increasing the height of the solder joint, using the smallest physical size component wherever possible, and by optimizing the thermal path between the component and the printed board. For more detailed information, see IPC-D-279, IPC-SM-785 and IPC-9701.

8 COMPONENT AND ASSEMBLY ISSUES

The mounting and attachment of components play an important role in the design of a printed board. In addition to their obvious effect on component density and conductor routing, these aspects of printed board design also impact fabrication, assembly, solder joint integrity, repairability and testing. Therefore, it is important that the design reflects appropriate tradeoffs that recognize these and other significant manufacturing considerations and that special mounting configurations be detailed within the printed board documentation.

All components **shall** be selected so as to withstand the vibration, mechanical shock, humidity, temperature cycling, and other environmental conditions the design will be required to endure during installation and subsequently through its entire lifetime usage. The following are requirements the designer should consider and detail on the assembly drawing in specific notes or illustrations.

As a minimum, component mounting and attachment **shall** be based on the following considerations, as applicable:

- Electrical performance and electrical clearance requirements of the circuit design.
- Environmental end use requirements.
- Selection of active and passive electronic components and associated hardware.
- Size and weight.
- Minimizing of heat generation and heat dissipation problems.
- Manufacturing, processing and handling requirements.
- Contractual requirements.
- Serviceability requirements.
- Equipment usage and useful life.
- Automatic insertion and placement requirements, when these methods of assembly are to be used.
- Test methods to be employed before, during and after assembly.
- Field repair and maintenance considerations.
- Stress relief.
- Adhesive requirements.

8.1 General Placement Requirements

8.1.1 Automatic Assembly When automatic component insertion and attachment is employed, there are several board design parameters that **shall** be taken into account that are not applicable when manual assembly techniques are used.

8.1.1.1 Printed Board Size The size of the board to be automatically assembled can vary substantially. Therefore, manufacturers' equipment specifications should be evaluated with respect to the finished board requirements (see 5.3.3).

Standardization of automatic assembly operations can be achieved through standard fixtures that can accommodate a variety of board sizes or assembling boards in panel format. Using the panel assembly concept requires close cooperation with the board manufacturer in order to establish tooling concepts, tool hole location, board location, coupon and fiducial locations.

8.1.1.2 Mixed Assemblies Automatic processes used for both surface mounted and through-hole mounted components require special design considerations in order that the components assembled in the first phase of the assembly do not interfere with insertion heads during the second phase.

Component placement **shall** consider the stresses that are put on the board with insertion equipment by isolating parts wherever possible to specific areas such that the second phase insertion/placement stresses do not impact previously soldered connections.

8.1.1.3 Surface Mounting Automatic assembly considerations for surface mounted components include pick-and-place machines used to place/position chip components, discrete chip carriers, small outline packages, and flat packs.

Special orientation symbols should be incorporated into the design to allow for ease of inspection of the assembled surface mounted part. Techniques may include special symbols, or special land configurations to identify such characteristics as a lead of an integrated circuit package.

8.1.2 Component Placement Whenever possible, through-hole parts and components should be mounted on the side of the board opposite that which would be in contact with the solder, if the board is machine soldered.

Intermixing of through-hole and surface mount parts, or mounting parts on both sides of the board, requires complete understanding of the assembly and attachment processes (see IPC-CM-770 and IPC-SM-780).

Whenever possible, if their leads are dressed through the holes, axial and nonaxial-leaded components should be mounted per IPC-CM-770 on only one side of the board assembly.

Except when required in high frequency applications, stacking of components should not be permitted in initial design. Stacking involves the soldering of surface mount chip components on top or along side of each other. Stacking usually occurs when the existing design needs to be modified to incorporate additional components on the assembly and the printed board does not permit proper mounting of the device. Stacking should be documented on the assembly drawing. See IPC-HDBK-001 and IPC-7711/21 for additional information.

Component leads **shall** be surface mounted, mounted in through-holes, or mounted to terminals. Lead and wire terminations **shall** be soldered, wire bonded, crimped or compliant pinned.

The variations in the actual placement of the component's leads into PTHs or on the termination area in addition to the tolerances on the component's envelope (body and leads) will cause movement of the component body from the intended nominal mounting location. This misregistration **shall** be accounted for such that worst case placement of components **shall** not reduce their spacing to adjacent printed wiring or other conductive elements by more than the minimum required electrical spacing.

If a component is bonded to the surface of the printed board utilizing an adhesive (structural or thermally conductive), the placement of the component **shall** consider the area of adhesive coverage such that the adhesive may be applied without flowing onto or obscuring any of the terminal areas. Part attachment processes **shall** be specified which control the quantity and type of bonding material such that the parts are removable without damage to the printed board assembly. The adhesive used **shall** be compatible with both the printed board material, the component, and any other parts or materials in contact with the adhesive. For some adhesives, contact with adjacent components may not be acceptable. Contact on solder terminations or stress relief areas of adjacent components is another area that is dependent on the material.

Thermal concerns, functional partitioning, electrical concerns, packing density, pick-and-place machine limitations, wave soldering holder concerns, vibration concerns, part interference concerns, ease of manufacture and test, etc., all affect the parts placement.

Parts should be placed on a 0.5 mm [0.0197 in] placement grid whenever possible. When a 0.5 mm [0.0197 in] grid is not adequate, a 50 µm [1,968 µin] placement grid should be used. Certain parts (such as some relays) have leads that are not on standard grids but otherwise the parts should be placed so that the through holes are on grid. Some components, such as TO cans, have leads that are not on grid. In these cases, it is recommended to place the center of the part on grid.

If equipment or other constraints do not allow for a metric grid, parts may be on 2.54 mm [0.100 in] placement grid. When this is not adequate, a 1.27 mm [0.050 in] grid may be used or even a 0.64 mm [0.025 in] grid. The 2.54 mm [0.100 in] placement grid facilitates not only parts insertion but also standard bed-of-nails testing of the printed board and of the assembly. If bed-of-nails testing is to be used (including in-circuit printed board assembly testing), the test fixturing becomes much more difficult when components are placed off grid.

Figure 7-1 illustrates the producibility design allowances for automatic component insertion. Through-hole mount printed boards should observe component to edge of the board spacing constraints on two opposite edges to allow direct insertion into wave solder fingers. Other designs will require fixturing.

Both component heatsink considerations and board heatsink requirements **shall** be addressed in parts placement.

If the printed board assembly will not be tested with a bed-of-nails testing then the assembly grid will be limited only by the assembly machinery. If the printed board assembly is testable with a bed-of-nails scheme, a 2.54 mm [0.100 in] grid for PTH spacing is preferred. A 1.91 mm [0.075 in] grid allows greater design density and is not a concern with the assembly machinery but is a concern with bare printed board and completed assembly testing if a bed-of-nails testing approach is utilized. Bare printed board testing will normally be done at the printed board supplier and there presently is no cost penalty for off grid nor reduced grid printed board testing.

The designer should allow sufficient component to printed board edge separation for test and assembly processes. If this is not possible, the designer should consider adding a removable section of printed board (i.e., breakaway tab). The edge of the component is defined as the physical edge of the component on sides where no leads protrude from the component, and the edge of the surface land pattern for the leaded side of a component. Preferably, components should be a minimum of 1.5 mm [0.0591 in] from the edge of the printed board and printed board guide or mounting hardware to allow for component placement, soldering, and test fixturing.

Components should not be grouped in such a way that they shadow one another during soldering. Do not align rows of components perpendicular to the direction of travel; stagger them.

Component polarities should be oriented consistently (in the same direction) throughout a given design.

For wave soldered surface mount chip types, components should be bonded to the printed board prior to automated soldering with an adhesive specially formulated for the purpose.

Specific requirements for part mounting are functions of the type of component, the mounting technology selected for the printed board assembly, the lead bending requirements for the component, the lead stress relief method selected, and placement of the components (either mounted over surfaces without exposed circuitry, over protected surfaces, or over circuitry). Additional requirements are dependent upon the thermal requirements (the operating temperature environment, maximum junction temperature requirements, and the component's dissipated power), and the mechanical support requirements (based on the weight of the component).

Mounting methods for components of the printed board assembly **shall** be selected so that the final assembly meets applicable vibration, mechanical shock, humidity, and other environmental conditions. The components **shall** be mounted such that the operating temperature of the component does not reduce the component's life below required design limits. The selected component mounting technique **shall** ensure that the maximum allowable temperature of the printed board material is not exceeded under operating conditions.

8.1.3 Orientation Many components have leads that need to be oriented with specific lands of a land pattern, even though mechanical features of the design will allow for other orientations. The design **shall** ensure that the orientation or polarization of the component has been adequately specified, and coordinated with assembly equipment orientation requirements. Techniques may include special symbols, or special land configurations to identify such characteristics as a lead of an integrated circuit package (generally pin 1), positive lead of a capacitor or cathode lead of a diode.

Components should be mounted orthogonally to an edge of the printed board. They should also be mounted parallel or perpendicular to one another in order to present an orderly appearance. When appropriate, the component should be mounted in such a manner as to optimize the flow of cooling air.

Assemblies are usually flow soldered with the long axis parallel to the direction of travel through the wave, mounting flanges and hardware against the fixture or conveyor fingers, and edge connector last. Surface mount components should be placed to facilitate solder flow in the wave. Rectangular components (with solder caps at the ends) should be oriented with the long axis parallel to the leading edge of the printed board, perpendicular to the direction of travel. This avoids the ''shadow'' effect, where the body of the component would otherwise prevent free flow of solder to the trailing solder joint (see Figure 8-1).

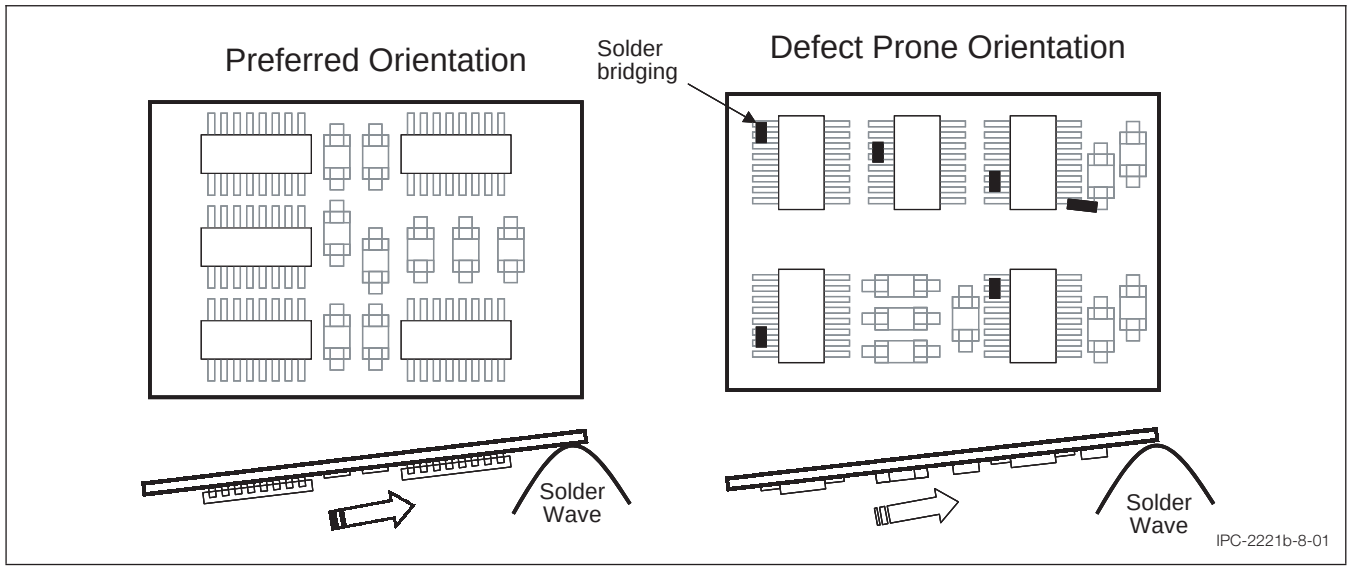


Figure 8-1 Component Orientation for Boundaries and/or Wave Solder Applications

8.1.4 Accessibility Electronic components **shall** be located and spaced so that the lands for each component are not obscured by any other component, or by any other permanently installed parts. Each component **shall** be capable of being removed from the assembly without having to remove any other component. These requirements do not apply to assemblies manufactured with no intent to repair (throw away assemblies) or as specified in 8.2.13.

8.1.5 Design Envelope The projection of the component, other than connectors on the printed board should not extend over the edge of the printed board or interfere with printed board mounting.

Unless otherwise detailed on the assembly drawing, the printed board edge is regarded as the extreme perimeter of the assembly, beyond which no portion of the component, other than connector, is allowed to extend. The designer **shall** prescribe the perimeter with due regard for maximum part body dimensions and the mounting provisions dictated by the printed board and assembly documentation.

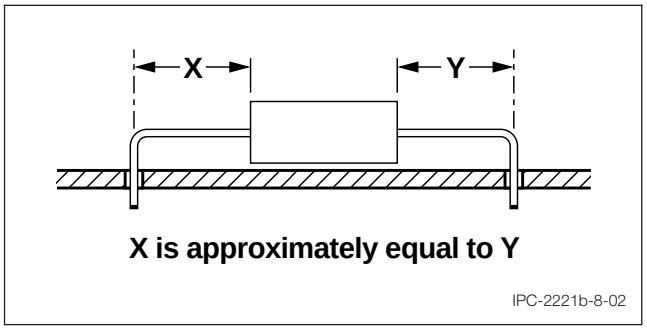


Figure 8-2 Component Body Centering

8.1.6 Component Body Centering Except as otherwise specified herein, the bodies (including end seals or welds) of horizontally mounted, axial leaded components should be approximately centered in the span between mounting holes, as shown in Figure 8-2.

8.1.7 Flush Mounting Over Conductive Areas Conductive areas, excluding soldered lands, under the parts **shall** be protected against moisture entrapment by one of the following methods:

- Application of conformal coating using material in accordance with IPC-CC-830 (usually specified on the assembly drawing)
- Application of cured resin coating by using low flow prepreg material
- Application of a permanent polymer coating (solder mask) using material in accordance with IPC-SM-840
- Other insulation (e.g., Kapton™ tape)

This requirement is applicable to components with or without sleeving (see Figure 8-3).

Metal-cased components **shall** be mounted so that they are insulated from adjacent electrically conductive elements. Insulation materials **shall** be compatible with the circuit and printed board material.

8.1.8 Clearances The minimum clearance between component leads or components with metal cases and any other conductive path **shall** be 0.13 mm [0.00512 in]. In general, uncoated conducting areas should provide for a clearance of approximately 0.75 mm [0.0295 in] as shown in Figure 8-4, but not less than the values shown in Table 6-1.

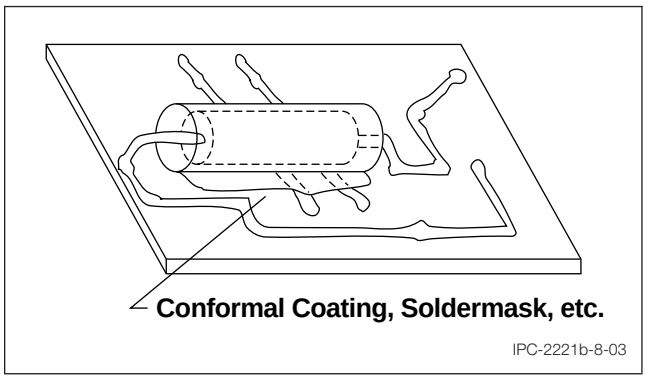


Figure 8-3 Axial-Leaded Component Mounted Over Conductors

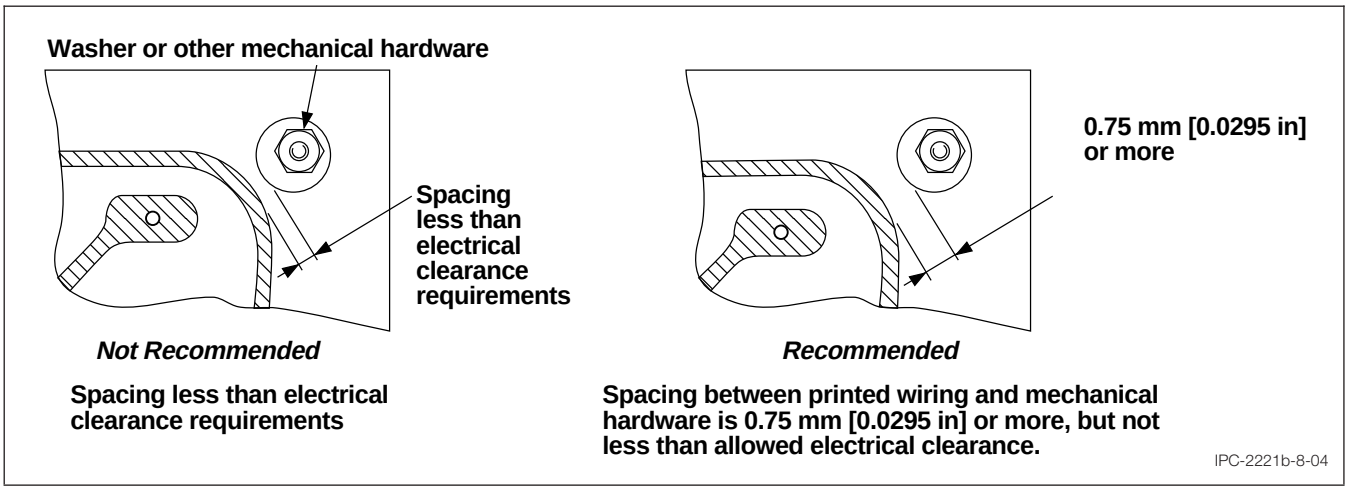


Figure 8-4 Uncoated Board Clearance

Parts and components **shall** be mounted such that they do not obstruct solder flow onto the topside termination areas of plated through-holes.

8.1.9 Physical Support Dependent upon weight and heat generation characteristics, components weighing less than 5 grams per lead which dissipate less than 1 watt, and are not clamped or otherwise supported **shall** be mounted with the component body in intimate contact with the printed board if practical, unless otherwise specified.

8.1.9.1 Component Mounting Techniques for Shock and Vibration The design stage should be such that axial-leaded components weighing less than 5 grams per lead **shall** be mounted with their bodies in intimate contact with the printed board. Dimensional criteria for lead bending and spacing **shall** be as specified in Figure 8-9. Axial-leaded components weighing 5 grams or more per lead should be secured to the printed board utilizing mounting clamps. If clamps are not practical due to density considerations, other techniques should be employed such that the solder connections are not the only means of mechanical support. These techniques are used for components weighing more than 5 grams when high vibration requirements apply (see 5.2.7 and Figure 8-5 and Figure 8-6).

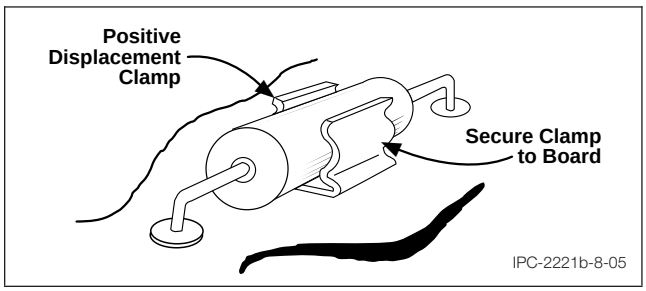


Figure 8-5 Clamp-Mounted Axial-Leaded Component

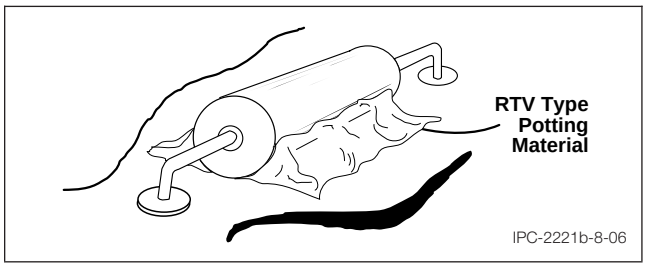


Figure 8-6 Adhesive-Bonded Axial-Leaded Component

When mounting chip components on edge, if the vertical dimension is greater than the thickness dimension, then chip components should not be used in assemblies subject to high vibration or shock loads. Vertical mounting **shall** be used for:

a) Low and tall profile SMDs with reflow termination pads located in a single base surface

b) Nonaxial-leaded devices with leads egressing from two or more sides of the device(s)

c) Nonaxial-leaded devices with leads egressing from a single base surface

For radial leaded components with three or more leads, such as transistors, that require the use of spacers between their base and the printed board surface for vertical mounting, special attention should be given to ensuring that there is no movement of the spacer during vibration that might cause damage to surface conductors.

8.1.9.1.1 Filleting Filleting, also called staking (particularly for NASA applications) is a significant method of securing components to printed boards in higher vibration environments, such as, launch conditions.

Typically, the requirement is to provide adhesive to both sides of a component, but not on the ends. A 1/4 to 1/8 of the height of the component minimum and 1/2 of the height maximum are common dimensional requirements.

Filleting is differentiated from bonding because the component is installed prior to the application of adhesive (see Figure 8-7). In bonding, the adhesive is applied first and the component is installed into the adhesive. Bonding provides better structural support, but because of processing is more expensive and not the method of choice. Bonding is more expensive because the adhesive application precedes a soldering operation. This means special handling.

The adhesive material used is dependant on a number of factors, such as, the weight of the part (epoxy for heavier parts), whether the component is glass (no epoxy) and how hot the component is (Silicones and some epoxies have good thermal conductivity.) Another common material is polyurethane.

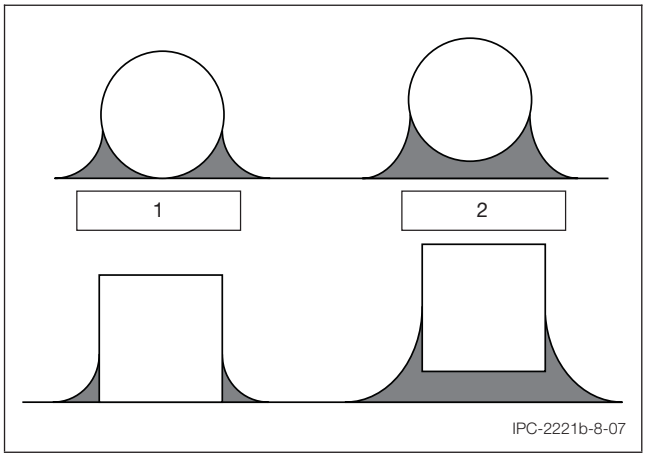


Figure 8-7 Example of Filleting Compared to Bonding
Note 1. Filleting.
Note 2. Bonding.

8.1.9.2 Class 3 High Reliability Applications Free standing components weighing more than 5.0 grams per lead **shall** be mounted with the base surface paralleling the surface of the printed board (see Figure 8-8). The component **shall** be supported on either:

- Feet or standoffs integral to the component body (see item A and B in Figure 8-8).
- Specially configured nonresilient footed standoff devices (see item C in Figure 8-8).
- Separate nonfooted standoffs which do not block plated through-holes nor conceal connections on the component side of the printed board.

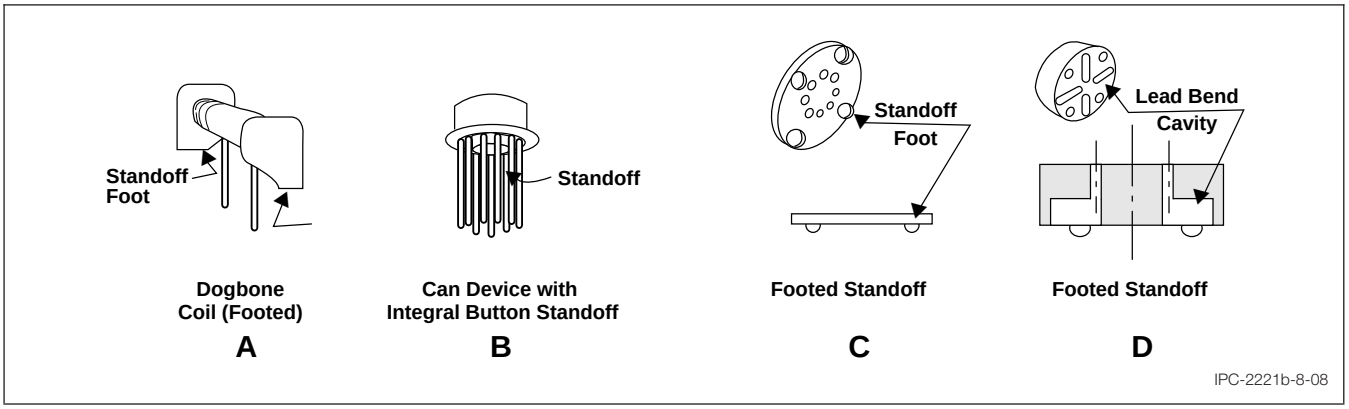


Figure 8-8 Mounting with Feet or Standoffs

Standoffs, footed or nonfooted, are intended to be mounted flush to the surface of the printed board. For this requirement, a button standoff as shown in item B of Figure 8-8 is considered a foot. Footed standoffs, as illustrated in items C and D in Figure 8-8, **shall** have a minimum foot height of 0.25 mm [0.00984 in].

When a separate footed standoff device or separate base nonfooted standoff is utilized and the component is mounted with the base surface paralleling the printed board surface, mounting should be such that the component base is seated in contact with, and flat to, the footed or nonfooted standoff. Mounting should also be such that the feet of the footed standoff maintain full contact with the printed board surface. No standoff **shall** be inverted, tilted, or canted, and should not be seated with any foot (or base surface) out of contact with the printed board or conductors thereon. Neither **shall** the component be tilted, canted nor separated from the mating surface of the resilient standoff device.

8.1.10 Heat Dissipation Design for heat dissipation of components **shall** insure that the maximum allowable temperature of the printed board material and the component is not exceeded under operating conditions. Heat dissipation may be accomplished by requiring a gap between printed board and component, using a clamp or thermal mounting plate, or attaching a compatible thermally-conductive material working in conjunction with a thermal bus plane to the component (see Figure 8-9 for examples).

Any heat dissipation technique or device **shall** permit appropriate cleaning to remove contaminants from the assembly. Conductive materials used to transfer heat between parts and heatsink **shall** be compatible with assembly and cleaning processes.

Components on Class 3 printed board assemblies which for thermal reasons require extensive surface contact with the printed board or with a heatsink mounted on the printed board, **shall** be protected from processing solutions at the conductive interface. To prevent risk of entrapment, compatible materials and methods **shall** be specified to seal the interface from entry of corrosive or conductive contaminants.

Note: Even completely nonmetallic interfaces that are prone to entrap fluids can have adverse effects on the fabricator's ability to pass required cleanliness tests.

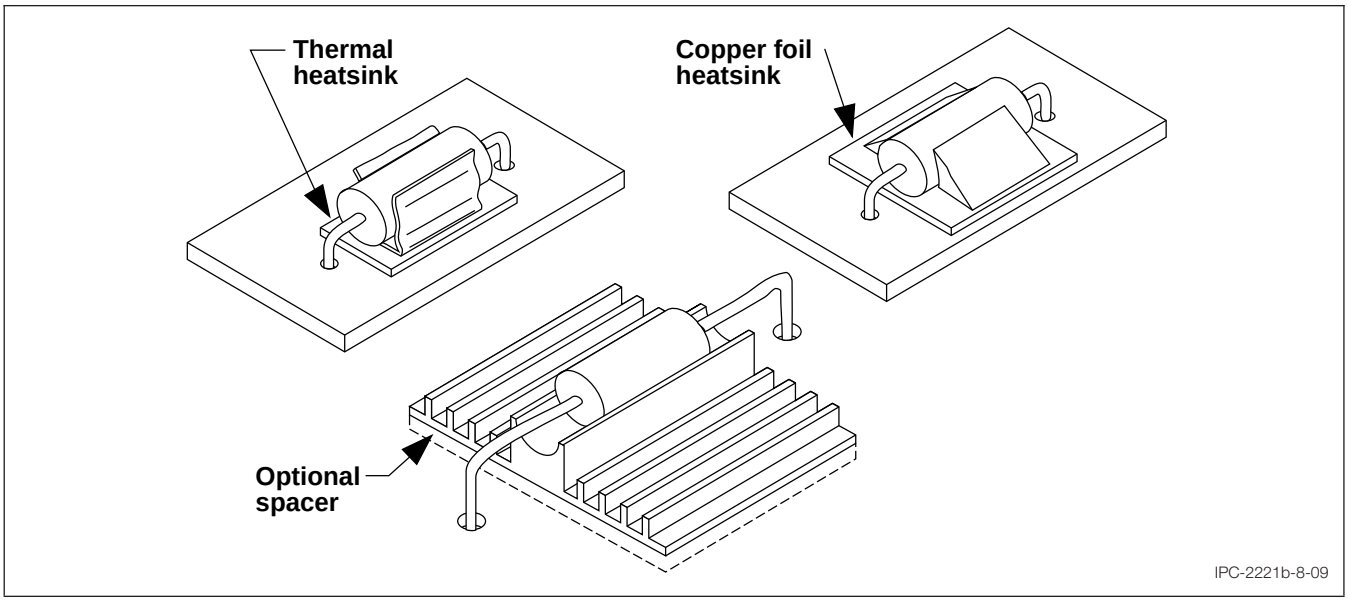


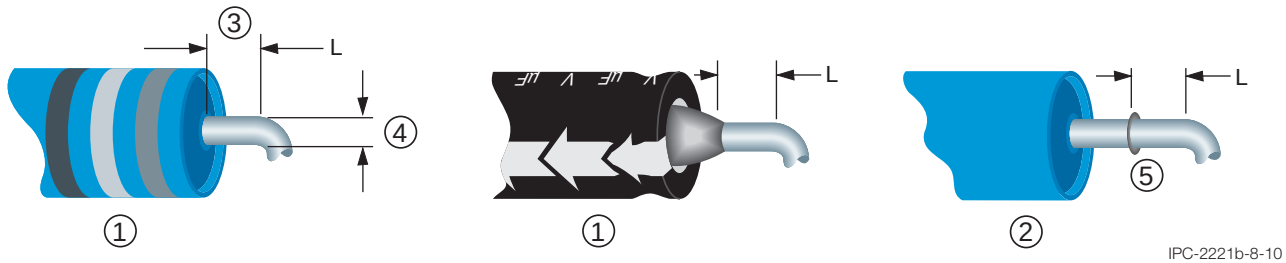
Figure 8-9 Heat Dissipation Examples

8.1.11 Stress Relief When designing for stress relief, lands and terminals **shall** be located by design so that components can be mounted or provided with stress relief bends in such a manner that the leads cannot overstress the part lead interface when subjected to the anticipated environments of temperature, vibration, and shock. Where the lead bend radius cannot be in accordance with Figure 8-10 in order to achieve design goals, the bends **shall** be detailed on the assembly drawing.

The leads of components mounted horizontally with their bodies in direct contact with the printed board **shall** be mounted with a method that ensures that stress relief is not reduced or negated by solder fill in the lead bends. Leads **shall** not be formed at the body of the component or between the body of a component and any lead weld. The lead **shall** extend straight from the body seal or lead weld before starting the bend radius as shown in Figure 8-10.

The requirements shown in Figures 8-10 and 8-11 should be implemented to prevent possible component damage, particularly glass-bodied parts. Lead bending equipment capability should be considered when selecting a lead configuration. The use of spacers under components not mounted directly in contact with the printed board is recommended.

DIPs mounted directly to heatsink frames, as described in section 8.1.10, may have special stress relief provisions included. The inclusion of a pliable spacer material between the heatsink frame and the printed board is an acceptable method for ensuring stress relief provided the resilient added material is of sufficient thickness (0.2 mm [0.0079 in] typical) to compensate for forces imposed during temperature change. Many of the pliable spacer materials tend to have low T_g and high CTE characteristics, imparting more stress than no spacer at all.



Lead Diameter	Minimum Bend Radius (R)
Less than to 0.08 mm [0.031 in]	1 diameter/thickness
From 0.8 to 1.2 mm [0.031 to 0.047 in]	1.5 diameters/thickness
Greater than 1.2 mm [0.047 in]	2 diameters/thickness

Figure 8-10 Lead Bends

Note 1. Standard bend
Note 2. Welded bend
Note 3. Straight for 1 diameter/lead thickness, but not less than 0.8 mm [0.031 in]
Note 4. Diameter/Thickness
Note 5. Weld
Note 6. The measurement shall be made from the end of the part (The end of the part is defined to include any coating meniscus, solder seal, solder or weld bead, or any other extension). The span for components mounted with a conventional lead form is 0.8 mm [0.031 in] minimum, and 33.0 mm [1.30 in] maximum.

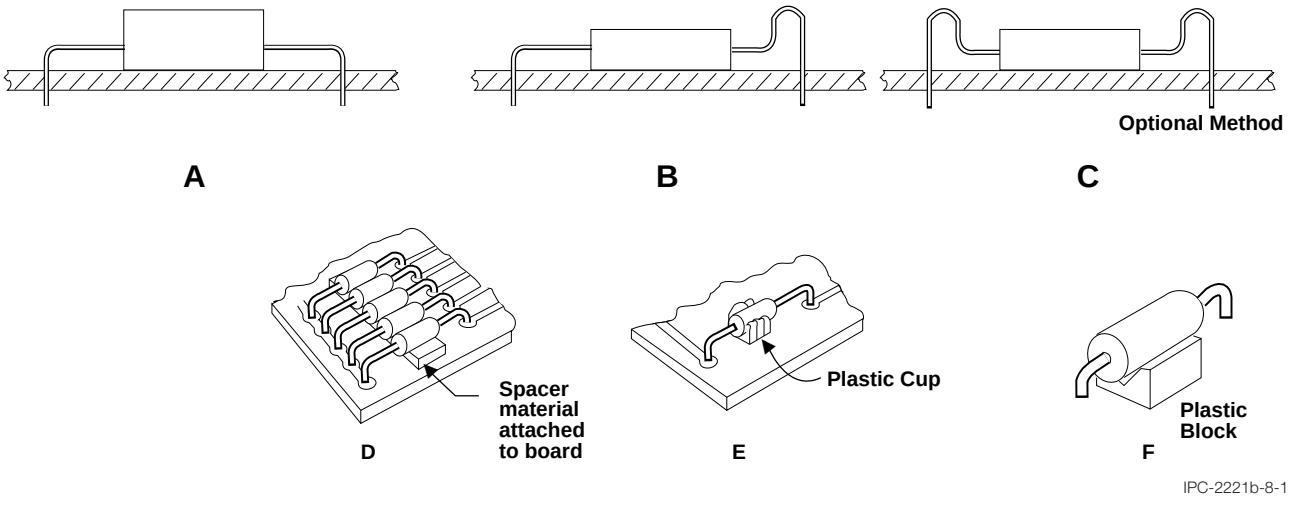


Figure 8-11 Typical Lead Configurations

8.2 General Attachment Requirements

8.2.1 Through-Hole For automatic assembly of printed boards with through-hole components, specific consideration should be given to providing the allowable clearances for the insertion and clinching of leads of the components. See Figure 7-1, 8.3.1 and IPC-CM-770 for specific details.

8.2.2 Surface Mounting Design restrictions **shall** maintain appropriate clearances for the automatic pick-and-place equipment to position the parts in their proper orientation and allow sufficient clearances for the placement heads (see IPC-SM-780). Clearances should be provided to allow for inspection of solder joints wherever possible (see IPC-7351).

8.2.3 Mixed Assemblies Design parameters for automatic processes used for both surface mounted and through-hole mounted components require special design considerations in order that the components assembled in the first phase of the assembly do not interfere with insertion heads during the second phase.

8.2.4 Soldering Considerations The designer **shall** ensure that components are capable of withstanding soldering temperatures used in the assembly process. Although the components are exposed to these temperatures for relatively short periods of time, due to the thermal capacity of the printed board assembly, component case temperatures remain near these temperatures for longer periods of time. Therefore, select components based upon the following typical process environments:

a) The wave soldering environment, e.g., 260 °C [500 °F] for one minute.

b) Surface mounted components in vapor phase environments, e.g., profile 216 °C [421 °F] for four minutes.

c) Surface mounted components in other processes, e.g., profile 225 °C [437 °F] for up to one minute.

The soldering temperatures noted above are for traditional lead bearing solders such as Sn63Pb37, etc. Higher temperatures apply when lead-free solders are used. Depending on the lead-free alloy involved, the temperature can exceed the 260 °C [500 °F] limit noted in IPC-J-STD-020 and/or IPC-J-STD-075.

When design restrictions mandate mounting components incapable of withstanding soldering temperatures, such components **shall** be mounted and hand-soldered to the assembly as a separate operation or **shall** be processed using a selective soldering technology.

Surface mounted components mounted to the bottom surface of assemblies intended to be wave soldered **shall** be capable of resisting immersion in 260 °C [500 °F] molten solder for five seconds. In addition, preheat is limited due to sensitivity of the underlying printed board substrate, so up to 120 °C [248 °F] of thermal shock can be expected when components enter the solder wave.

The reliability of completed solder connections depends primarily on the quantity and location of solder paste deposited on the printed board. Solder paste is deposited using various methods, such as with the use of a stencil for surface mount components. The size, geometry and location of stencil openings and the type and thickness of the stencil are important parameters that should be carefully chosen to provide sufficient and correctly placed solder paste that when reflowed, is capable of forming solder connections conforming to IPC-J-STD-001 and IPC-A-610 acceptance criteria. Designers should consult IPC-7525 for guidance on recommended stencil design criteria.

8.2.4.1 Thermal Stress Methodologies The procurement documentation **shall** specify the thermal stress test method to be used. During the selection process, the user should take into consideration the following when determining the appropriate thermal stress test method:

• Wave solder, selective solder, hand solder assembly processes

• Conventional (eutectic) reflow processes

• Lead-free reflow processes

Thermal stress methodology is required for structural integrity conformance test routines (microsection testing). As such, the choice of method is usually considered with respect to soldering survivability simulation. IPC-TM-650, Method 2.6.8, is more appropriate for THT, but not necessarily microvias, and IPC-TM-650, Method 2.6.27, is more appropriate for printed boards predominately using SMT and microvias. However, one should note that convection reflow simulation is often used as preconditioning prior to printed board reliability testing. In cases where thermal cycling or thermal shock is required as a predictor of reliability, one should note that the well accepted default six cycles of IPC-TM-650, Method 2.6.27, significantly decreases the expected cycles to failure; sometimes by more than half. Because this is generally considered appropriate acceleration, and because large proprietary databases of such data exist (e.g., the IPC-PCQR^2 Database), one should be highly cognizant of the performance expectations. A design activity may find it very useful to define a maximum number of soldering cycles for a product, and therefore limit the damage to the printed board. It could be assumed that this maximum number would carry through the quality assurance program and thereby limit the thermal stress cycles both for lot conformance and reliability testing. This concept may be exceptionally important in industry segments for which product validation/certification closely scrutinizes design for reliability.

IPC-TM-650, Method 2.6.8, is a solder float test for ten seconds. This is the heritage default test method utilized to mimic a wave solder or hand solder dwell of heat and solder on a PTH intended for leaded components. Due to test simplicity it evolved into an assessment of thermal impact on via structures as well. The 2.6.8 method has three Test Conditions, A, B, and C at 288 ± 5 °C [550 ± 9 °F], 260 ± 5 °C [500 ± 9 °F] and 232 ± 5 °C [450 ± 9 °F] respectively. Test Condition A is the default and most commonly used. The optional use of multiple floats and/or an alternate condition is AABUS. Assembly designs intended to go through wave solder once for assembly, followed perhaps by hand soldering for rework or touch up of solder joints, are well suited for this test method. Typically this test is applied only once, however in recent years some users have required it be repeated up to four times to account for initial soldering and an assurance that some life is left for rework or field repair. This heritage test method has proven successful for many years but has been found to not match the thermal impact experienced in surface mount reflow processes very well. This holds especially true for lead-free process temperatures.

IPC-TM-650, Method 2.6.27, was developed specifically to mimic reflow solder profiles. Today many assemblies that are reflowed are required to go through multiple solder processes for complete assembly. It is not uncommon to reflow a printed board assembly twice, once for each side, and then follow up with a selective hand or machine solder of a connector area. If BGAs (or any component) are on the assembly and require rework or replacement, then an additional two thermal reflow cycles (one to remove and a second to replace) are necessary in addition to the initial assembly.

Some printed boards have been shown to survive twelve or more solder float cycles of IPC-TM-650, Method 2.6.8, but fail after lead-free processing. This was a driver for the development of IPC-TM-650, Method 2.6.27, which would have shown failure after three lead-free reflow cycles. As such the IPC-TM-650, Method 2.6.27, solder reflow test is considered more severe than the solder float test. For printed board assemblies requiring only tin-lead solder, the heritage IPC-TM-650, Method 2.6.8, should provide a low cost test that will allow more freedom on laminate selection to survive this less difficult test. The long history of this test has proven it to still be acceptable for tin-lead wave solder applications. For assemblies that will see reflow, or a mix of reflow and wave (or select) solder operations, IPC-TM-650, Method 2.6.27, should be used since it is a more robust test. Test failures may indicate that higher temperature laminate systems may be required in order to assure reliability. The printed board designer should refer to laminate properties in the applicable data sheets for information on optional thermal testing properties, such as values for decomposition temperature (Td), T260, T288 and T300, for laminate selection. Implementing IPC-TM-650, Method 2.6.27, on legacy designs without material consideration may introduce compliance difficulty and have an adverse impact on yields. Microvias are typically very robust and are better evaluated by the more robust reflow test method than the heritage solder float test method. When complex via structures are used to provide interconnects for high density routing, the reflow method is critical to assess assembly thermal impact on useable life.

IPC-TM-650, Method 2.6.27, was developed with more than one solder reflow to be considered. The default number of assembly cycles is six passes through reflow. Repeating the solder reflow up to six times has been found to be necessary to assure that sufficient life is left in the printed board assembly to survive any future rework or field repair effort. The type of solder (tin-lead, or lead-free) and the number of times each test is applied **shall** be determined from the assembly processes that will be used. Tailoring the number of cycles or combinations of test is recommended as to not induce false indicators on less complex assemblies. The test temperature(s) established in IPC-TM-650, Method 2.6.27, mimic the solder alloy types employed in the assembly process. When specified within procurement documentation, test condition 230 °C Reflow Profile or 260 °C Reflow Profile **shall** be specified to properly identify this method. The AQL is identical between both methods and applied equally in performance specifications such as the IPC-6010 performance series.

See IPC-9631 for additional guidance on the implementation of IPC-TM-650, Method 2.6.27.

8.2.5 Connectors and Interconnects One of the major advantages of using printed board assemblies, as opposed to other types of component mounting and interconnection methods, is their ability to provide ease of maintainability. Devices (connectors) have been developed to provide the desired mechanical/electrical interface between the printed board assemblies, or between a printed board assembly and discrete interconnection wiring.

Printed board size and weight are important factors in choosing connector mounting hardware, and in deciding whether the printed board will be mounted horizontally or vertically. It is common practice to mount a connector either to a motherboard or to printed board racks or frames, and then insert the component printed board into the connector using appropriate guiding and support mechanisms. In general, if the assembly is to encounter a great deal of vibration, the printed board should be attached to a connector or supported by mechanical means other than relying on contact friction to provide the mechanical interface.

Connectors may be mounted to the printed board by soldering, welding, crimping, press fitting or other means. Leads may be extended through holes or contact may be made to lands provided on the printed board. Holes may be plated through or simply drilled. The exact method will depend on the connector design.

Interface connectors (i.e., a connector that is used to mate the printed board into its next-higher assembly), or otherwise for mating on the printed board, **shall** be provided with a means of keying. This keying can including keying of the printed board using notches or other means, keying of the connector, or otherwise keying of the printed board mounting bracket hardware.

8.2.5.1 One-Part Connectors One part connectors provide the female receptacle for communication between the printed board with an edge printed board connector and its environment.

If low signal levels, or frequent mating, or adverse environmental conditions are anticipated, the contacts should be gold plated. Whenever it is possible to install a connector on the printed board two different ways, or install a connector on the wrong printed board, a key **shall** be provided in the contact field (see Figure 8-12).

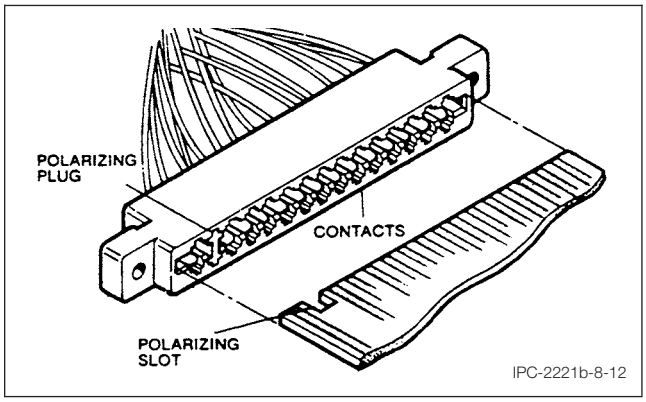


Figure 8-12 Typical Keying Arrangement

8.2.5.2 Dual In-line Connectors In-line printed board connectors may be mounted in full contact with the printed board. Connectors mounted in full contact with the printed board **shall** be designed so that there are both stress relief provisions internal to the connector body and cavities (either visible or hidden) which preclude blocking of plated through-holes.

8.2.5.3 Edge Printed Board Connectors Edge printed board connectors use one edge of the printed board as the plug dielectric with printed/plated conductors as the male contacts.

The width of the printed board edge (tang) that mates with the one-part connector (‘‘T’’ of Figure 8-13), **shall** be dimensioned in such a manner that when T reaches its maximum dimension (MMC), the size of the tang will be no greater than the minimum throat of the one-part connector. (See 5.4.3 for establishing connector circuit pattern.) In addition, it will be necessary to provide for special processing of the printed board tang to accommodate the mating of the printed boards edge contacts with the one-part connector in order to permit ease of mating and prevent undue wear or damage of the printed board. This consists of beveling (chamfering) the leading edge and corners of the printed board tang (see Figure 8-14). The uneven tang configurations shown in Figure 8-14 enable some connections to be made, or broken, before others. As an example, applying power before making signal connections.

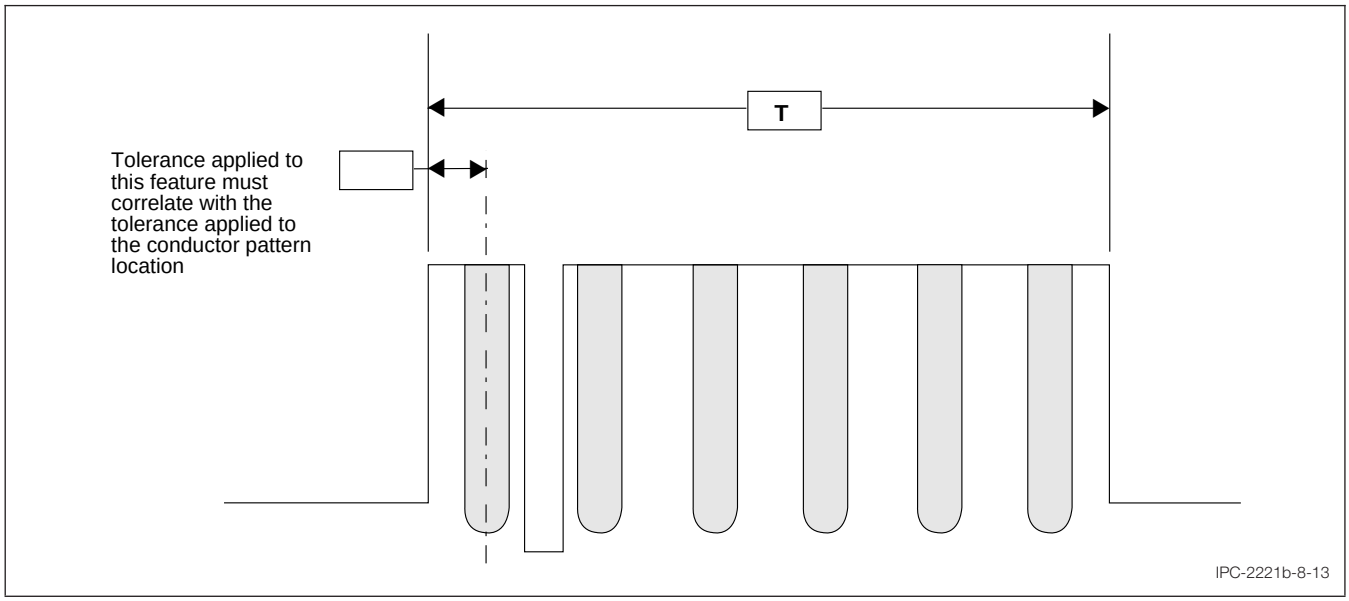


Figure 8-13 Printed Board Edge Tolerancing

Whenever it is possible to install a connector on the printed board two different ways, or install a connector on the wrong printed board, keying slots **shall** be cut into the printed board to be used with keying devices in the connector to ensure proper installation (see Figure 8-12).

If low signal levels, or frequent mating, or adverse environmental conditions are anticipated, the contacts should be gold-plated.

8.2.5.4 Two-Part Multiple Connectors Two-part multiple connectors consist of self-contained multiple contact plug and receptacle assemblies. Usually, although not always, the receptacle is an unmoveable connector assembly which mounts to an interconnection-wiring backplane (motherboard) or chassis (see Figure 8-15). Each connector half may have either male or female contacts. For safety, the receptacle usually contains female power contacts.

8.2.5.5 Two-Part Discrete-Contact Connectors Two-part discrete-contact connectors that consist of individual plug (male), and receptacle (female) contacts are mounted directly to the printed board, usually without being part of molded dielectric assemblies.

8.2.5.6 Edge Printed Board Adapter Connectors Edge printed board adapter connectors may be used in lieu of printed/plated conductors as the male contacts (see Figure 8-16). These connectors eliminate many of the problems associated with the edge printed board connectors, such as varying printed board thicknesses and printed board warping problems. Use of these connectors does not require special printed board processing, e.g., gold plating of contacts or tang chamfer on the printed board.

The mounting method **shall** be capable of withstanding the forces of repeated connector mating and withdrawal.

When one part of the connector is mounted to a printed board backplane using press-fit technology, the backplane should be designed in accordance with the guidelines of IPC-D-422.

8.2.6 Fastening Hardware The installed location and installation orientation for fastening hardware **shall** be prescribed on the assembly drawing for such devices as rivets, machine screws, washers, inserts, nuts and bracketry. Specifications and precautions of tightening torques **shall** be provided wherever general assembly practice might be inadequate or detrimental to the assembly's structure or functioning. The use of such hardware **shall** be in accordance with the clearance requirements of this section.

8.2.7 Stiffeners Stiffeners are designed into the printed board to provide rigidity to the assembly and prevent flexing of the circuitry which could cause solder and copper foil cracking during mechanical stress.

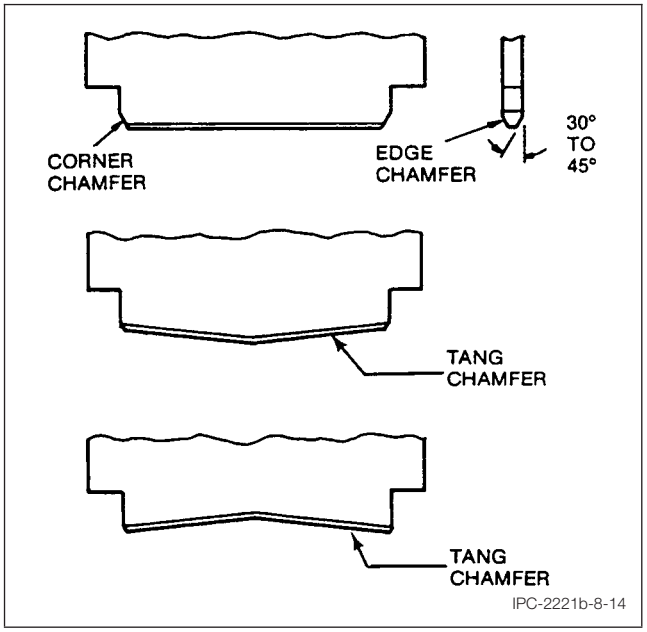


Figure 8-14 Lead-In Chamfer Configuration

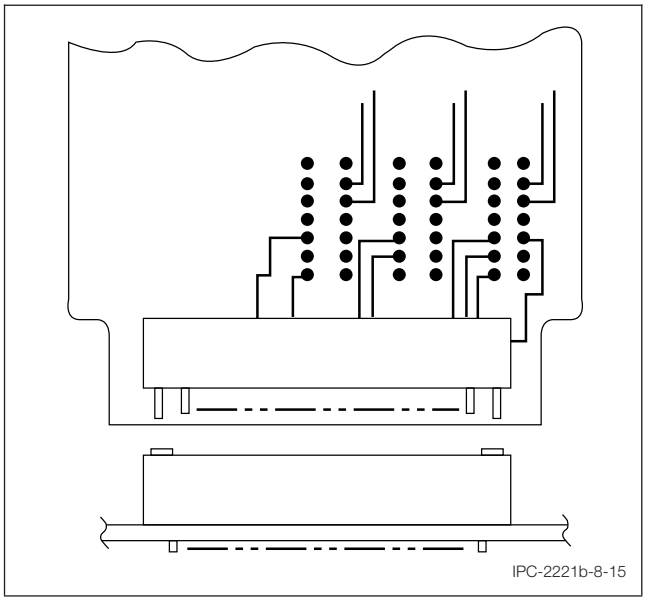


Figure 8-15 Two-Part Connector

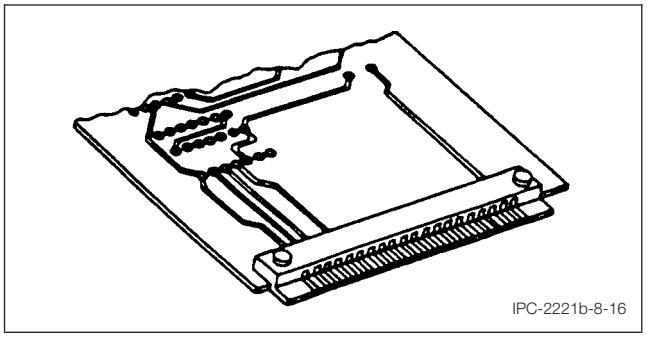


Figure 8-16 Edge-Board Adapter Connector

Stiffeners may be fabricated from aluminum, steel with adequate protective finish, plastic or fiber reinforced material. Stiffeners may be attached to the printed board with solder or by fasteners (rivets, nuts and bolts). If the stiffener is soldered using flow solder process, the printed board typically is required to be held flat by flow solder fixtures.

Adequate physical and electrical clearance should be provided between stiffeners, conductors, and components. Fiber or plastic insulators should be incorporated where adequate clearance from circuitry cannot be provided.

During the fabrication process of large printed boards, a physical bow and/or twist of the printed board occasionally occurs. The magnitude of these phenomena can normally be controlled by balancing the metal planes in multilayer printed boards, and adhering to proven fabrication processes. However, cases have been experienced whereby large unsupported printed boards may warrant special stiffening to reduce the degree of bow particularly during flow solder assembly process.

The following is to be used as a general design guide for establishing the mechanical characteristics of the subject stiffening member(s):

$$E = \frac{E^1 h^3}{I} \frac{W_o\,(a + 5)}{300Z}$$

where:

E = Young's modulus of stiffener material (lb./inch^2)
I = Moment of inertia (lb. inch^2)
E^1 = Flexural modulus of elasticity of the printed board base material (lb./inch^2)
h = Thickness of the printed board (inch)
W_o = Initial offset of the printed board, due to bow (inch)
a = Dimension of the printed board, in the direction of bow (inch)
Z = Allowable offset of the printed board after the stiffening member is added (inch)

Provision for the addition of stiffening member(s) should be provided to otherwise unsupported printed boards (typically larger than 230 mm [9.055 in] as measured along the printed board connector side). To allow for proper engagement of the printed board connector, the stiffener should be adjacent to the printed board connector(s).

8.2.8 Lands for Flattened Round Leads The designer should provide specific land attachments for flattened round (coined) leads. These should provide seating so that the heel and the terminal relationship is in accordance with Figure 8-17. Lead and land size should be designed so that a minimum side overhang may occur. (Class 3 product allows for a manufacturing process allowance of up to 1/4 of the lead diameter to overhang.)

A manufacturing allowance for toe overhang is acceptable provided it does not violate the minimum designed conductor spacing. If flattened leads are used, the flattened thickness **shall not** be less than 40% of the original diameter (see J-STD-001).

8.2.9 Solder Terminals Single-/double-ended, or single-/multisectioned turret solder terminals may be used to facilitate the installation of components, jumper wires, input/output wiring, etc. The wires or leads of components **shall** be soldered to the posts of the solder terminals.

Eyelets and solder terminals should be considered components and specified on the assembly drawing or a subassembly drawing for printed board fabrication.

8.2.9.1 Terminal Mounting-Mechanical Solder terminals that are not connected to conductive patterns or copper planes **shall** be of the rolled flange configuration (see item A in Figure 8-18).

8.2.9.2 Terminal Mounting-Electrical For printed boards or printed board assemblies, solder terminals **shall** be of the flange configuration shown in item B of Figure 8-18. The terminal **shall** be approximately perpendicular to the printed board surface and may be free to rotate.

Flat body flanges **shall** be seated to the base material of the printed board and not on ground planes or lands. Flared flanges **shall** be formed to an included angle between 35° and 120° and **shall** extend between 0.4 mm [0.016 in] and 1.5 mm [0.0591 in] beyond the surface of the land provided minimal electrical spacing requirements are maintained (see item B of Figure 8-18) and the flare diameter does not exceed the diameter of the land.

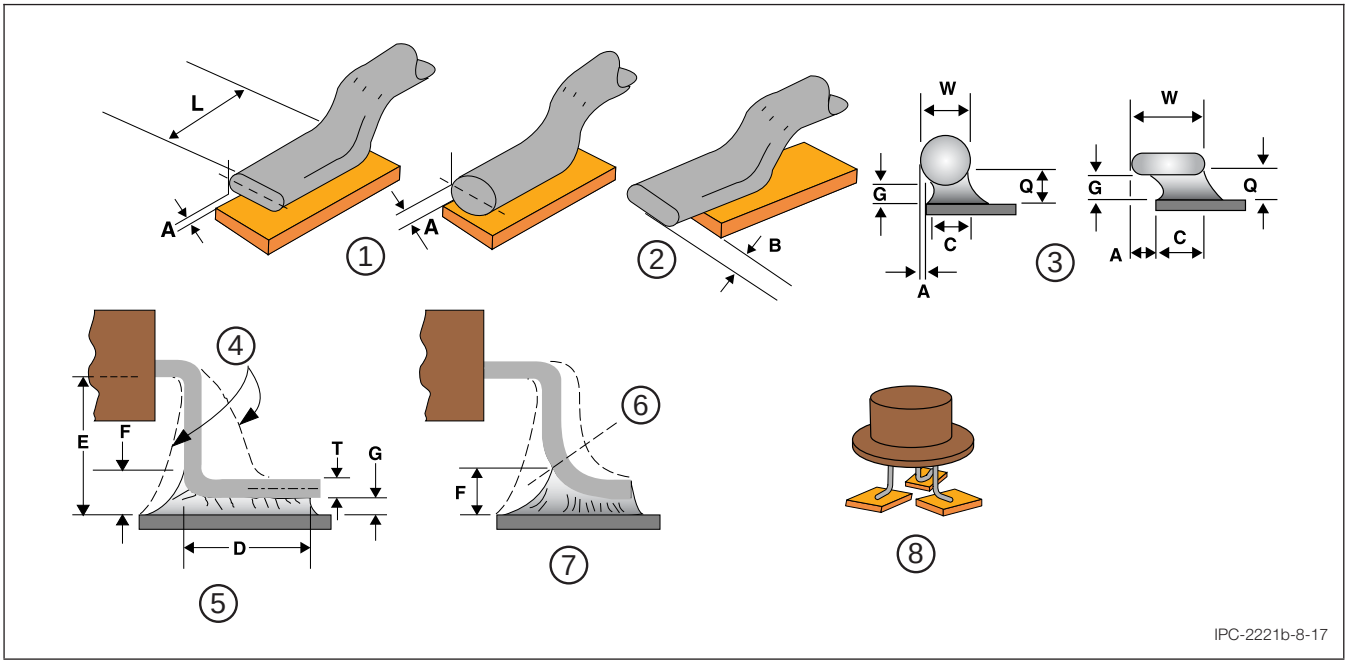


Figure 8-17 Round or Flattened (Coined) Lead Joint Description

Note 1. Side overhang
Note 2. Toe overhang
Note 3. End joint width
Note 4. Solder fillet may extend through the top bend. Solder does not touch package body or end seal, except for plastic SOIC or SOT devices. Solder should not extend under the body of surface mount components whose leads are made of Alloy 42 or similar metals.
Note 5. Side joint length
Note 6. Line bisecting lower bend
Note 7. Toe down heel fillet height
Note 8. Other land configurations
Note 9. A = Maximum Side Overhang; B = Maximum Toe Overhang; C = Maximum End Joint Width; D = Minimum Side Joint Length; E = Maximum Heel Fillet Height; F = Minimum Heel Fillet Height; G = Solder Thickness; L = Formed Foot Length; Q = Minimum Solder Joint Height; T = Thickness of Lead at Joint Site (over land); W = Flattened Lead Width or Diameter of Round Lead

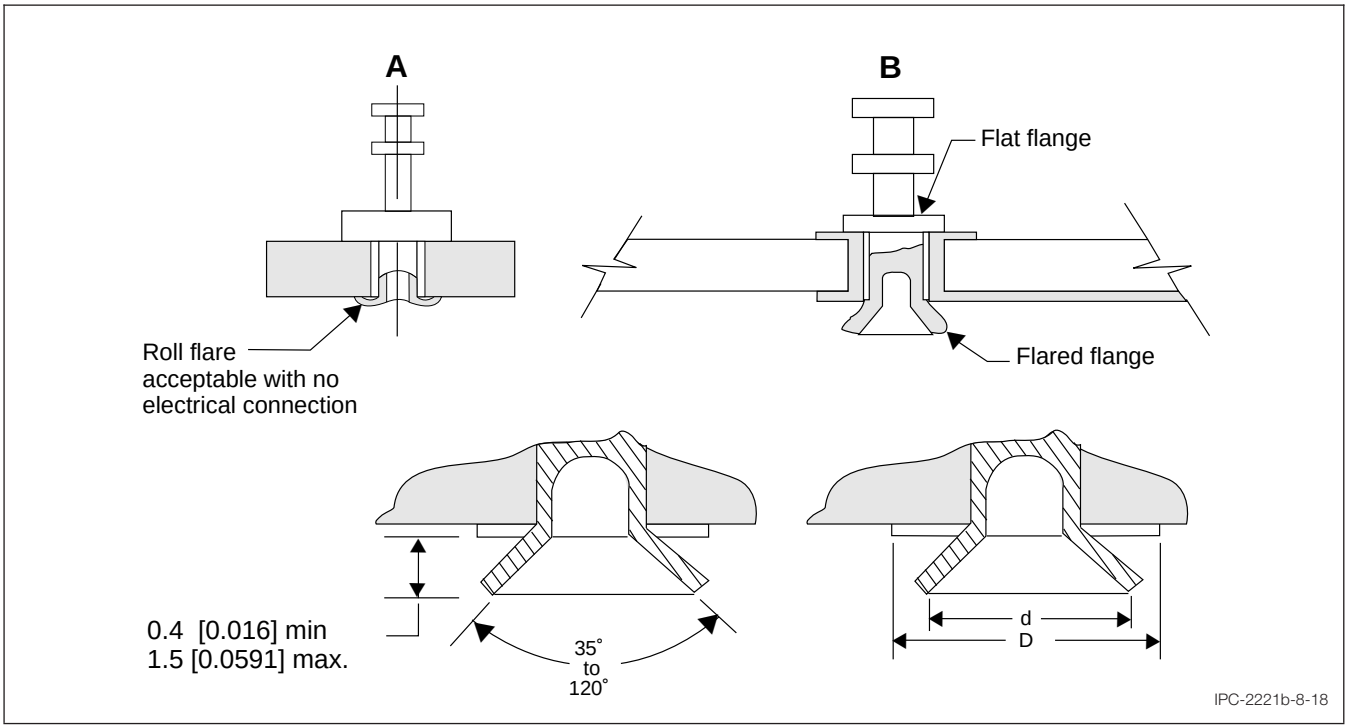


Figure 8-18 Standoff Terminal Mounting, mm [in]

Terminals should only be mounted in unsupported holes or in PTHs in Type 2 printed boards with a nonfunctional land on the component side (see item B of Figure 8-18). If it is essential that a terminal be utilized for interfacial connection, on Type 3 through Type 6 (inclusive) printed boards, a dual hole configuration incorporating a supported plated-through hole **shall** be combined with the terminal hole interconnected by a land on the solder side of the printed board (see Figure 8-19).

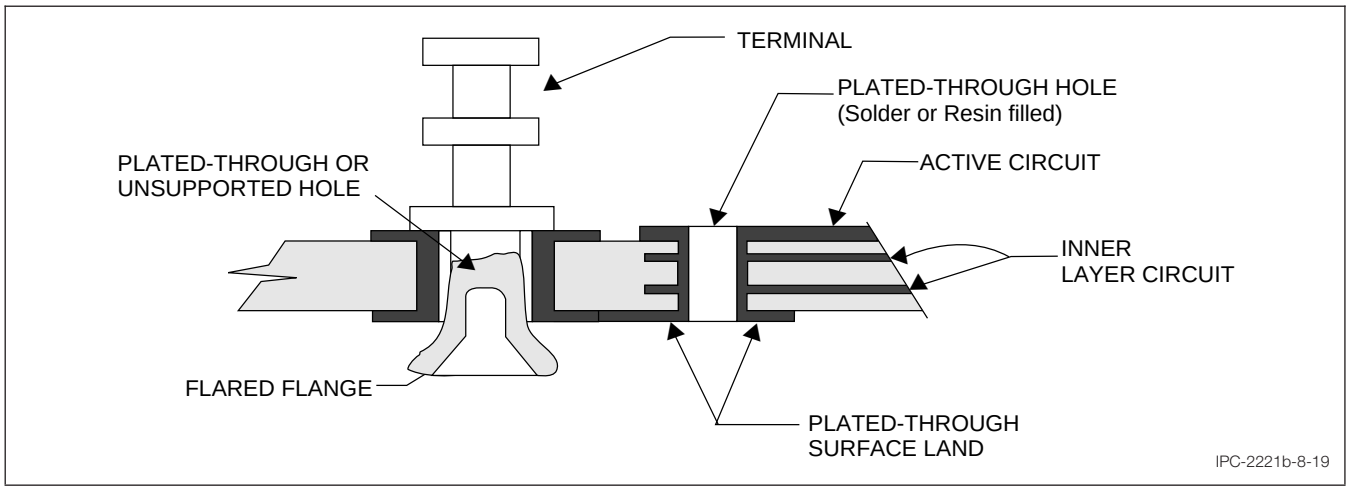


Figure 8-19 Dual Hole Configuration for Interfacial and Interlayer Terminal Mountings

8.2.9.3 Attachment of Wires/Leads to Terminals In cases in which more than one wire is attached to a terminal, the largest diameter wire should be mounted to the bottom-most post for ease of rework and repair. No more than three attachments should be made to each section of a turret of bifurcated terminal. As an exception, bus bar terminals (see sectional standards for more information) may hold more than three wires or leads per section when specifically designed to hold more.

8.2.10 Eyelets The requirements for the use of eyelets on printed boards are similar to those for solder terminals. The criteria for their use should be provided by the assembly drawing.

Interfacial connections **shall not** be made with eyelets. Eyelets installed at an electrically functional land **shall** be of the funnel flange type.

8.2.11 Special Wiring

8.2.11.1 Jumper Wires It may be necessary to include point-to-point wiring to a printed board as a part of the original design. Such wiring **shall not** be considered as being part of the printed board, but as part of the printed board assembly process, and considered as components. Therefore, their use **shall** be documented on the printed board assembly drawing.

Jumper wires **shall** be terminated in holes, on lands or standoffs. Jumper wires **shall not** be applied over or under other replaceable components (including uninsulated jumper wires).

Jumper wires **shall** be permanently fixed to the printed board at intervals not to exceed 25 mm [0.984 in]. Jumper wires less than 25 mm [0.984 in] length whose path does not pass over conductive areas and does not violate the spacing requirements may be uninsulated. Insulation, when required on jumper wires, **shall** be compatible with the use of any conformal coatings. When using nonsealed wire insulation, consider the assembly cleaning process.

8.2.11.2 Types Point-to-point (jumper) wires are usually of the following types:

- Bare bus wire that consists of a single strand of wire that is of sufficient cross-section to be compatible with the electrical requirements of the circuit without the use of sleeving or other insulation
- Sleeved bus wire that consists of a single-strand of bare buswire (see above) that is covered by insulation tubing.
- Insulated bus wire that consists of a single-strand wire purchased with its own insulation, such as varnish coating
- Insulated stranded wire that consists of multiple strands of wire purchased with an insulating material, such as a polymer coating

8.2.11.3 Application Designs using jumper wires **shall** adhere to the following rules:

- Bare bus wires should not be longer than 25 mm [0.984 in].

• Bare bus wires **shall not** cross over printed board conductors

• Bend radii for jumper wires should conform to that of normal component bend requirements (see 8.1.11)

• The shortest X-Y path of jumper routing should be used unless printed board design considerations dictate otherwise

Sleeving **shall** be of sufficient length to ensure that its slippage at either end of the jumper wire will not result in a gap between the insulation and solder connection or wire bend that violates minimum electrical clearance distances. Also, the sleeving chosen **shall** be able to withstand the jumper wire or printed board soldering operations.

8.2.12 Heat Shrinkable Devices Heat shrink soldering devices are typically used to terminate shields on cables. The devices are composed of a solder ring enclosed in a solder sleeve insulator. The device is placed over the terminations to be soldered and heated with a hot air device. The heat melts the solder to form a joint and simultaneously encases the connection in insulation. Heat shrinkable devices may be self-sealing and may encapsulate the entire solder connection.

Solder sleeves compose a unique category because they form a portion of the design, yet are not integral to the printed board.

8.2.13 Bus Bar Bus bars are usually in the form of preformed components that are part of the printed board assembly and serve the function of providing most, if not all, of the power and ground distribution over the printed board surface. Their use is primarily to minimize the use of printed board circuitry for power and ground distribution and/or to provide a degree of power and ground distribution not cost-effectively provided by the printed board.

The number of conductor levels in the bus bar, the type and number of their terminals, the size and finish of their conductors, and the dielectric strength of their insulation depends on the application. However, these parameters should be clearly defined on the procurement document for these parts. Whenever possible, their interface with the printed board should be at PTHs, while conforming to conventional lead size-to-hole and lead bending requirements (see 8.1.11). Also, for optimum printed board design efficiency, the bus bar terminals should interface with the printed board on a uniform termination pattern, may share the same holes as an integrated circuit and may be placed under an integrated circuit.

8.2.14 Flexible Cable When the design includes flexible cable becoming part of a printed board, the terminations **shall** be accomplished in a manner that imposes no undue stress on the cable/printed board interconnection.

Sometimes this interconnection uses pins, where a pin passes through the printed board and the flexible cable to provide the proper interconnection. At other times, the flexible cable may be surface soldered directly to land patterns on the printed board or may be integral to the printed board as in rigid-flex applications. Proper mechanical support, using tie-down bars, or adhesives, **shall** be used to prevent stresses on the solder joints.

8.3 Through-Hole Requirements For automatic assembly of printed boards with components whose leads pass through the printed board, specific consideration should be given to providing the allowable clearances for the insertion and clinching of leads of the components. See 8.3.1 through 8.3.1.5 and IPC-CM-770 for specific details.

8.3.1 Leads Mounted in Through-Holes Part attachment **shall** be described on the assembly drawing following the methods specified herein. Requirements for lead-to-hole relationships are detailed in the related design sectional. Component leads, jumper wires and other leads **shall** be mounted such that there is only one lead in any one hole except as specified in 8.2.13. The recommended design for component leads in unsupported holes **shall** be such that they extend a minimum of 0.50 mm [0.0197 in] and a maximum of 1.5 mm [0.0591 in] from the surface of the plating or foil.Component leads in supported holes **shall**, as a minimum, be discernable in the completed solder connection. The lead should not extend more than 1.5 mm [0.0591 in] (measured vertically) from the printed board surface, and the lead **shall not** violate minimum electrical spacing requirements.

8.3.1.1 Straight Through-Hole Mounted Leads The straight-through leads on connectors or other devices with tempered leads may extend from 0.25 mm [0.00984 in] to 2.0 mm [0.0787 in], provided there is no electrical or mechanical interference.

8.3.1.2 Unclinched Leads Unclinched leads, straight or partially bent for retention **shall** be soldered in component holes or eyelets in accordance with J-STD-001 as applicable (see IPC-CM-770).

8.3.1.3 Clinched Leads When maximum mechanical retention of a lead or terminal is required by design, the lead or terminal **shall** be clinched. Component holes may be PTHs, unsupported holes, or eyeletted holes. Clinching requirements **shall** be defined on the assembly drawing. The lead end **shall not** extend beyond the edge of its land, or its electrically connected

conductor pattern, if it violates the minimum spacing requirements. Partial clinching of leads for part retention **shall** be considered under the requirements of 8.3.1.4 (see Figure 8-20). Clinched leads **shall not** be used for tempered pins or for leads over 1.3 mm [0.0512 in] in diameter.

Class 3 lead terminations in unsupported holes **shall** be clinched a minimum of 45°.

8.3.1.4 Partially Clinched Partially clinched leads are typically bent between 15° to 45° as measured from a vertical line perpendicular to the printed board. Partially clinched lead terminations **shall not** be used for manually inserted components except on diagonally opposite corner pins of dual in-line packages (DIPs) (see Figure 8-21).

8.3.1.5 Dual In-line Packages Leads on DIPs may be clinched in either direction for part retention. Clinch angle should be limited to 30° from the lead's original centerline. The clinch may be limited to two leads per side (four leads per part) (see Figure 8-21).

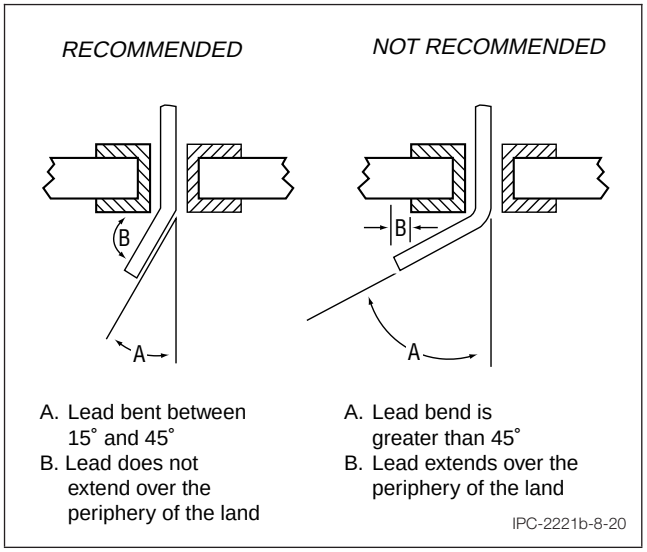


Figure 8-20 Partially Clinched Through-Hole Leads

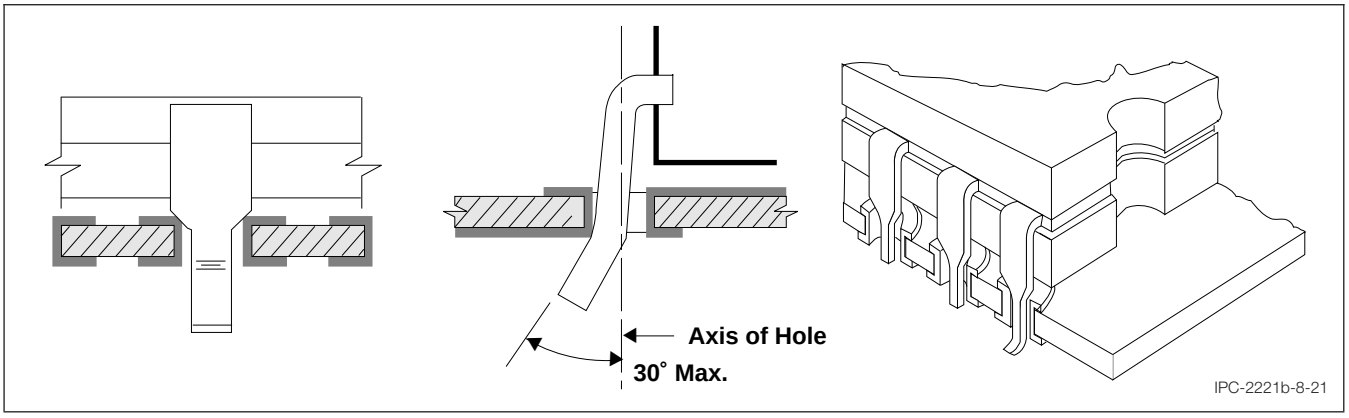


Figure 8-21 Dual In-Line Package (DIP) Lead Bends

Dual in-line packages may be surface mounted provided the leads are intended for surface mount applications. For applications in which severe thermal stress is evident and the printed board provides the thermal management function, butt mounted packages **shall not** be used.

8.3.1.6 Axial Leaded Components The design for axial leaded components should follow 8.1.11. Lead bends **shall** be stress relieved as identified in that general paragraph. See Figure 8-2 for component body centering and Figure 8-10 for lead bend extensions.

The leads of components mounted horizontally with bodies in direct contact with the printed board **shall** be formed to ensure that excess solder is not present in the formed bends of the component leads (see Figure 8-22). Solder may be present in the formed bends of axial-leaded components provided that it is a result of normal lead interface wetting action and that the topside bend radius is discernible. Solder **shall not** extend so that it contacts the component body (see J-STD-001).

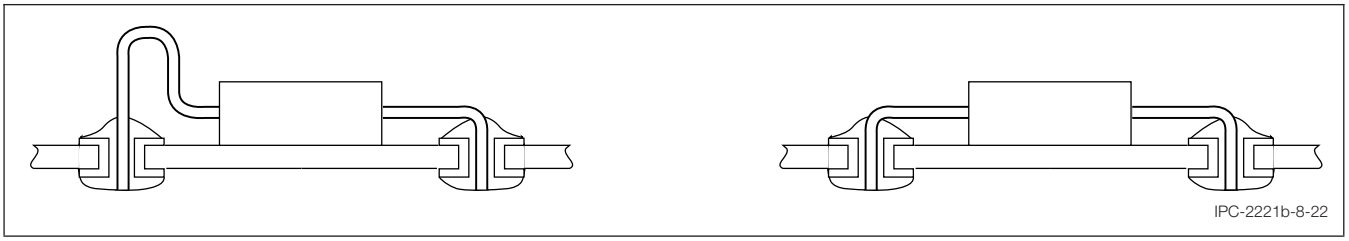


Figure 8-22 Solder in the Lead Bend Radius

8.3.1.7 Radial-Lead Components

a) *Radial-Lead Components (2 Leads)* – Radial-leaded components vary in lead spacing. The design lead spacing is generally a function of the spacing at which the leads exit the body of the component (see Figure 8-23) and the nearest grid intersection.

Dual-lead components of configurations A through E of Figure 8-23 should be mounted freestanding with the larger sides perpendicular to the printed board surface within 15° as shown in Figure 8-24 when:

Angularity is required for clearance in the next higher assembly; or

That edge of the body nearest the surface of the printed board parallels the printed board surface within 10° and is no less than 1.0 mm [0.0394 in] and no more than 2.3 mm [0.0906 in] from the surface. Components of configurations F through J of Figure 8-23 are not included under the angularity exception.

Radial-leaded components with coating meniscus on one or more leads should be mounted such that there is visible clearance between the meniscus and the solder fillet. Trimming of the meniscus is prohibited (see Figure 8-25).

b) *Radial-Leaded Components (3 or more Leads)* – Radial-leaded components with three or more leads vary in lead spacing. The design lead spacing is generally a function of the spacing at which the leads exit from the body of the component (see Figure 8-26) and the nearest pattern of grid intersections that provides for suitable conductor routing.

c) *Class 3 High Reliability Requirements* – For Class 3 high reliability applications, components **shall** be mounted freestanding (i.e., with the base surface separated from the surface of the printed board with no support other than the component leads) only if the weight of the component is 3.5 gm per lead or less. When components have an integral seating plane, the seating plane may be in contact with the printed board. When components are mounted freestanding, the spacing between the surface of the component and the surface of the printed board **shall** be a minimum of 0.25 mm [0.00984 in] and a maximum of 2.5 mm [0.0984 in].

In no instance **shall** nonparallelism result in nonconformance with the minimum or maximum spacing limit.

8.3.1.8 Perpendicular (Vertical) Mounting Axial-leaded components without support and weighing less than 14 grams may be mounted on the assembly using vertical mounting criteria that have the major axis of the component body perpendicular to the printed board surface (as shown in Figure 8-27). The space between the end of the component body (or lead weld) and the printed board should be between 0.8 - 1.5 mm [0.031 - 0.059 in] and should be specified on the assembly documentation. Height restriction for general component

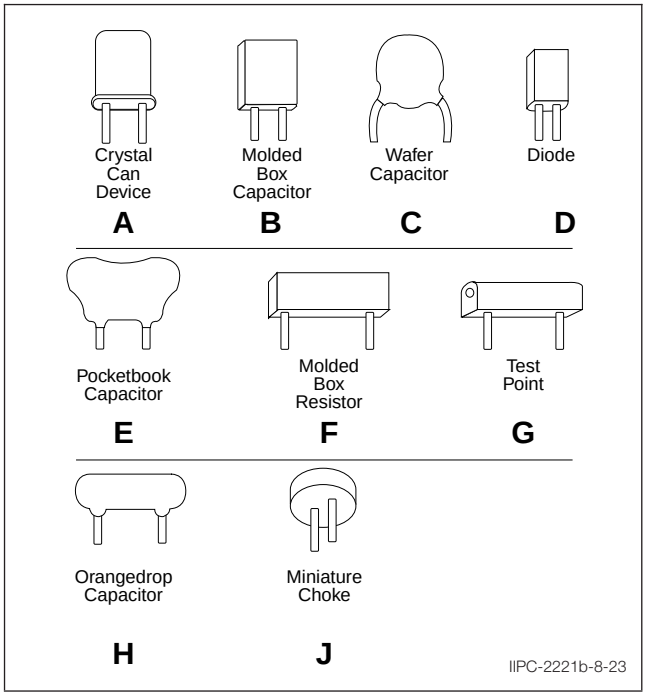


Figure 8-23 Two-Lead Radial-Leaded Components

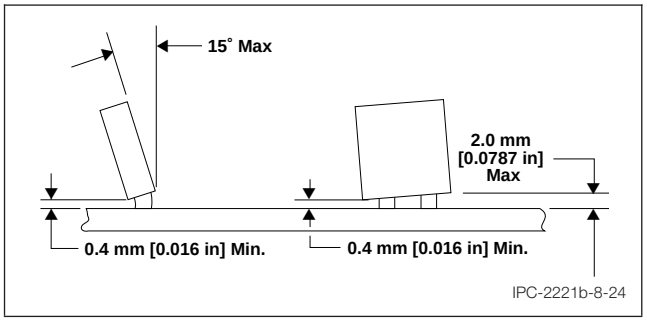


Figure 8-24 Radial Two-Lead Component Mounting, mm [in]

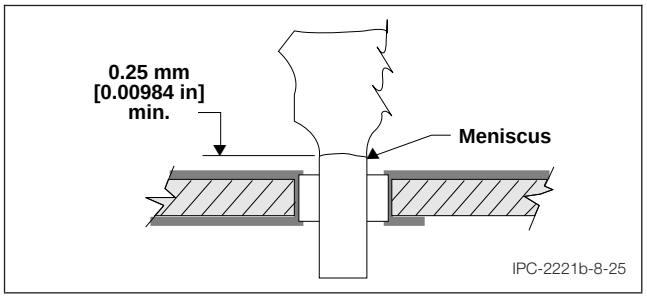


Figure 8-25 Meniscus Clearance, mm [in]

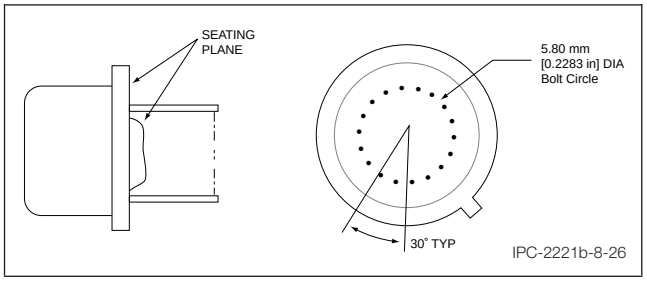


Figure 8-26 "TO" Can Radial-Leaded Component, mm [in]

mounting normally pertains to axial-leaded components mounted vertically. In general, the profile of components should be kept as low as possible to the surface of the printed board.

8.3.1.9 Flat-Packs Flat-pack components normally have flat ribbon leads that exit from the component body on 1.27 mm lead centers (see Figure 8-28). Forming of the leads may be required to prevent stressing the lead exit at the component body, especially for through-hole mounted applications (see Figure 8-29). An off-printed board clearance of 0.25 mm [0.00984 in] minimum is required for cleaning purposes.

The body of the component **shall not** be in contact with any vias unless the vias are coated per 8.1.10. Leads **shall** extend from the body of the part a minimum of one lead diameter or thickness but not less than 0.8 mm [0.0315 in] from the body or weld before the start of the bend radius (see Figure 8-10 and J-STD-001).

8.3.1.10 Metal Power Packages When the design includes metal power packages, they **shall not** be mounted free standing. Stiffeners, heatsinks, frames and spacers may be utilized to provide needed support.

Metal power packages with leads that are neither tempered nor greater than 1.25 mm [0.0492 in] (compliant leads) may be terminated in PTHs or with through-hole terminations. With through-hole terminations the leads **shall** be provided with stress relief (see Figure 8-30).

With plated-through hole terminations the package **shall** be mounted off the printed board and spacers used to provide stress relief for the leads (see Figure 8-31). Side mounting may also be employed.

Metal power packages with noncompliant leads may also be mounted with the leads terminated in PTHs or with through hole termination. The requirements for PTH terminations **shall** be the same as those for packages with compliant leads (see Figure 8-30). For through-hole terminations, the leads **shall** be terminated to the printed board by jumper connections (see Figure 8-32). The termination of the jumper to the printed board **shall** be made either to a plated-through hole or to a land.

Care should be exercised when the mounting utilizes spacers to ensure that any electrical connection between the component case and the printed board circuitry remains constant under all operating conditions.

Whenever the terminations are made in PTHs, the mounting **shall** ensure that the connections can be cleaned between the component and the printed board. Metal power packages, the standoffs, heatsink frames, and resilient spacers on which metal power packages are mounted **shall** be of configurations which do not block PTHs, preclude excessive stresses (provide stress relief), and facilitate cleaning.

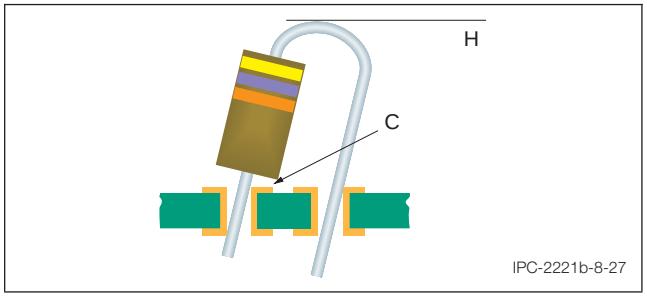


Figure 8-27 Perpendicular Part Mounting, mm [in]

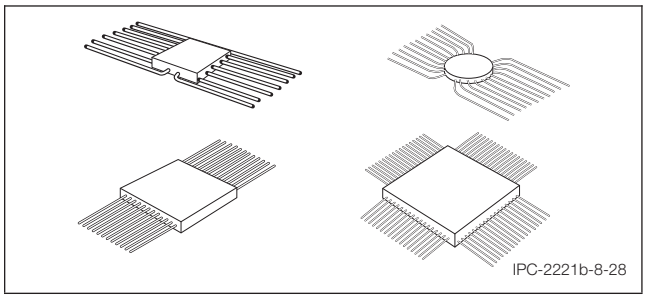


Figure 8-28 Flat-Packs and Quad Flat-Packs

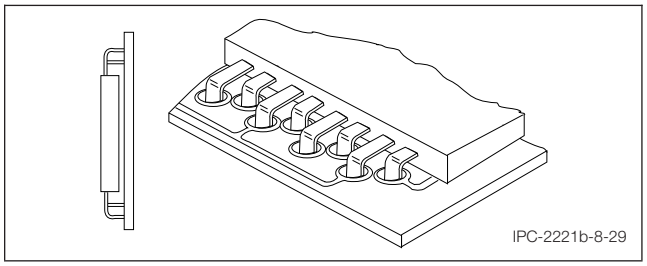


Figure 8-29 Examples of Configuration of Ribbon Leads for Through-Hole Mounted Flat-Packs

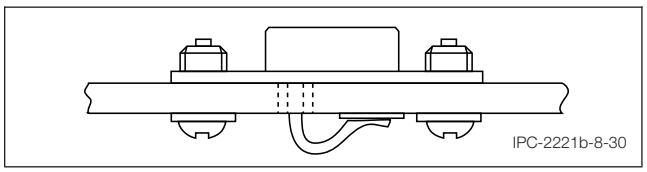


Figure 8-30 Metal Power Packages with Compliant Leads

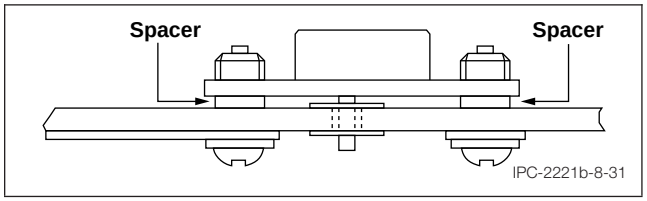


Figure 8-31 Metal Power Package with Resilient Spacers

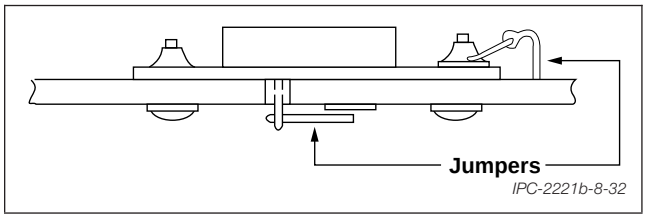


Figure 8-32 Metal Power Package with Noncompliant Leads

8.4 Standard Surface Mount Requirements Automatic assembly considerations for surface mounted components are driven by pick-and-place machines used to place/position chip components, discrete chip carriers, small outline packages, and flat packs. Printed board designs **shall** maintain appropriate clearances for the automatic pick-and-place equipment to position the parts in their proper orientation and allow sufficient clearances for the placement heads (see IPC-SM-780).

Typically, fine pitch devices could be between 250 and 775 mm^2 case size for automatic placement without vision. Generally, the largest component that can be placed with vision alignment is 1300 mm^2 [51.181 in^2], measured to the outside of the leads. Large packages exaggerate the effects of the thermal mismatch between the component and substrate. Normally, the minimum size leadless component that can be placed with automatic equipment is 1.5 mm [0.0591 in] nominal length by 0.75 mm [0.0295 in] nominal width. Smaller components require high placement accuracy. Vacuum pickup with standard equipment is also difficult.

Avoid extremely small passive components. Leadless passive components should have an aspect ratio greater than one and less than three. High aspect ratio parts tend to fracture during soldering. Square devices (aspect ratio = 1) are difficult to orient.

Smaller components are easier to solder, but footprints should be large enough to permit reliable placement of adhesive without smearing onto the conductor. Avoid components which require mounting land spacings (on the same component) closer than 0.75 mm [0.0295 in], due to process limitations on applying (chip bonding or thermal adhesive). High profile SMT components (higher than 2.5 mm [0.0984 in]) interfere with wave solder flow to adjacent components, and should be avoided.

Special orientation symbols should be incorporated into the design to allow for ease of inspection of the assembled surface mounted part. Techniques may include special symbols, or special land configurations to identify such characteristics as pin 1 of an integrated circuit package. Special orientation symbols **shall** be provided for Class 3 product.

Land pattern geometries should be designed in accordance with IPC-7351, which provides the appropriate size, shape and tolerance of surface mount land patterns to insure sufficient area for the appropriate solder fillet to meet the requirements of IPC-J-STD-001, and also to allow for inspection, testing and rework of those solder joints.

8.4.1 Surface-Mounted Leaded Components The requirements and considerations of 8.1.7 apply to the surface-mounting of leaded components. Lead forming is a major design consideration. Custom lead forms should be described on the assembly drawing to provide for lead stress relief to ensure fit to the land pattern to allow underbody clearance for cleaning, and to provide any designed-in provisions for thermal transfer (see Figure 8-33 and IPC-7351).

Axial leaded components may be surface mounted provided the leads are coined (see Figure 8-34). However, they **shall not** be surface mounted in a perpendicular orientation (see Figure 8-27).

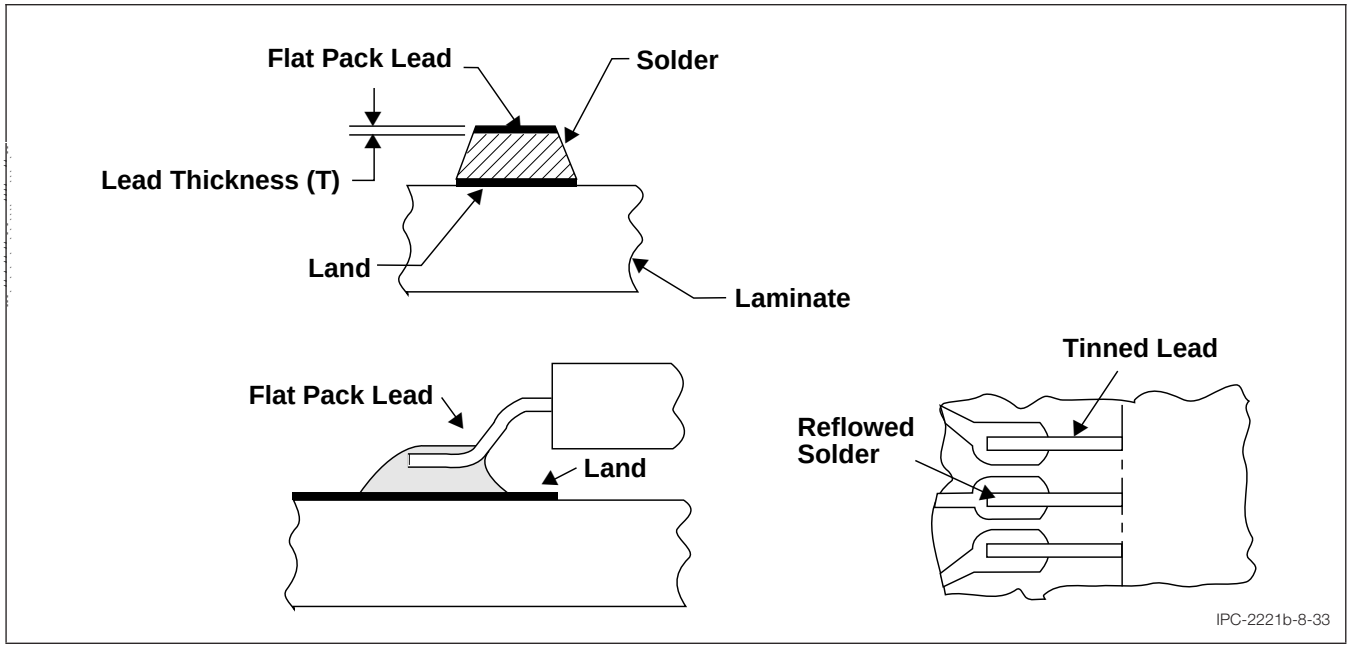


Figure 8-33 Examples of Flat-Pack Surface Mounting

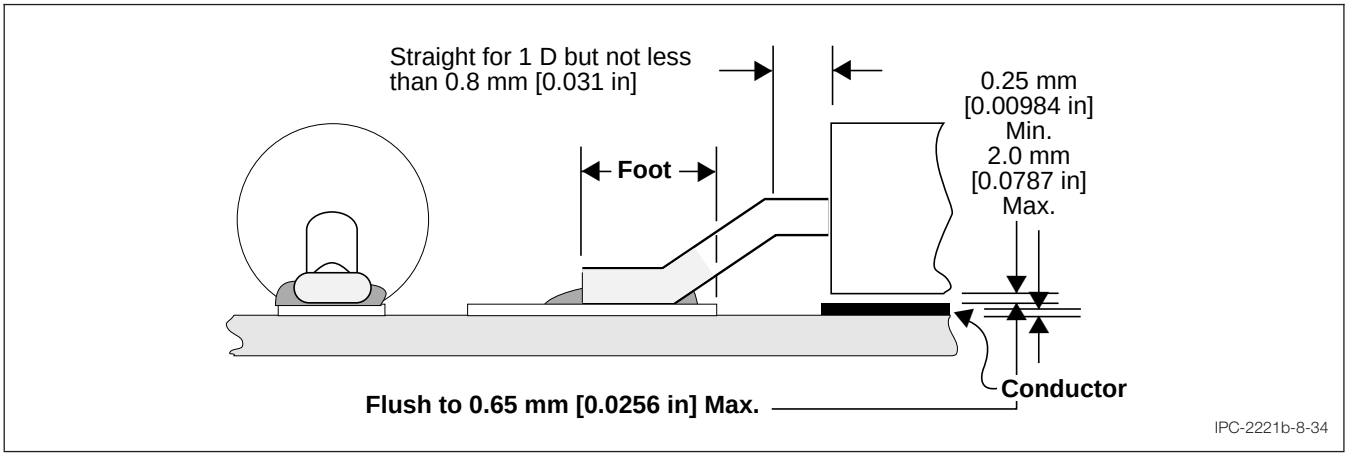


Figure 8-34 Round or Coined Lead

8.4.2 Flat-Pack Components Flat-pack components normally have flat ribbon leads that exit from the component body on 1.27 mm [0.05 in] lead centers (see Figure 8-35). Although they generally have from 14 to 16 leads, flat-packs with up to 50 leads are available.

When planar mounted flat-packs require lead forming, the leads **shall** be configured as shown in Figure 8-35. Non-insulated parts mounted over exposed circuitry **shall** have their leads formed to provide a minimum of 0.25 mm [0.00984 in] between the bottom of the component body and the exposed circuitry. The maximum clearance between the bottom of the leaded component body and the printed wiring surface should be 2.0 mm [0.0787 in]. Parts insulated from circuitry or over surfaces without exposed circuitry may be mounted flush. If the component requires thermal transfer to the printed board, special consideration for cleaning should be given.

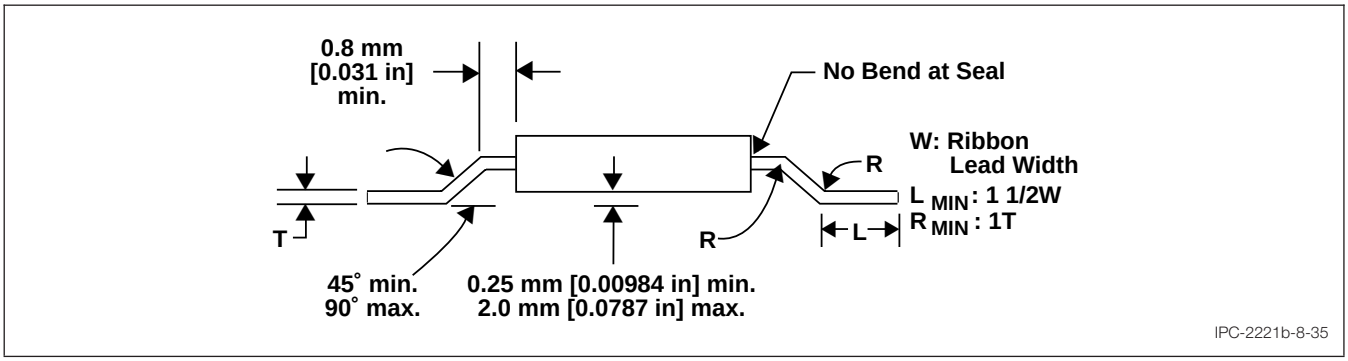


Figure 8-35 Configuration of Ribbon Leads for Planar Mounted Flat-Packs

8.4.3 Ribbon Lead Termination Flat-wire ribbon leads may be attached to lands on the printed board (see Figure 8-36). Connections **shall** be made by soldering or wire bonding only.

8.4.4 Round Lead Termination In some instances, components with round leads may be attached to the surface lands without first passing through a hole. The land **shall** be designed with the proper shape and spacing to comply with proper soldering techniques. Components with axial leads of round cross-section may be coined or flattened to provide positive mounting (see Figure 8-34).

8.4.5 Component Lead Sockets Normally, component lead sockets **shall not** be used for Class 3 product because of reliability concerns (spread contacts, extra circuit interconnects, intermittent circuits during shock or vibration environment, etc.). However, such sockets may be used when specified, or

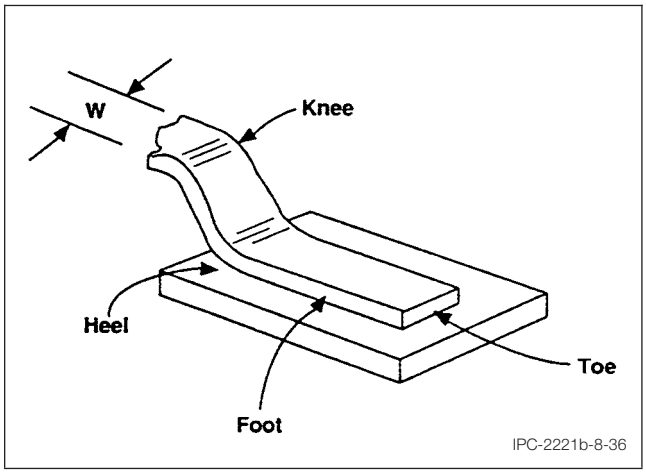


Figure 8-36 Heel Mounting Requirements

otherwise AABUS, when deemed acceptable by engineering analysis. Care should be taken in specifying the use of non-noble platings or finishes on either sockets or the component leads because of the possibility of producing inherent heat or open circuits due to fret corrosion during vibration or temperature cycling.

The socket contact material **shall** be chosen for compatibility with the component lead finish to preclude galvanic corrosion. Material combinations such as gold socket contacts with solder or tin/lead plated component leads may result in galvanic corrosion in a humid operating environment.

8.5 Fine Pitch SMT (Peripherals) Fine pitch surface mount peripherals typically encompass two or four sided gullwing leaded devices, including thin shrink small outline packages (TSSOP) and shrink quad flat packages (SQFP).

The TSSOP components are available in four different pitches: 0.30 mm, 0.40 mm, 0.50 mm, and 0.65 mm. They are typically specified by their two largest dimensions-the plastic body size (in the short dimension), and the nominal toe-to-toe length (in the long dimension). Their use has grown because their height (less than 1.6 mm) allows them to be used in memory card technology. In general, as the long dimension increases, the pitch decreases (see Figure 8-37).

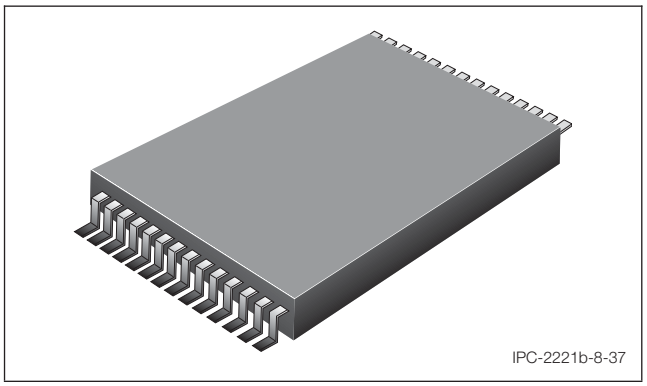


Figure 8-37 TSSOP Package Construction

The shrink quad flat pack (SQFP) has been developed for applications requiring low height and high density. The SQFP, along with the TSOP components, are frequently used in memory card applications. The square SQFP/QFP family has leads on a 0.80 mm, 0.65 mm, 0.63 mm, 0.50 mm, 0.40 mm, or 0.30 mm pitch. See Figure 8-38 for an example of SQFP construction.

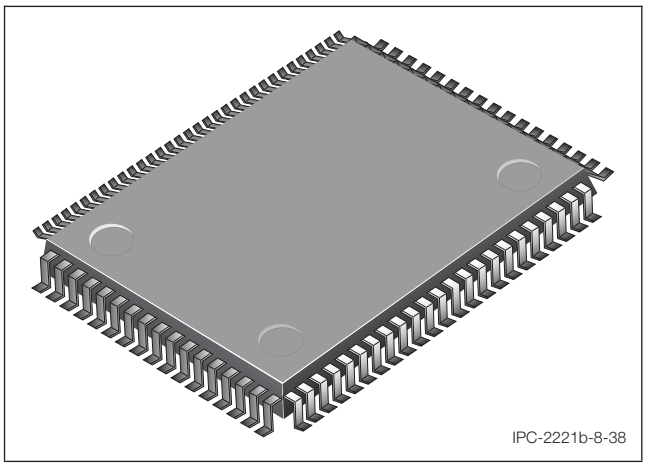


Figure 8-38 SQFP Package Construction

8.6 Bare Die

8.6.1 Wire Bond See IPC-MC-790.

8.6.2 Flip Chip See IPC-7094.

8.6.3 Chip Scale Chip scale packaging is, by definition, a package in which the area is no greater than 120% of the area of the die. Placement is frequently the rate limiting step, and the most expensive in the assembly process. The factors that contribute most significantly to the cost include:

- Throughput (number of placements/time)
- Vision system requirements
- Die presentation options
- Chip to substrate alignment accuracy
- Chip to substrate coplanarity requirements
- Additional required features such as supplying heat and pressure during assembly

For further discussion of chip scale packaging and placement, see IPC-7094.

8.7 Tape Automated Bonding See SMC-TR-001.

8.8 Grid Array SMT The area array device family includes square and rectangular package configurations and is furnished in a variety of base materials. This device family includes Ball Grid Array (BGA) parts (rigid, flexible or ceramic substrate); Fine Pitch Ball Grid Array (FBGA) parts (rigid or flexible substrate); Land Grid Array (LGA) parts; and Column Grid Array (CGA) parts (ceramic substrates).

Area array devices including BGA, FBGA, CGA, and LGA are typically attached to the host interface structure using eutectic or lead free solder alloy, however, optional methods of attachment may include electrically conductive epoxy or polymer.

There is also a process difference between the solder application for those terminations that collapse (solder balls) slightly during soldering and those terminations that do not collapse where a significant amount of additional solder paste is required.

Since the solder connections are under the component body, grid array SMT devices will require specialized equipment for inspection (X-ray) and component removal in case of rework (hot air station). Assemblers also need to characterize their reflow profile to minimize solder joint voiding (see IPC-7093 and IPC-7095).

In situations where large boards (> 250 x 250 mm [9.84 x 9.84 in]) are used with large BGAs (> 25 x 25 mm [0.984 x 0.984 in]), it may be a good idea to increase printed board thickness to at least 2.0 mm [0.079 in] to minimize board bending and flexing. This will reduce or eliminate interfacial failures due to mechanical stress that is caused by bending and flexing of the printed board.

Thicker boards require higher processing temperatures and/or dwell times. This can affect finish material choices at the board level, since board materials have temperature limits.

Figure 8-39 through Figure 8-41 illustrate examples of area array devices. For more information on these devices and their interface to the printed board, see IPC-7095 and IPC-7351.

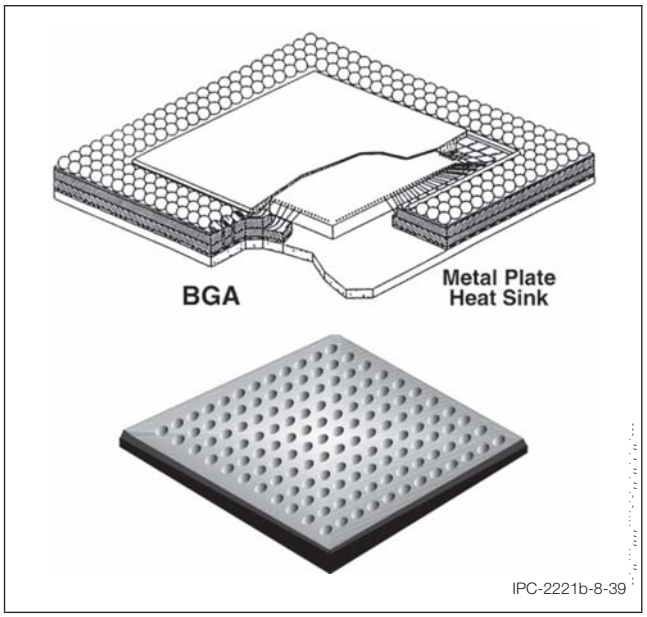


Figure 8-39 Examples of Ball Grid Array (BGA) Package Construction

8.9 No-Lead Devices The no-lead device family includes Quad Flat No-Lead (QFN) and Small Outline No-Lead (SON) devices, which lack lead terminations and consist instead of metal terminals along the bottom and side of the encapsulated package.

The Quad Flat No-Lead (QFN) package is a near CSP plastic encapsulated package with a copper leadframe substrate. This is a leadless package where electrical contact to the printed board is made by soldering the lands on the bottom surface of the package to the printed board, instead of the conventional formed perimeter leads. The exposed die attach paddle on the bottom efficiently conducts heat to the printed board and provides a stable ground through down bonds or electrical connections through conductive die attach material (see Figure 8-42).

The Small Outline No-lead Package (SON) is a rectangular semiconductor package with metal terminals along two sides of the bottom of the package. The terminals are either flush with the bottom or protruding slightly below the bottom of the package, with plastic mold compound present on three sides of each contact. The main body of the component is generally a molded plastic. The SON package is similar to the leaded SOIC family, though consuming less of the printed board area in comparison with the leaded SOIC. The part is a ‘‘leadless’’ package design with bottom paddles which can be soldered to the printed board. See Figure 8-43 for an example of a SON component.

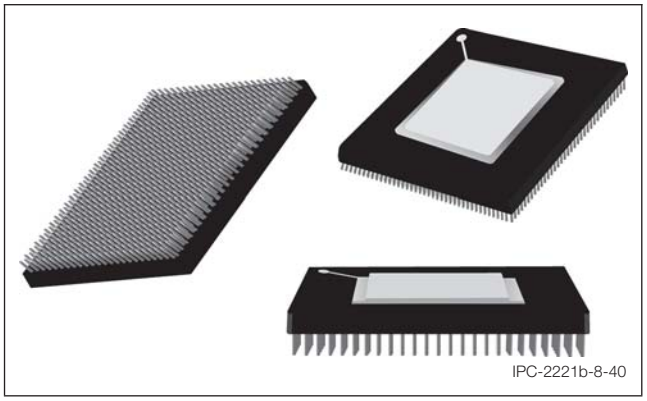


Figure 8-40 Ceramic Column Grid Array (CGA) Package Construction

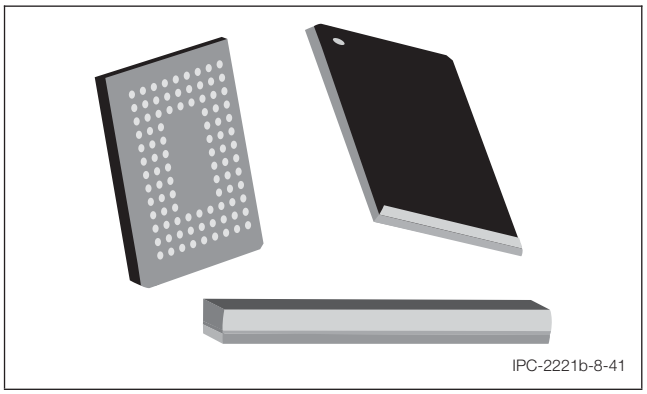


Figure 8-41 Land Grid Array (LGA) Package Construction

8.9.1 Small Outline and Quad Flat No Lead with Pullback Leads (PQFN, PSON) The pullback lead variants of the QFN and SON package types, labeled PQFN and PSON, respectively, consist of the pullback of the terminal metal from the edge

of the plastic body, as shown in Figure 8-44. These terminations are often referred to as peripheral leads or half etched pullback leads and require the same solder joint fillet on all four sides of the termination; there are no separate solder requirements for a toe, heel or side fillet as a result of the peripheral terminal construction.

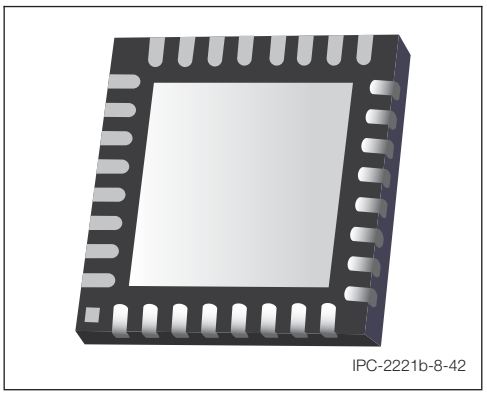

IPC-2221b-8-42

Figure 8-42 Quad Flat No-Lead (QFN) Construction

8.10 Compliant Pin Design Guidelines Although most vendor recommendations for hole finish are solder plating, space end use applications has a concern that the solder is incompatible with the gold finish of the pins (dissimilar metals). Under some circumstances, a corrosion cell can be created which can generate chemical reactions which can be deleterious to the hardware.

Space end use applications have made use of electrolytic gold plating with a nickel undercoating in compliant holes without problems. The finished hole size specified by the connector manufacturer is the correct finished size for the pin regardless of whether the finish is gold or solder. Because the pin is compliant and collapses structurally, the hardness of the gold or nickel is not a problem.

See section 9.2.2.5 for additional information on compliant pin systems.

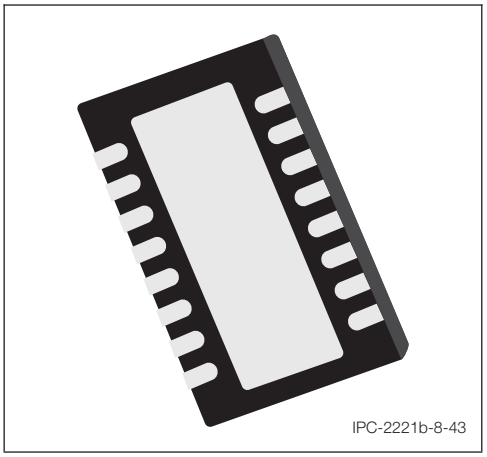

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Figure 8-43 Small Outline No-lead (SON) Construction

9 HOLES/INTERCONNECTIONS

9.1 General Requirements for Lands with Holes Lands **shall** be provided for each point of attachment of a part lead or other electrical connection to the printed board. Circular lands are most common, but it should be noted that other land shapes may be used to improve producibility. If breakout is allowed, modified land shapes **shall** be used. These may include, for example, filleting to create additional land area at the conductor junction, corner entry on rectangular lands or ''keyholing'' to create additional land area along the axis of the incoming lead (see Figure 9-1). The modified land shape **shall** provide for the current carrying capacity of the circuit design.

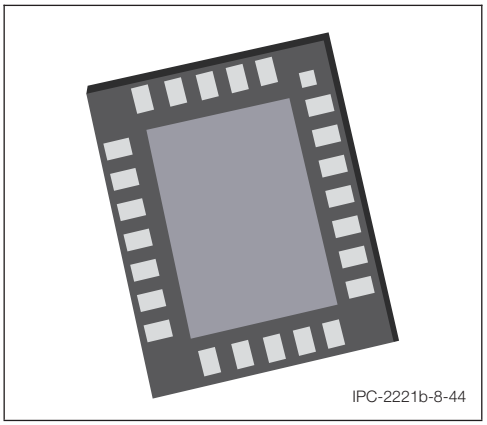
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Figure 8-44 Pullback Quad Flat No Lead (PQFN) Construction

9.1.1 Land Requirements All lands and annular rings **shall** be maximized wherever feasible, consistent with good design practice and electrical clearance requirements. When clearances are provided for unsupported holes in the place of external lands these **shall** meet the minimum edge spacing requirement. Failure to provide adequate land or clearance for unsupported holes will result in excessive rejections due to the common ''50-percent'' rule for ''nicks'' and ''crazing.'' Printed boards constructed with laminates prone to crazing such as polyimide but including other ''brittle'' materials will benefit from the use of oversized external lands and clearances. To meet the annular ring requirements specified in section 9.1.2, the minimum land surrounding a supported, or unsupported, hole **shall** be determined by the following.The worst-case land-to-hole relationship is established by the equation:

Land size, minimum = a + 2b + c

where:

a = Maximum diameter of the finished hole.

Note: For external layers, the requirement is the maximum diameter of the finished hole. For internal layers, the drill hole diameter is used.

b = Minimum annular ring requirements (see Section 9.1.2).

Note: Etchback, when required, **shall** be included within the calculation.*

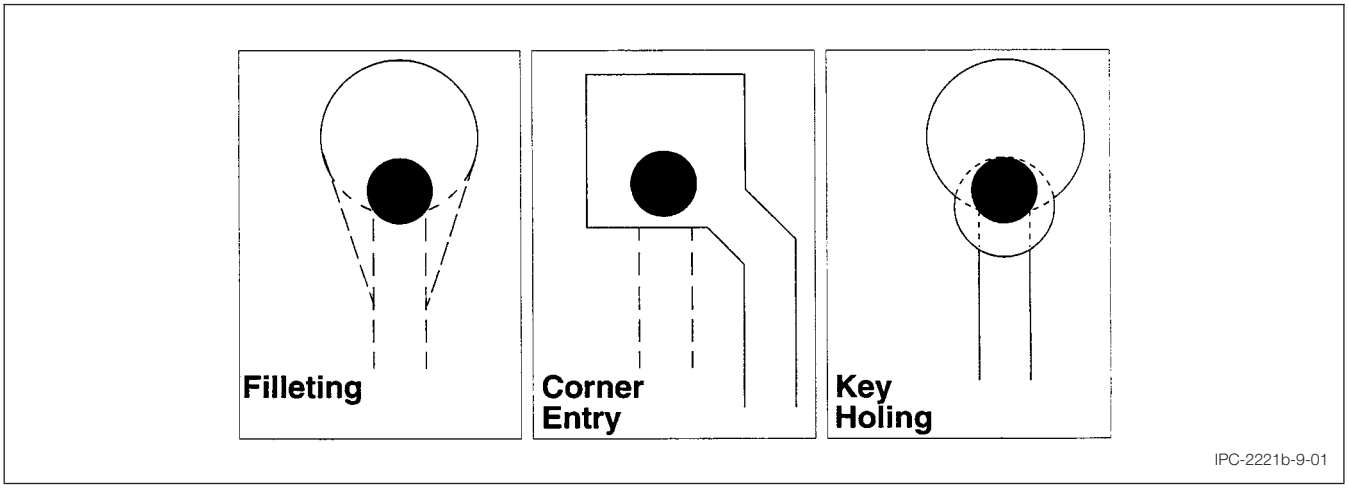


Figure 9-1 Examples of Modified Land Shapes

c = A standard fabrication allowance, detailed in Table 9-1, which considers production master tooling and process variations required to fabricate printed boards.

Note: Refer to the specific sectional design standard for additional processing allowance.

*Etchback, when required, will reduce the insulation area that supports the internal land. The minimum annular ring considered in the design **shall not** be less than the maximum etchback allowed.

Table 9-1 Minimum Standard Fabrication Allowance for Interconnection Lands

Level A	Level B	Level C
0.4 mm [0.016 in]	0.25 mm [0.00984 in]	0.2 mm [0.0079 in]

Note 1. For copper weights greater than 1oz/sq.ft.,add 50 µm [1,968 µin] minimum to the fabrication allowance for each additional oz/sq. ft. of copper used.
Note 2. For more than 8 layers add 50 µm [1,968 µin].
Note 3. See 1.6.3 for definition of Levels A, B and C.
Note 4. Refer to IPC-2226 for allowances for HDI and micro-BGA substrates.

9.1.2 Annular Ring Requirements An annular ring **shall** be required for all PTHs in Class 3 designs. The performance specifications for Class 1 and Class 2 products may allow partial hole breakouts. The design for these products should take into consideration that breakout is undesirable and the design should require adequate hole and land size so that breakout does not appear in the finished product. Landless holes or holes with partial circumscribing lands **shall** only be used when approved by the acquiring activity prior to the start of the design process and require conformance specimen that reflect the approach being used.

The minimum annular ring on external layers is the minimum amount of copper (at the narrowest point) between the edge of the hole and the edge of the land after plating of the finished hole (see Figure 9-2). The minimum annular ring on internal layers is the minimum amount of copper (at the narrowest point) between the edge of the drilled hole and the edge of the land after drilling the hole (see Figure 9-3).

9.1.2.1 External Annular Ring The minimum annular ring for unsupported and supported holes **shall** be in accordance with Table 9-2 and Figure 9-2.

9.1.2.2 Internal Annular Ring The minimum annular ring for internal lands on multilayer and metal core printed boards **shall** be in accordance with Table 9-2 and Figure 9-3. Etchback, when required, will reduce the insulation supporting the annular ring of internal lands. The minimum annular ring considered in the design **shall** be not less than the maximum etchback allowed.

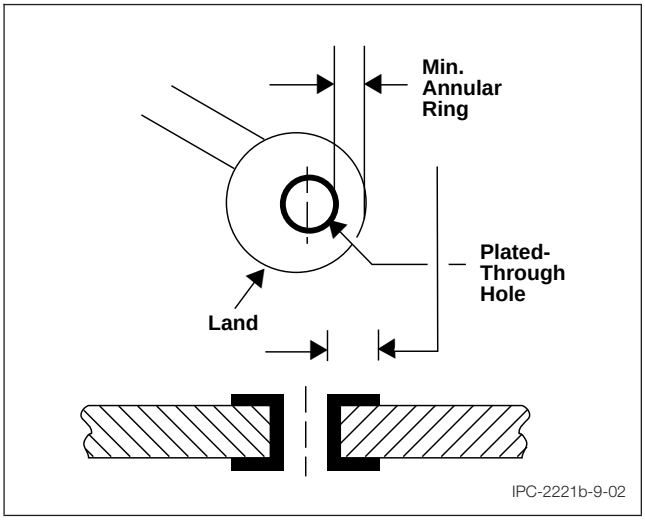


Figure 9-2 External Annular Ring

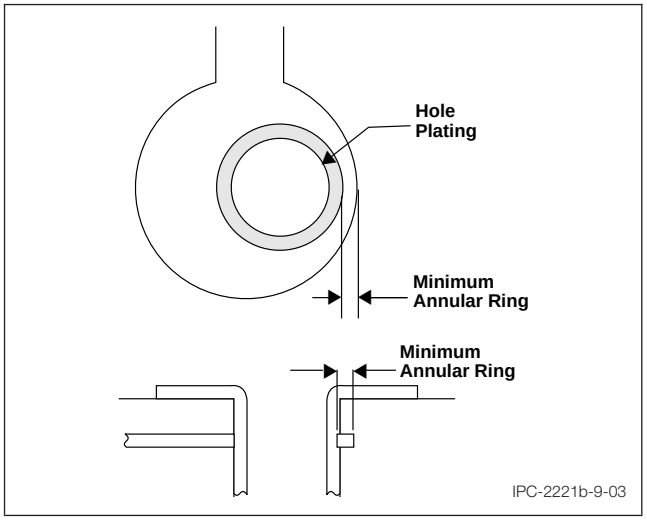


Figure 9-3 Internal Annular Ring

Table 9-2 Annular Rings (Minimum)

Annular Ring	Class 1, 2 and 3
Internal Supported	25.0 µm [984 µin]
External Supported	50.0 µm [1,968 µin]
External Unsupported[1]	0.150 mm [0.00591 in]

Note 1. The annular ring value for unsupported holes is greater to provide for larger external lands minimizing the loss or damage of pads during processing (drilling, etc.). Printed boards constructed with laminates with low peel strength (e.g., polyimides, etc.) will benefit from the use of oversized external lands.

9.1.3 Thermal Relief in Conductor Planes Thermal relief is only required for holes that are subject to soldering in large conductor areas (ground planes, voltage planes, thermal planes, etc.). Relief is required to reduce soldering dwell time by providing thermal resistance during the soldering process.

These type connections **shall** be relieved in a manner similar to that shown in Figure 9-4. The relationship between the hole size, land and web area is critical. See the sectional standards for more detailed information.

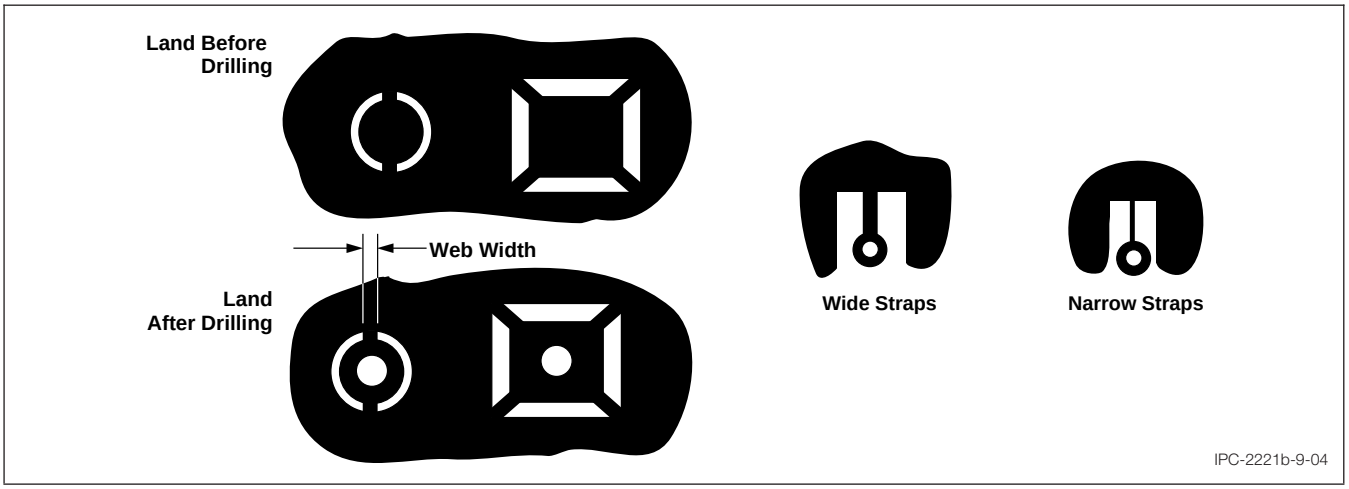


Figure 9-4 Typical Thermal Relief in Planes

9.1.4 Lands for Flattened Round Leads Flattened round (coined) leads **shall** have a land which will provide the seating so that the heel and the terminal relationship is in accordance with Figure 8-33.

Lead and land size should be designed to minimize side overhang. (Class 3 product allows up to 1/4 of the lead diameter to overhang.) Toe overhang is acceptable provided it does not violate the minimum designed conductor spacing. If flattened leads are used, the flattened thickness **shall not** be less than 40% of the original diameter (see J-STD-001).

9.2 Holes

9.2.1 Unsupported Holes These types of holes pass through the entire printed board thickness. They do not contain plating or other types of reinforcement. They may be used for tooling, mounting or component attachment.

Since unsupported holes are a critical element for alignment of printed board assemblies, they typically are listed as datums in fabrication drawings. For optimal alignment in an assembly, plated holes should be drilled in the same set-up as when the datum holes are drilled. When a pad is placed on an unsupported hole, the manufacturer is forced to drill the unsupported hole in a second set-up, which degrades the alignment between the plated and unsupported holes. The second drill step also increases the risk of haloing or crazing, since it is typically done after the surface copper is removed. For these reasons, the practice of placing pads on unsupported holes is not recommended.

There are instances in which the designer may want to place a pad on an unsupported hole. The pad may serve as a washer to prevent the hardware from cutting into the base material. It may also serve as a grounding connection for the hardware. When adding a pad to an unsupported hole, the designer should add a minimum of 0.38 mm [0.015 in] radial clearance around the hole to create a ''donut.'' This gives the fabricator enough room for resist to tent the hole during the plating process, thus avoiding the second drill set up. If holes cannot be reliably tented during plating, they would need to be drilled as a secondary step.

9.2.1.1 Tooling Holes This type of hole is a physical feature in the form of a hole, or slot, on a printed board fabrication panel or assembly panel. Tooling features are used exclusively to position a printed board or assembly during fabrication, assembly, and test procedures. This includes:

a) Registration of phototooling.

b) Positioning core layers during lamination.

c) Panels during drilling.

d) Printed boards at bare printed board testing.

e) Panels of printed boards during automated assembly.

f) Functional test.

The designer is responsible for indicating the tooling holes that stay with the printed board or panel. The printed board manufacturer is responsible for determining the tooling holes needed for printed board fabrication.

9.2.1.2 Mounting Holes These are holes that are used for the mechanical support of a printed board or for the mechanical attachment of components to a printed board.

9.2.2 Plated Holes This type of hole has plating on its wall that makes an electrical connection between conductive patterns on internal or external layers, or both, of a printed board.

These holes may also be used for component attachment, mounting, electrical interconnection or thermal transfer.

9.2.2.1 Blind Vias Blind via PTHs extend from the surface and connect the surface layer with one or more internal layers. The blind via can be produced by two methods: (1) After multilayer lamination by drilling a hole from the surface to the internal layers desired and electrically interconnecting them by plating the blind via holes during the plating process; or (2) Before multilayer lamination by drilling the blind via holes from the surface layers to the first or last buried layers and plating them through, imaging and etching the internal sides, and then laminating them in the multilayer bonding process. For the second process if an interconnection is desired between the surface layer and more than one internal layer, sequential etching, laminating, drilling and plating-through of these layers together before final multilayer lamination is required. Blind via holes should be filled or plugged with a polymer or solder mask to prevent solder from entering them as solder in the small holes decreases reliability.

9.2.2.2 Buried Vias Buried via PTHs do not extend to the surface but rather interconnect internal layers only. Most commonly the interconnection is between two adjacent internal layers. These are produced by drilling the thin laminate material, plating the holes through, and then etching the internal layer pattern on the layers prior to multilayer lamination. Buried vias between nonadjacent layers requires sequential etching of inside layers, laminating them together, drilling the laminated panel, plating the holes through, etching external sides and laminating this panel into the final multilayer panel.

9.2.2.3 Hole Size of Blind and Buried Vias Small holes are usually used for either blind or buried vias and may be produced mechanically, by laser, or by plasma techniques. The minimum drilled hole size for buried vias is shown in Table 9-3

and the minimum drilled hole size for blind vias is shown in Table 9-4. In either case plating aspect ratios **shall** be considered as small, deep blind vias are very difficult to plate due to decreased throwing-power and limited plating solution exchange in the holes. Blind and buried vias may be plated shut; thus, the master drawing call out should be similar to that used for through-hole vias. See sectional standards for more information.

Table 9-3 Minimum Drilled Hole Size for Buried Vias

Layer Thickness	Class 1	Class 2	Class 3
<0.25 mm [<0.00984 in]	0.10 mm [0.00393 in]	0.10 mm [0.00393 in]	0.15 mm [0.00591 in]
0.25 - 0.5 mm [0.020 in]	0.15 mm [0.00591 in]	0.15 mm [0.00591 in]	0.20 mm [0.00787 in]
>0.5 mm [>0.020 in]	0.15 mm [0.00591 in]	0.20 mm [0.00787 in]	0.25 mm [0.00984 in]

Table 9-4 Minimum Drilled Hole Size for Blind Vias

Layer Thickness	Class 1	Class 2	Class 3
<0.10 mm [<0.00393 in]	0.10 mm [0.00393 in]	0.10 mm [0.00393 in]	0.20 mm [0.00787 in]
0.10 - 0.25 mm [0.00984 in]	0.15 mm [0.00591 in]	0.20 mm [0.00787 in]	0.30 mm [0.0118 in]
>0.25 mm [>0.00984 in]	0.20 mm [0.00787 in]	0.30 mm [0.0118 in]	0.4 mm [0.016 in]

9.2.2.4 Thermal Vias Thermal vias are PTHs usually located under high power devices in groups that form a connection to the device package, either directly or through a thermally conductive medium. Their connection to internal planes and/or external planes serves to transfer heat out of the device packages. Thermal vias are typically larger than blind and buried vias and are not subjected to the same integrity requirements as other component and via holes.

9.2.2.5 Compliant Pin Systems A compliant pin is an electrical contact that is designed to be pressed into a PTH of a printed board. The resulting hole wall deformation that occurs during installation is necessary in order to achieve a reliable gas tight joint at the interface of the pin and the barrel of the hole wall. A variety of different pin configurations are in use today which result in a variety of different mounting and testing challenges. Typically, pins are installed into a backplane or assembly either as a single or multiple pin component.

There are many advantages for using compliant pins that come from not needing a solder joint. These include eliminating thermal stress on the printed board, no shorting of pins due to solder bridging, no need to clean after assembly to remove flux residue, eliminating solder joint inspection and plane layers that can be connected without regard to the heat sink effect. In addition, some connectors offer the ability to remove and replace individual pins if one is damaged and to replace a pin with an insulated version to make electrical modifications without drilling out the plating from the hole. Compliant pin connectors can be assembled to both sides of a printed board more easily than soldered connectors. The disadvantages include the need for special tooling and equipment to install the pins and the more critical parameters for the PTHs. Although both through-hole soldered connectors and compliant pin connectors can be used on the same printed board the design would result in a less efficient assembly. If active parts are needed on a backplane, the use of SMT components with compliant pin connectors is recommended.

9.2.2.5.1 Compliant Pin System Considerations Compliant pin interconnect **shall** be designed and qualified as a system to a specification which may include insertion and retention forces, transition resistance, hole wall deformation, assembly process and rework ability. Following are some specification options which should be referenced on the procurement documentation:

- MIL-A-28870 (Assemblies, electrical backplane).
- MIL-C-28859 (Connector component parts, electrical backplane).
- IEC-60352-5 (Solderless connections, press-in connections).
- Independent Qualification - e.g., Telcordia GR-1217-CORE.
- Internal Qualification.

Note: Suppliers listed under QML-28870 are qualified to install compliant pins certified to MIL-C-28859.

Epoxy-based printed boards have traditionally been used to qualify connectors. Designers should ensure that the material selected is compatible with the qualified connector installation process. The allowable deformation of the hole wall is a variable that **shall** be considered when using other materials.

It is important to ensure that the finished printed board thickness is consistent with the operational range in accordance with the requirements defined in the compliant pin specification.

The designer **shall** verify that the printed board finish is compatible with the compliant pin system being used. Eutectic tin-lead solder has typically been used for most applications. A Ni/Au finish may not be recommended by some compliant pin manufacturers due to the hardness of the Ni. Space environments yield a concern where the solder is incompatible with the connector pin's gold finish (dissimilar metals). Under some circumstances, a corrosion cell can be created which can generate chemical reactions deleterious to the hardware. Electrolytic gold plating with a nickel undercoating in compliant pin holes has been successfully used in space applications. The printed board hole size **shall** be as specified by the pin manufacturer.

End use environmental conditions may require the use of conformal coating and/or back-sealed connectors. Pins that are designed to pierce the appropriate conformal coatings are preferred. Not all pins will pierce conformal coatings; therefore the following should be considered:

- Mask pin fields and apply conformal coat prior to installation of pins not qualified to pierce conformal coating
- Non conformal coat piercing pins or unsealed connectors may require touch up with a compatible coating material after installation

Printed board drawings **shall** define the primary drill hole size and tolerance, finished hole size and tolerance, hole wall copper plating thickness range and final plating finish as defined by the pin specification.

The designer may be required to provide a compliant pin test coupon for qualification of the compliant pin system.

9.2.3 Location All holes and profiles **shall** be dimensioned in accordance with 5.4.

Note: The lead patterns of the majority of the components to be mounted on a printed board should be the major influence in the choice of a measurement system (metric or imperial).

9.2.4 Hole Pattern Variation When a modular grid increment is selected, see 5.4.2, parts whose leads emanate in a pattern that varies from the grid intersections of the modular dimensioning system of the printed board, **shall** be mounted on the printed board with one of the following hole patterns:

A hole pattern where the hole, for at least one part lead, is located at a grid intersection of the modular dimensioning system, and the other holes of the pattern are dimensioned from that grid location.

A hole pattern where the center of the pattern is located at a grid intersection of the modular dimensioning system, and all holes of the pattern are dimensioned from that grid location.

9.2.5 Location Tolerances Most holes are located to a basic grid. With GD&T (see 5.4.1), the grid has no tolerance. Holes are related to a position on the grid by a diameter of true position (DTP) tolerance, and this includes both plated and non-plated (unsupported) through-holes. PTHs are easier to inspect because one may hold true position through an annular ring requirement. Non-plated through holes (NPTHs) are more difficult to inspect, since they have no reference. If their position is critical, however, it is recommended that they be dimensioned and toleranced accordingly. Those NPTH's that relate to a specific component pattern are generally dimensioned to the other holes in that pattern or to the centroid of the component.

Other NPTHs are typically mounting or tooling holes. These holes are dimensioned to the datum planes, with an appropriate tolerance for the application.

Table 9-5, based on glass/epoxy materials, shows the values for hole location tolerances that **shall** be applied to the basic hole position. All tolerances are expressed as DTP. These tolerances only take into account drill positioning and drill drift. The basic hole position may be further affected by material thickness, type and the copper density. The effect is usually a reduction (shrinkage) between basic hole positions.

9.2.5.1 NPTH Tolerances

9.2.5.1.1 Tooling Holes Tooling holes are toleranced tightly in order to avoid movement between the tooling pin and the printed board. This is especially important if the holes are being used for registration. Registration pins are usually very precise, with tolerances in the range of 25.0 µm [984 µin] or less. The holes also have precise tolerances which are generally

Table 9-5 Minimum Hole Location Tolerance, dtp

Level A	Level B	Level C
0.25 mm [0.00984 in]	0.2 mm [0.0079 in]	0.15 mm [0.00591 in]

in the range of 50.0 µm [1,968 µin]. Maximum Material Condition (MMC) and Least Material Condition (LMC) are terms used to describe the relationship between the hole and the pin. Line to line conditions are considered as an interference fit, thus the MMC of the hole (when the hole is smallest) is usually considered with as small a clearance as possible with the MMC of the pin (when the pin is as large as possible). A 25.0 µm [984 µin] clearance is usually sufficient provided that the hole does not get too large or the pin too small.

9.2.5.1.2 Mounting Holes Tolerances normally follow standard fit and fastener techniques (see IPC-2615).

9.2.5.2 PTH Tolerances

9.2.5.2.1 Plated-Through Hole Tolerances When using the basic dimensioning system, PTHs used to attach component leads or pins to the printed board should be expressed in terms of MMC and LMC limits.

9.2.5.2.2 Printed Board Mounting Holes These are holes that are used for the mechanical support and attachment of the printed board to its assembly. They may also be used for electrical connections. Tolerances normally follow standard fit and fastener techniques (see IPC-2615).

9.2.6 Quantity A separate component hole **shall** be provided for each lead, terminal of a part, or end of a jumper wire that is to be through-hole mounted, except as specified in 8.2.11.

9.2.7 Spacing of Adjacent Holes The spacing of unsupported or PTHs (or both) **shall** be such that the lands surrounding the holes meet the spacing requirements of 6.3. Consideration should be given to the printed board material structural requirements, with the residual laminate material being no less than 0.5 mm [0.020 in].

9.2.8 Aspect Ratio The aspect ratio of PTHs plays an important part in the ability of the manufacturer to provide sufficient plating within the PTH. See IPC-2222 for additional information regarding hole aspect ratio.

9.3 Via Protection

9.3.1 Via Protection Requirements There are 7 types of via protection strategies that are noted in Table 9-6 as defined in IPC-4761. The selection should be based on performance needs; however, no unprotected copper **shall** be allowed. The requirements are dictated by processing, assembly or end item requirements. Single-sided via protection **shall not** be allowed if the barrel of the hole wall is bare copper. It is recommended that a via be protected on both sides in order to prevent entrapment of contaminants. See IPC-4761 for additional design guidelines.

9.3.2 Via Fill The process of filling vias may be required in some printed board designs. The requirement is driven most often by routing density utilizing buried via structures or Via-in-Pad constructions. When high-density area array components are utilized, the quantity of vias per square inch greatly increases in the local area at the device. If these vias are sublevel buried vias, they can starve the bonding resin from the local area where they are concentrated. To prevent this from occurring, the fabricator often is required to pre fill the vias prior to a build up lamination. Since this is an added fabrication material to the design construction, it requires a drawing note to invoke the via fill process and specify a fill material type. The fabricator often has preferences for the type of material used for via fill. This may complicate source selection or dictate the use of a service center for the process. Most often the limitation is due to available process resources. Just as printed board suppliers often have preferences for a specific solder mask brand, they also often prefer use of a specific via fill material that they have developed their processes around. Preferences can be driven by specific via fill material characteristics, i.e., accessibility, equipment availability, process supportability, plateability, cost, conductivity and/or shelf/pot life. The fabricator may not always know the reliability of their preferred material for a given via structure or end use environment. Currently an industry based material specification for via fill material does not exist, so standardized testing and determining material properties may be difficult. IPC-4761 provides some guidelines on various via protection methods but does not evaluate the reliability of the methods. Determining properties from the material suppliers may be possible for some properties, while others may be more difficult to obtain, e.g., modulus has not been noted on any of the manufacturers' data sheets as of the publication of this revision to IPC-2221.

Table 9-6 Through-Hole Diameters Minimum and Maximum and Aspect Ratio, mm [in]

	Tented, No Fill	Tented and Covered	Plugged	Plugged and Covered	Filled	Filled and Covered	Filled and Capped
Via Protection Type[1]	I	II	III	IV	V	VI	VII
Minimum Hole Diameter, Class 1 and 2	N.A.	N.A.	0.254 [0.010]	0.254 [0.010]	0.254 [0.010][2]	0.254 [0.010][2]	0.254 [0.010][2]
Minimum Hole Diameter, Class 3	N.A.	N.A.	0.254 [0.010]	0.254 [0.010]	0.254 [0.010][2]	0.254 [0.010][2]	0.254 [0.010][2]
Maximum Hole Diameter, Class 1 and 2	0.66 [0.0256]	1.0 [0.040]	1.27 [0.050]	1.27 [0.050]	1.0 [0.040][2]	1.0 [0.040][2]	1.0 [0.040][2]
Maximum Hole Diameter, Class 3	0.66 [0.0256]	0.66 [0.0256]	1.27 [0.050]	1.27 [0.050]	1.0 0.040[2]	1.0 [0.040][2]	1.0 [0.040][2]
Maximum Aspect Ratio[3], Class 1 and 2	N.A.	N.A.	N.A.	N.A.	8	8	8
Maximum Aspect Ratio[3], Class 3	N.A.	N.A.	N.A.	N.A.	8	8	8
Minimum Aspect Ratio[4], Class 1 and 2	N.A.	N.A.	N.A.	N.A.	3	3	3
Minimum Aspect Ratio[4], Class 3	N.A.	N.A.	N.A.	N.A.	3	3	3

Note 1. Assumes option (b) for each via protection type defined in IPC-4761, which consists of protection from both sides of the via structure.
Note 2. The diameter of holes for fill may vary from these limits based on aspect ratios, hole fill material and environment.
Note 3. Maximum Aspect Ratio dependent on hole fill material and thickness. This aspect ratio refers to the minimum hole size mentioned in the table, i.e., 0.254 mm [0.010 in] hole and aspect ratio of 8.
Note 4. Minimum aspect ratio is for thin printed boards/cores below 0.79 mm [0.031 in].

10 GENERAL CIRCUIT FEATURE REQUIREMENTS

10.1 Conductor Characteristics Conductors on the printed board may take a variety of shapes. They may be in the form of single conductors, or conductor planes.

Critical pattern features which may affect circuit performance such as characteristic impedance, capacitance, etc., or reliability such as surface mount land geometry **shall** be identified, and a tolerance provided. There are two methods to verify conformance; one method being electrical verification of circuit performance, and the other being dimensional verification of pattern geometry. Unless otherwise specified, circuit design tolerances **shall** be in accordance with IPC-6010 series.

Note: Conformance may be verified in accordance with 12.3.

10.1.1 Conductor Width and Thickness The thickness and width of conductors on the finished printed board **shall** be determined on the basis of the signal characteristics, current carrying capacity required and the maximum allowable temperature rise (See IPC-2141 and IPC-2152). In determining the thickness of conductors on or within the finished printed board, the designer should take into consideration that processing may vary the thickness of copper on layers affected by the construction requirements, such as for sequentially laminated parts, or the via requirements, such as for blind or buried vias (See IPC-6012). When utilizing circuits sensitive to voltage drop, one should take this into account and consider stating a minimum thickness value within the procurement documentation based on actual design constraints.

Table 10-1 provides the internal layer minimum copper foil allowances per IPC-4562 and further copper thickness reduction based on layer processing.

Table 10-2 applies to external surface conductors associated with constructions having through-holes, buried and/or blind vias/microvias, and internal layers produced as sub-constructed cores having plating applied during the manufacturing cycle(s). The calculated final surface thickness provides a standard acceptable allowance for external conductors based on the minimum copper foil plus the minimum copper plating (by performance classification), less a processing allowance. The minimum surface conductor thickness (after processing) values given in Table 10-2 are determined by the following equation:

Minimum Surface Conductor Thickness = a + b - c
where:
a = Absolute copper foil minimum (IPC-4562 nominal less 10% reduction).
b = Minimum copper plating thickness (20 µm [787 µin] for Class 1 and Class 2; 25 µm [984 µin] for Class 3).
c = A maximum variable processing allowance reduction.

Table 10-1 Internal Layer Foil Thickness After Processing

Weight	Absolute Cu Min. (IPC-4562 less 10% reduction) (µm) [µin]	Maximum Variable Processing Allowance Reduction[1] (µm) [µin]	Minimum Final Finish after Processing (µm) [µin]
1/8 oz. [5.10]	4.60 [181]	1.50 [59]	3.1 [122]
1/4 oz. [8.50]	7.70 [303]	1.50 [59]	6.2 [244]
3/8 oz. [12.00]	10.80 [425]	1.50 [59]	9.3 [366]
1/2 oz. [17.10]	15.40 [606]	4.00 [157]	11.4 [449]
1 oz. [34.30]	30.90 [1,217]	6.00 [236]	24.9 [980]
2 oz. [68.60]	61.70 [2,429]	6.00 [236]	55.7 [2,193]
3 oz. [102.90]	92.60 [3,646]	6.00 [236]	86.6 [3,409]
4 oz. [137.20]	123.50 [4,862]	6.00 [236]	117.5 [4,626]
Above 4 oz. [137.20]	IPC-4562 value less 10% reduction	6.00 [236]	6 µm [236 µin] below minimum thickness of calculated 10% reduction of foil thickness in IPC-4562

Note 1. Process allowance reduction does not allow for rework processes for weights below ½ oz. For ½ oz. and above, the process allowance reduction allows for one rework process.

Table 10-2 External Conductor Thickness After Plating

Weight[1]	Absolute Cu Min. (IPC-4562 less 10% reduction) (µm) [µin]	Plus minimum plating for Class 1 and 2 (20 µm) [787 µin][2]	Plus minimum plating for Class 3 (25 µm) [984 µin][2]	Maximum Variable Processing Allowance Reduction[3] (µm) [µin]	Minimum Surface Conductor Thickness after Processing (µm) [µin]	
					Class 1 & 2	Class 3
1/8 oz.	4.60 [181]	24.60 [967]	29.60 [1,165]	1.50 [59]	23.1 [909]	28.1 [1,106]
1/4 oz.	7.70 [303]	27.70 [1,091]	32.70 [1,287]	1.50 [59]	26.2 [1,031]	31.2 [1,228]
3/8 oz.	10.80 [425]	30.80 [1,213]	35.80 [1,409]	1.50 [59]	29.3 [1,154]	34.3 [1,350]
1/2 oz.	15.40 [606]	35.40 [1,394]	40.40 [1,591]	2.00 [79]	33.4 [1,315]	38.4 [1,512]
1 oz.	30.90 [1,217]	50.90 [2,004]	55.90 [2,201]	3.00 [118]	47.9 [1,886]	52.9 [2,083]
2 oz.	61.70 [2,429]	81.70 [3,217]	86.70 [3,413]	3.00 [118]	78.7 [3,098]	83.7 [3,295]
3 oz.	92.60 [3,646]	112.60 [4,433]	117.60 [4,630]	4.00 [157]	108.6 [4,276]	113.6 [4,472]
4 oz.	123.50 [4,862]	143.50 [5,650]	148.50 [5,846]	4.00 [157]	139.5 [5,492]	144.5 [5,689]

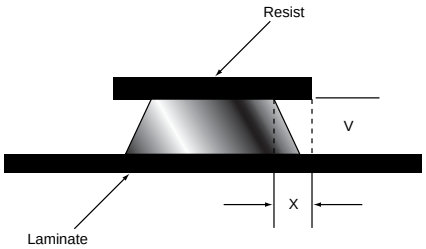
Note 1. Starting foil weight of design requirement per procurement documentation.
Note 2. Process allowance reduction does not allow for rework processes for weights below ½ oz. For ½ oz. and above, the process allowance reduction allows for one rework process.
Note 3. Reference: Min. Cu Plating Thickness

Class 1 = 20 µm [787 µin] Class 2 = 20 µm [787 µin] Class 3 = 25 µm [984 µin]

When product safety certification organizations such as Underwriters Laboratories (UL) impose requirements, the specified minimum conductor width **shall** be within the limits approved by the safety certification organization for the printed board manufacturer. For ease of manufacturing and durability in usage, conductor width and spacing requirements should be maximized. The minimum spacing in the design **shall** take into consideration the allowance required for etch compensation. The nominal finished conductor width and acceptable tolerances **shall** be shown on the master drawing.

Standard conductor width and spacing tolerances are provided for in the applicable printed board performance specification(s) according to product classification. This ranges from 80% to 90% of the supplied pattern for conductor width and from a 10% to 30% reduction of conductor space depending on the specified product type and performance class. These percentage allowances are default values where otherwise not specified. It should be understood that conductor width tolerance by a percentage allowance will vary according to the feature size and may impact design performance for large features. The designer should review all etched features in light of the applicable product type and performance class when defaulting to percentage tolerances.

Critical to function tolerances may be required to control specific design conductor characteristics (see 10.1). The nominal finished conductor width can generally be determined based on a 1:1 etch factor as shown in Figure 10-1. Minimum conductor width is determined at the base of the conductor. Critical to function tolerances, when required, **shall** be shown on the master drawing. This dimension need only be shown on the master drawing for a typical conductor of that nominal width.



$$\text{Etch Factor} = \frac{V}{X}$$

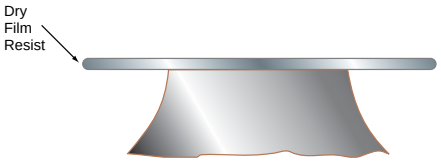
"A" POINT OF NARROWEST CONDUCTOR WIDTH: This is not "Minimum Conductor Width" noted on master drawings or performance specifications.

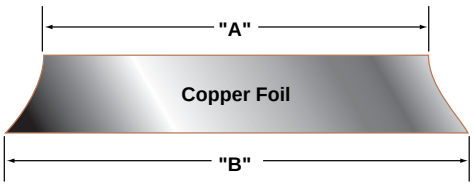
"B" CONDUCTOR BASE WIDTH: The width that is measured when "Minimum Conductor Width" is noted on the master drawing or performance specification.

"C" PRODUCTION MASTER WIDTH: The width usually determines the width of the metal or organic resist on the etched conductor.

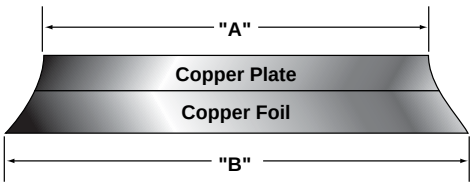
Design width of the conductor is specified on the master drawing and is most often measured at the conductor base "B" for compliance to "minimum conductor width" requirements.

The following two configurations show that conductor width may be greater at the surface than at the base.

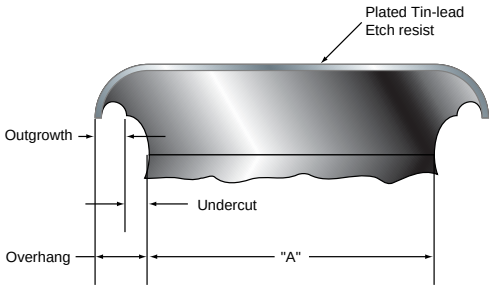




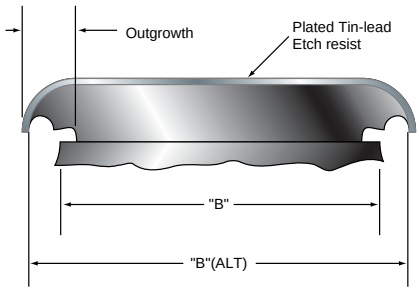
Internal layer after etch



Internal plated layer as used for buried vias



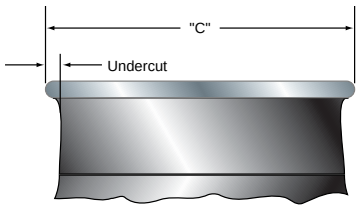
Pattern plating (dry film resist) with outgrowth



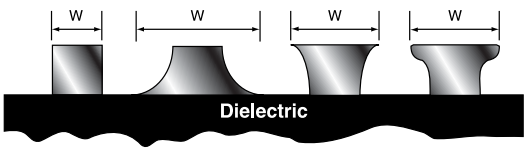
Pattern plating (liquid resist) with outgrowth

Note: The extent of outgrowth, if present, is related to the dry film resist thickness. Outgrowth occurs when the plating thickness exceeds the resist thickness.

"B" (ALT) would be used to determine compliance with "Minimum Conductor Width" for this etch configuration.



Thin clad & pattern plating (etch resist)



The effective width of a conductor may vary from the conductor width from surface obstructions (W).

Note: The different etch configurations may not meet intended design requirements.

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Figure 10-1 Etched Conductor Characteristics

The inspection methodology for critical to function toleranced conductor features as specified on the master drawing should be AABUS. AOI technology may not be adequate for accurately assessing a dimensional tolerance. For these critical features, an alternate inspection methodology should be defined to include magnification and measurement location/frequency, which can be a cost driver.

The width of the conductor should be as uniform as possible over its length; however, it may be necessary because of design restraints to ''neck down'' a conductor to allow it to be routed between restricted areas, e.g., between two PTHs. The use of ''necking down'' such as that shown in Figure 10-2, can also be viewed as ''beefing up.'' Single width, having a thin conductor throughout the printed board, as opposed to the thin/thick approach is less desirable from a manufacturing point of view as the larger width conductor is less rejectable due to edge defects rated as a percentage of the total width.

In any event, if the conductor width change is used, the basic design requirements defined herein **shall not** be violated at the necking down location.

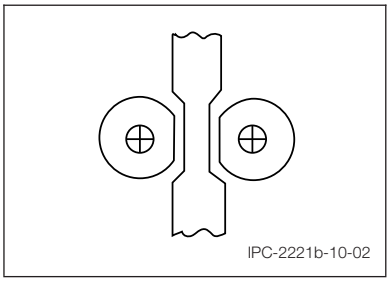


Figure 10-2 Example of Conductor Beef-Up or Neck-Down

10.1.2 Electrical Clearance Clearances are applicable for all levels of design complexity (A, B, C) and performance classes (1, 2, 3). Conductive markings may touch a conductor on one side, but minimum spacing between the character marking and adjacent conductors **shall** be maintained (see Table 6-1).

To maintain the conductor spacing shown on the master drawing, space widths on the production master may require compensation for process allowances as defined in 10.1.1. The minimum spacing between PTHs and internal conductors **shall** meet the same minimum clearance as required for spacing between internal conductors (see 10.1.4). See 6.3 for more information on electrical clearance. See 10.1.3 for information related to maintaining electrical spacing while performing circuit routing.

10.1.3 Conductor Routing The length of a conductor between any two lands should be held to a minimum. However, conductors which are straight lines and run in X, Y, or 45° directions are preferred to aid computerized documentation for mechanized or automated layouts. All conductors that change direction, where the included angle is less than 90°, should have their internal and external corners rounded or chamfered.

In certain high speed applications, specific routing rules may apply. A typical example is serial routing between signal source, loads and terminators. Routing branches (stubs) may also have specified criteria.

Internal lands should not be removed to ''make enough room'' to route a circuit between holes. To help maintain internal minimum spacing, circuit routing should always be performed with all of the lands in place on all layers for each hole. After all circuits have been routed, nonfunctional lands may be removed (see IPC-2222).

10.1.4 Conductor Spacing Minimum spacing between conductors, between conductive patterns, and between conductive materials (such as conductive markings, see 10.1.2, or mounting hardware) and conductors **shall** be defined on the master drawing. Spacings between conductors should be maximized and optimized whenever possible (see Figure 10-3). To maintain the conductor spacing shown on the master drawing, conductor spacing should be sufficient to allow for etch compensation of features by the fabricator. Typical etch compensation is twice the etched copper thickness. These process allowances include but are not limited to, etch factors, conductor imperfections, and copper wicking between PTHs and adjacent plane layers.

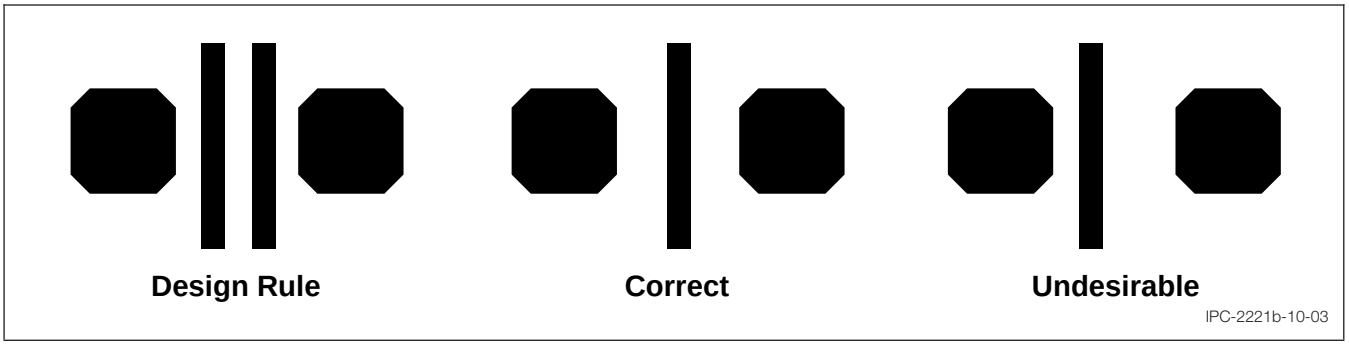


Figure 10-3 Conductor Optimization Between Lands

10.1.5 Plating Thieves Plating thieves are added metallic areas which are nonfunctional. When located within the finished printed board profile, they allow uniform plating density, giving uniform plating thickness over the printed board surface. They **shall** neither adversely impact the minimum conductor spacing nor violate the required electrical parameters.

10.2 Land Characteristics

10.2.1 Manufacturing Allowances The design of all land patterns **shall** consider the manufacturing allowances, specifically those relating to conductor width and spacing.

Processing allowances similar to the characteristics shown in Figure 10-1 **shall** be built into the design to allow the manufacturer to produce a part that will meet the end-item requirements detailed on the master drawing (see IPC-2611).

10.2.2 Lands for Surface Mounting When surface attachment is required, the requirements of 10.1 **shall** be considered in the design of the printed board. The selection of the design and positioning of the land geometry, in relation to the part, may significantly impact the solder joint. The possibility of heat thieving is reduced by ''necking down'' the conductor near the soldering area. The designer should understand the capabilities and limitations of the manufacturing and assembly operations (see IPC-7351).

The various soldering processes associated with surface mounting have specific land pattern requirements. It is desirable that the land pattern design be transparent to the soldering process to be used in manufacturing. This will be less confusing for the designer and reduce the number of land sizes.

10.2.3 Test Points When required by the design, test points for probing **shall** be provided as part of the conductor pattern, and **shall** be identified on the assembly drawing. Vias, wide conductors, or component mounting lands may be considered as probe points, provided that sufficient area is available for probing, and maintaining the integrity of the via, conductor, or component solder connection. Test points **shall** be free of coating material prior to test unless otherwise specified. After test has been completed, test points may be coated if specified.

10.2.4 Orientation Symbols Special orientation symbols should be incorporated into the design to allow for ease of inspection of the assembled part. Techniques may include special symbols, or special land configurations to identify such characteristics as pin 1 of an integrated circuit package. Care should be taken to avoid adversely affecting the soldering process. Special orientation symbols **shall** be provided for Class 3 product.

10.3 Large Conductive Areas Large conductive areas are related to specific products and are addressed in sectional design standards.

11 DOCUMENTATION

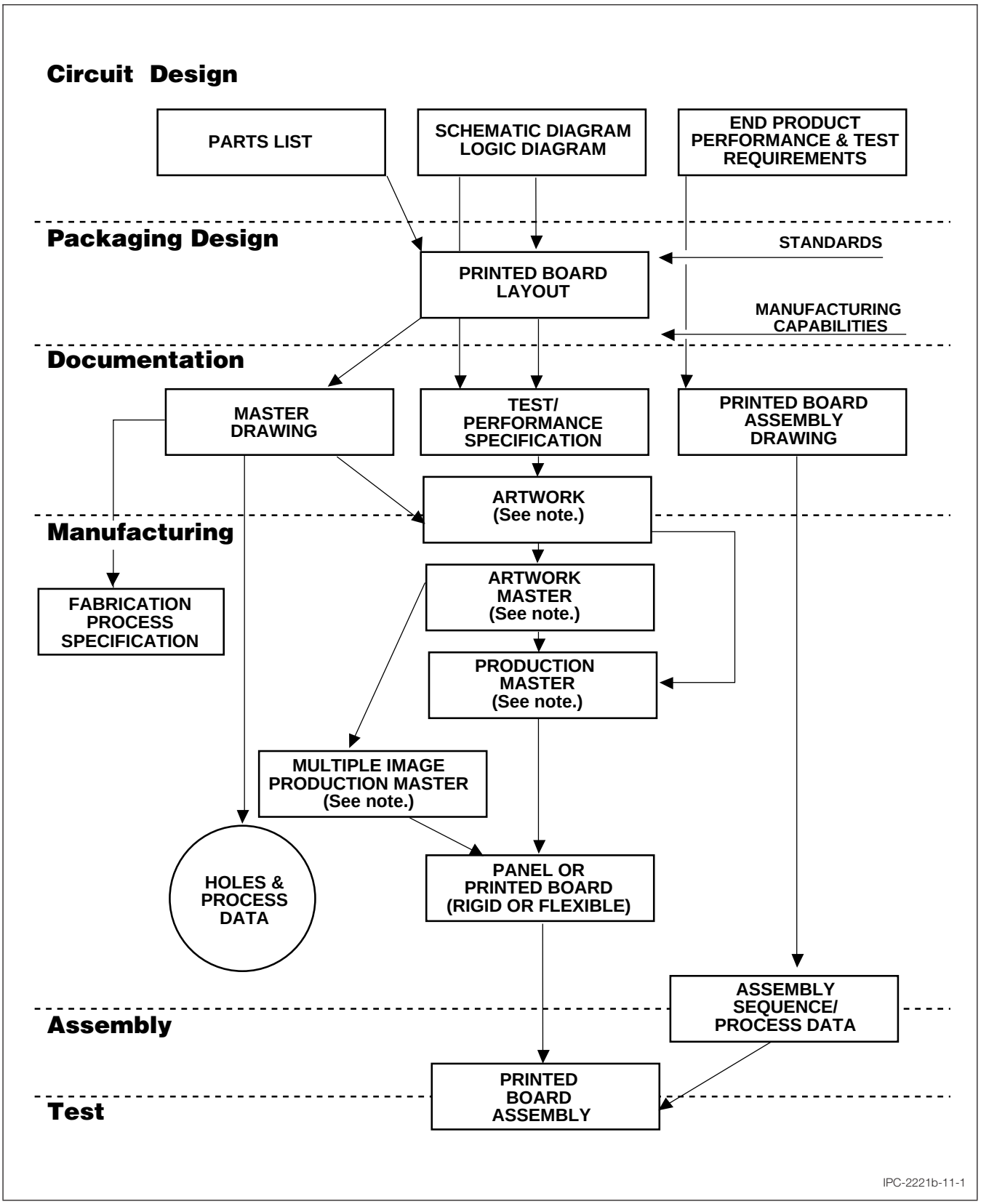
The printed board documentation package consists of the master drawing, copies of the artwork (film, paper or data), printed board assembly drawing, parts lists, and schematic/logic diagram.

The documentation package may be provided in either hard copy or electronic data. All electronic data should meet the requirements of the IPC-2500 series of standards.

Other documentation may include numerical control data for drilling, routing, libraries, test, artwork, and special tooling. There are design and documentation features/requirements that apply to the basic layout, the production master (artwork), the printed board itself, and the end-item printed board assembly; all should be taken into consideration during the design of the printed board. Therefore it is important to understand the relationships they have with one another as shown in Figure 11-1.

The printed board documentation **shall** meet the requirements of IPC-2610. In order to provide the best documentation package possible, it is important to review IPC-2610 and identify all the criteria that are affected by the design process, such as:

- Parts information
- Nonstandard parts information
- Master drawing
- Artwork masters production
- Master pattern drawing



Note: The term ''original'' may be used to preface any of the drafting and photographic tooling terms used in the figure. The ''original'' is not usually used in manufacturing processes. In the event a ''copy'' is made, the copy **shall** be of sufficient accuracy to meet its intended purpose if it is to take on the name of any one of the terms used in this figure. Other adjectives may also be used to help describe the kind of copy, e.g.: ''nonstable,'' ''first generation,'' ''record,'' etc.

Figure 11-1 Flow Chart of Printed Board Design/Fabrication Sequence

11.1 Special Tooling During the formal design review prior to layout, special tooling that can be generated by the design area in the form of artwork or numerical control data **shall** be considered. This tooling may be needed by fabrication, assembly, or testing. Examples of such tooling are:

- Plots of numerical data to be used as check film.
- Buried or blind via land masters to assist in determining the location of the vias during layer fabrication for composite printed boards.
- Via land masters for composite printed boards to assist in distinguishing between vias that are to be drilled before lamination and vias that will be drilled after lamination.
- Artwork overlays to provide aids such as drill origin, spotter lands for nonplated through-holes without lands on the artwork, printed board coordinate zero, printed board profile, coupon profile, or profile of internal routed areas.
- Artwork for solder mask stripping which is used in some processes for solder mask over bare copper. The artwork should be designed to allow a solder mask overlap onto the solder at the copper/solder interface.
- Artwork overlays that can be used in assembly to assist with component insertion.
- Numerical data for auto-insert equipment at assembly.
- Solder paste stencil data.

11.2 Layout

11.2.1 Viewing The layout should always be drawn as viewed from the primary side of the printed board. For phototool generation purposes, the viewing requirements **shall** be identical to the layout.

The definition of layers of the printed board **shall** be as viewed in Figure 11-2. Distinguishing characteristics **shall** be used to differentiate between conductors on different layers of the printed board.

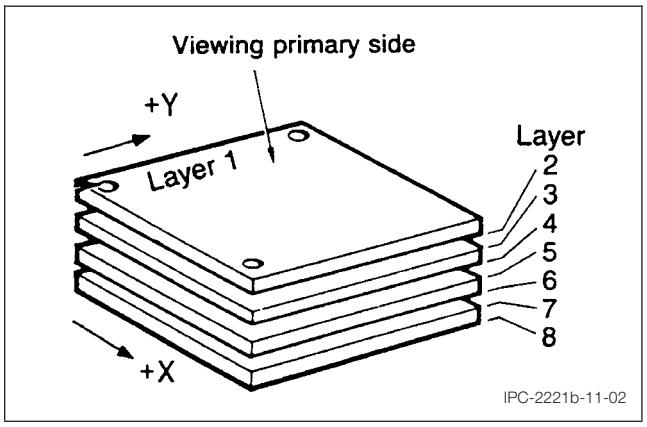


Figure 11-2 Multilayer Printed Board Viewing

11.2.2 Accuracy and Scale The accuracy and scale of the layout **shall** be sufficient to eliminate inaccuracies when the layout is being interpreted during the artwork generation process. This requirement can be minimized by strictly adhering to a grid system which defines all features on the printed board.

11.2.3 Layout Notes The layout should be completed with the addition of appropriate notations, marking requirements, and revision/status-level definition. This information should be structured to assure complete understanding by all who view the layout. Notes are especially important for the engineering review cycle, the digitizing effort, and when the document is used by someone other than the originator.

11.2.4 Automated-Layout Techniques All the information listed in 11.2.1 through 11.2.3 is applicable to both manual and automated layout generation. However, when automated layout techniques are used, they should also match the design system being employed. This may include the use of computer-aided drafting assistance that primarily helps in the defining of components and conductors, or may be as sophisticated as to add the placement of digital circuit gates, the placement of components, and the routing of conductors.

When automated systems are required to communicate with each other, it is recommended that standard files be used for this technique. IPC-D-356 and the IPC-2510 series of documents have been developed to serve as the standard format to facilitate the interchange of information between automated systems. Archiving of data should be in accordance with those documents. Delivery of computer-generated data as a part of a documentation package should meet these requirements.

With automated techniques, the data base should detail all the information that will be needed to produce the printed board. This includes all notes, plating requirements, printed board thickness, etc. A check plot should be employed to verify that the data base matches the requirements.

11.3 Deviation Requirements Any deviation from this standard or drawing **shall** have been recorded on the master drawing or a customer-approved deviations list.

11.4 Phototool Considerations The same land pattern configuration and nominal dimensions may be used for preparing the phototool for the stencil or screen used for solder paste application.

11.4.1 Artwork Master Files An electronic data file or alternative physical media, which defines the master image for each layer, that **shall** be provided as part of the master drawing set.

11.4.2 Film Base Material The artwork master, if supplied, **shall** be on a minimum of 0.165 mm [0.0065 in] thick biaxially oriented, dimensionally stable, polyester type film, or on glass photographic plates. Common film thickness ranges from 0.18 mm [0.007 in] to 0.28 mm [0.011 in]. Photographical glass plates range from 1.5 mm [0.0591 in] to 4.75 mm [0.190 in].

11.4.3 Solder Mask Coating Phototools Solder mask coating phototools may be prepared in two ways. The first method is to provide a special land pattern for each component using larger shapes to establish the solder mask clearance around the conductive pattern (see Figure 11-3 and Figure 11-4). There may be other factors, such as fiducials, mounting holes and printed board edges which may require clearances.

The second method is to provide the same land pattern shapes for solder mask windows as used to establish the conductive pattern. In this method, the manufacturer of the printed board photographically expands the solder mask pattern to provide the necessary clearances. Thus, the same phototool may be used to establish the conductive pattern, the solder mask openings, and the solder paste deposition tool. The ability to use the same phototool for the three processing steps enhances registration capabilities of the three image-dependent procedures and also keeps computer library symbol (land pattern) types to a manageable limit when computer aided design (CAD) systems are used. When utilizing this option, maximum clearance values **shall** be specified on the master drawing.

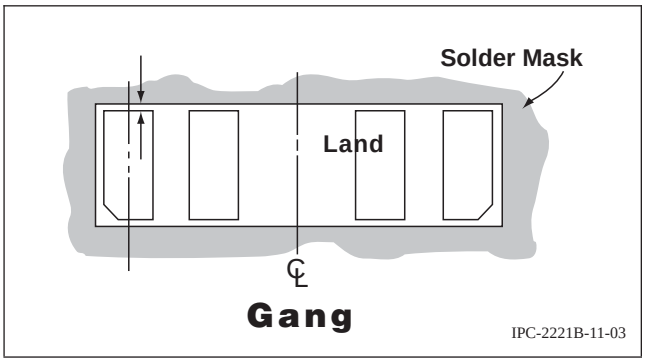


Figure 11-3 Gang Solder Mask Window

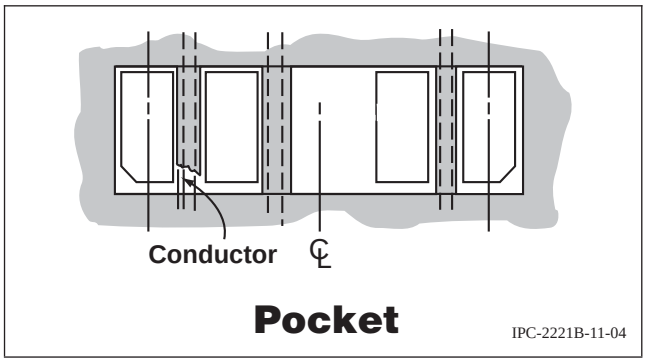


Figure 11-4 Pocket Solder Mask Window

12 QUALITY ASSURANCE

For Class 2 and Class 3 end product, quality assurance **shall** be considered in all aspects of printed board design. Quality assurance evaluations relating to design **shall** consist of the following unless otherwise AABUS:

- Material
- Conformance inspection
- Processes

This section defines the various fabrication coupons that **shall** be considered during the design process. Also included is the rationale and purpose for the use of each coupon.

12.1 Conformance Test Coupons Conformance test coupons **shall** be in accordance with this section. Quality assurance provisions often require the use of specific test procedures or evaluations to determine if a particular product meets the requirements of the customer or specifications. Some of the evaluations are done visually, others are done through destructive and nondestructive testing.

Some quality evaluations are performed on test coupons because the test is destructive or the nature of the test requires a specific design which may not exist on the printed board. Test coupons are used in these types of tests as representatives of the printed boards fabricated on the same panel.

A test coupon is a suitable sample for destructive testing since it has been subjected to the same processes as the printed boards on the same panel; however, the design and location of the test coupons are critical in order to ensure that the coupons are truly representative of the printed boards. A production printed board may be used for destructive tests. Tests requiring specific circuit configuration (e.g., insulation resistance) may also be performed on production printed boards if appropriate circuitry is included in the design.

12.2 Material Quality Assurance Material inspections normally consist of certification by the manufacturer supported by verifying data based on statistical sampling that all materials which become a part of the finished product are in accordance with the master drawing, material specifications, and/or procurement documentation.

12.2.1 Laminates Conformance coupons are defined in the detailed specifications for the base material. As an example, copper foil is tested for tensile strength, ductility, elongation, fatigue ductility, peel strength, and carrier release strength. In most instances, the conformance test coupons for metal foil consist of a specific length and width.

Laminate specifications, however, require conformance coupons that relate more to performance of the end product printed board. Not only are peel strength, dielectric breakdown, and water absorption tested, the methods of examination require that specific coupon geometries be prepared in order to make the test as meaningful as possible. When a design requires verification of the base material at the end product printed board level, conformance coupons are used to establish that evaluation is identical or similar to those defined in existing base material specifications.

Each design sectional allows for a minimum dielectric thickness between layers of a multilayer printed board, when agreed upon between user and supplier. Some users may require more than one ply of reinforcement and greater than 50 µm [1,968 µin] dielectric thickness. Example: Some military specifications require two ply reinforcement and greater than 90 µm [3,543 µin] dielectric thickness. When this requirement is agreed upon, conformance test coupons **shall** be provided as a part of the design to verify the specific resin and resin content, glass style, dielectric withstanding voltage between claddings and moisture resistance verification.

12.2.2 Compliant Pin It is recommended that the appropriate and applicable documentation require evidence of conformance to the engineering specifications, such as:

- Each lot of pin/connectors
- Assembly tooling traceability back to the application qualification testing
- The correct drill size and final plating thickness(es)

12.3 Conformance Evaluations Conformance evaluations are performed on production printed boards and/or conformance coupons. If a production printed board is selected for conformance evaluation, it **shall** meet the requirements of Table 12-1 or Table 12-2. Coupons required for conformance evaluation **shall** be as defined herein. Additional conformance coupons may be added by the manufacturer. Conformance coupons **shall** be traceable to the production panel.

12.3.1 Coupon Quantity and Location The conformance test circuitry **shall** be a part of every panel used to produce printed boards when required by the procurement documentation or applicable performance specification. The coupons outlined in Table 12-1 and Table 12-2 constitutes the minimum requirements to be compatible with most performance specifications. Coupons of custom configuration may be designed to accomplish specific user/supplier agreements. The custom coupons should incorporate features on the same dimensional plane to ensure compatibility with other standard coupons and the applicable performance specification.

All applicable configurations of test coupons **shall** be defined on the master artwork, the master drawing or added to the build artwork by the manufacturer to accommodate requirements of the performance specification. The location of the construction integrity coupons should be positioned within 12.7 mm [0.500 in] of the printed board profile to reflect build and plating characteristics. Figure 12-1 and Figure 12-2 provide examples of the usage of panel utilization concepts between the IPC-2221 legacy conformance coupon designs and the current IPC-2221 Revision B designs (see 12.4 for details on individual coupon design). The fabricator may position the coupons within the process verification coupon zone and/or the useable printed board real estate zone in order to optimize panelization, tooling and material utilization. While coupons on all four sides are shown in Figure 12-1 and Figure 12-2, the fabricator should designate coupon regions to span a minimum of two sides provided the placement requirements for position-sensitive coupons are met. When specified, an additional coupon set should be ganged together in a common strip and furnished with the printed boards for traceability purposes. Figure 12-3 provides an example of a ten layer stack-up utilizing these coupon designs.

Table 12-1 Appendix A Coupon Requirements[1,2]

Coupon ID	Purpose	Location	Usage[3]	Comment
AB/R, A/R	Rework Simulation	Optional	QC	May require additional coupons (see A/R1 in Figure 12-1)
	Plated Hole Evaluation	Opposing Corners, Opposing Axes	LC	
	Internal Annular Ring (Registration)			
B/R	Plated Hole Evaluation	Opposing Corners, Opposing Axes	LC	360° electrical internal registration assessment available for B_3 holes only. B_1 and B_2 hole registration **shall** be assessed through microsection. See Figure 12-3 for B_1 - B_3 hole definitions.
	Internal Annular Ring (Registration)			
G	Solder Mask Adhesion	Optional	LC	
P	Peel Strength	Optional	Special	
	Plating Adhesion		LC	
S	Though Hole Solderability	Optional	LC	
W	SMT Solderability, Finish Plating Thickness	Optional	LC	
E	Moisture and Insulation Resistance	Optional	QC	
H	Surface Insulation Resistance	Optional	Special	
D	Thermal Shock	Optional	Special	D_1 - A and B Holes, D_2 - B_1 and B_2 holes, D_3 - B_3 holes.
Z	Impedance	Optional	Special	

Note 1: Identical coupon ID's in Appendix A and Appendix B differ in design. Quantity of coupons **shall** be sufficient to perform the tests described in the IPC-6010 performance series.
Note 2: The latest version of Appendix A is available on the IPC web site at www.ipc.org/standards.
Note 3: LC = Lot Confomance Testing, QC = Quality or Periodic Testing.

Table 12-2 Appendix B (Legacy) Coupon Requirements[1]

Coupon ID	Purpose	Location	Usage[2]	Comment
A/B, A, B	Plated Hole Evaluation	Opposing Corners, Opposing Axes	LC	
B_N	Plated Hole Evaluation	Opposing Corners, Opposing Axes	LC	
A/B, A, S	Through-hole Solderability	Optional	LC	Multiple coupons required to meet minimum 30 holes per AQL sample unit
	Rework Simulation		QC	
C	Plating Adhesion, Coating Thickness	Optional	LC	May be substituted with ''N''
G	Solder Mask Adhesion	Optional	LC	
M	SMT Solderability, Finish Plating Thickness	Optional	LC	
T	Solder Mask Tenting (if used)	Optional	Special	Used for Lot Conformance when specified
E	Moisture and Insulation Resistance	Optional	QC	
H	Surface Insulation Resistance	Optional	Special	
N	Surface Mount Bond Strength (Optional for SMT)	Optional	LC	May be substituted with ''C''
D	Interconnect Resistance	Optional	Special	
F	Registration (Option 1 or 2)	Opposing Corners	Special	Not Recommended
R	Registration (Optional)	Opposing Corners	Special	
X	Bending Flexibility, Flexible Endurance	Optional	QC	
Z_N	Impedance (if used)	Optional	Special	Used for Lot Conformance when specified

Note 1: Identical coupon ID's in Appendix A and Appendix B differ in design. Quantity of coupons **shall** be sufficient to perform the tests described in the IPC-6010 performance series.
Note 2: LC = Lot Confomance Testing, QC = Quality or Periodic Testing.

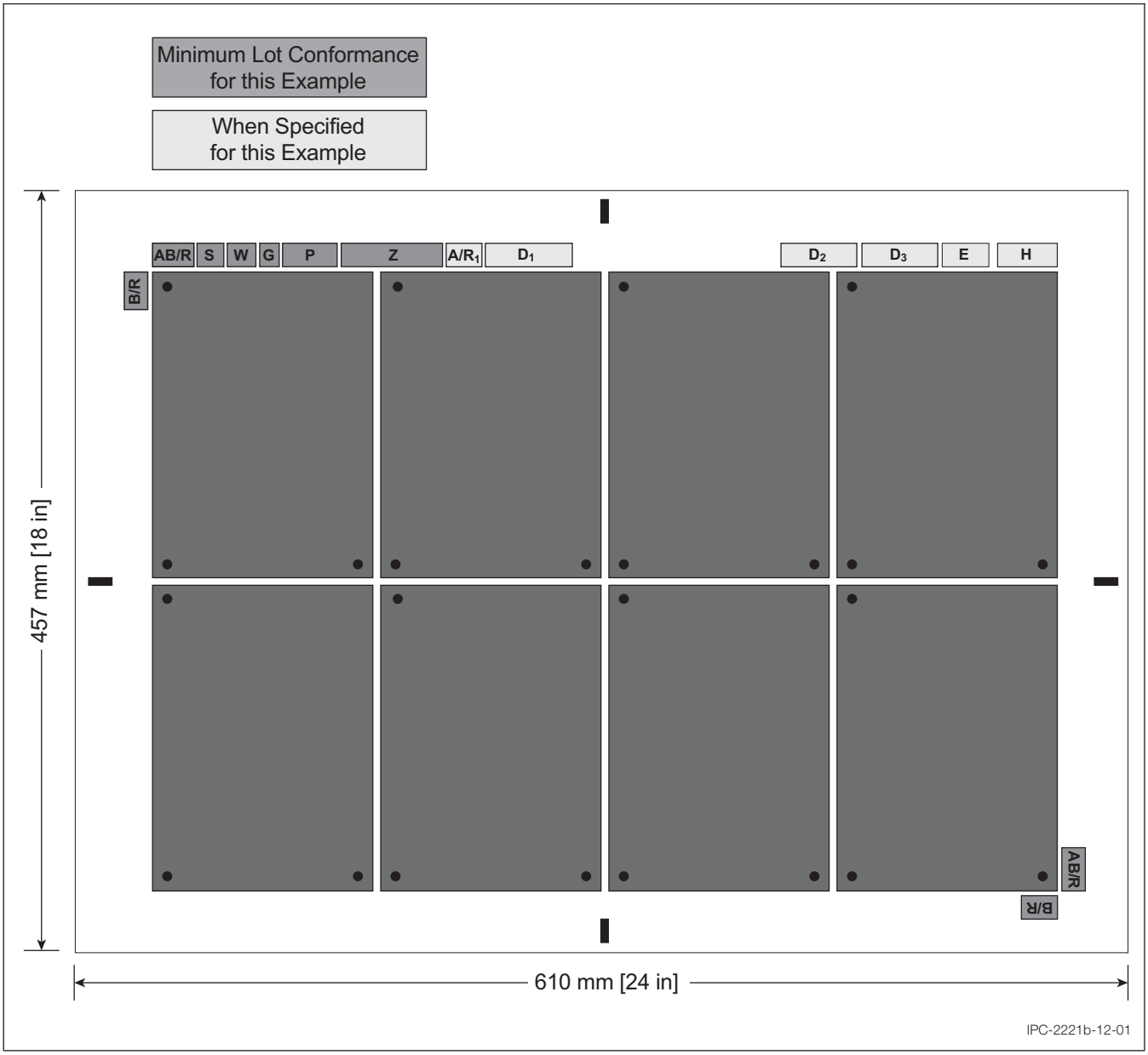


Figure 12-1 Panel Utilization among IPC-2221B Conformance Coupon Designs

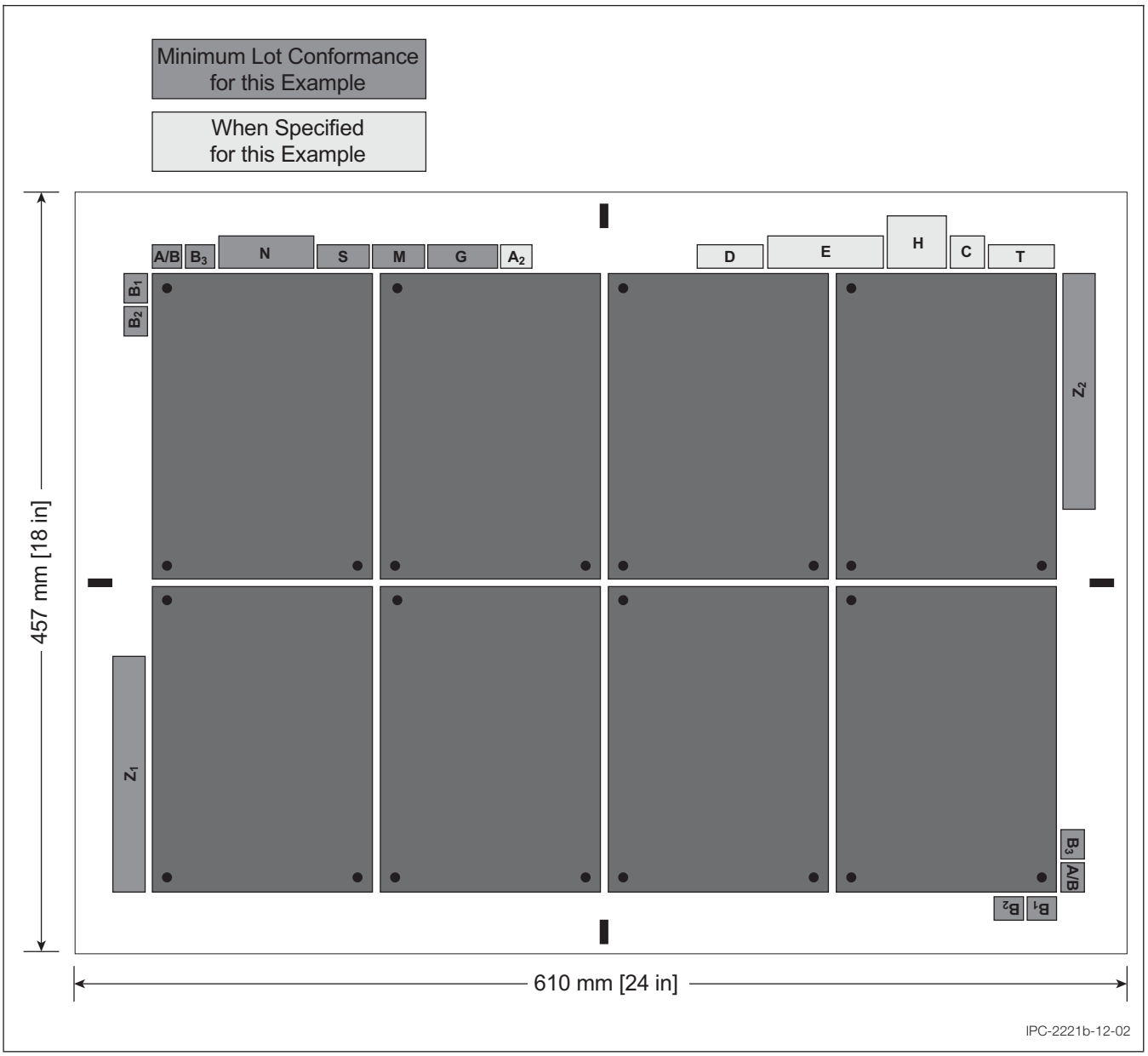


Figure 12-2 Panel Utilization among Legacy Conformance Coupon Designs

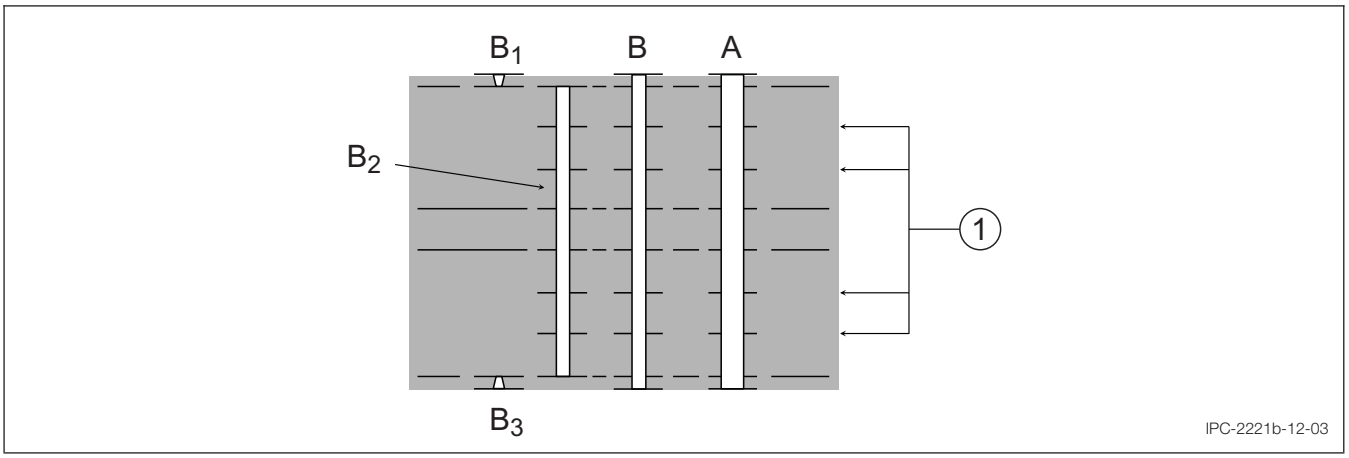


Figure 12-3 Example Stack-up for a Ten Layer Printed Board

Note 1. 50Ω Single ended and 100Ω differential impedance required on layers 3, 4, 7 and 8.

12.3.2 Coupon Identification Conformance test circuitry **shall** provide space for:

- Printed board part number and revision letter.
- Traceability identification.
- Lot date code.
- Manufacturer's identification, e.g., Commercial and Government Entity (CAGE), logo, etc.

Special coding systems may be used provided they are identified on the master drawing.

12.3.3 General Coupon Requirements Test coupons should reflect the specific printed board characteristics. This information consists of meeting the requirements for holes, conductors, spaces, etc. When coupons are used to establish process control parameters, they **shall** consistently use a single hole size or land configuration which reflects the process. Process characteristics and general printed board characteristics should be matched (e.g., threshold technology, leading edge technology, etc.).

12.3.3.1 Tolerances Tolerances for the fabrication of test coupons **shall** be the same as those for the printed board.

12.3.3.2 Etched Letters Etched letters shown on coupons are for reference only.

12.3.3.3 Interlayer Connection Holes Whenever a multilayer design incorporates interlayer connection holes in the form of blind or buried vias, Coupons A, B, and D **shall** be designed so as to incorporate these types of holes connecting the appropriate layers. The individual coupon description contains information on how these holes are to be incorporated. The specific number of holes for evaluation should be a minimum of three in each individual test coupon with a minimum of two test coupons required on each individual panel.

12.3.3.4 Metal Cores Whenever a multilayer design uses metal cores, the same core(s) **shall** be incorporated into the design of the coupon.

If the metal core(s) has interlayer connection holes that pass through the core without contact, the design of the coupon **shall** be representative of that characteristic. If the hole contacts the core, that characteristic **shall** also be represented in the coupon. The minimum number of holes for this evaluation are three per coupon with a minimum of two coupons on each individual panel. Additional A and B coupons may be required for horizontal microsections.

Composite printed boards **shall** have separate coupons for the top side printed board, the bottom side printed board, and the composite printed board. The coupon for the composite printed board **shall** include the core material.

12.4 Individual Coupon Design Individual test coupons are designed to evaluate specific individual characteristics of the printed boards they represent. Revision B of IPC-2221 includes updated conformance coupon designs which are recommended for use and detailed in Appendix A.[11] Design inputs for the generation of Appendix A coupons are extracted from individual printed board designs. This standard identifies generic physical design principles involved in the creation of test coupons and is to be supplemented by an IPC software coupon generation tool not yet available at the time of publication of Revision B. Appendix B contains the legacy conformance coupon designs described in previous versions of IPC-2221. Master drawings for legacy IPC-2221A coupon designs (e.g., IPC-100103 and IPC-100043) are provided through the IPC-A-47 and IPC-A-43 artwork phototool packages, respectively. Variations in specified coupon design **shall** meet the intent of the original design and be representative of the printed board.

12.4.1 Plated Hole Evaluation (Thermal Stress, Rework Simulation, Registration) Coupons All via structures **shall** be represented in the thermally stressed evaluations. Unique constructions (e.g., blind, buried, unfilled through-hole, filled through-hole, etc.) and plating steps define a via structure.

12.4.1.1 AB/R Coupon Coupon AB/R combines the heritage A, B and R coupon design features along with a C feature which represents the smallest via or component hole which has the smallest annular ring. See Appendix A for coupon parameters and layout.

12.4.1.2 Legacy A, B or A/B Coupons The A Revision of the IPC-2221 introduced the concept of an A/B coupon. It has been generated to provide a single coupon for either designers or those printed board fabricators who do not want to microsection two separate coupons to view small and large holes. It incorporates most aspects of the heritage A and B coupons

11. Appendix A may be updated independent of revision updates to this standard. The latest version of Appendix is available on the IPC web site at www.ipc.org/standards.

in one coupon. The heritage A and B coupons are acceptable for existing designs but should be updated by the manufacturer when practical. The second row of holes within the A/B coupon provides a single view of small and large holes for PTH evaluation and thermal stress. The outer row provides for rework simulation of component holes. The general design of the legacy A, B or A/B coupons are provided in Appendix B.

12.4.2 Moisture and Insulation Resistance Coupons These coupons are used for evaluating insulation resistance, bulk resistance and cleanliness of the material after exposure to an elevated cyclic temperature and humidity under an applied voltage. The coupon can also be used for evaluating dielectric withstanding voltage.

12.4.2.1 E Coupon This coupon is used to evaluate moisture and insulation resistance of laminated base materials. See Appendix A for coupon parameters and layout.

12.4.2.2 Legacy E Coupon Legacy coupon E is used for general testing purposes. It is less sensitive to dirt and ionic contaminants than the legacy coupon H. The ''Y'' pattern of legacy coupon E can provide a useful tool for cleanliness and insulation resistance property evaluations. The general design of the coupon is provided in Appendix B.

12.4.3 Hole Solderability Coupons

12.4.3.1 S Coupon Coupon S is used to evaluate through-hole solderability. See Appendix A for coupon parameters and layout.

12.4.3.2 Legacy S Coupon This coupon may be used to evaluate PTH solderability to IPC-J-STD-003 when a larger population of holes is required. The general design of the coupon is provided in Appendix B. If it is used, the test method and performance criteria **shall** be specified in the procurement documentation.

12.4.4 Surface Mount Solderability Coupons

12.4.4.1 W Coupon Coupon W is used to evaluate surface mount land solderability. See Appendix A for coupon parameters and layout.

12.4.4.2 Legacy M Coupon This coupon may be used to evaluate solderability of surface mount lands to IPC-J-STD-003 requirements. The general design of the coupon is provided in Appendix B. If it is used, the test method and performance criteria **shall** be specified in the procurement documentation.

12.4.5 Interconnect Resistance and Continuity Coupons

12.4.5.1 D Coupon Coupon D is used to evaluated plated hole and via reliability by thermal stress. See Appendix A for coupon parameters and layout.

12.4.5.2 Legacy D Coupon The legacy D coupon is used to evaluate interconnection resistance, continuity, correct lay-up, and other performance criteria. See Appendix B for the general design of coupon D and the modifications to be made for buried vias.

12.4.6 Solder Mask Adhesion Coupons

12.4.6.1 G Coupon Coupon G is used to evaluate solder mask adhesion over copper/surface finish, laminate and conductor width. See Appendix A for coupon parameters and layout.

12.4.6.2 Legacy G Coupon The legacy G test coupon is used for evaluating solder mask adhesion. See Appendix B for the general design of coupon G.

12.4.7 Surface Insulation Resistance Coupons

12.4.7.1 H Coupon Coupon H is used to quantify the effects of process and/or handling residues on surface insulation resistance. See Appendix A for coupon parameters and layout.

12.4.7.2 Legacy H Coupon Legacy coupon H is used for higher level insulation testing, such as telecommunications. See Appendix B for typical design. This legacy coupon is not referenced in IPC-6012. If it is used, the test method and performance criteria **shall** be specified in the procurement documentation.

12.4.8 Peel Strength and Plating Adhesion Coupons

12.4.8.1 P Coupon Coupon P is used to evaluate the peel strength of metallic foils laminated to the outer layers of a printed board during the foil lamination process and to evaluate plating adhesion. Design parameters and illustrations are provided in Appendix A. At least one coupon P for each foil laminated side of the printed board **shall** be placed on the panel where space is available.

12.4.8.2 Legacy C Coupon This coupon is used to evaluate peel strength of metallic foils. Design parameters and illustrations are provided in Appendix B.

12.4.9 Controlled Impedance Coupons A legacy coupon design for determining impedance values was not created for previous revisions of IPC-2221.

12.4.9.1 Z Coupon Coupon Z is used to determine the impedance value of controlled impedance structures of the printed board. See Appendix A for coupon parameters and layout.

12.4.10 Optional Legacy Registration Coupons The purpose of the registration coupon is to evaluate the internal annular ring. When legacy coupons A and B or A/B, or coupon AB/R are used for registration evaluation, the technique requires multiple microsections. i.e., in both the x and y axes.

The legacy F coupon is used to evaluate layer-to-layer registration and annular ring without microsection.

The advantages of the legacy R coupon is that it can be evaluated for annular ring by X-ray after drilling, and provides a quick electrical check to determine if the correct annular ring is present.

12.4.11 Legacy N Coupon (Peel Strength, Surface Mount Bond Strength - Optional for SMT) The legacy N coupon is used for evaluating peel strength and may be used to evaluate the bond strength of surface mount lands. See Appendix B for typical design. If it is used, the test method and performance criteria **shall** be specified in the procurement documentation.

12.4.12 Coupon X (Bending Flexibility and Endurance, Flexible Printed Board) This coupon is used to validate bending flexibility and bending endurance of flexible printed board applications. See Appendix B for typical design.

12.4.13 Process Control Test Coupon Process control test coupons are used at strategic points in the process flow to evaluate a specific process or set of processes. The designs of the process control test coupons are at the option of the printed board fabricator. Each design is specific to the processes for which the fabricator intends to evaluate.

Process control evaluations are established through a systematic path for implementing statistical process control. This includes those items shown in Figure 12-4.

If the contract permits the use of process control coupons in lieu of conformance coupons, the design of the coupon **shall** be agreed to between the user and manufacturer.

The design of existing test coupons can serve as a guide for the design of process control test coupons. In general, the design of the coupon is consistent with the process to be evaluated rather than an attempt to represent a printed board design. Finished conductor width **shall** be 0.5 mm ± 0.07 mm [0.020 in ± 0.0028 in] and finished land size **shall** be 1.8 mm ± 0.13 mm [0.0709 in ± 0.00512 in]. Hole size **shall** be consistent with process(es) being evaluated. The location of test coupons on the panel and hole diameters **shall** remain constant. The design dimensions may require compensation for process allowances.

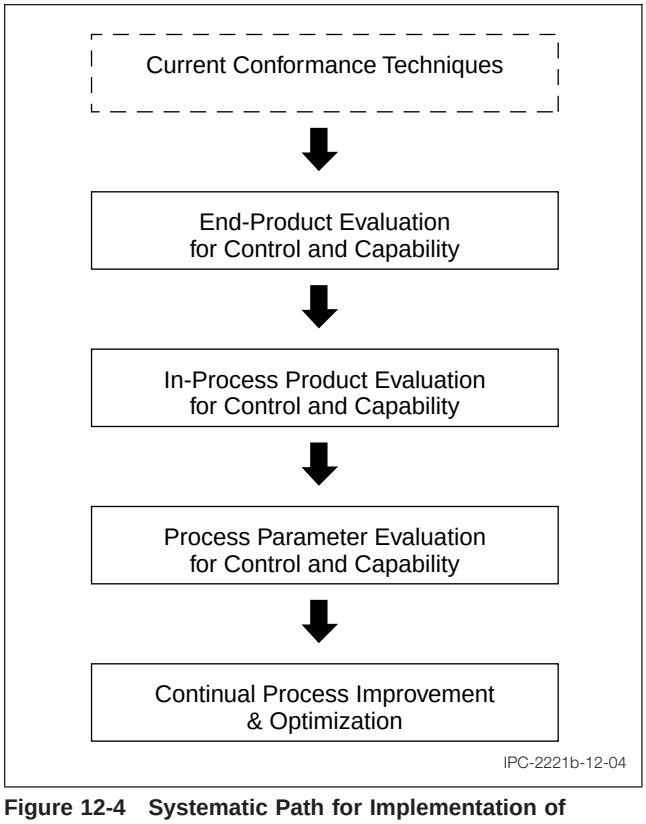


Figure 12-4 Systematic Path for Implementation of Statistical Process Control (SPC)

APPENDIX A

A.1 INTRODUCTION This appendix was developed by the IPC 1-10c Test Coupon and Artwork Generation Task Group and is included in this current document revision as a resource for the design of conformance and qualification coupons. The intent is to provide guidance as to the coupon designs, however if conflicts arise or the information provided is incomplete, the design of the coupon features should be in accordance with the associated product board design requirements.

It is the task group's recommendation that the coupons be designed by the printed board fabricator in order to ensure that the correct drill sizes are used. Additionally, etch and solder mask fabrication compensation **shall** be applied uniformly to both the coupons and product board after the coupons have been designed.

Solder mask layers are documented for each of the coupons, however they are only to be used if the associated product board design requires solder mask.

Table A.1-1 provides a summary of coupon designs that are described within this appendix.

Table A.1-1 IPC Coupons

Section	Coupon	Description	Purpose
A.2	AB/R	General purpose AB coupon for through features	Plated hole/via evaluation, feature size and spacing, registration, thermal stress and rework simulation
A.3	A/R	General purpose A coupon for use when B features are not present	Plated hole evaluation, feature size and spacing, registration, thermal stress and rework simulation
A.4	B/R	B coupon for non-through (propagated) via features	Plated hole evaluation, registration and thermal stress
A.5	E	Moisture and insulation resistance coupon	Moisture and insulation resistance
A.6	S	Hole solderability coupon	Hole solderability
A.7	W	Surface mount solderability coupon	Surface mount solderability
A.8	D	General purpose AB daisy-chain via coupon	Plated hole/via thermal stress
A.9	G	Solder mask coupon	Solder mask adhesion
A.10	H	Surface insulation resistance coupon	Surface insulation resistance
A.11	P	Peel strength coupon	Peel strength and plating adhesion
A.12	Z	Controlled impedance coupon	Controlled impedance

A.2 AB/R COUPON Coupon AB/R combines the heritage A, B and R coupon design features along with a C feature which represents the smallest via or component hole which has the smallest annular ring. In order to better represent the product board the B1 feature contains internal lands only on layers 2 and n-1, the B2 feature contains lands only on internal signal layers and the B3 feature contains internal lands only on plane layers. The design also includes features to allow the assessment of minimum conductor and space widths from the product board. To accomplish this, the B4 lands are square and the minimum conductor for each layer is located adjacent to the B4 lands at the minimum spacing for each layer.

The R feature provides a method to electrically assess 360° registration without the need for microsectioning. Due to the contribution of etch variation with heavier innerlayer foils use of the R features is recommended for design with foil weights of 1 oz. or less. The design parameters for coupon AB/R are shown in Table A.2-1.

Table A.2-1 AB/R Coupon Parameters, mm [in]

Feature	Description	Design Requirements
A	Largest component hole with its smallest associated D+ Round lands on all layers	Drill size **shall** be ≤1.07 [0.042] Land size **shall** be ≤1.65 [0.065]
B1	Smallest via with its smallest associated D+ Round lands on layers 2 and n-1	Land size **shall** be ≤1.02 [0.040] Grid size: 1.27 [0.050]
B2	Smallest via with its smallest associated D+ Round lands on signal layers	
B3	Smallest via with its smallest associated D+ Round lands on plane layers	
B4	Smallest via with its smallest associated D+ Square lands on all layers	
C	Smallest D+ with its smallest associated via or component hole Round lands on all layers	Drill size **shall** be ≤1.07 [0.042] Land size **shall** be ≤1.65 [0.065]
RA	Registration based on the A feature	Anti-land calculation (minimum of): (Land diameter + 0.0127 [0.0005]) - (2 x annular ring requirement) or (Drill diameter + 2 x minimum edge of hole-to-copper spacing + 0.0127 [0.0005]) - (2 x minimum copper-to-copper spacing requirement)
RB	Registration based on the B feature	
RC	Registration based on the C feature	
RB1	Registration based on the B feature with a 0.0254 [1.0] allowance	Anti-land calculation: RB anti-land + 0.0508 [0.002]
G	Common connection for "R" measurements	Maximum drill size is 0.51 [0.020] Land size is 1.02 [0.040]
L	Minimum conductor width (in line with B4 lands)	Minimum conductor for each layer
S	Minimum space width (in line with B4 lands)	Minimum space for each layer
T	Tooling hole	Drill size is 2.00 [0.0787]

Note 1. Thieving may be added to the coupon provided it is in accordance with the associated product board design.
Note 2. The "R" measurements should be used with caution for copper weights greater than 1 oz. or when positive etchback greater than 0.0127 [0.0005] is present.
Note 3. For direct plane layer connections B3 and B4 pad size are 1.02 [0.040].
Note 4. B1, B2 and B3 **shall** have lands on every layer for designs using non-functional lands.
Note 5. When the smallest B land exceeds 1.02 [0.040], a modified A/R coupon with a unique designation (e.g., A/R-1) **shall** be used to assess the via feature. Complete documentation of this new coupon and its design requirements will be provided in a subsequent revision to this Appendix.

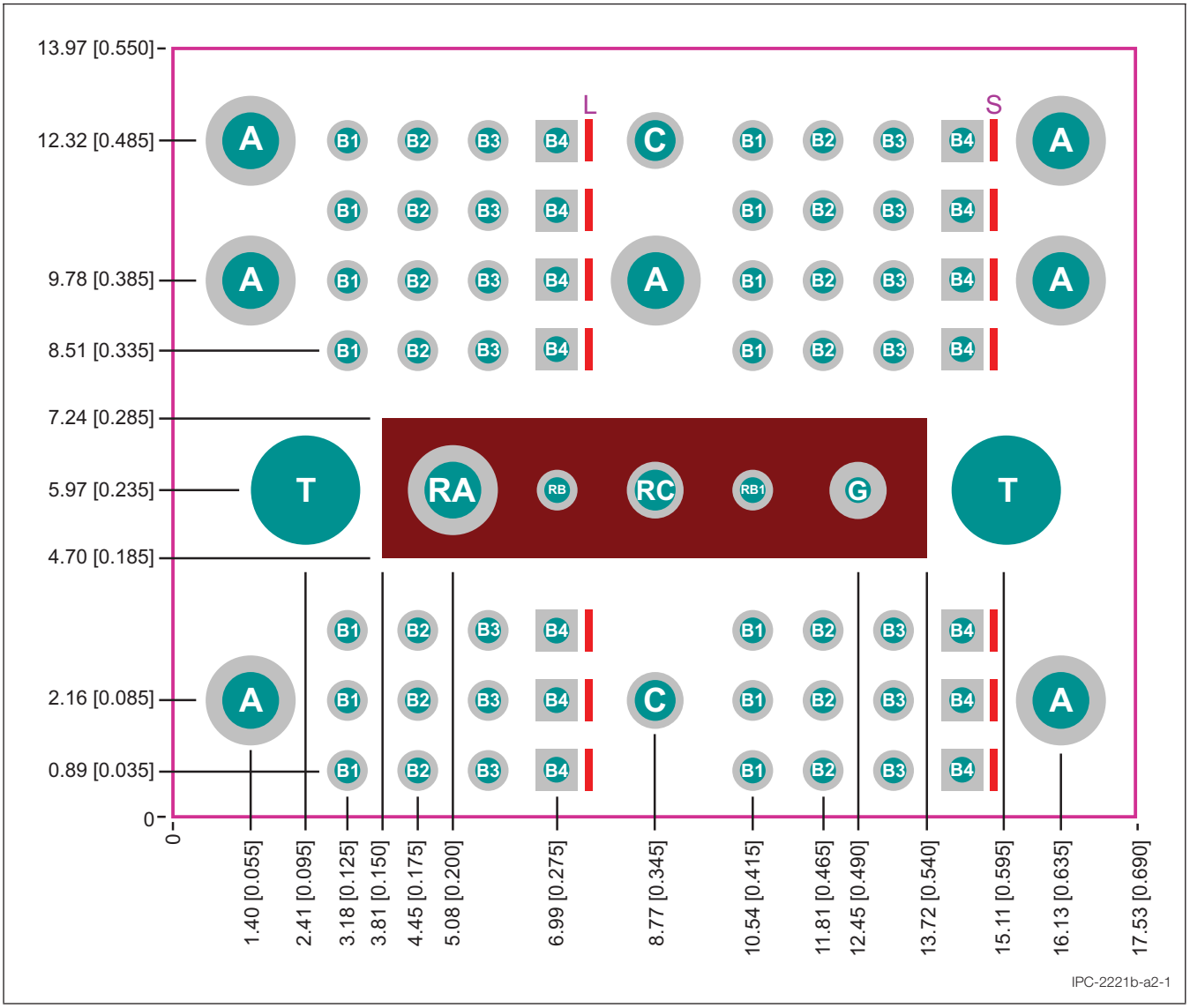


Figure A.2-1 AB/R Coupon Layout, mm [in]

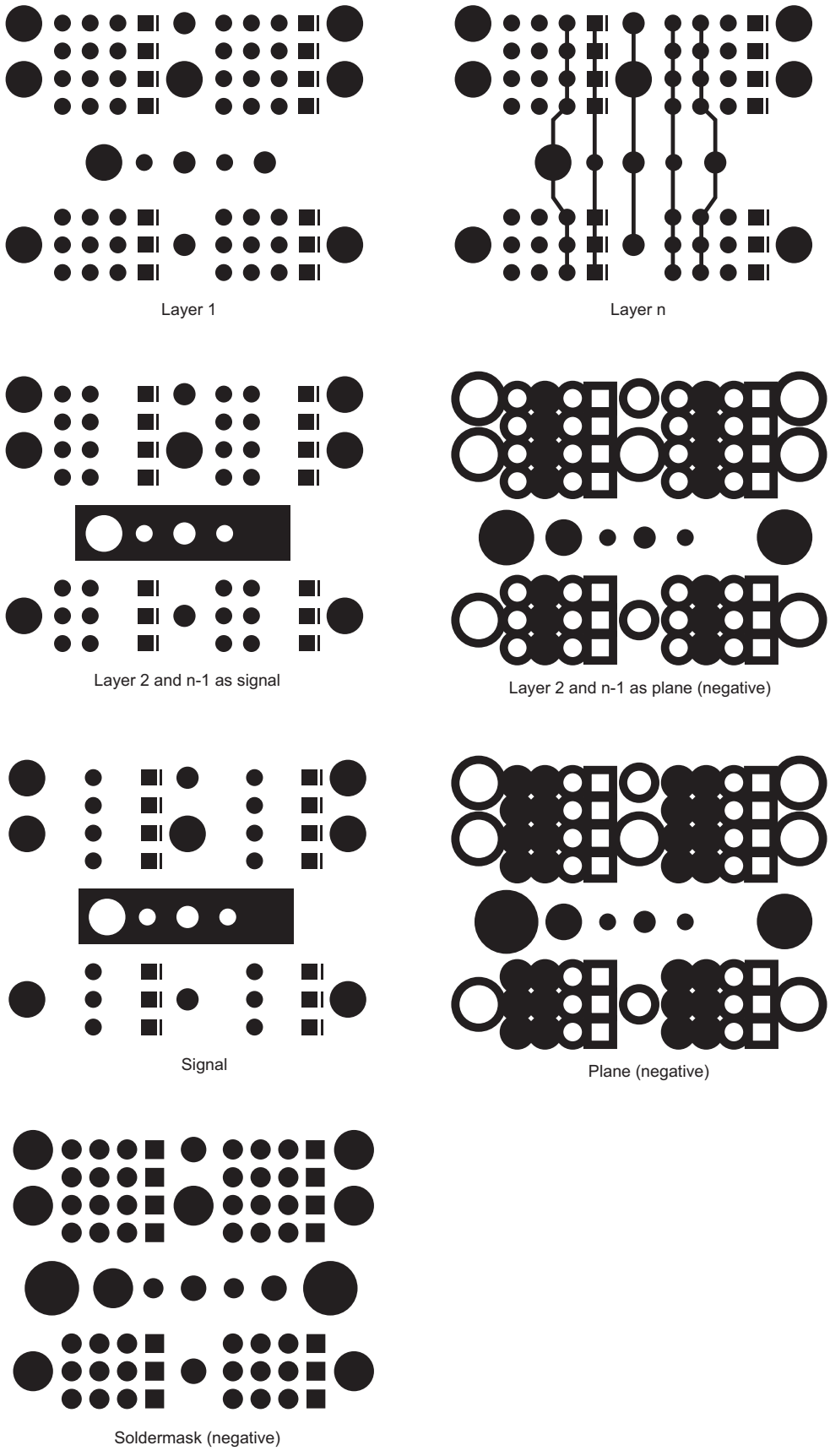


Figure A.2-2 AB/R Coupon Example Layers

A.3 A/R COUPON Coupon A/R follows the same design intent as the AB/R except that it is intended for use when the product board does not contain any vias. The design parameters for coupon A/R are shown in Table A.3-1.

Table A.3-1 A/R Coupon Parameters, mm [in]

Feature	Description	Design Requirements
A1	Largest component hole with its smallest associated D+ Round lands on layers 2 and n-1	Drill size **shall** be ≤1.07 [0.042] Land size **shall** be ≤1.65 [0.065] Grid: 1.91 [0.075]
A2	Largest component hole with its smallest associated D+ Round lands on signal layers	
A3	Largest component hole with its smallest associated D+ Round lands on plane layers	
A4	Largest component hole with its smallest associated D+ Square lands on all layers	
RA	Registration based on the A feature	Anti-land calculation (minimum of): (Land diameter + 0.0127 [0.0005]) - (2 x annular ring requirement) or (Drill diameter + 2 x minimum edge of hole-to-copper spacing + 0.0127 [0.0005]) - (2 x minimum copper-to-copper spacing requirement)
RA1	Registration based on the A feature with a 0.0254 [1.0] allowance	Anti-land calculation: RA anti-land + 0.0508 [0.002]
G	Common connection for ''R'' measurements	Maximum drill size is 0.51 [0.020] Land size is 1.02 [0.040]
L	Minimum conductor width (in line with B4 lands)	Minimum conductor for each layer
S	Minimum space width (in line with B4 lands)	Minimum space for each layer
T	Tooling hole	Drill size is 2.00 [0.0787]

Note 1. Thieving may be added to the coupon provided it is in accordance with the associated product board design.
Note 2. The ''R'' measurements should be used with caution for copper weights greater than 1 oz. or when positive etchback greater than 0.0127 [0.0005] is present.
Note 3. For direct plane layer connections A3 and A4 pad size are 1.65 [0.065].
Note 4. A1, A2 and A3 **shall** have lands on every layer for designs using non-functional lands.

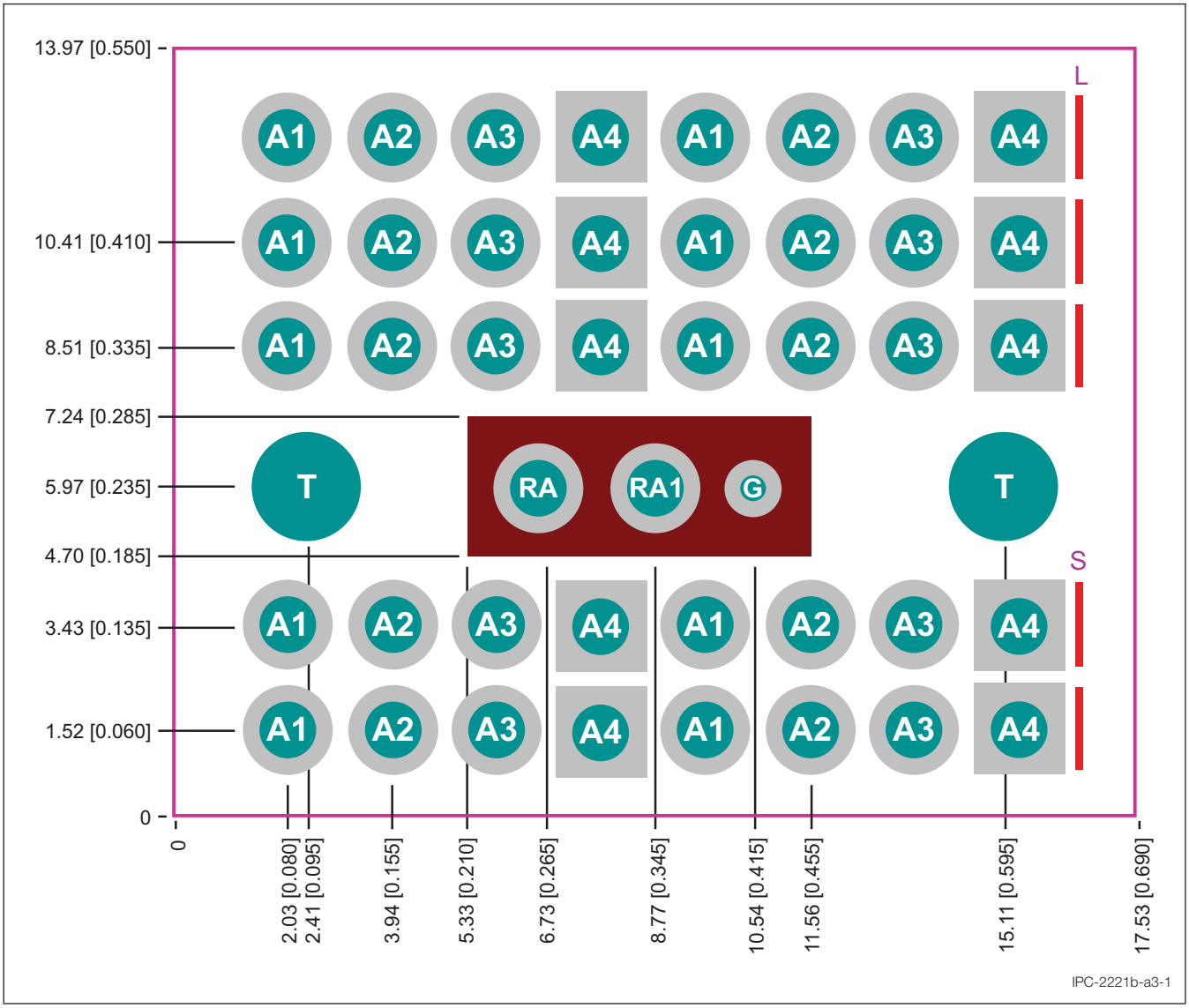


Figure A.3-1 A/R Coupon Layout, mm [in]

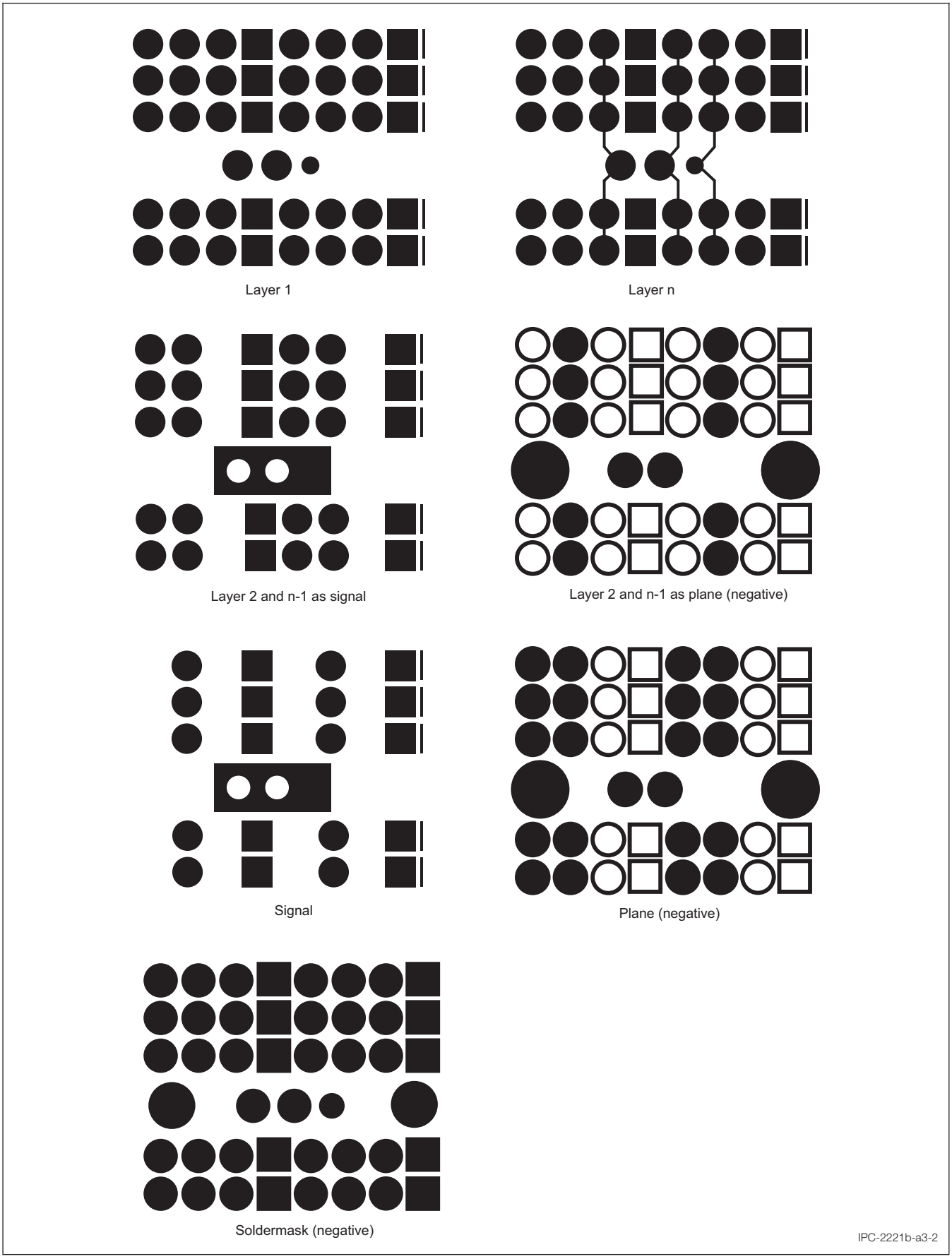


Figure A.3-2 A/R Coupon Example Layers

A.4 B/R COUPON Coupon B/R follows the same design intent as the AB/R except that it is intended for uses with non-through (propagated) via structures. The design provides the opportunity to add up to three different propagated via structures per coupon. The pitch of the B/R design in this Appendix does not support microvia stacked on buried via structures. In the case of microvias the design provides nine holes, each offset in alignment by 0.00635 mm [0.00025 in] to improve the probability of meeting the 10% via diameter requirement during microsectioning. The design parameters for coupon B/R are shown in Table A.4-1.

Table A.4-1 B/R Coupon Parameters, mm [in]

Feature	Description	Design Requirements
BX	Smallest via of type "X" with its smallest associated D+ Round lands on representative layers	Land size **shall** be ≤1.02 [0.040] Grid size: 1.27 [0.050] or Land size **shall** be ≤0.31 [0.012] X grid size: 0.38 [0.015] Y grid size: 0.00635 [0.00025]
BY	Smallest via of type "Y" with its smallest associated D+ Round lands on representative layers	
BZ	Smallest via of type "Z" with its smallest associated D+ Round lands on representative layers	
RBX RBY RBZ	Registration based on the BX, BY and BZ features **Note:** Only applicable to sub-composite via structures which span 3 or more layers	Anti-land calculation (minimum of): (Land diameter + 0.0127 [0.0005]) - (2 x annular ring requirement) or (Drill diameter + 2 x minimum edge of hole-to-copper spacing + 0.0127 [0.0005]) - (2 x minimum copper-to-copper spacing requirement)
G	Common connection for "R" measurements	Maximum drill size is 0.51 [0.020] Land size is 1.02 [0.040]
T	Tooling hole	Drill size is 2.00 [0.0787]

Note 1. Internal or external thieving may be added to the coupon provided it is in accordance with the associated product board design.
Note 2. The "R" measurements should be used with caution for copper weights greater than 1 oz. or when positive etchback greater than 0.0127 [0.0005] is present.
Note 3. BX, BY, and BZ **shall** have lands on every layer for designs using non-functional lands.

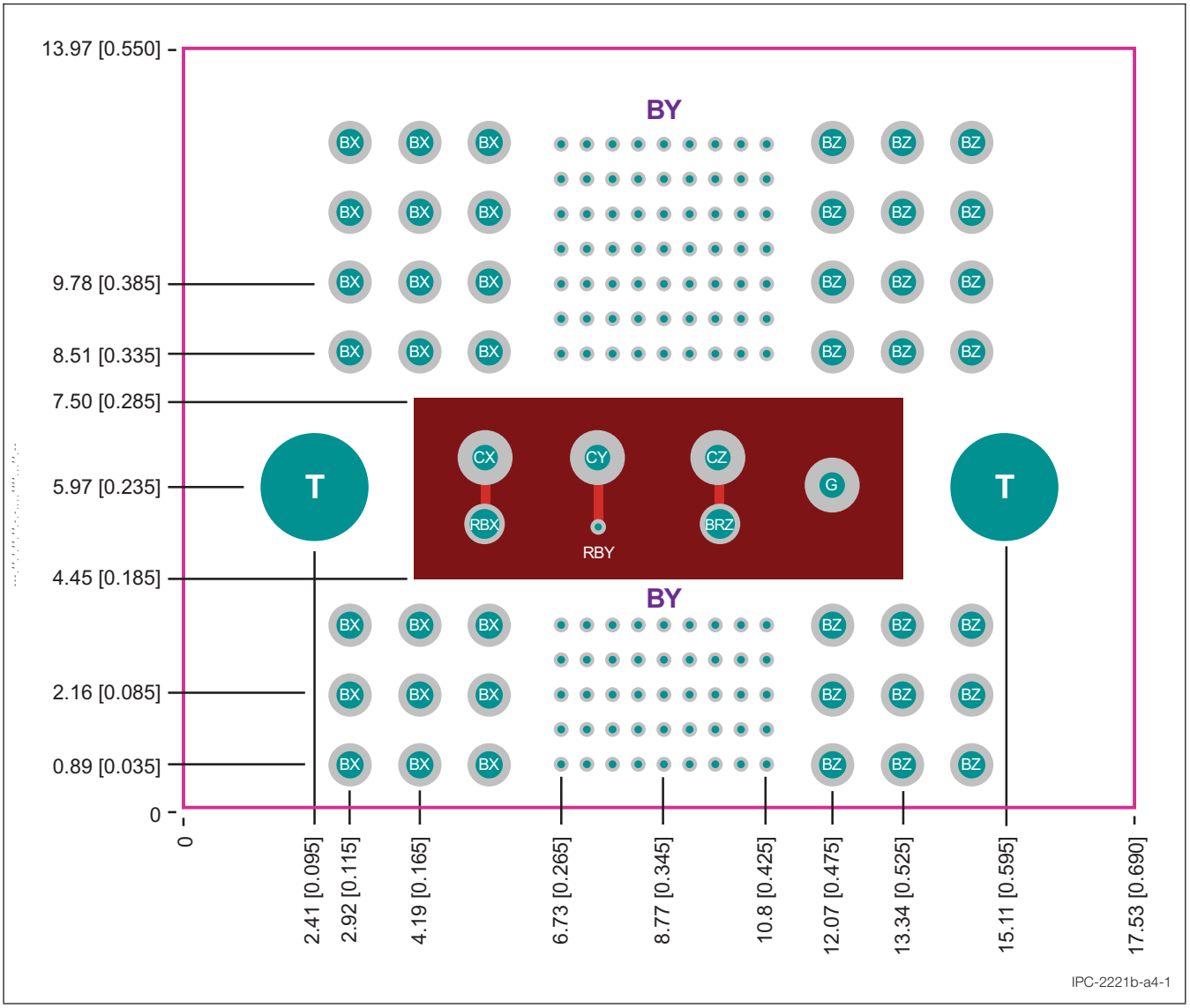


Figure A.4-1 B/R Coupon Layout, mm [in]

A.5 E COUPON Coupon E is used to evaluate moisture and insulation resistance of laminated base materials. The coupon is designed to test a maximum of ten layers. For designs with more than 10 layers additional coupons are required and each **shall** contain the last layer of the preceding coupon (e.g., L1 - 10, L10 - 19, L19 - 28, etc.). The design parameters for coupon E are shown in Table A.5-1.

Table A.5-1 E Coupon Parameters, mm [in]

Feature	Description	Design Requirements
1 - 10	Plated-through test points	Recommended drill size: 1.02 [0.040] Recommended land size: 1.52 [0.060] Grid: 2.54 [0.100]
Electrodes	Parallel electrodes	Width: 0.635 [0.025] Length: 25.40 [1.000] Gap width: 0.635 [0.025] Plane clearance: 0.635 [0.025]

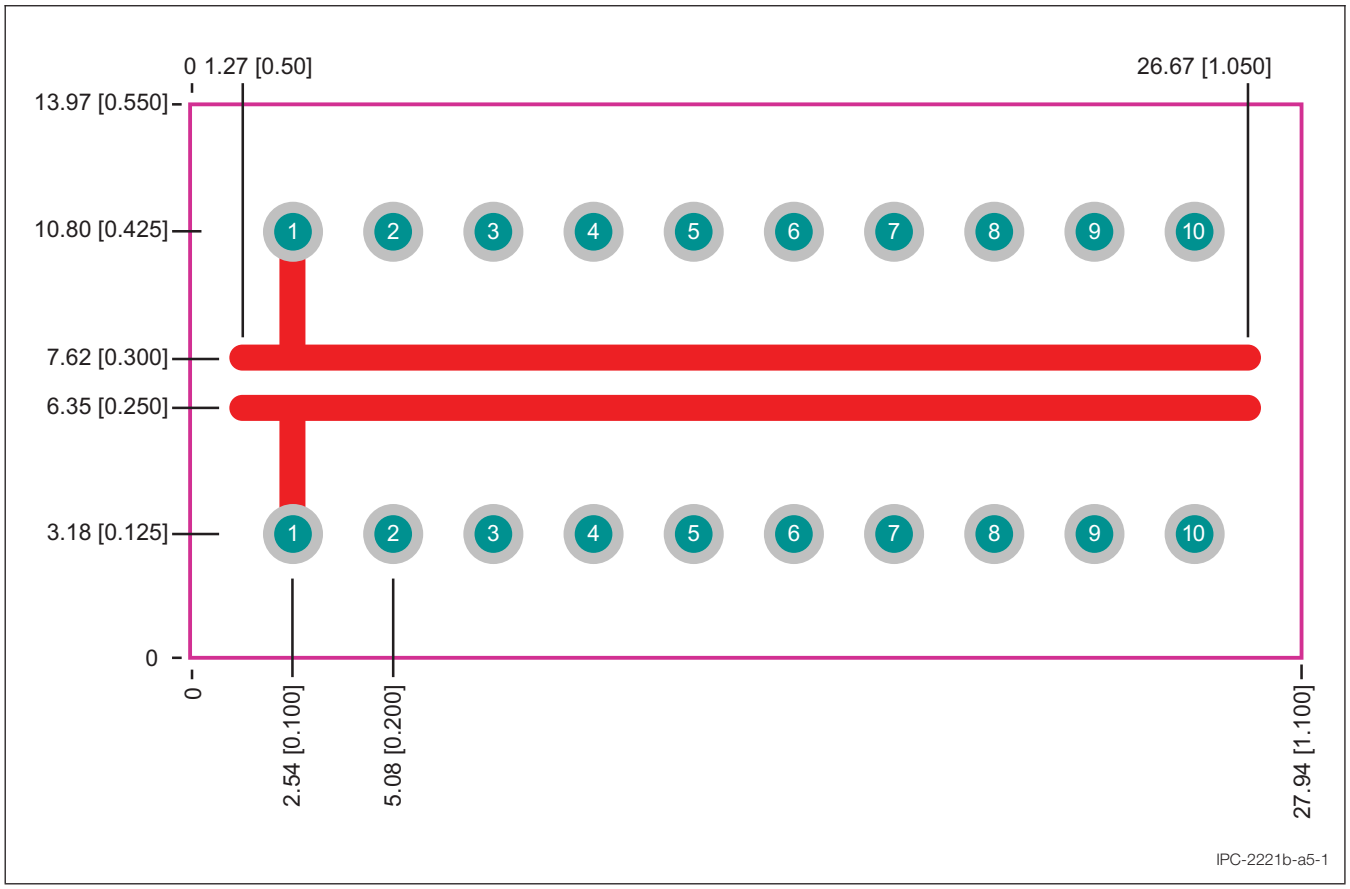


Figure A.5-1 E Coupon Layout, mm [in]

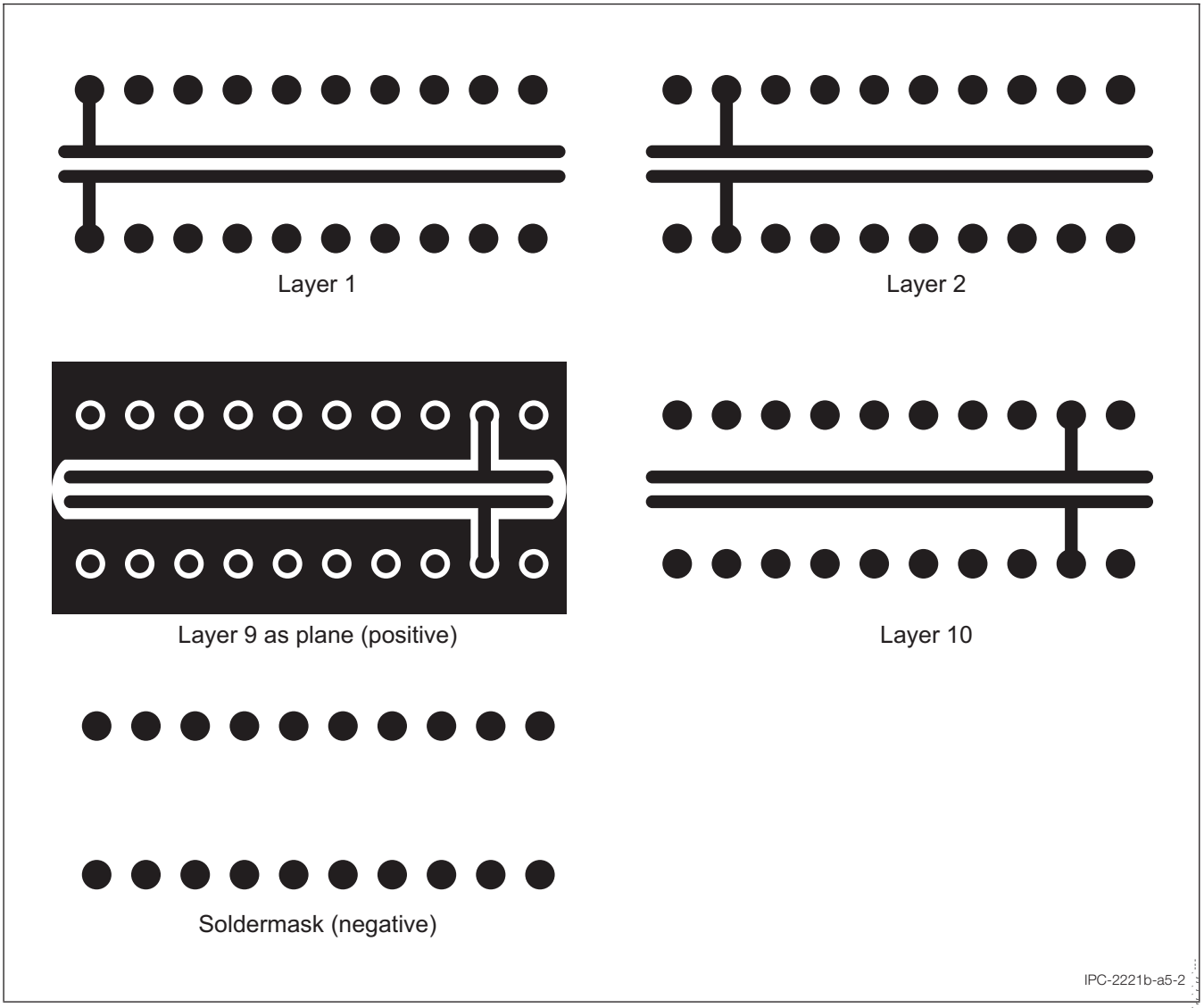


Figure A.5-2 E Coupon

A.6 S COUPON Coupon S is used to evaluate through hole solderability. No innerlayer lands are to be included in the design coupon. The design parameters for coupon S are shown in Table A.6-1.

Table A.6-1 S Coupon Parameters, mm [in]

Feature	Description	Design Requirements
S	Plated-through holes (32 each)	Drill size: 0.81 [0.032] Recommended land size: 1.52 [0.060] Grid: Staggered (see Figure A.6-1)

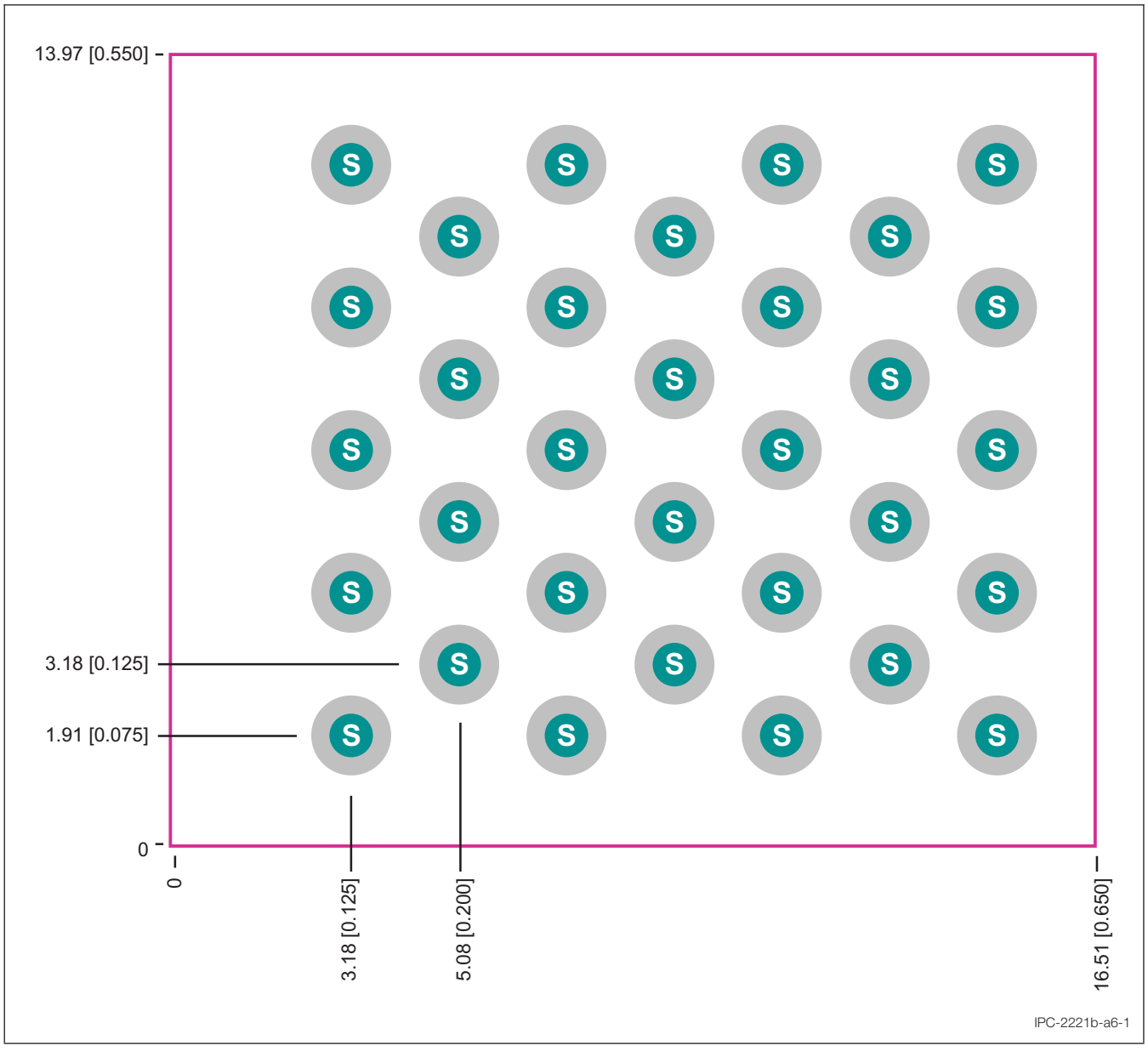


Figure A.6-1 S Coupon Layout, mm [in]

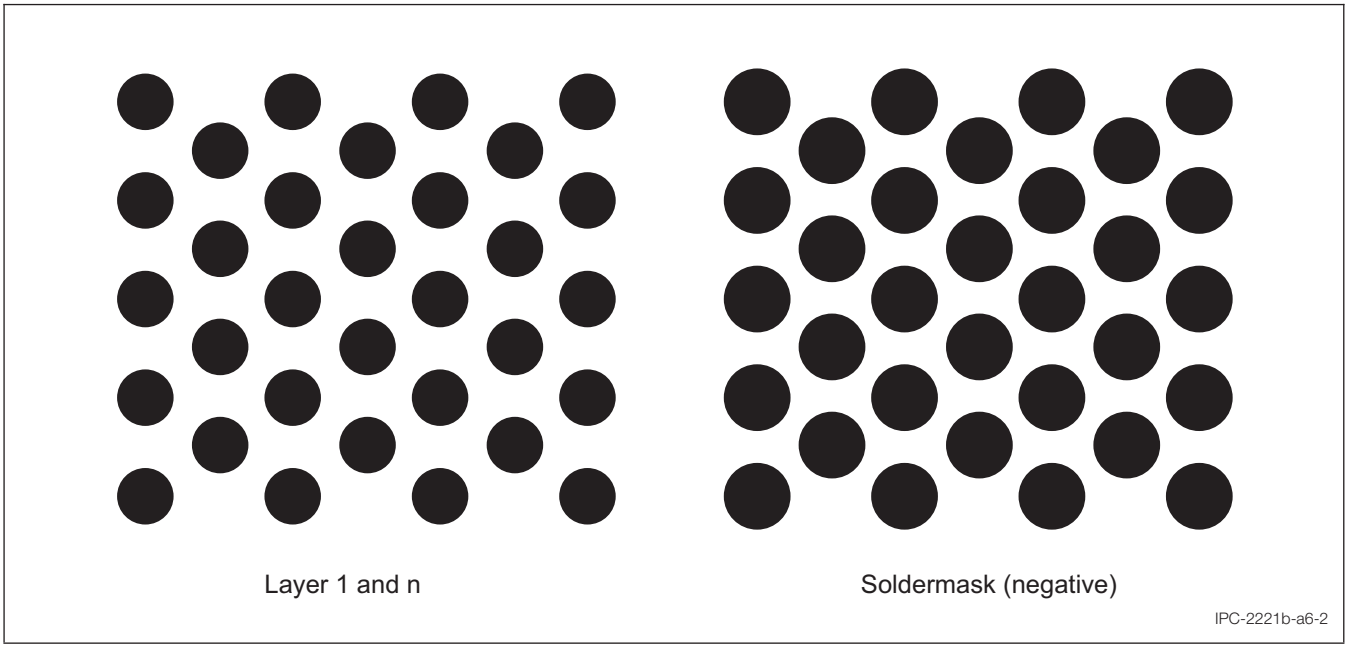


Figure A.6-2 S Coupon Example Layers

A.7 W COUPON Coupon W is used to evaluate surface mount land solderability. By intent, no innerlayers or via structures are included. The design parameters for coupon W are shown in Table A.7-1.

Table A.7-1 W Coupon Parameters, mm [in]

Feature	Description	Design Requirements
1	Round surface mount lands (7 each)	Land size: 1.52 [0.060] Drill Size: 0.81 [0.032] Pitch: 1.91 [0.075] Solder mask clearance: 0.152 [0.006] greater than land
2	Rectangular surface mount lands (7 each)	Land size: 4.45 x 1.52 [0.175 x 0.060] Pitch: 1.91 [0.075] Solder mask clearance: 0.152 [0.006] greater than land
3	Rectangular surface mount lands (22 each)	Land size: 2.00 x 0.50 [0.079 x 0.020] Pitch: 0.81 [0.032] Solder mask clearance: 0.152 [0.006] greater than land

Figure A.7-1 W Coupon Layout, mm [in]

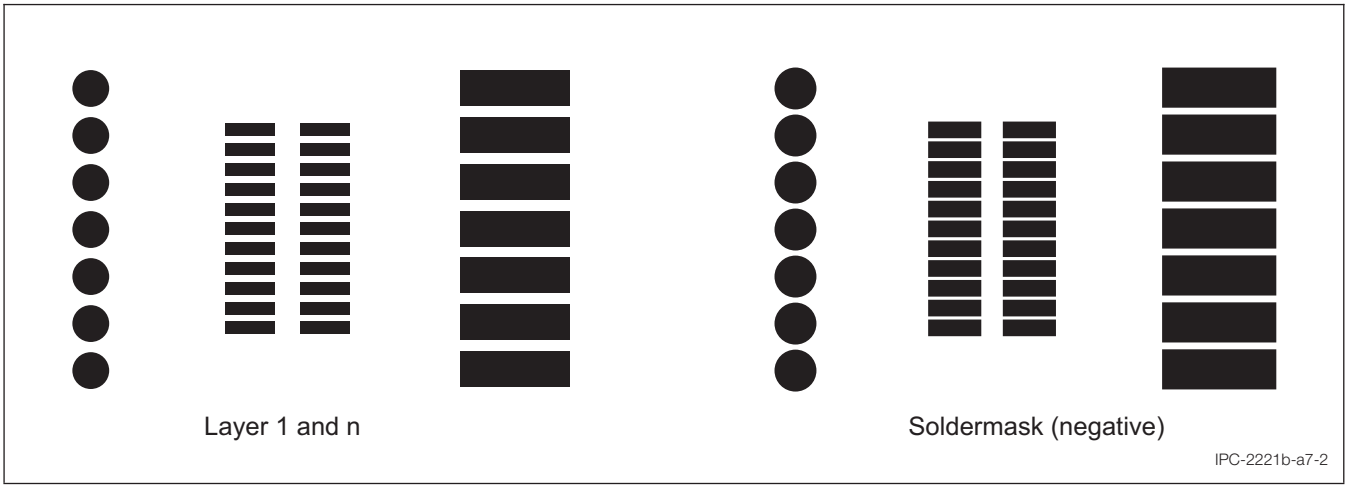


Figure A.7-2 W Coupon Layout

A.8 D COUPON Coupon D is used to evaluate plated hole and via reliability by thermal stress. The coupon is designed to have a sufficient number of plated holes or vias in a chain to obtain precision resistance measurement. The coupon may also be used for propagated via structures as described in Section A.4 by replacing the A and B features with the required propagated via features. The design parameters for coupon D are shown in Table A.8-1.

Table A.8-1 D Coupon Parameters, mm [in]

Feature	Description	Design Requirements
A	Largest component hole with its smallest associated D+ Round lands on layers 2 and n-1	Drill size **shall** be ≤1.07 [0.042] Land size **shall** be ≤1.65 [0.065] Grid: 1.91 [0.075] Interconnect conductors: 0.254 [0.010] Interconnect sequence: Layer 2 to n-1
B	Smallest via with its smallest associated D+ Round lands on layers 2 and n-1	Land size **shall** be ≤1.02 [0.040] Grid size: 1.27 [0.050] Interconnect conductors: 0.254 [0.010] Interconnect sequence: Layer 2 to n-1
Connector	VH: Four-wire resistance high voltage input IH: Four-wire resistance current source VL: Four-wire resistance low voltage input IL: Four-wire resistance current sink	Finished hole size: 1.02 ± 0.076 [0.040 ± 0.003] Land size: 1.91 [0.075] Grid size: 2.54 [0.100] Interconnect conductors: 0.254 [0.010] on Layer 1

Note 1. Each of the chains **shall** contain only one unique via structure.

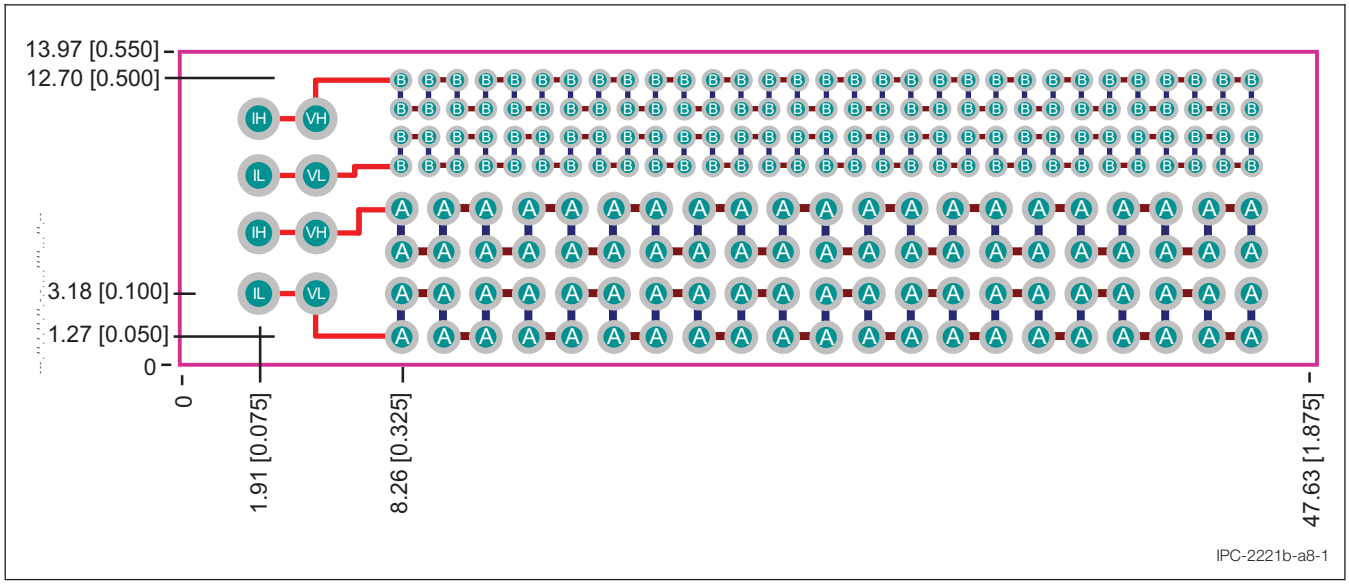


Figure A.8-1 D Coupon Layout with A and B Features, mm [in]

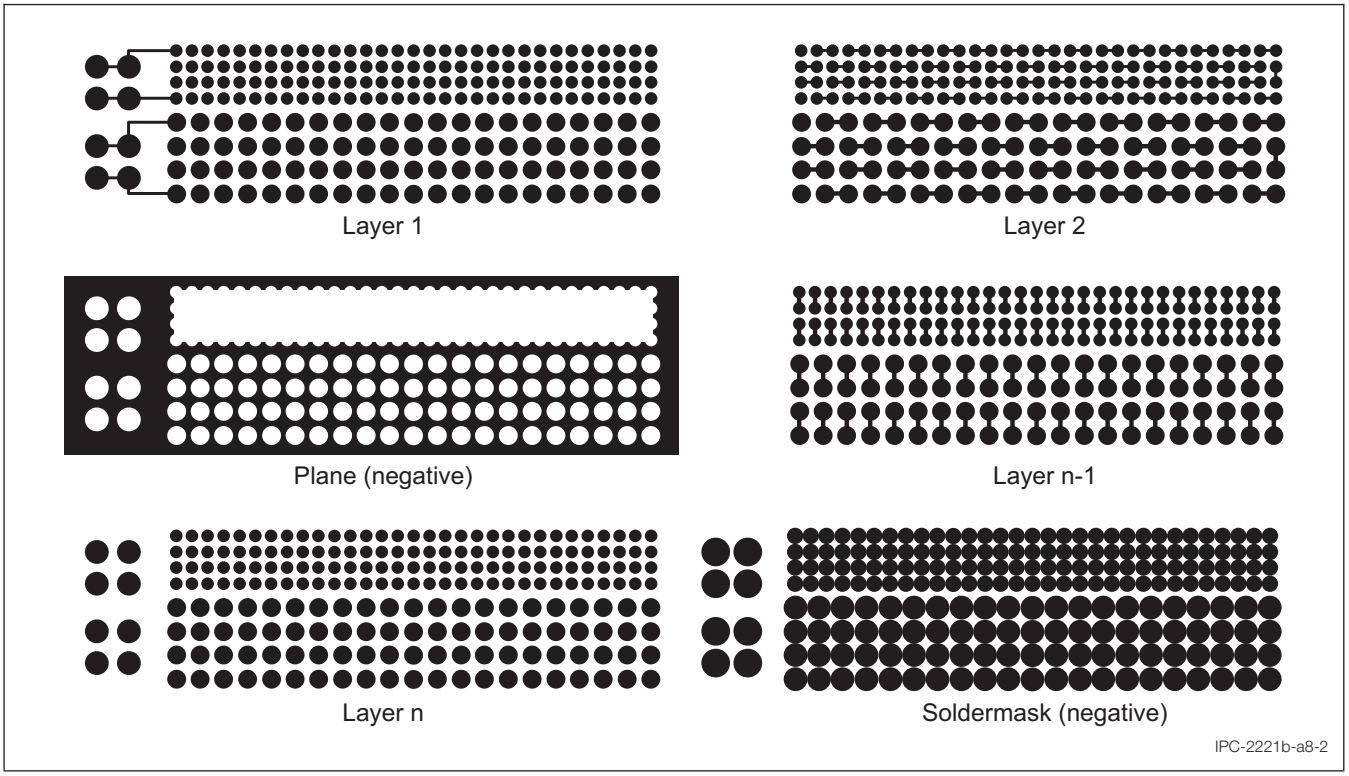


Figure A.8-2 D Coupon Example Layers with A and B Features

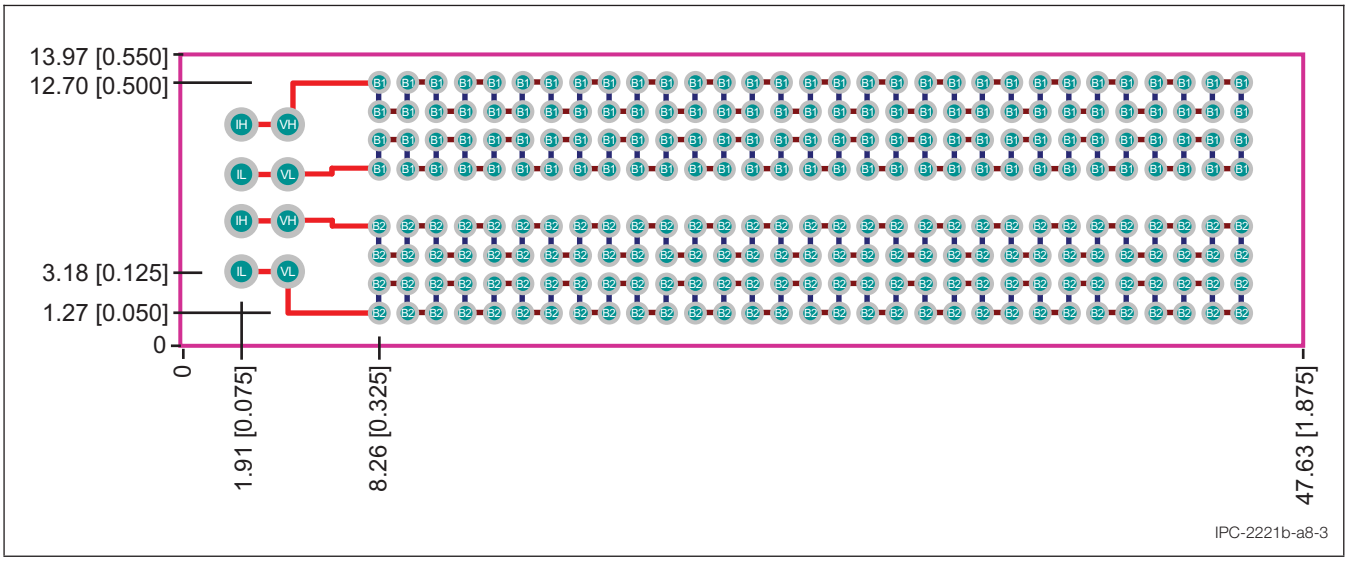


Figure A.8-3 D Coupon Layout with Non-through Via B Features, mm [in]

A.9 G COUPON Coupon G is used to evaluate solder mask adhesion and is divided into three regions 1) solder mask over copper or surface finish, 2) solder mask over laminate and 3) minimum solder mask web and minimum interconnect conductor width. The surface finish **shall** represent the product board design and the minimum web spacing and minimum conductor are per the product board. The design parameters for coupon G are shown in Table A.9-1.

Table A.9-1 G Coupon Parameters, mm [in]

Feature	Description	Design Requirements
1	Rectangular lands	Grid size: 1.27 [0.050] Solder mask anti-land calculation: 1.27 [0.050] - minimum solder mask web Land calculation: Solder mask anti-land - (2 x minimum solder mask clip back)
2	Round lands	
C	Minimum conductor	Minimum interconnect conductor associated with the solder mask web features
SMOC	Solder mask over copper or surface finish	Solder mask anti-land size: 0.61 [0.024] Grid size: 0.64 [0.025]
SMOL	Solder mask over laminate	Solder mask anti-land size: 0.61 [0.024] Grid size: 0.64 [0.025]

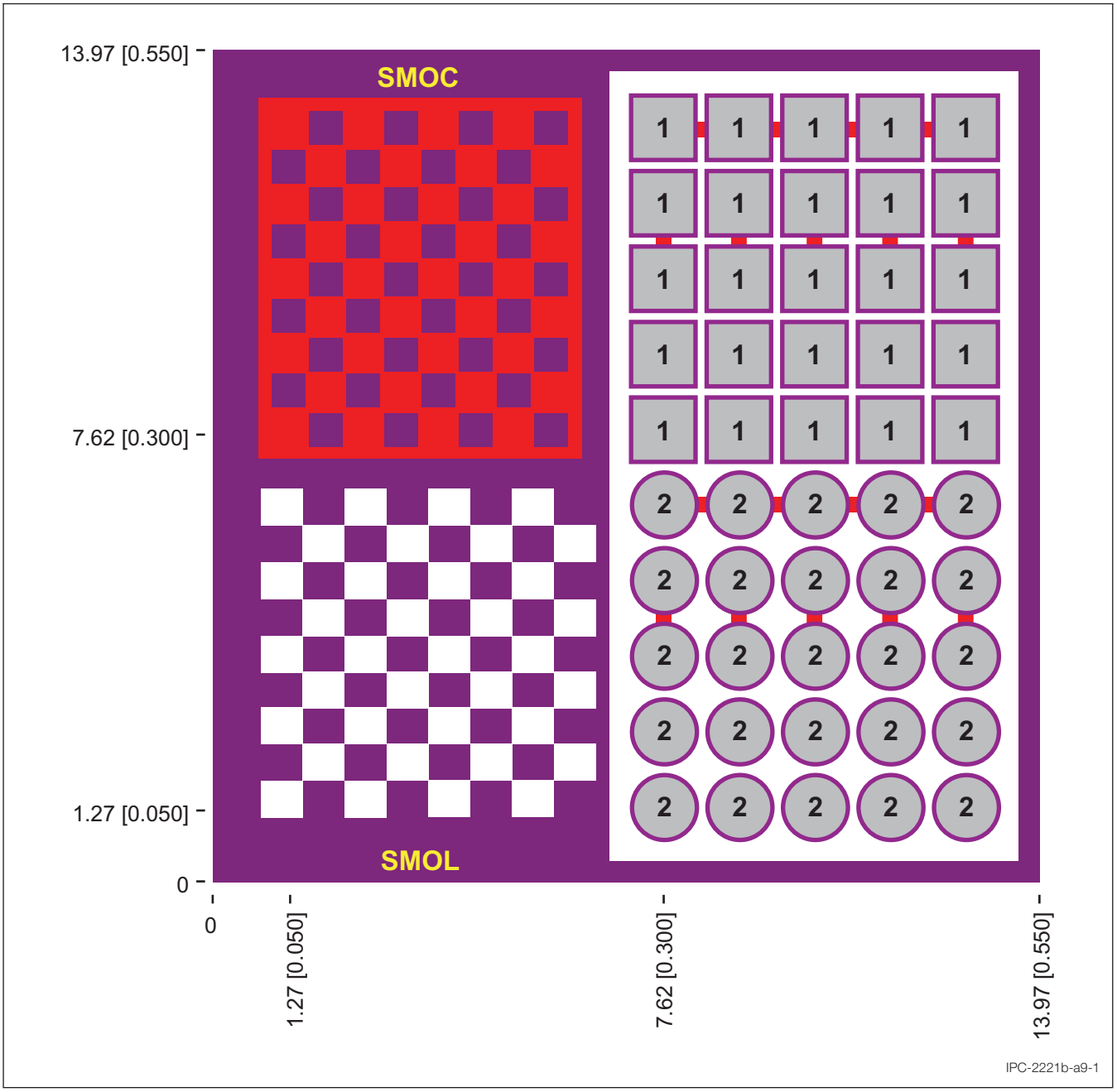


Figure A.9-1 G Coupon Layout, mm [in]

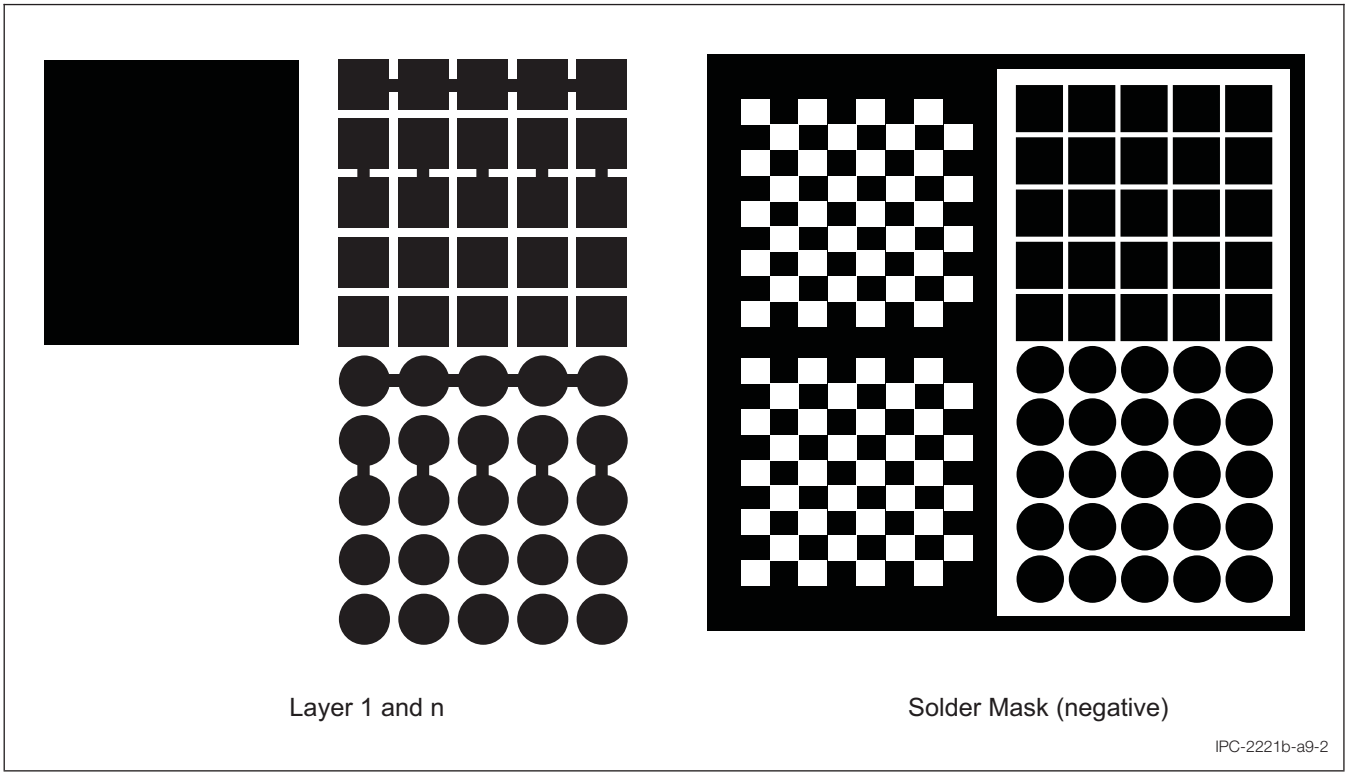


Figure A.9-2 G Coupon Example Layers

A.10 H COUPON Coupon H is used to quantify the effects of process and/or handling residues on surface insulation resistance. The coupon consists of an interstitial comb pattern per panel side. While a solder mask image is documented, the pertinent performance specification may preclude the use of solder mask on the coupon. The design parameters for coupon H are shown in Table A.10-1.

Table A.10-1 H Coupon Parameters, mm [in]

Feature	Description	Design Requirements
1	Plated-through test points	Recommended drill size: 1.02 [0.040] Recommended land size: 1.52 [0.060]
Electrodes	Parallel electrodes	Width: 0.40 [0.016] Pitch: 0.60 [0.024]

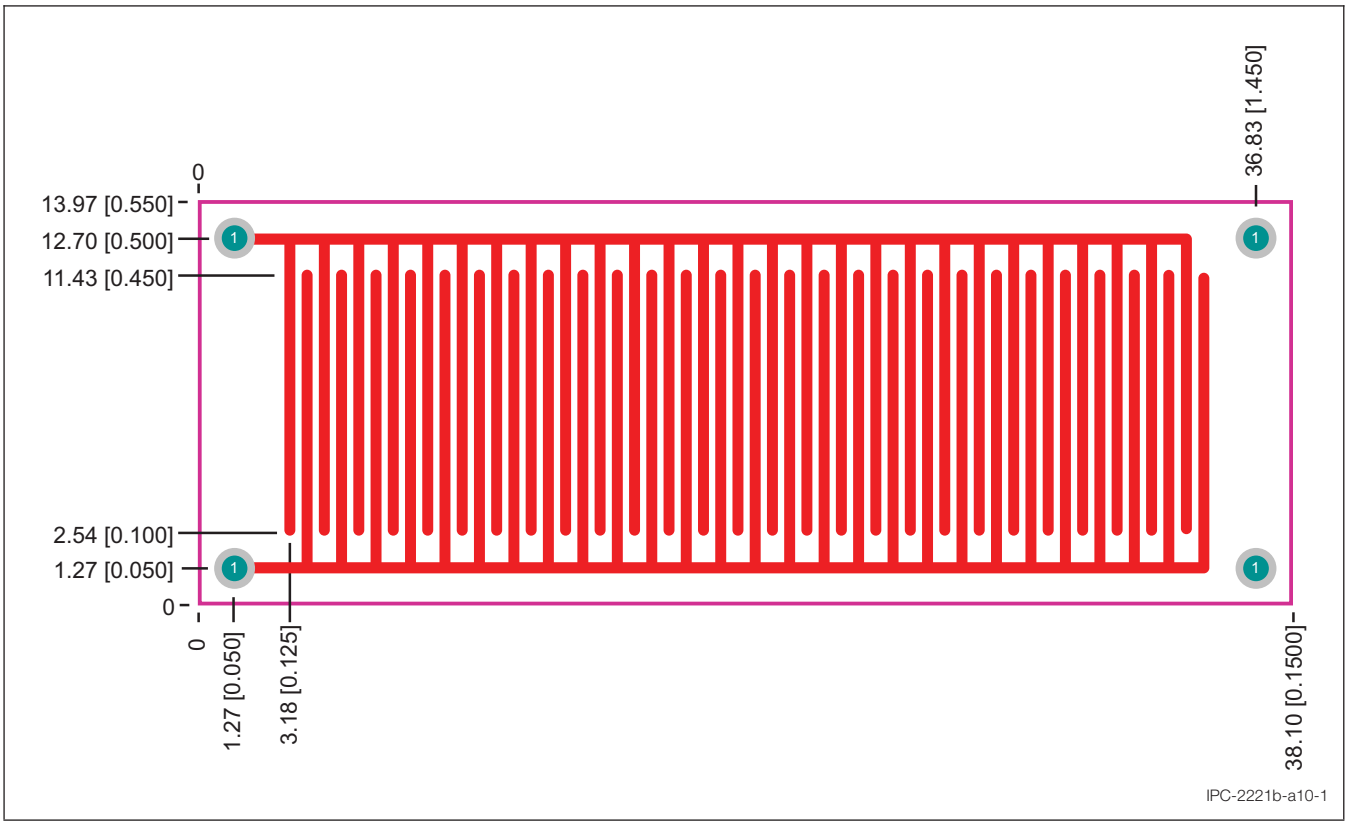


Figure A.10-1 H Coupon Layout, mm [in]

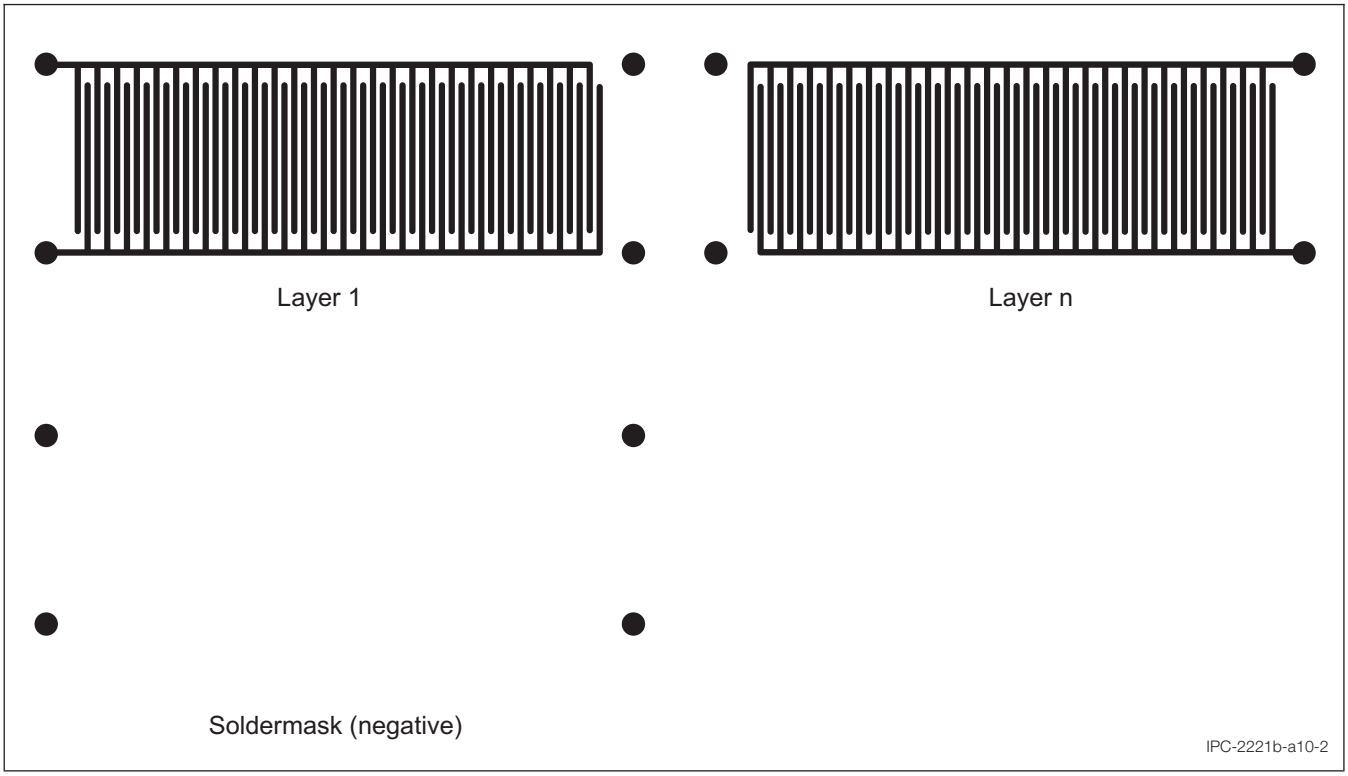


Figure A.10-2 H Coupon Example Layers

A.11 P COUPON Coupon P is used to evaluate the peel strength of metallic foils laminated to the outer layers of a printed board during the foil lamination process and to evaluate plating adhesion. The coupon consists of a conductor pair per panel side that provides a minimum test length of 30.48 [1.200]. The design parameters for coupon P are shown in Table A.11-1.

Table A.11-1 P Coupon Parameters, mm [in]

Feature	Description	Design Requirements
Peel	Peel conductor	Width: 3.18 [0.125] Minimum length: 30.48 [1.200]
Tab	Peel tab	Width: 5.72 [0.225] Length: 6.99 [0.275]

Note 1. Performance specifications preclude the use of surface finish on the coupon.

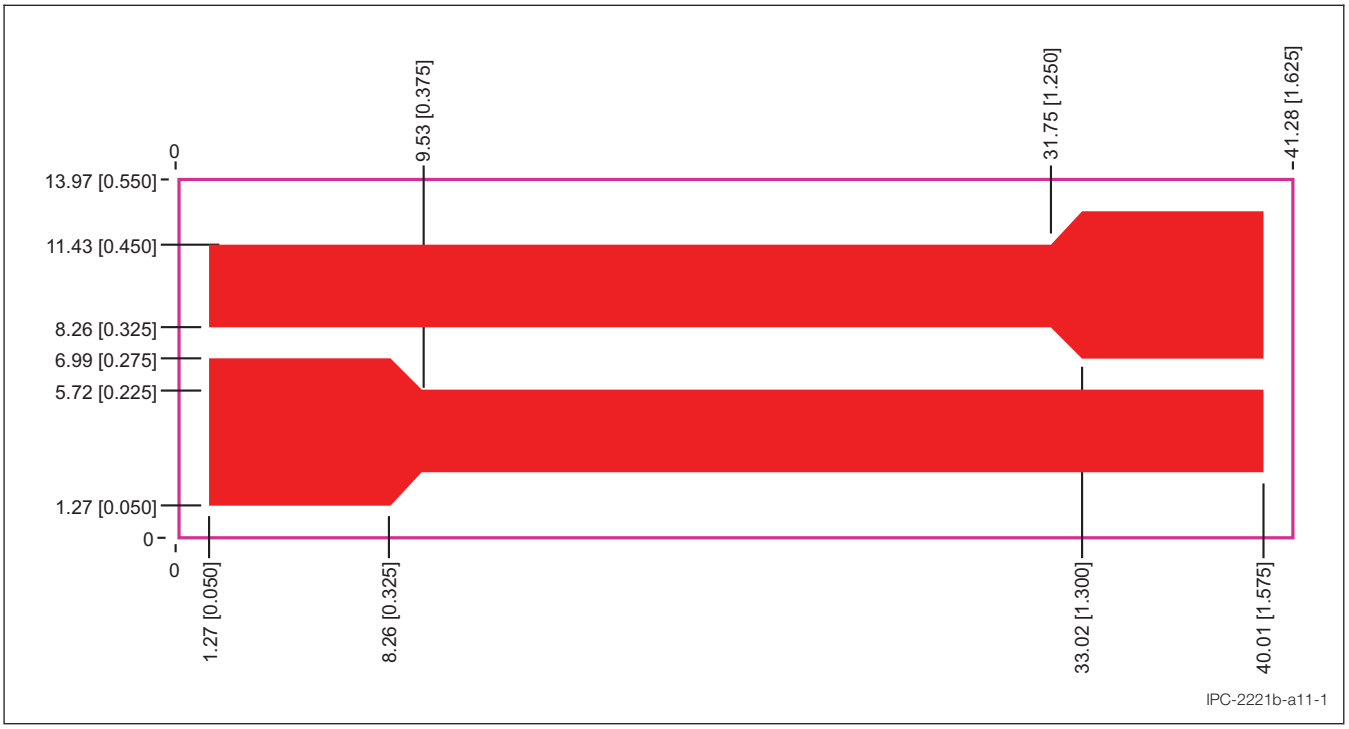


Figure A.11-1 P Coupon Layout, mm [in]

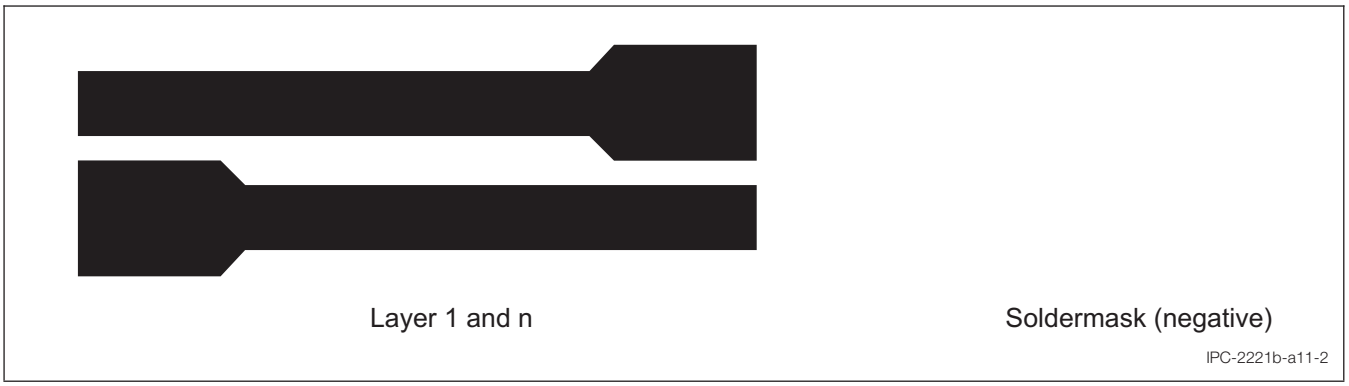


Figure A.11-2 P Coupon Example Layers

A.12 Z COUPON Coupon Z is used to determine the impedance value of controlled impedance structures of the printed board. Two structures either single-ended and/or differential per layer may be incorporated. The coupon may be designed with up to 24 single-ended structures, 12 differential structures or a combination of the two. The coupon provides for a minimum conductor length of 114.30 [4.50]. The design parameters for coupon Z are shown in Table A.12-1.

Table A.12-1 Z Coupon Parameters, mm [in]

Feature	Description	Design Requirements
TP	Plated-through test points (48 each)	Recommended drill size: 1.02 [0.040] Recommended land size: 1.52 [0.060] Grid size: 2.54 [0.100]
Conductors	Single-ended (2 test points): •Microstrip •Stripline Differential (4 test points): •Edge-coupled microstrip •Edge-coupled stripline •Broadside coupled stripline	Width(s): Per product board requirements Minimum length(s): 114.30 [4.50] Differential spacing: Per product board requirements Corners: Radiuses or 45 degree turns **Note:** Care should be taken to ensure constant separation of conductors on differential corners.
Planes	Reference planes	Edge of coupon clip-back: 0.254 [0.010] Spacing to edge of test-pad: 0.508 [0.020]

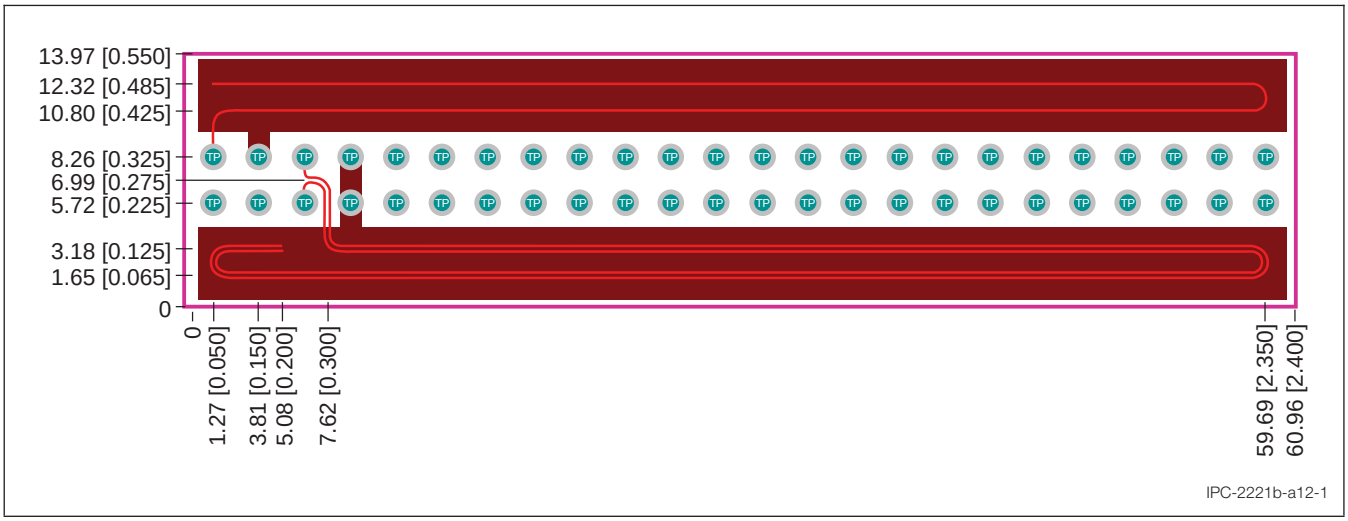


Figure A.12-1 Z Coupon Layout (Microstrip and edge-coupled microstrip), mm [in]

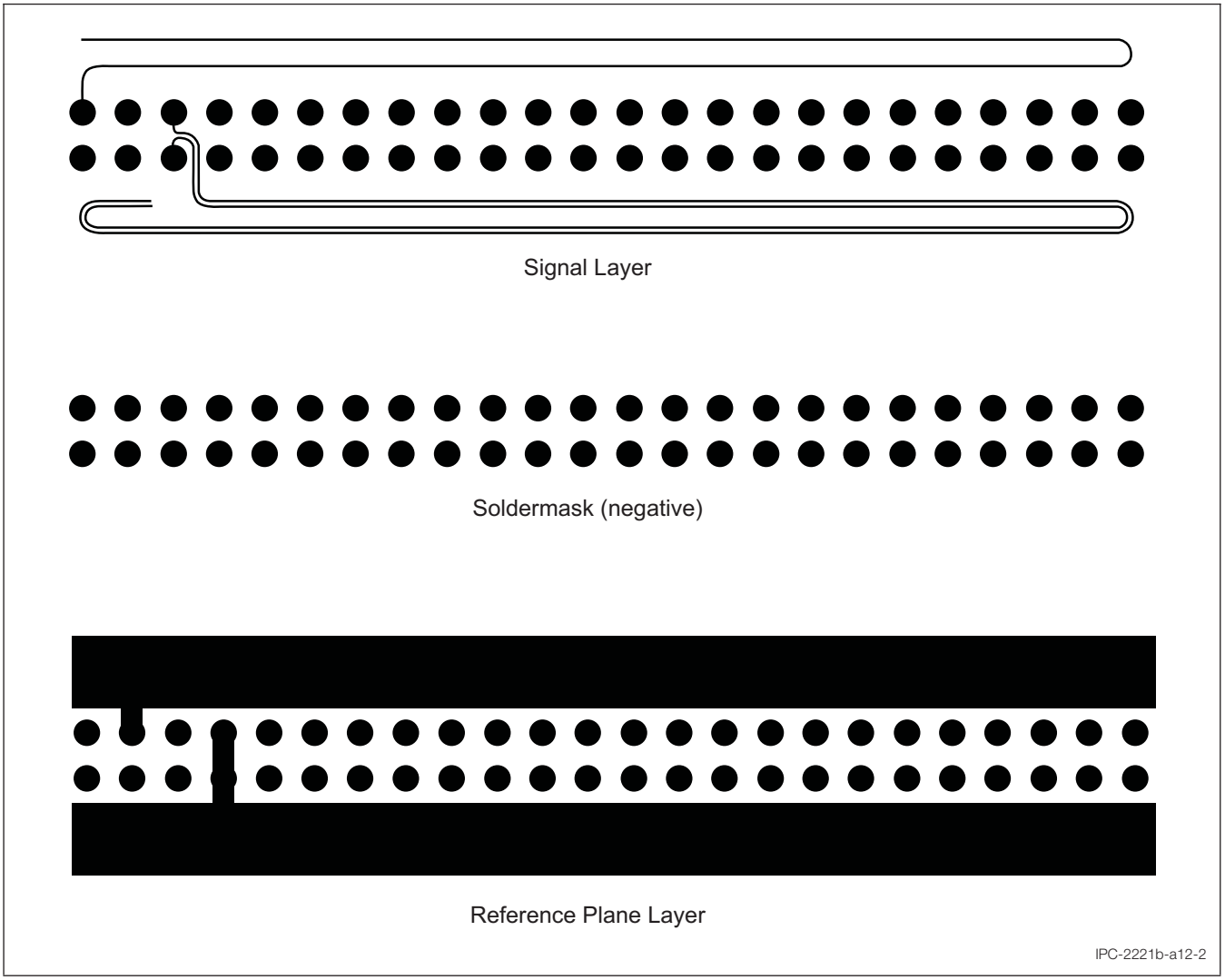


Figure A.12-2 Z Coupon Example Layers

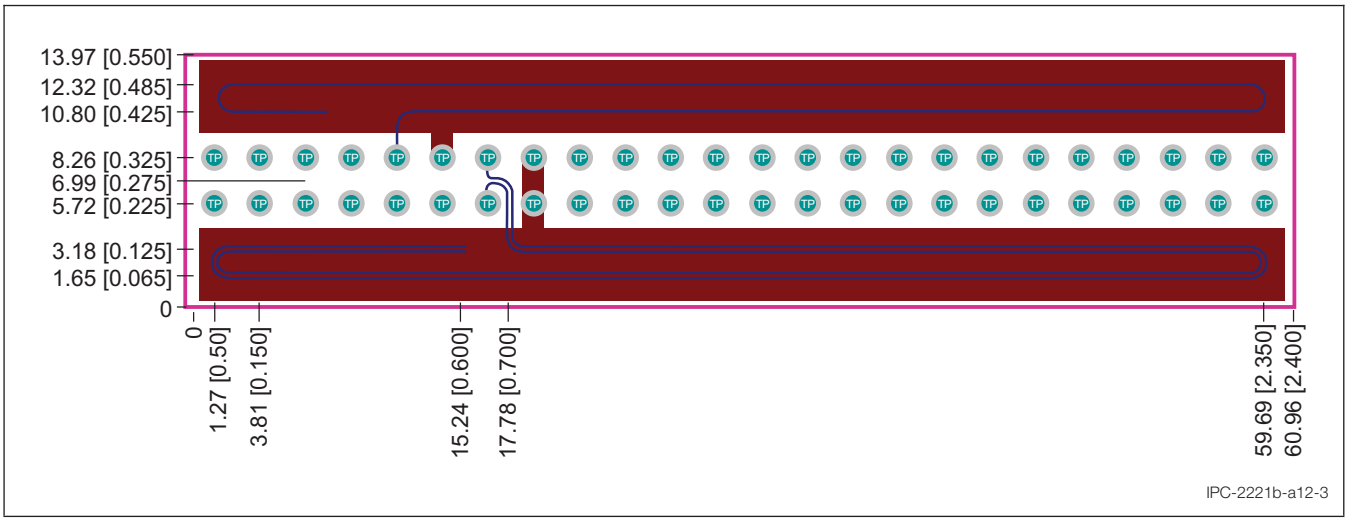


Figure A.12-3 Z Coupon Layout (Microstrip and edge-coupled microstrip using alternative test points), mm [in]

APPENDIX B

B.1 Introduction This appendix is included as a resource for the design of legacy qualification and conformance coupons from IPC-2221 Revision A. The intent is to provide guidance as to the coupon designs, however if conflicts arise or the information provided is incomplete, the design of the coupon features should be in accordance with the associated production printed board design requirements.

It is the recommendation of the IPC D-31b IPC-2221/2222 task group that the coupons be designed by the printed board fabricator in order to ensure that the correct drill sizes are used. Additionally, etch and solder mask fabrication compensation **shall** be applied uniformly to both the coupons and the production printed board after the coupons have been designed.

Solder mask layers are documented for some of the coupons, however they are only to be used if the associated production printed board design requires solder mask.

Table B.1-1 provides a summary of coupon designs that are described within this appendix.

Table B.1-1 IPC-2221 Legacy Coupons

Section	Coupon	Description	Purpose
B.2	A, B or A/B	Plated hole evaluation coupon	Plated hole/via evaluation, registration, thermal stress and rework simulation
B.3	E	Moisture and insulation Resistance coupon	Moisture and insulation resistance, cleanliness
B.4	S	Hole solderability coupon	Plated hole solderability to IPC-J-STD-003
B.5	M	Surface mount solderability coupon	Solderability of surface mount lands to IPC-J-STD-003
B.6	D	Interconnect resistance coupon	Interconnect resistance, continuity, lay-up
B.7	G	Solder mask coupon	Solder mask adhesion evaluation
B.8	H	Surface insulation resistance coupon	High level surface insulation resistance (SIR), predominately for surface mount designs
B.9	C	Peel strength coupon	Peel strength evaluation of metallic foils
B.10	F or R	Registration coupons	Layer-to-layer registration and annular ring evaluation without microsection (e.g., x-Ray)
B.11	N	Bond strength evaluation coupon	Peel strength and bond strength evaluation for surface mount lands
B.12	X	Bending flexibility coupon	Bending flexibility and bending endurance

B.2 Legacy A, B or A/B Coupon These coupons are used to evaluate plated holes as established in the applicable performance specification. Figures B.2-1 and B.2-3 show the general configuration of the coupons for through holes. A conductor may be included in between the small holes on the external layer of the coupons. These surface conductors are provided as assistance for coupon mounting and to maintain/confirm axis orientation post grinding and provide planar information only. It is recommended that they should not be used for conductor quality verification purposes. The land/hole relationship within the coupon **shall** represent the printed board design except when the design attributes fall outside the min/max configuration illustrated in Figure B.2-3. In this situation, choose the next available size employed in the design. Imaged layers **shall** represent printed board design, e.g., land size and plane layers, except that nonfunctional lands **shall** be included on all layers for purposes of construction integrity analysis such as registration, annular ring, post separation interconnect, etc. Layer numbers are positioned throughout the coupon to indicate axis orientation when optional horizontal mounting and grinding is employed. The layer numbering will be offset on each successive layer to prevent buildup as indicated in Figure B.2-3.

Thermal Stress testing is used to indicate innerlayer separations or barrel cracking. Both component holes and vias **shall** be subjected to this test.

When testing for rework simulation, test coupon A/B or coupon A **shall** contain the largest diameter component hole not exceeding 1.905 mm [0.075 in] on the printed board and the land associated with that hole diameter, without violating minimum electrical spacing between the lands. It has been shown that plated holes with large diameters are more susceptible to innerlayer separation as a result of higher radial tensile stresses and bending moments acting on the innerlayer interconnects near the surfaces of printed boards. See IPC-TR-486 for a detailed explanation on innerlayer post separation.

When testing for barrel cracking, test coupon A/B or heritage coupon B **shall** contain holes with the smallest diameter hole on the printed board and land associated with that hole diameter down to a minimum of 0.15 mm [0.006 in]. It has been shown that plated through holes with smaller diameters and high aspect ratios are more difficult to plate and are subjected to the greater tensile stresses in the barrels near the printed board central z axis. In the case of test coupon A/B, care **shall** be taken to ensure that grinding extends past the outer holes such that the smallest diameter holes can be evaluated. See IPC-TR-579 for a detailed explanation on the reliability of small diameter holes. The coupon outline border on layer one is optional and may be produced by screening or etch. The border may be solid or segmented in order to accommodate placement of tooling holes for automated polishing equipment.

For blind and buried via interconnects, a minimum of one additional heritage B or A/B coupon **shall** be added to represent the most complex build construction. See Figure B.2-2 for an example of additional heritage B coupon use and Figure B.2-4 for an example of additional A/B coupon use.

Note: Coupon A/B or heritage coupons A and B are not required for nonplated-through hole SMT designs. Figures B.2-1 and B.2-3 illustrate typical clearance areas in plane areas per the design minimum.

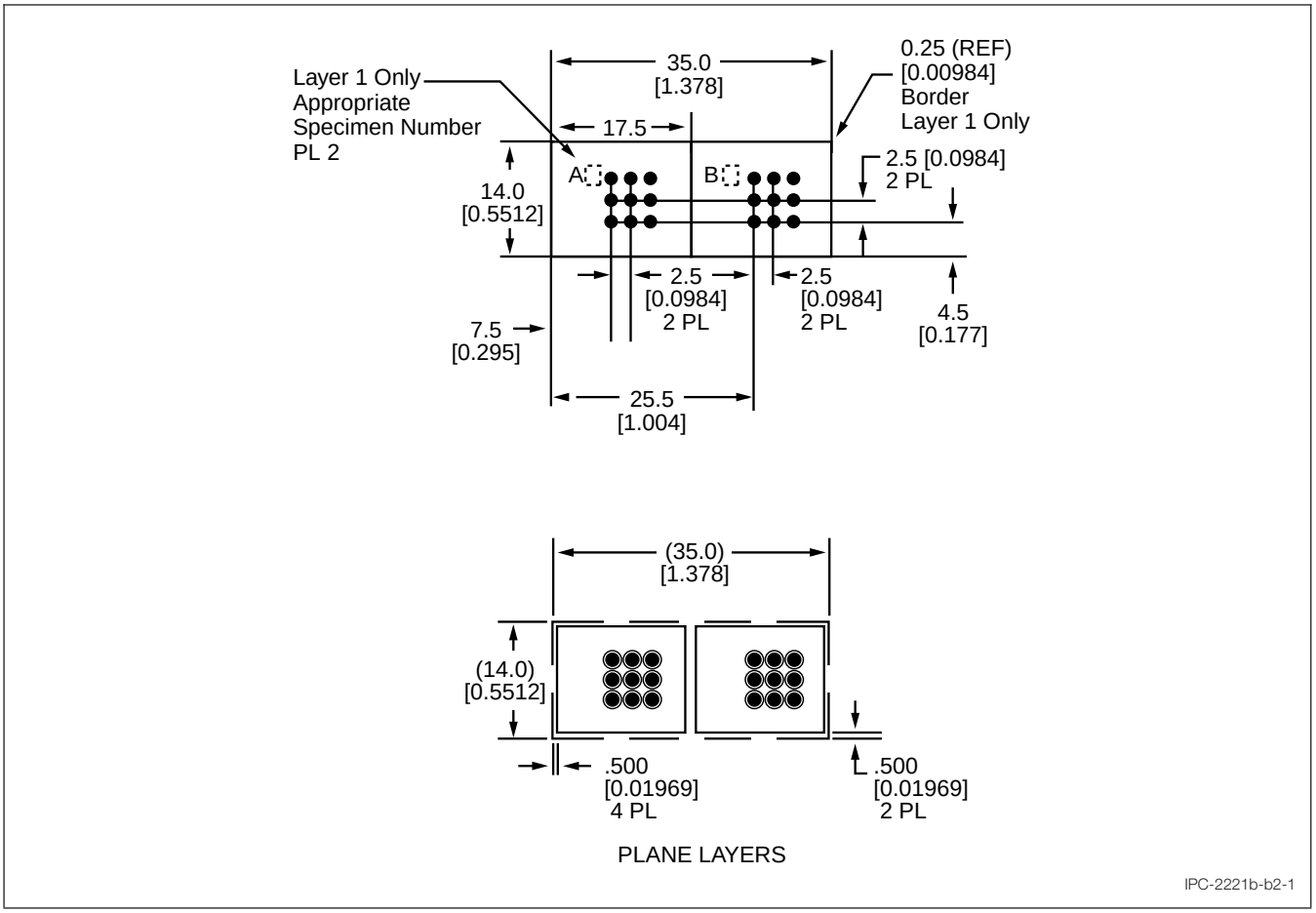
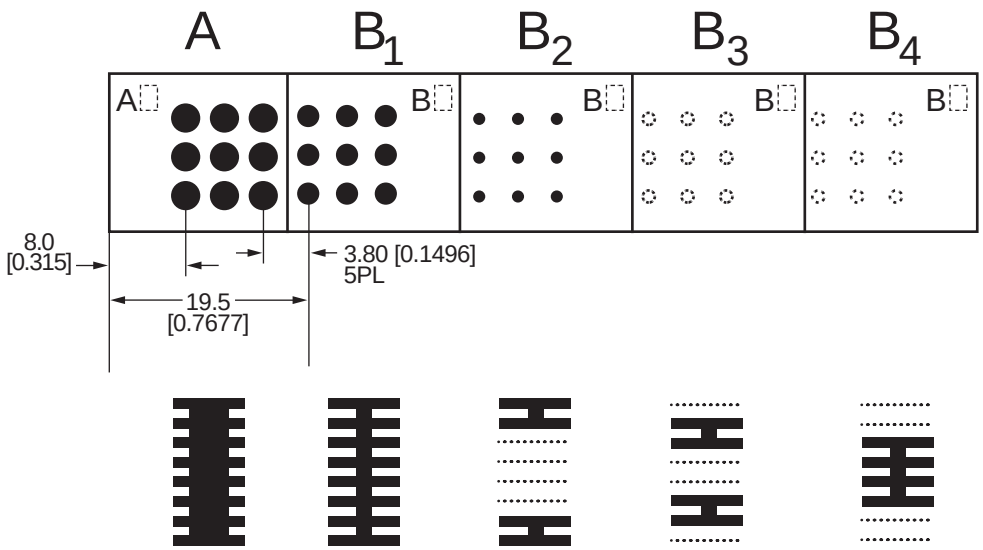


Figure B.2-1 Test Coupons A and B, mm [in]



A = Component holes; solderability & rework. (as required)

B_1 = Through vias thermal stress. (most complex through-hole)

B_2 = Blind vias thermal stress; separate sequential plating cycle.

B_3 = Buried vias thermal stress; separate sequential plating cycle.

B_4 = Buried vias thermal stress; separate sequential plating cycle.

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Figure B.2-2 Test Coupons A and B (Conductor Detail), mm [in]

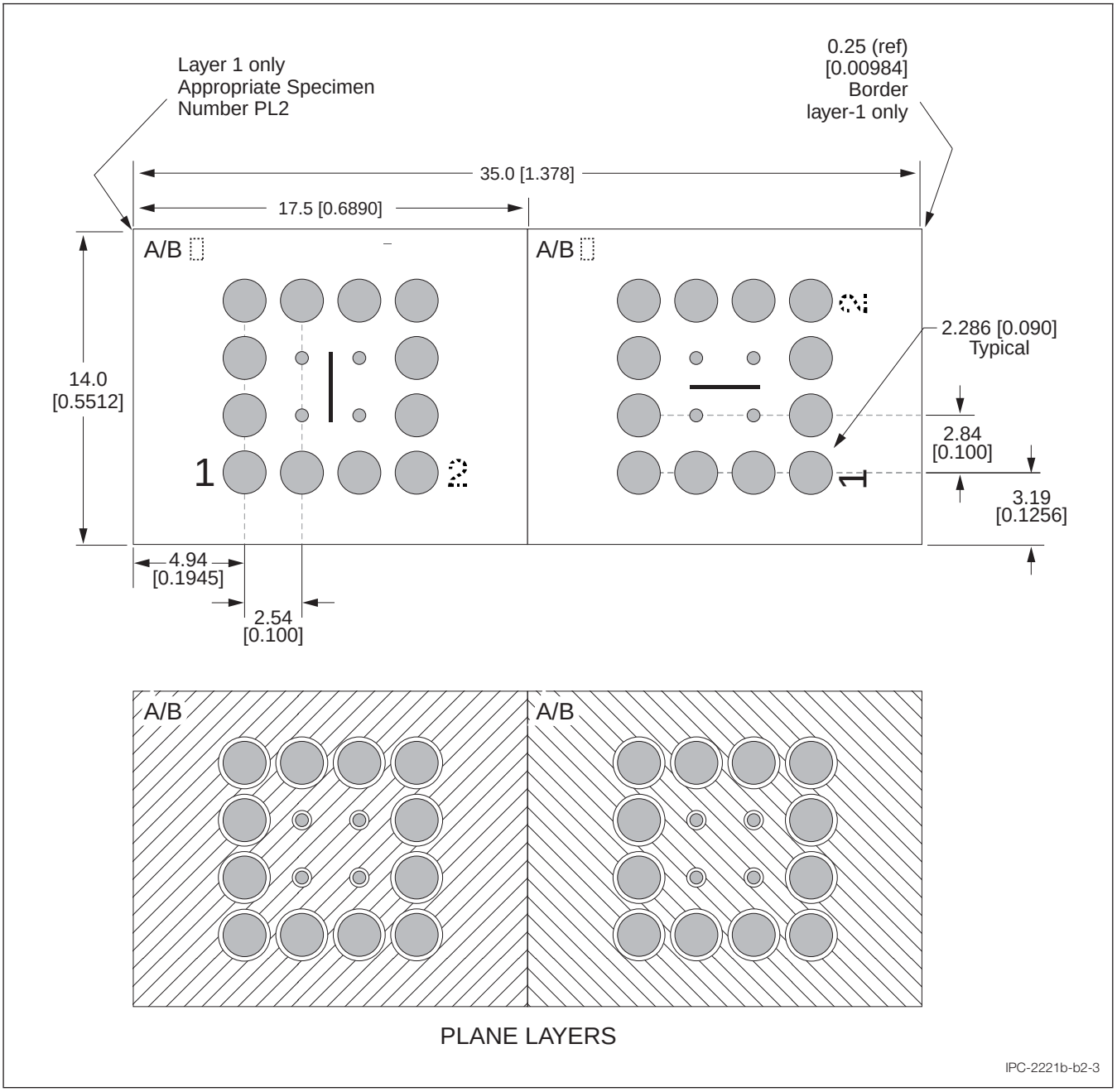
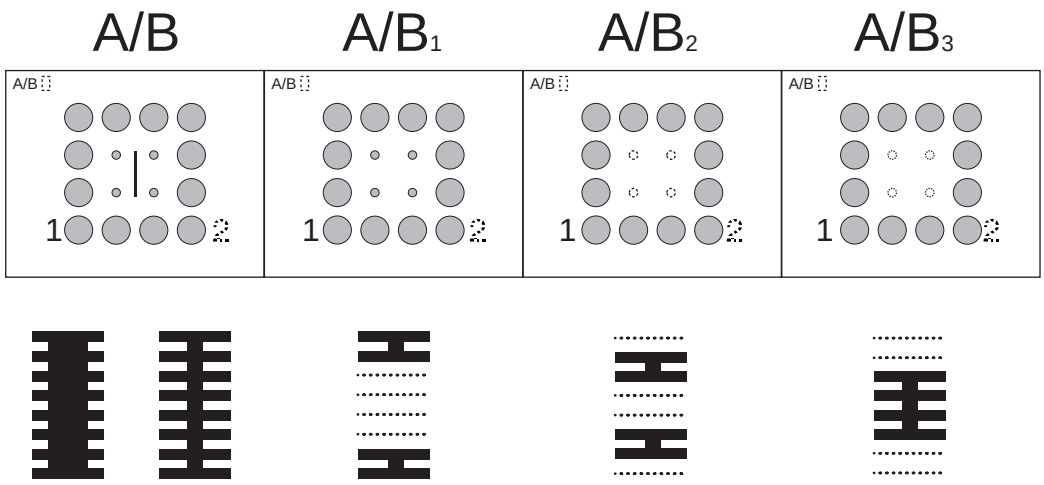


Figure B.2-3 Test Coupon A/B, mm [in]



A/B = Component holes; solderability & rework simulation (as required); through vias thermal stress (most complex through-hole)

A/B_1 = Blind vias thermal stress; separate sequential plating cycle.

A/B_2 = Buried vias thermal stress; separate sequential plating cycle.

A/B_3 = Buried vias thermal stress; separate sequential plating cycle.

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Figure B.2-4 Test Coupon A/B (Conductor Detail), mm [in]

B.3 Legacy E Coupon Legacy coupon E is used for general testing purposes.

The design of the coupon **shall** be in accordance with Figure B.3-1 except as noted below. The minimum land hole diameter **shall** be any leaded component hole or, if there are no component holes, the minimum land hole diameter **shall** be 0.50 mm [0.020 in]. The holes **shall** be left open. A pair of holes and a pair of conductors **shall** be provided for all layers of the coupon.

The ''Y'' pattern of legacy coupon E can provide a useful tool for cleanliness and insulation resistance property evaluations. When using surface mount patterns, alternate coupons containing comb patterns such as the H and legacy H coupons described in 12.4.7 may be used to evaluate both insulation resistance and cleanliness of the bare printed board before and after solder mask. As in most instances, the coupon under large surface mount devices should be a comb pattern.

If a ''Y'' pattern is assigned to a chip component, the position can be left empty or can be filled to reflect cleanliness/insulation resistance properties of the bare printed board, or cleanliness/insulation resistance properties of the assembly (see Figure B.3-2).

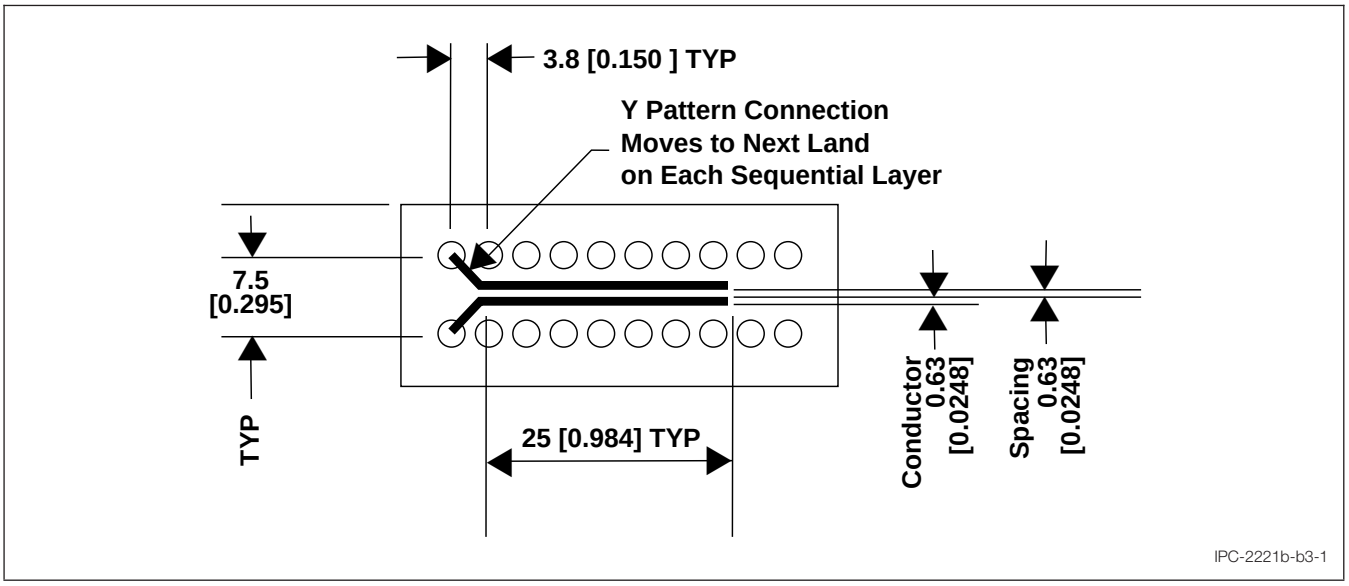

Figure B.3-1 Coupon E, mm

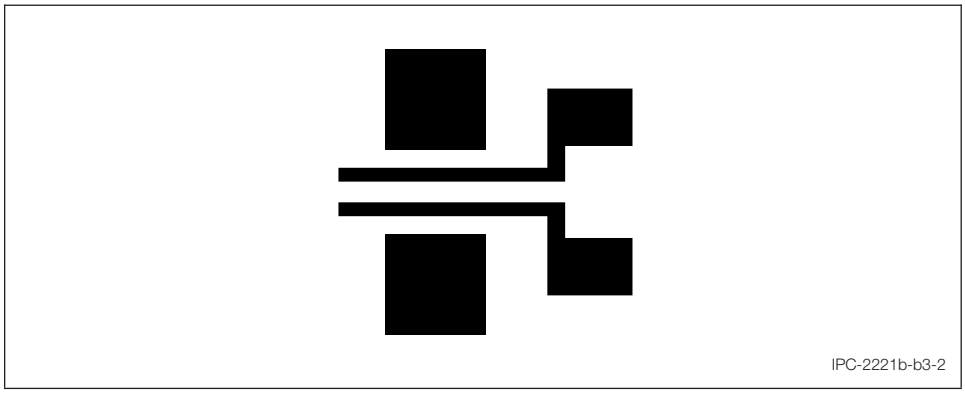

Figure B.3-2 ''Y'' Pattern for Chip Component Cleanliness Test Pattern

B.4 Legacy S Coupon This coupon may be used to evaluate PTH solderability to IPC-J-STD-003 when a larger population of holes is required. The general design of the coupon is provided in Figure B.4-1. The hole diameter **shall** be 0.8 mm ± 0.13 mm [0.031 in ± 0.00512 in] required to be solder filled.

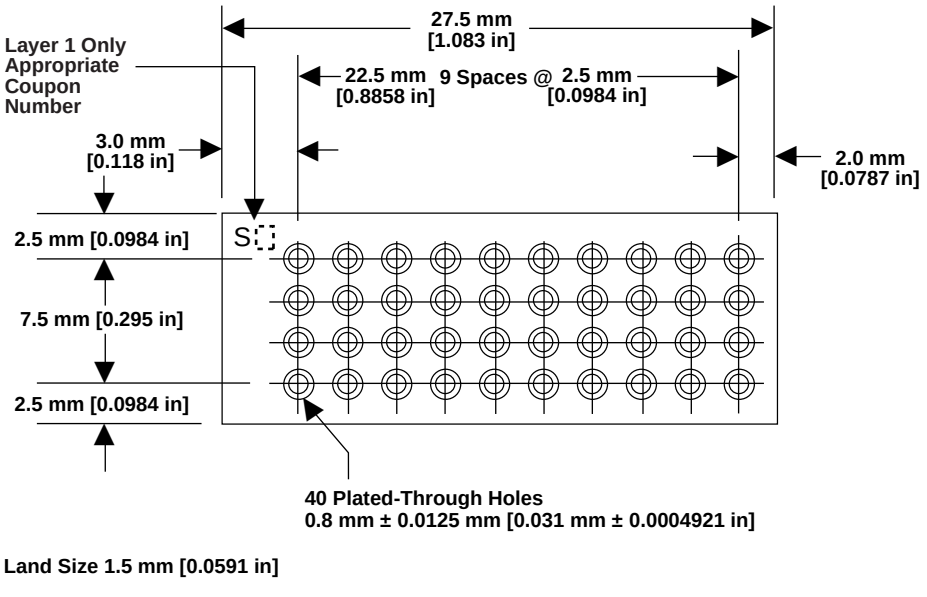

Figure B.4-1 Test Coupon S, mm [in]

B.4.1 Legacy S Coupon (Solder mask Tented Coupon T) This coupon **shall** be used to validate tenting characteristics when solder masks are used to tent PTHs (see 4.5.1 of IPC-2221). The legacy T coupon is the same as the legacy S coupon except that the entire coupon **shall** be covered with solder mask on both sides.

The hole diameter **shall** be the largest plated hole which will be tented with solder mask. This coupon is not referenced in IPC-6012. If it is used, the test method and performance criteria **shall** be specified in the procurement documentation.

B.5 Legacy M Coupon This coupon may be used to evaluate solderability of surface mount lands to IPC-J-STD-003 requirements. The general design of the coupon is provided in Figure B.5-1. If it is used, the test method and performance criteria **shall** be specified in the procurement documentation.

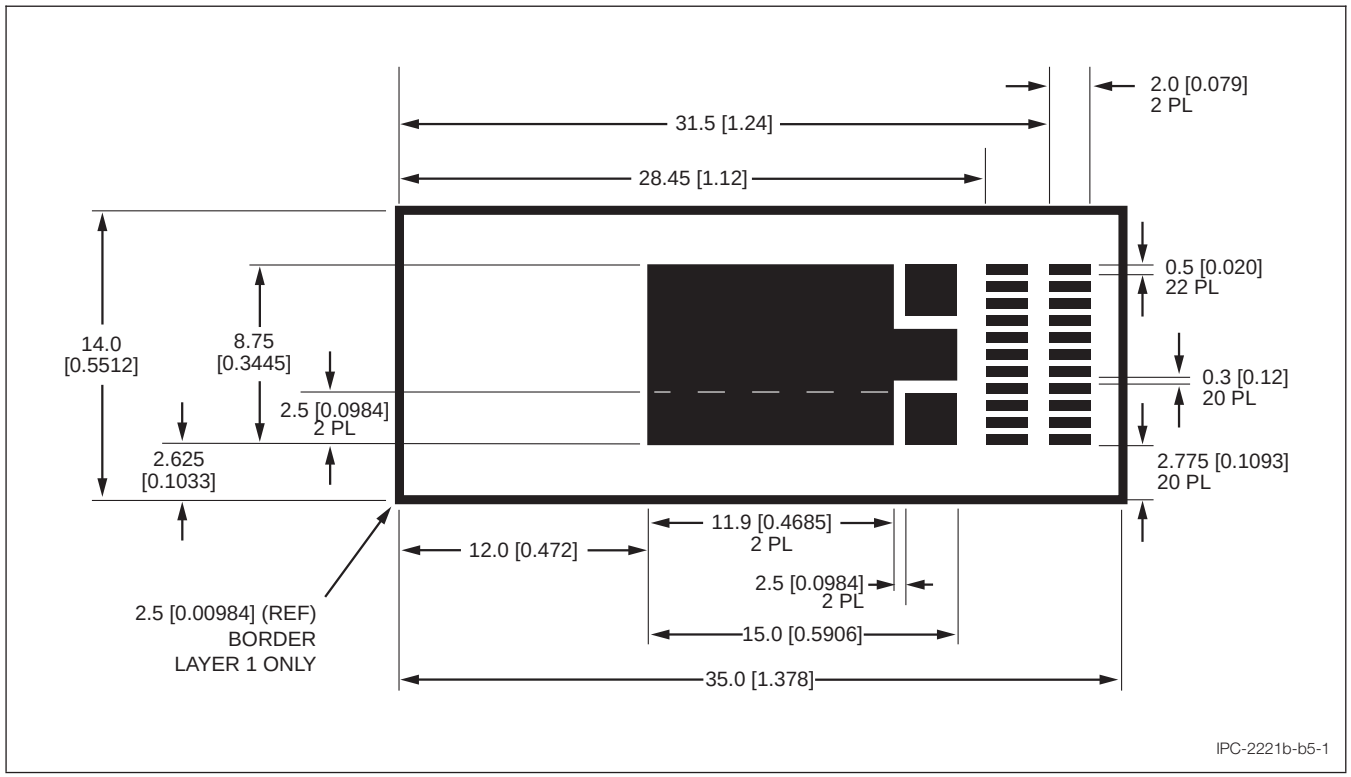

Figure B.5-1 Test Coupon M, Surface Mounting Solderability Testing, mm [in]

B.6 Legacy D Coupon The legacy D coupon is used to evaluate interconnection resistance, continuity, correct lay-up, and other performance criteria for conformance testing or for process control. Coupon parameters are described in Figure B.6-1.

B.6.1 Legacy D Coupon for Conformance Testing For conformance testing, the number of layers, lay-up, layer configuration, and use of nonfunctional lands **shall** be modified to reflect the printed board design. The land size **shall** be representative of the printed board and the hole diameter **shall** be the smallest in the associated printed board with the exception of A1, A2, B1, and B2 which **shall** be a minimum of 0.75 mm [0.0295 in]. Since the smallest hole represents the most difficulty in meeting plating requirements, this will ensure that the evaluation of the legacy D coupon parallels the characteristic with the most variability. The length of the coupon will vary with the number of layers.

A typical example of a ten-layer, coupon legacy D modified to include blind and buried vias is shown in Figure B.6-2 and Figure B.6-3. In general, the conductor **shall** be continuous from holes A1/A2 to holes B1/B2 and **shall** be arranged symmetrically around the centerline of the coupon.

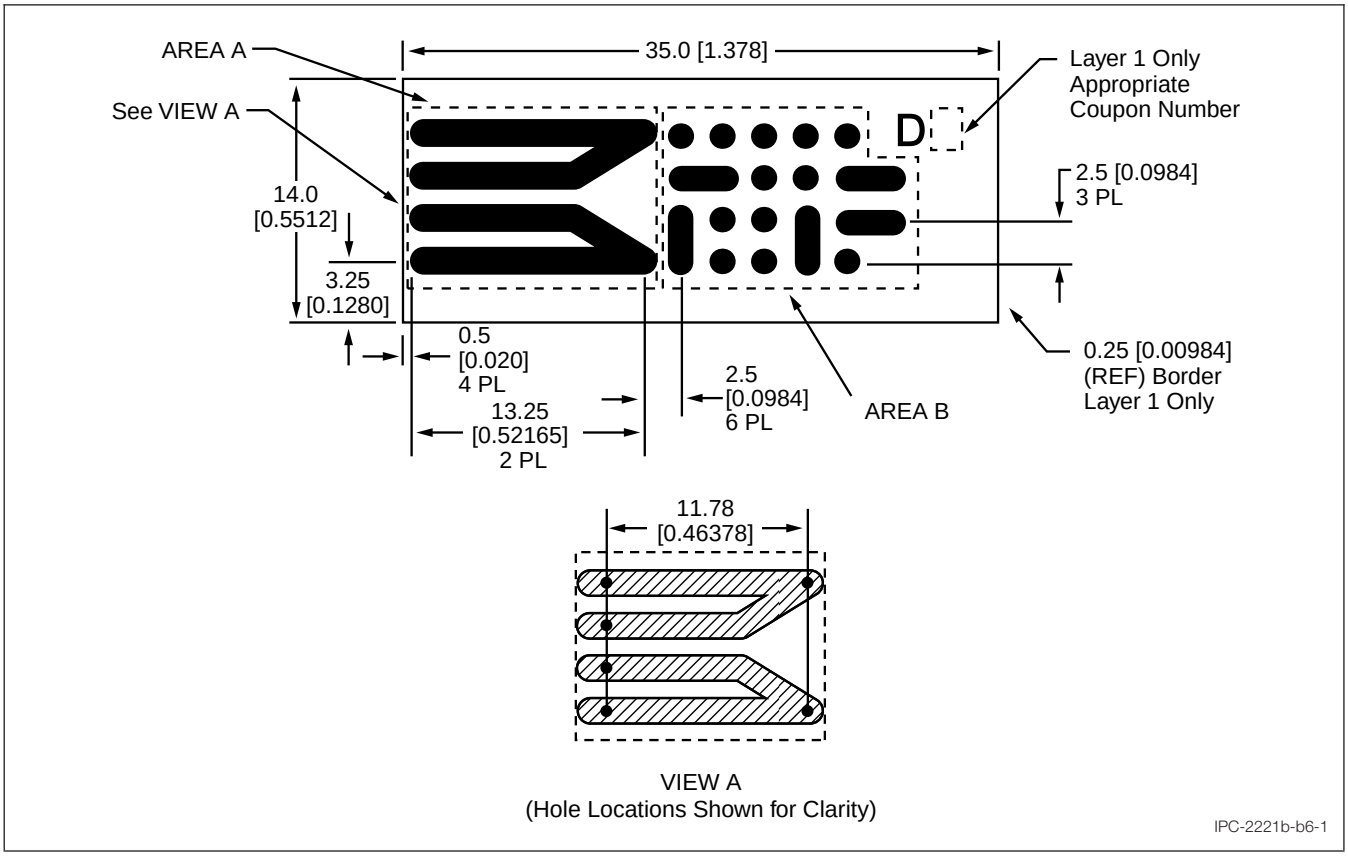

Figure B.6-1 Test Coupon D, mm [in]

The conductors **shall** not be routed stepwise through the coupon, but rather arranged so that the interconnects in a specific hole are separated to the greatest extent possible. The maximum number of holes in the coupon are not restricted; however, the minimum number of holes **shall** be two times the number of layers plus four (for holes A1, A2, B1, and B2).

Except for plane layers, there **shall** be a minimum of two conductor paths for each layer of the printed board design, one on each side of the centerline. If there are no conductors on the external layers, the connections **shall** be moved to layer 2 and layer n-1 respectively.

With the exception of the layer 1 conductors connecting holes A1/A2 to 01 and B1/B2 to 24, respectively, the conductor width on each layer **shall** be the minimum used on that layer of the printed board design. The conductors on layer 1 used to establish connection to holes 01 and 24 **shall** be of sufficient size to accommodate the 0.75 mm [0.0295 in] hole diameter for A1/A2 and B1/B2, and to allow for the attachment of source wiring of the precision resistance measurement equipment. Constraining cores and plated layers **shall** represent printed board design, e.g., ground ties on specific layers, deleted nonfunctional lands, etc. Blind and buried vias **shall** be included in the coupon design.

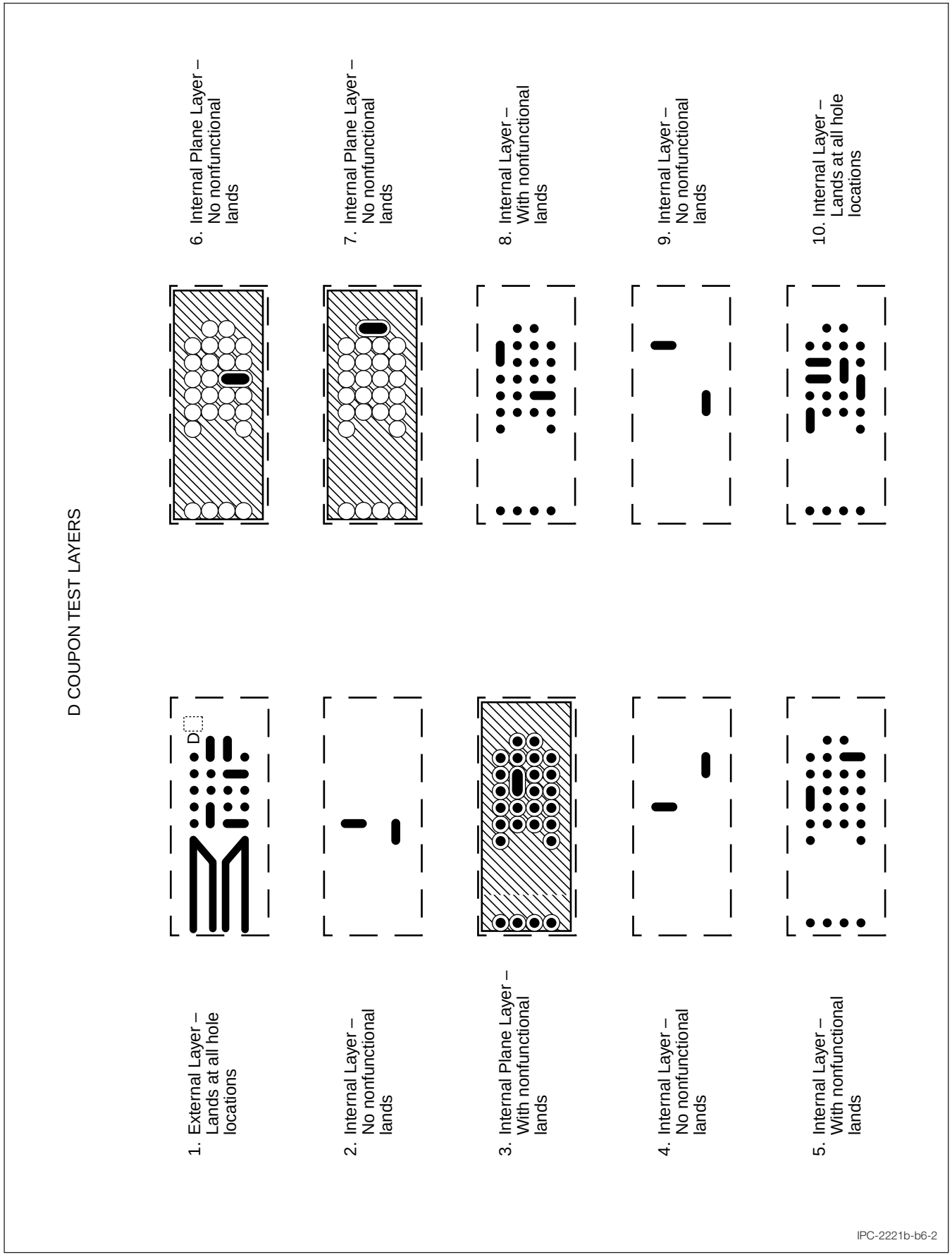

Figure B.6-2 10 Layer Example

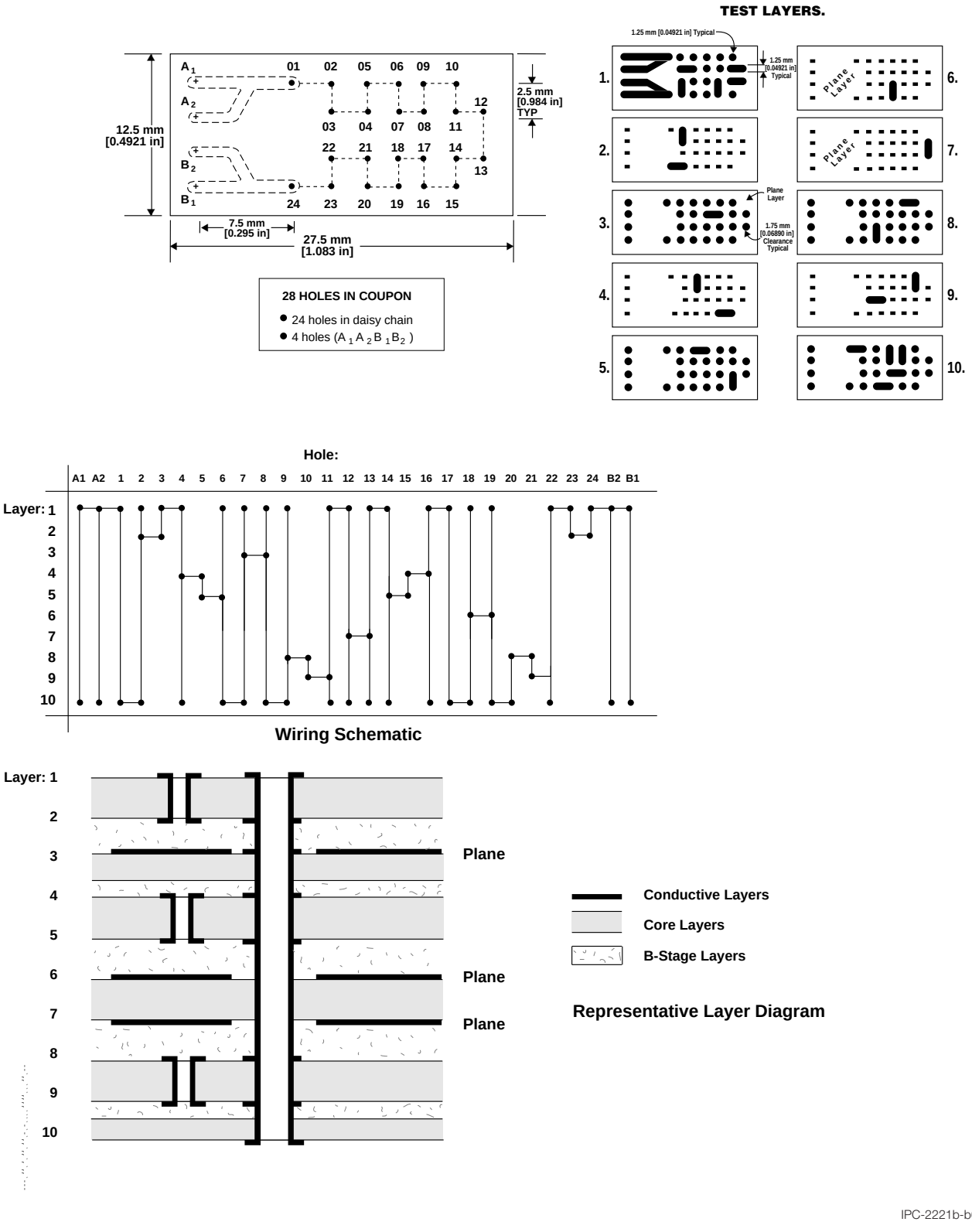

Figure B.6-3 Example of a 10 Layer Coupon D, Modified to Include Blind and Buried Vias

B.6.2 Legacy D Coupon for Process Control See Figure B.6-4 as an example of a process control legacy D coupon.

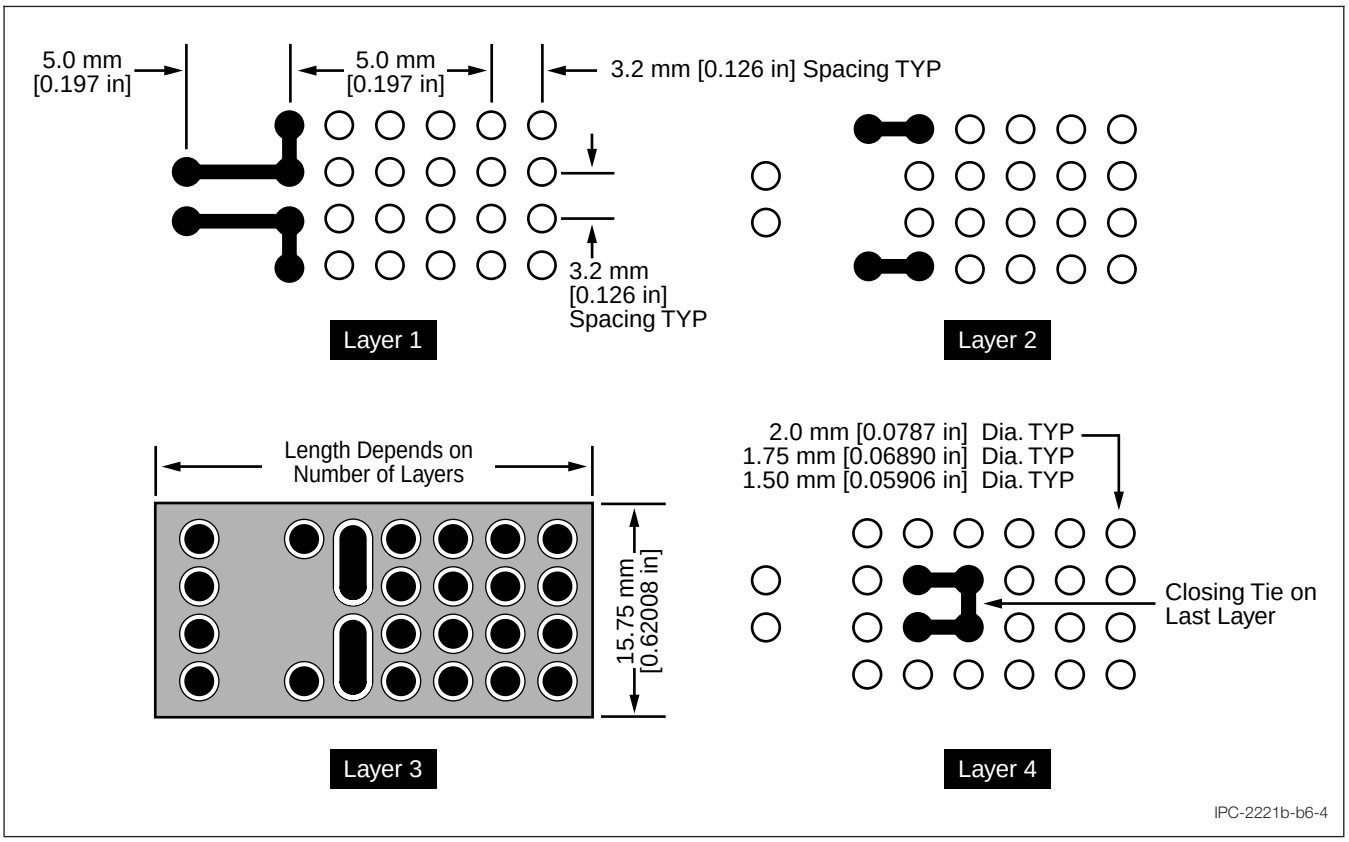

Figure B.6-4 Test Coupon D for Process Control of 4 Layer Printed Boards

B.7 Legacy G Coupon The legacy G test coupon for evaluating solder mask adhesion **shall** be as described in Figure B.7-1. The artwork **shall** provide for solder mask to cover the entire coupon.

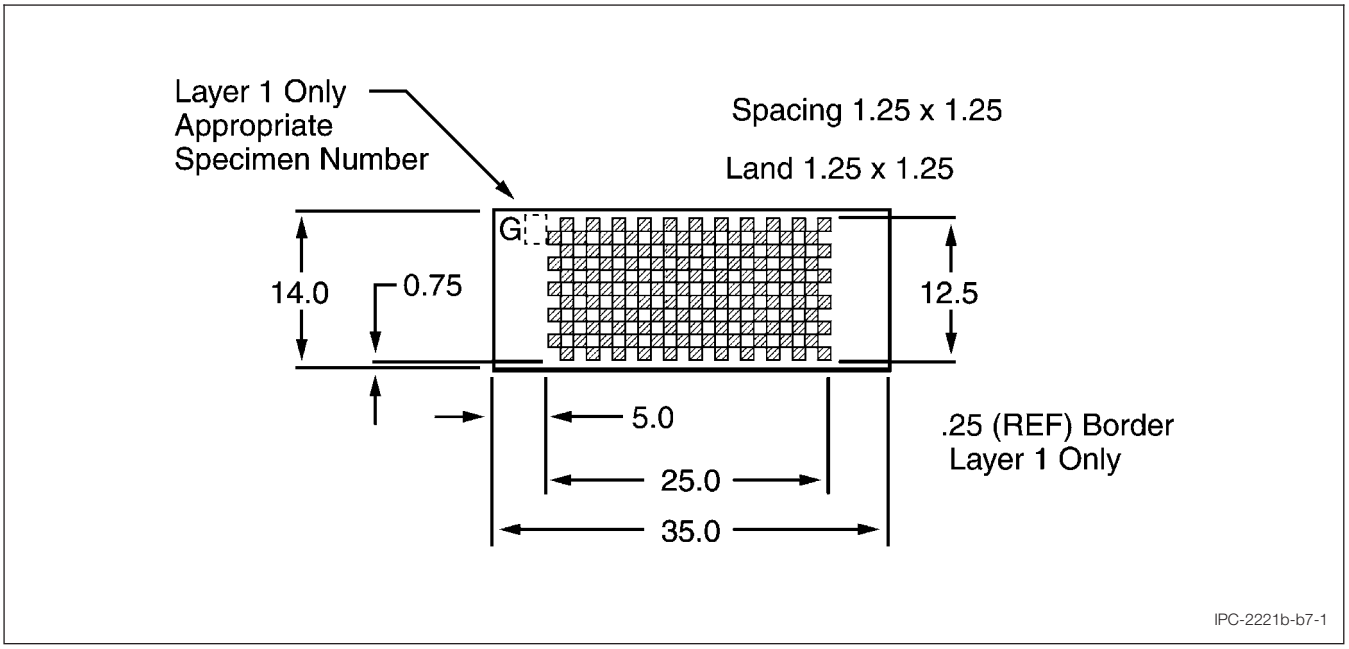

Figure B.7-1 Test Coupon G, Solder Resist Adhesive, mm [in]

B.8 Legacy H Coupon Legacy coupon H is used for higher level insulation testing, such as telecommunications. The comb pattern requires a more intensive cleaning process than that of legacy coupon E.

The design of the coupon **shall** be in accordance with Figure B.8-1 except as noted below. The minimum land hole diameter **shall** be any leaded component hole or, if there are no component holes, the minimum land hole diameter **shall** be 0.50 mm [0.020 in]. The holes **shall** be left open. A pair of holes and a pair of conductors **shall** be provided for all layers of the coupon.

Figure B.8-2 shows several comb pattern combinations to evaluate land patterns used for surface mounting. These coupons and concepts may be incorporated directly on the printed board in a spare position for a component, or may be incorporated as conformance coupons on the panel for evaluation when assembling surface mount component in panel format.

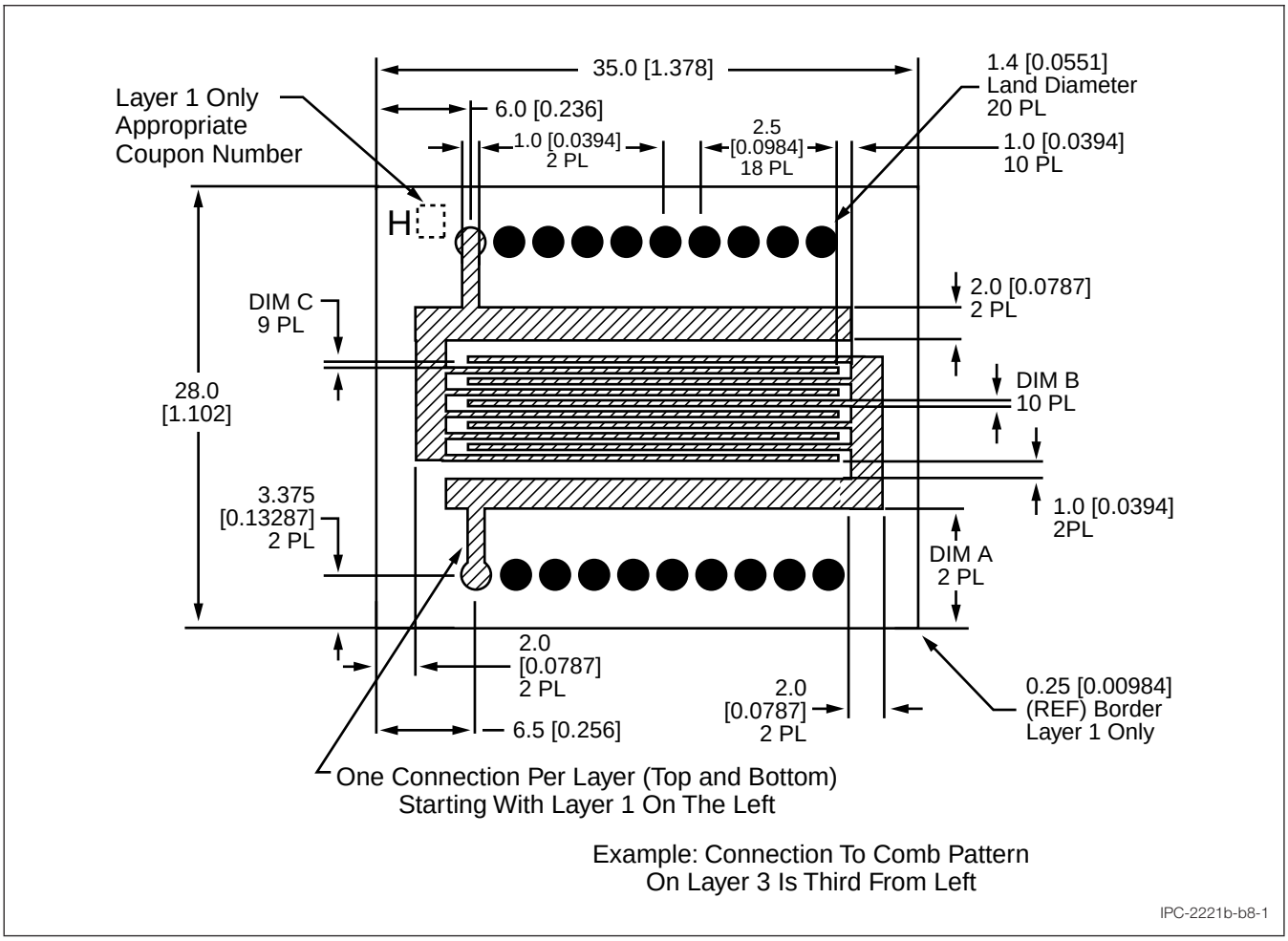

Figure B.8-1 Optional Coupon H, mm [in]

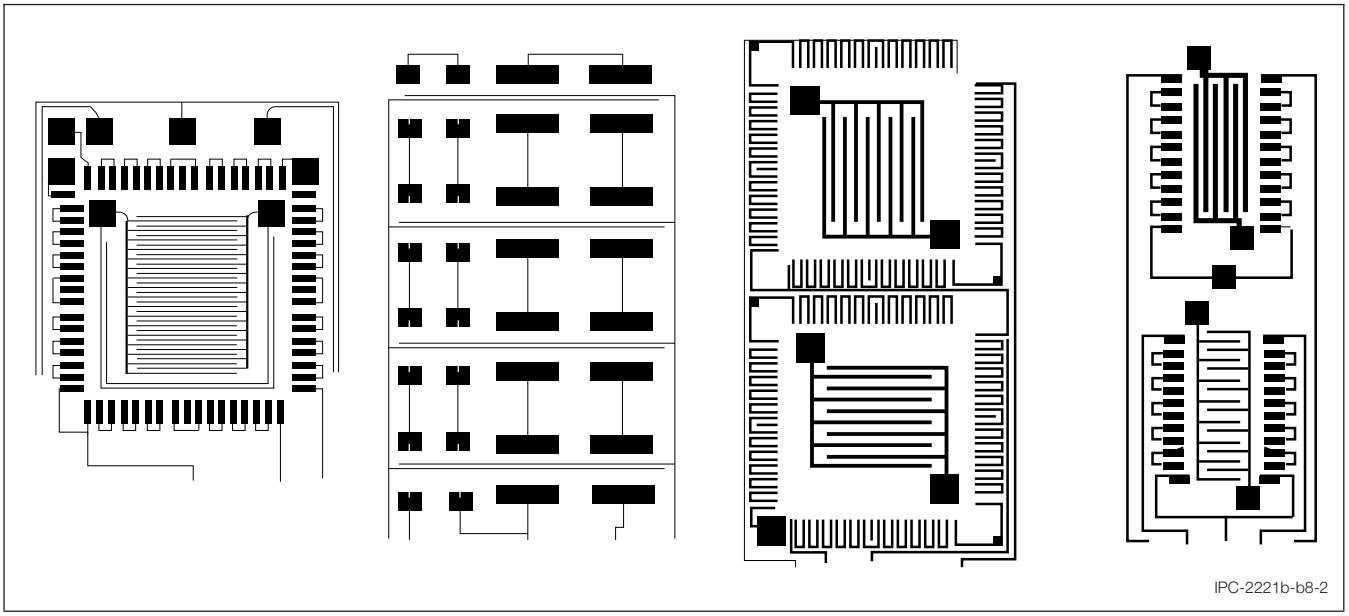

Figure B.8-2 Comb Pattern Examples

B.9 Legacy C Coupon This coupon is used to evaluate peel strength of metallic foils. Design parameters and illustrations are provided in Figure B.9-1.

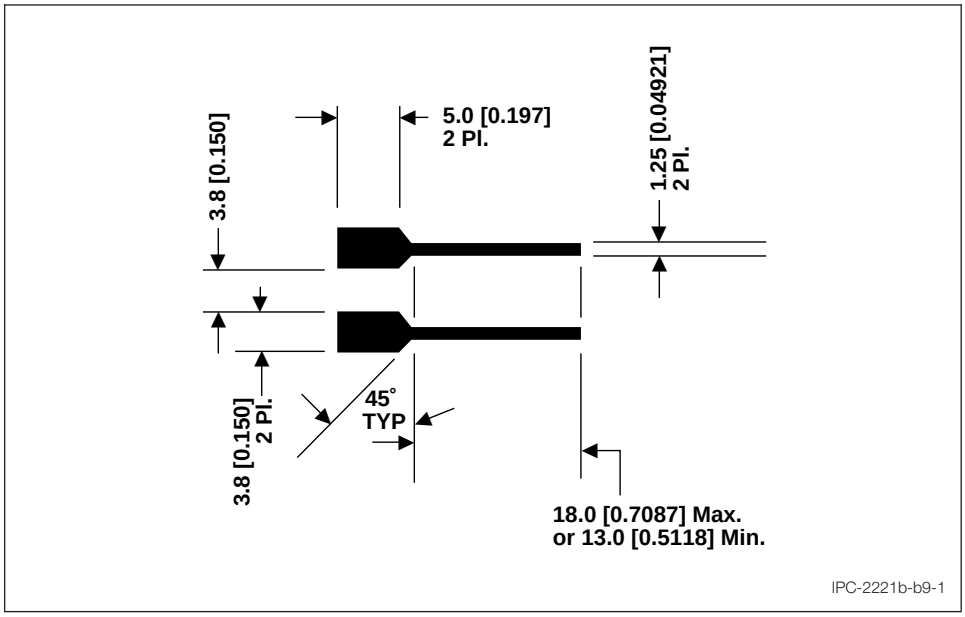

Figure B.9-1 Coupon C, External Layers Only, mm [in]

B.10 Legacy F and R Registration Coupons The purpose of the F and R registration coupons are to evaluate the internal annular ring. When legacy coupons A and B or A/B, or coupon AB/R are used for registration evaluation, the technique requires multiple microsections. i.e., in both the x and y axes.

The legacy F coupon is used to evaluate layer-to-layer registration and annular ring without microsection.

The advantages of the legacy R coupon is that it can be evaluated for annular ring by X-Ray after drilling, it provides a quick electrical check to determine if the correct annular ring is present, and provides a digital measurement of the annular ring which makes it an effective method of process control. The disadvantages are that the etch factor **shall** be known for each layer, the X-Ray **shall** have a resolution of less than 25 µm [984 µin], a separate land **shall** be present for each layer, and the coupon cannot be evaluated electrically until after the holes are plated.

Either legacy coupons F or R, or a combination, may be used to evaluate misregistration of the layers.

The coupon **shall** be placed in the corners of the panels, since that is where the most material movement occurs.

Figure B.10-1 for legacy coupon F and Figure B.10-2 for legacy coupon R dimensions apply to qualification testing only.

B.10.1 Coupon F, Conformance Testing (Option 1) The design of the coupon **shall** be in accordance with Figure B.10-1 with the hole diameter at the option of the manufacturer. The land size for this option includes an annular ring. Constraining cores and plated layers **shall** represent printed board design. The advantages to this option are that the coupon may be evaluated immediately after drilling, and the etch factor does not need to be considered. The disadvantage is that it requires an X-Ray with a resolution of less than 25 µm [0.984 mil] to measure the annular ring.

This concept places a land on every layer. If the manufacturer wishes to use another hole diameter, the land size **shall** be calculated for each internal layer separately using the formula in 9.1.1. The coupons are evaluated after drilling by measuring the annular ring using X-Ray.

B.10.2 Coupon F, Conformance Testing (Option 2) The design of the coupon **shall** be in accordance with Figure B.10-1 with the hole diameter at the option of the manufacturer. The land size for this option does not include an annular ring. Constraining cores and plated layers **shall** represent printed board design. This is the preferred coupon. The advantages to this option are that the coupons may be evaluated after drilling by X-Ray for breakout, evaluation may be after etchback or hole clean using a visual inspection, and the etch factor need not be considered.

This concept places a land on every layer. If the manufacturer wishes to use another hole diameter, the land size **shall** be calculated for each internal layer separately using the formula in 9.1.1.

The coupon can be evaluated after drilling by inspecting for breakout using X-Ray, or the coupon can be inspected after hole clean or etchback for a continuous ring in the drilled hole using a back-lit table.

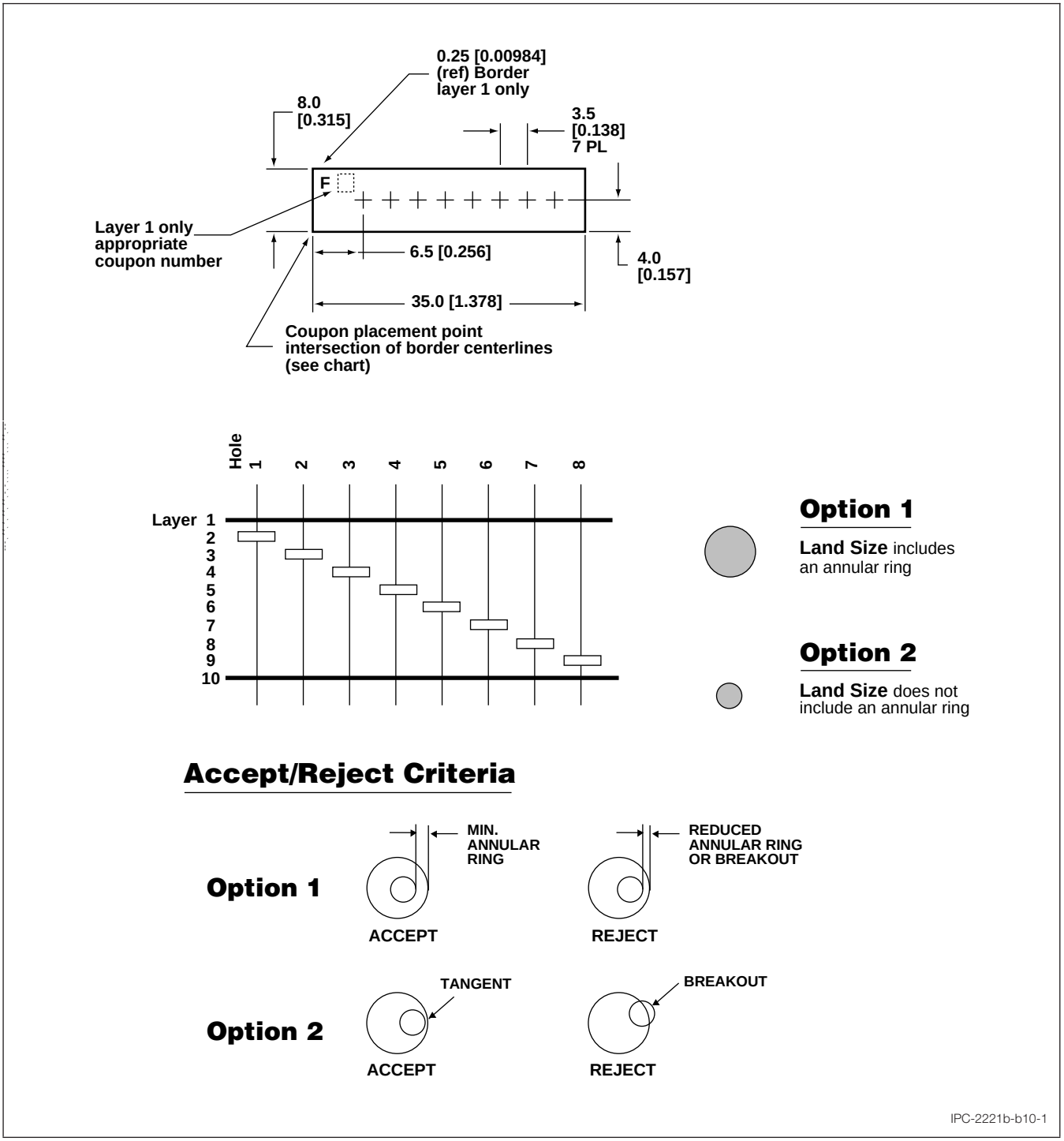

Figure B.10-1 Test Coupon F, mm [in]

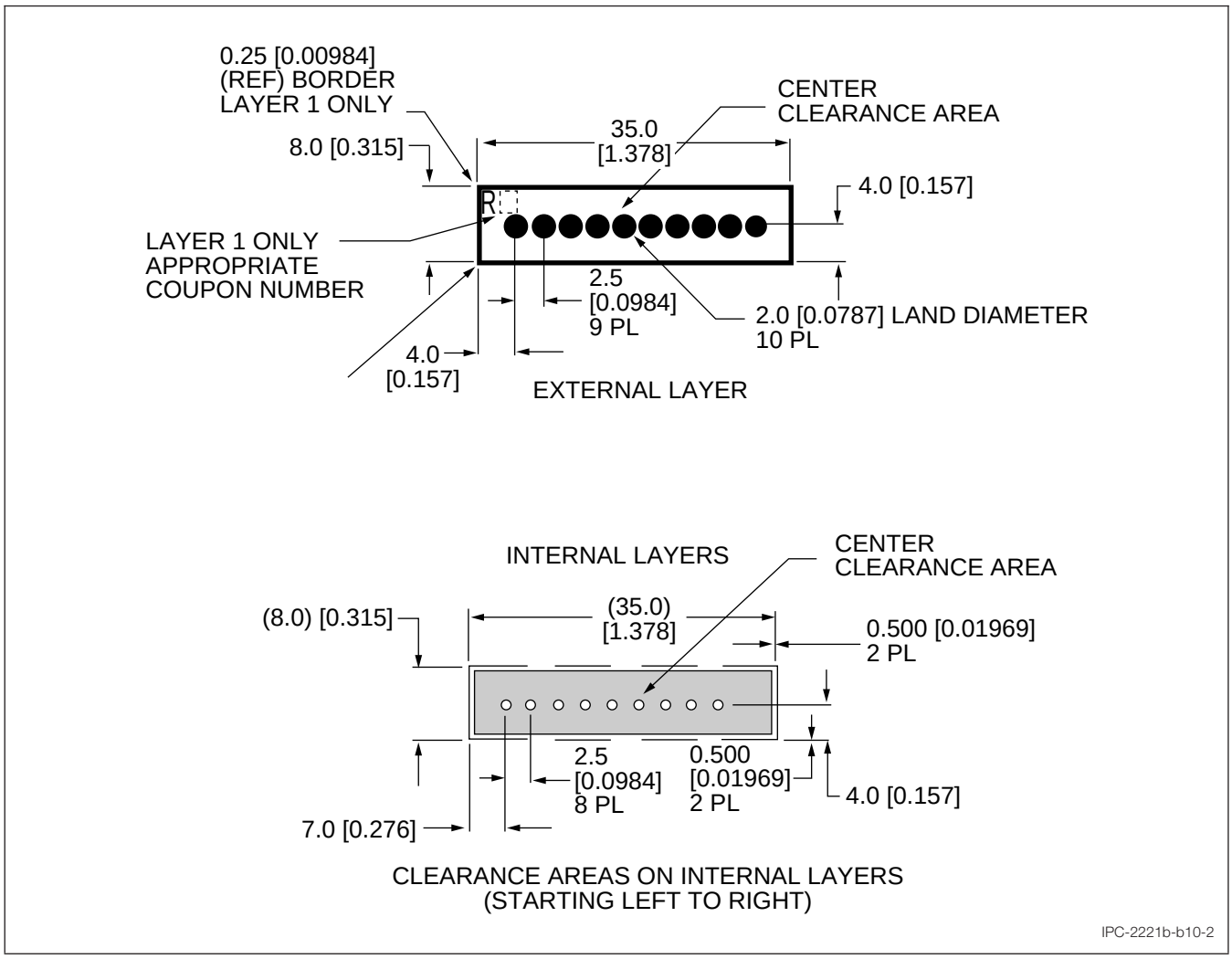

Figure B.10-2 Test Coupon R, mm [in]

B.10.3 Coupon R, Conformance Testing R coupon parameters are described in Figure B.10-2. The hole size and external lands are at the option of the fabricator. On internal layers, the coupon uses a ten hole pattern on 2.5 mm [0.0984 in] centers through a copper plane with circular clearance areas around nine of the holes. The clearance diameters are stepped in 50.0 µm [1,968 µin] increments for the first nine holes. There is no clearance area for the tenth hole so that the hole will make contact with the plane. The center clearance area **shall** be designed for the worst case hole-to-land diameter difference for the layer. Since the manufacturing allowance may vary from layer-to-layer, see Figure B.10-3, the diameter of the artwork center clearance area **shall** be calculated for each internal layer separately as follows:

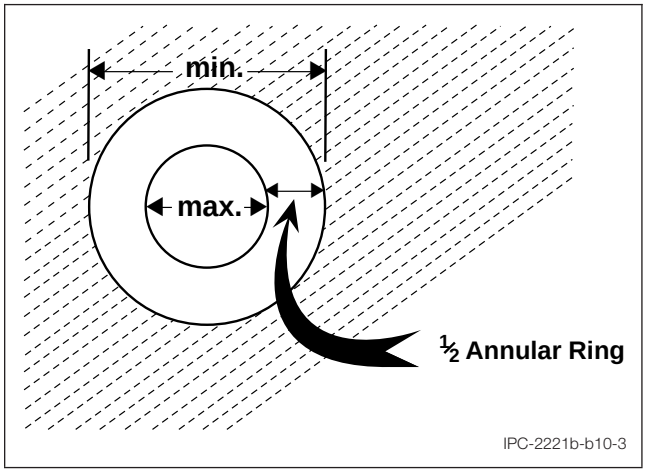

Figure B.10-3 Worst-Case Hole/Land Relationship

Clearance diameter = nominal drilled hole diameter + manufacturing allowance

Manufacturing allowance = smallest difference between any functional plated hole and land on that layer - 2X annular ring.

Evaluation of the coupon can only take place after determining the etch factor for each layer. The etch factor **shall** be determined before lamination as follows:

Etch loss = the diameter of the center clearance area after etch - the diameter of the center clearance on the artwork

The reference hole for annular ring evaluation will be to the left or the right of the center clearance area based on the etch factor. For example: If the etch factor is +0.1 mm [+0.0039 in], the reference hole **shall** be two holes to the right of the center clearance area. If the etch factor is -50.0 µm [-1,968 µn], the reference hole **shall** be one hole to the left of the center clearance area.

The coupon can be evaluated after drilling by measuring the annular ring using X-Ray. To accept the coupon using X-Ray, the reference hole **shall not** touch the plane.

The coupons are designed to measure annular ring after the holes are plated. The coupons are acceptable if there is no electrical connection between the reference hole and the tenth hole. The dimension of the annular ring can be determined by finding the first hole which makes electrical connection to the tenth hole and noting its position in relation to the reference hole. Each hole to the left or right of the reference hole represents a +25 µm [+0.984 mil] or -25 µm [-0.984 mil] respectively to the reference annular ring. This coupon is not referenced in IPC-6012. If it is used, the test method and performance criteria **shall** be specified in the procurement documentation.

B.11 Legacy N Coupon This legacy coupon **shall** be as described in Figure B.11-1. The legacy N coupon is used for evaluating peel strength and may be used to evaluate the bond strength of surface mount lands.

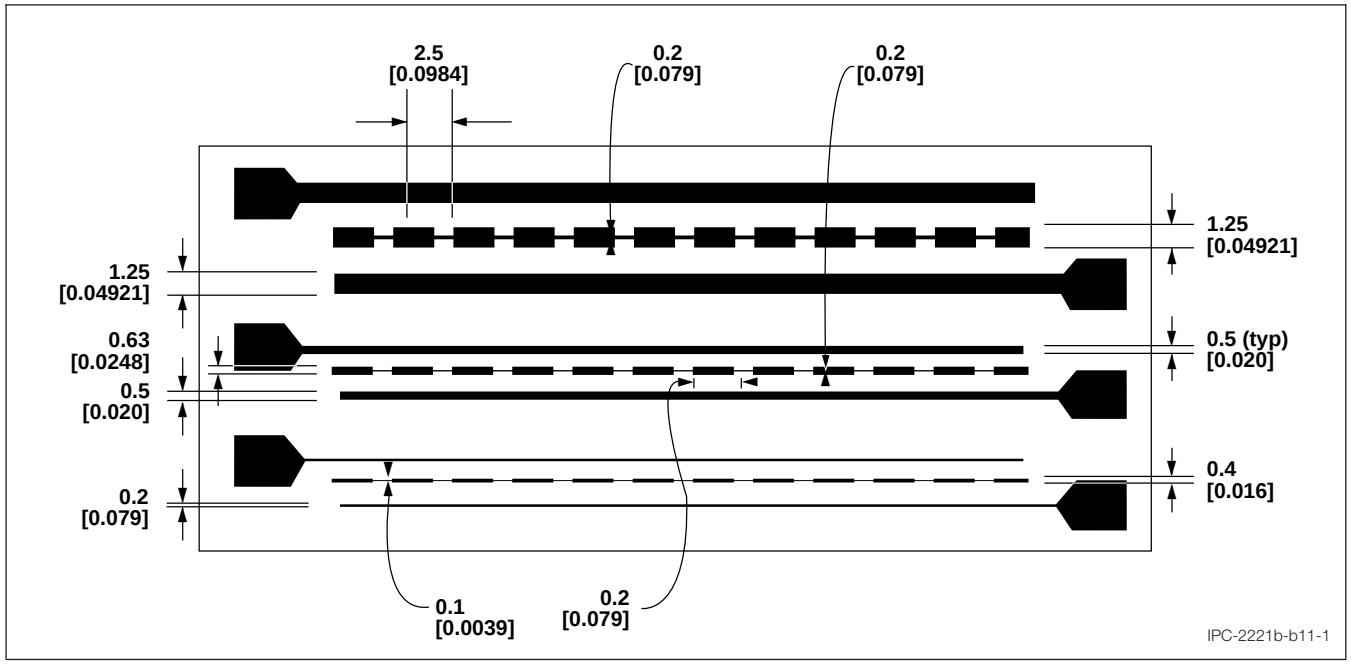

Figure B.11-1 Test Coupon N, Surface Mounting Bond Strength and Peel Strength, mm [in]

B.12 Coupon X (Bending Flexibility and Endurance, Flexible Printed Board) This coupon is used to validate bending flexibility and bending endurance of flexible printed board applications. This legacy coupon **shall** be as described in Figure B.12-1. The outline length of the coupon as shown in Figure B.12-1 is an example of one construction and may be deviated from in order to accommodate the test method fixture and circuit design. For example, rigid flex designs will have layers that do not span the flex area. The coupon **shall** reflect the construction of the specific portion of the finished flexible printed board that is being evaluated for bending flexibility and bending endurance. Accordingly, the final configuration of the coupon should be determined with regard for the end product application and by user/supplier agreement. The following minimum parameters **shall** be specified on the master drawing:

Bending Flexibility test requirements; See Figure B.12-2:

- Direction of bend (a)
- Degree of bend (b)
- Number of bend cycles (c)
- Diameter of mandrel (d)
- Point(s) of bend application

Note: Bend cycle is defined as taking one end of the specimen and bending it around a mandrel and then bending back to the original starting position, traveling 180° in one direction and 180° in the opposite direction. A bend cycle may also be defined as bending (using opposite ends) the ends toward each other (bend the same direction) and then bending them back to the original starting position, with each end traveling 90° in one direction and 90° in the opposite direction.

Bending endurance testing can be accomplished with test equipment specific to the circuit application. Requirements are end product specific and typically not defined in the applicable performance specification. Refer to IPC-TM-650, Method 2.4.3.1.

Bending Endurance test requirements:

- Number of flex cycles
- Diameter of the bend mandrels or separation of the loop-defining plates
- Flexing rate
- Points of application
- Travel of loop

The method for determining end of life cycle performance (visual, electrical test, resistance change, etc.) is an electrical discontinuity during monitoring, or passing the predetermined number of flex cycles without electrical discontinuity.

Refer to IPC-2223 for specific design flexibility guidelines.

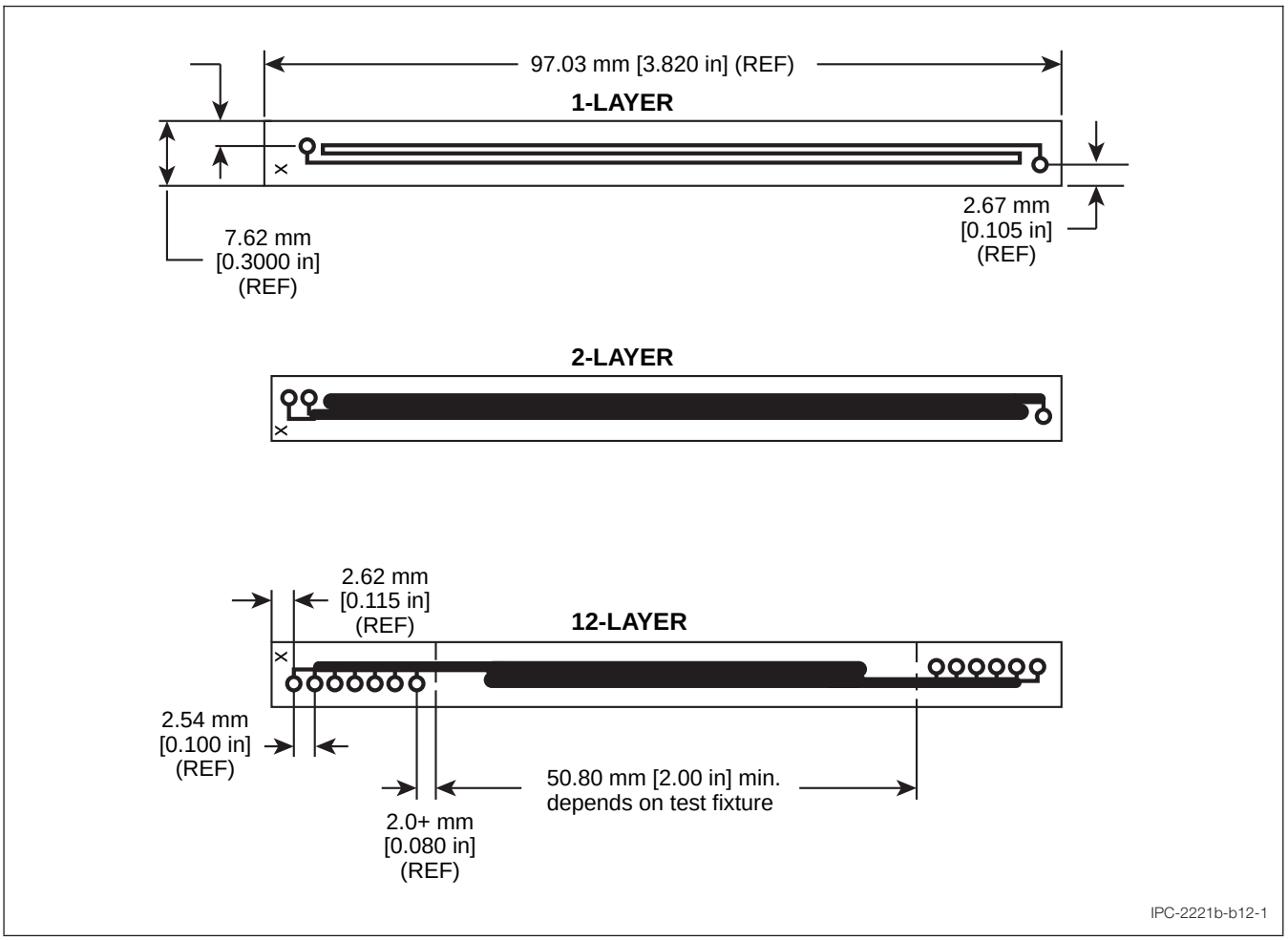

Figure B.12-1 Test Coupon X, mm [in]

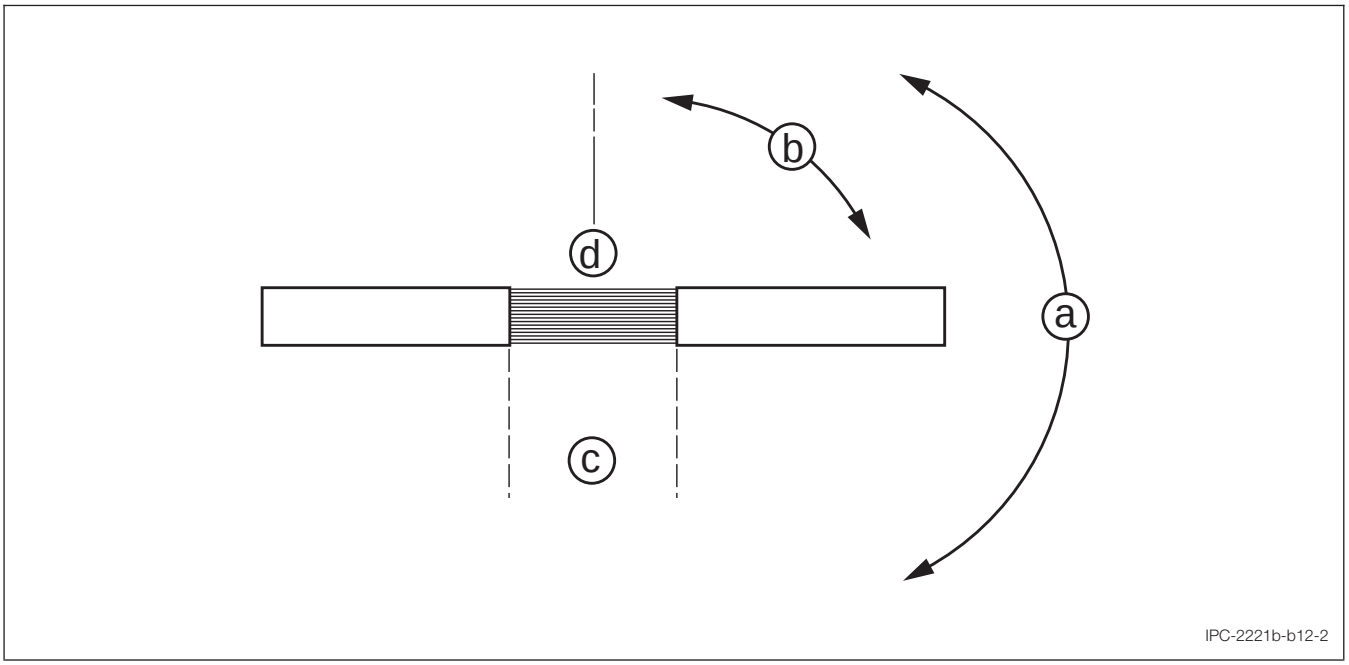

Figure B.12-2 Bending Test

APPENDIX C
Example of a Testability Design Checklist

- Route test/control points edge connector to enable monitoring and driving of internal board functions and to assist in fault diagnosis.
- Divide complex logic functions into smaller, combinational logic sections.
- Avoid one-shots; if used, route their signals to the edge connector.
- Avoid potentiometers and ''select-on-test''components.
- Use a single, large-edge connector to provide input/output pins and test/control points.
- Make printed board input/output signal logic-compatible to keep test equipment interface costs low and give flex ibility.
- Provide adequate decoupling at the board edge and locally at each integrated circuit.
- Provide signals leaving the board with maximum fan-out drive, or buffer them.
- Buffer edge-sensitive components from the edge connector - such as clock lines and flip-flop outputs.
- Do not tie signal outputs together.
- Never exceed the logic rated fan-out; in fact, keep it to a minimum.
- Do not use high fan-out logic devices. Do use multiple fan-out devices, and keep their outputs separate.
- Keep logic depth on any board to a low level by using edge terminated test/control points.
- Single-load each signal entering the board whenever possible.
- Terminate unused logic pins with a resistive pull-up to minimize noise pick-up.
- Do not terminate logic outputs directly into transistor bases. Do use a series current-limiting resistor.
- Buffer flip-flop output signals before they leave the board.
- Use open-collector devices with pull-up resistors to enable external override control.
- Avoid using redundant logic to minimize undetectable faults.
- Bring outputs of cascaded counters to higher-order counters so that they can be tested without large counts.
- Construct trees to check the parity of selected groups of eight bits or fewer.
- Avoid ''wired'OR'' and ''wired'AND'' connections. If you cannot, use gates from the same integrated circuit package.
- Provide some way to bypass level-changing diodes in series with logic outputs.
- Break paths when a logic element fans out to several places that converge later.
- Use elements in the same integrated circuit package when designing a series of inverters or inverters following a gate function.
- Standardize power-on and ground pins to avoid test-harness multiplicity.
- Bring out test points as near to digital-to-analog conversion as possible.
- Provide a means of disabling on-board clocks so that the tester clock may be substituted.
- Provide mounted switches and resistor-capacitor networks with override lines to the edge-board connector.
- Route logic drivers of lamps and displays to the edge connector so that the tester can check for correct operation.
- Divide large printed boards into subsections whenever possible, preferably by function.
- Separate analog circuits from digital logic, except for timing circuits.
- Uniformly mount integrated circuits and clearly identify them to make it easier to locate them.
- Provide sufficient clearance around integrated circuit sockets and direct-soldered integrated circuits so that clips can be attached whenever necessary.
- Add top-hat connector pins or mount extra integrated circuit sockets when there are not enough edge-board connector pins for test/control points.
- Use sockets with complex integrated circuits and long, dynamic shift registers.
- Wire feedback lines and other complex circuit lines to an integrated circuit package.
- Use jumpers that can be cut during debugging. The jumpers can be located near the edge-board connector.

• Fix locations of power and ground lines for uniformity among several board types.
• Make the ground conductor large enough to avoid noise problems.
• Group together signal lines of particular families.
• Clearly label all parts, pins and connectors.

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ANSI/IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits Definition Submission/Approval Sheet

The purpose of this form is to keep current with terms routinely used in the industry and their definitions. Individuals or companies are invited to comment. Please complete this form and return to:

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❑ This is an **ADDITION** to an existing term and definition(s).
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Term	Definition

If space not adequate, use reverse side or attach additional sheet(s).

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IPC Office	**Committee 2-30**
Date Received: _____	Date of Initial Review: _____
Comments Collated: _____	Comment Resolution: _____
Returned for Action: _____	Committee Action: ❑ Accepted ❑ Rejected
Revision Inclusion: _____	❑ Accept Modify

IEC Classification

Classification Code • Serial Number

Terms and Definition Committee Final Approval Authorization:
Committee 2-30 has approved the above term for release in the next revision.

Name: _____ Committee: IPC 2-30 Date: _____

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Put IPC MEMBERSHIP to WORK for your COMPANY

A trusted leader for more than 50 years, IPC is the premier source for industry standards, training, market research and public policy advocacy — supporting the needs of the estimated $1.7 trillion global electronics industry.

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Joseph F. O'Neil
President
Hunter Technology Corp

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- Stay abreast of global environmental directives, legislation and regulations, and how these specifically impact each segment of our industry's supply chain.

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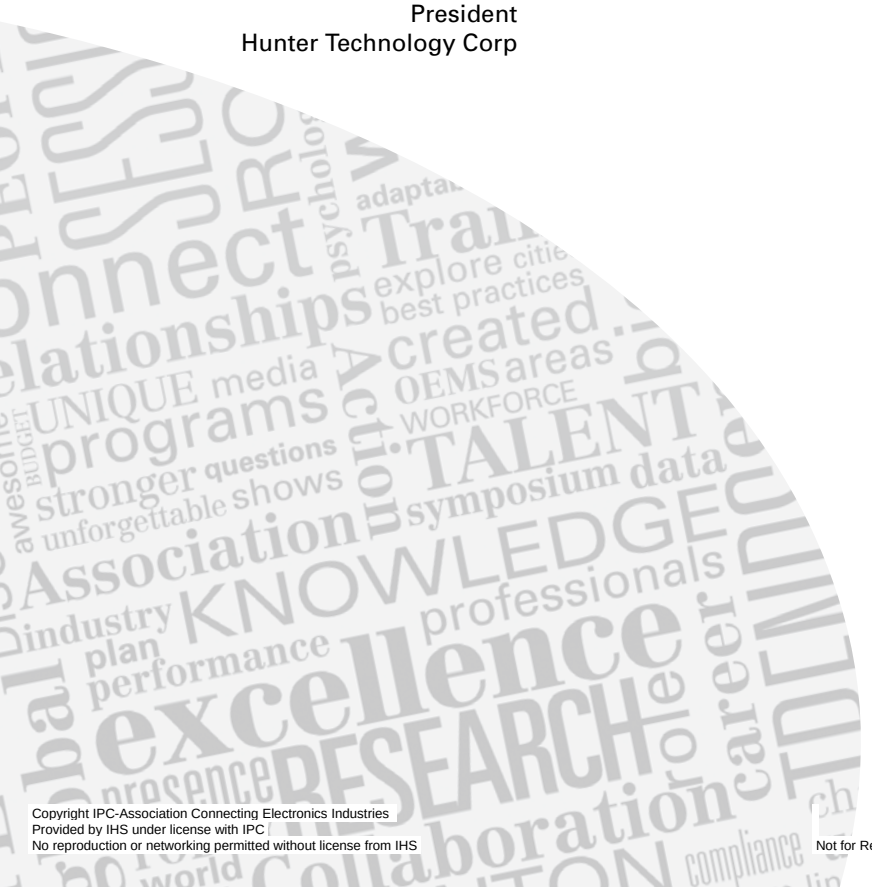

"Graphic PLC has enjoyed the privilege of being an IPC member for more than 30 years and the technical benefits derived to focus us as a world player in the manufacture of PCBs have superceded the cost of membership many times."

Rex Rozario, OBE
Chairman
Graphic Plc.,UK

"Being a part of the fast-changing global electronics marketplace requires constant intelligence about market trends, standards and solutions to the challenges throughout the supply chain. IPC is an invaluable partner in providing that intelligence through conferences, white papers and technical standards."

Andy Hyatt
Executive Vice President
Business Development
Creation Technologies

Increase your knowledge and train your people

- IPC workshops and international conferences provide an exchange of technical information that is unequalled.
- IPC's training and certification programs offer a cost-effective, industry-recognized way to demonstrate your commitment to quality.
- Facilitate your staff's continuous learning through IPC's award-winning CD- and DVD-based training materials.

"IPC's role in defining industry technical standards, addressing industry concerns, and promoting knowledging sharing through conferences and training, significantly benefits member companies and the industry as a whole, especially in today's global outsourcing environment."

Dongkai Shangguan, Ph.D.
Vice President
Flextronics International

Expand your network and build your visibility

- Network with your peers through IPC committees, PCB/EMS management councils and IPC events.
- Participate in problem-solving exchanges through IPC's technical e-forums.
- Get answers to your technical questions from IPC's technical staff.

"Juki gets tremendous value from our IPC membership … we get quarterly market data which would cost us thousands of dollars if we commissioned it on our own. The industry standards generated by IPC committees allow us to design our equipment with certainty that it will meet industry requirements. The returns for our company are so great, they are beyond calculable."

Bob Black
President and CEO
Juki Automation Systems Inc.

Help shape the industry

- Participate in developing or updating the global industry standards that your company, customers, competitors and suppliers use.
- Take an active role in IPC-organized environmental and public policy activities to advocate for regulations and legislation favorable to your company and the global electronics community.

Market your business

- Use the IPC member logo to highlight your company's leadership in the industry.
- Build your brand visibility through IPC's Products and Services Index (PCB and EMS companies only), and IPC's annual trade shows and conferences, including IPC APEX EXPO.
- Gain valuable exposure by sponsoring market research conferences and executive management meetings.

Put the resources of the entire industry behind your company by joining IPC today!

To learn more about IPC membership or to apply online, visit www.ipc.org.

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+1 847-615-7105 **fax**

Visit www.IPC.org/offices for the locations of IPC offices worldwide.

Association Connecting Electronics Industries

Application for Site Membership

Thank you for your decision to join IPC. Membership is **site specific**, which means that IPC member benefits are available to all individuals employed at the site designated on this application.

To best serve your specific needs, please indicate the most appropriate member category for your facility.
(Check one box only.)

☐ Printed Circuit Board Manufacturer

Facility manufactures and sells printed circuit boards (PCBs) or other electronic interconnection products to other companies.
What products do you make for sale? (check all that apply)

☐ One and two-sided rigid, multilayer printed boards ☐ Flexible printed boards ☐ Other interconnections

☐ Printed electronics

☐ Electronics Manufacturing Services (EMS) Company

Facility manufactures printed circuit assemblies, on a contract basis, and may offer other electronic interconnection products for sale.

☐ OEM — Original Equipment Manufacturer

Facility purchases, uses and/or manufactures printed circuit boards or other interconnection products for use in a final product, which we manufacture and sell.

What is your company's primary product line?_____

☐ Industry Supplier

Facility supplies raw materials, equipment or services used in the manufacture or assembly of electronic products.

Which industry segment(s) do you supply? ☐ PCB ☐ EMS ☐ Both ☐ Printed electronics

What products do you supply? _____

☐ Government, Academia, Nonprofit

Organization is a government agency, university, college or technical or nonprofit institution which is directly concerned with design, research and utilization of electronic interconnection devices.

☐ Consulting Firm

What services does the firm provide?_____

Association Connecting Electronics Industries

Application for Site Membership

Site Information

Company Name

Street Address

City | State | Zip/Postal Code | Country

Main Switchboard Phone No. | Main Fax

Company E-mail address | Website URL

Name of Primary Contact

Title | Mail Stop

Phone | Fax | E-mail

Payment Information (Purchase orders not accepted as a form of payment)

Membership Dues

Membership will begin the day the application and dues payment are received, and will continue for one or two years based on the choice indicated below. All fees are quoted in U.S. dollars.

Please check one:

Primary facility: ☐ One year $1,050.00 ☐ Two years $1,890.00 **(SAVE 10%)**	**Government agency, academic institution, nonprofit organization** ☐ One year $275.00 ☐ Two years $495.00 **(SAVE 10%)**
Additional facility: Membership for a facility of an organization that already has a different location with a primary facility membership ☐ One year $850.00 ☐ Two years $1,530.00 **(SAVE 10%)**	**Consulting firm (employing less than 6 individuals)** ☐ One year $625.00 ☐ Two years $1,125.00 **(SAVE 10%)**
Company with an annual revenue of less than $5,000,000 ☐ One year $625.00 ☐ Two years $1,125.00 **(SAVE 10%)**	

Enclosed is a check for $_____

Bill credit card: (check one) ☐ MasterCard ☐ American Express ☐ Visa ☐ Diners Club

Card No. | Expiration Date | Security Code

Authorized Signature

Mail application with check or money order to:

IPC
3491 Eagle Way
Chicago, IL 60678-1349

*Fax/Mail application with credit card payment to:

3000 Lakeside Drive, Suite 309 S
Bannockburn, IL 60015
Tel: +1 847-615-7100
Fax: +1 847-615-7105
www.ipc.org

**Overnight deliveries to this address only.*

Contact membership@ipc.org for wire transfer details

Please attach business card of primary contact here

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Standard Improvement Form

IPC-2221B

The purpose of this form is to provide the Technical Committee of IPC with input from the industry regarding usage of the subject standard.

Individuals or companies are invited to submit comments to IPC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, IL 60015-1249
Fax: 847 615.7105
E-mail: answers@ipc.org
www.ipc.org/standards-comment

1. I recommend changes to the following:

___ Requirement, paragraph number _____

___ Test Method number _____, paragraph number _____

The referenced paragraph number has proven to be:

___ Unclear ___ Too Rigid ___ In Error

___ Other _____

2. Recommendations for correction:

3. Other suggestions for document improvement:

Submitted by:

Name Telephone

Company E-mail

Address

City/State/Zip Date

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