CP319 Project Report

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Intro

For our digital system design we decided to design a digital timer. Our design measures intervals of time in seconds then displays that interval on a seven segment display. The system receives two inputs one for what time to count down too and a switch which starts the countdown.

The general design of our digital timer is based off of integrated timing circuits which are commonly used to source clock pulses to drive subsequent timer circuits. The integrated circuit can be set up in numerous ways allowing for a large amount of flexibility. By reducing the number of components and simplifying it into a single integrated circuit this caused a decrease in the physical mechanical maintenance of the circuit aswell as increasing the efficiency and quality of our circuit.

Potential Applications:

Digital timers have a wide range of uses in any task that require dealing with accurate measurements of time. Some potential applications involving digital timers include:

- Alarm Clocks
- Microwaves
- CPUs
- Etc.

Proposed Solution:

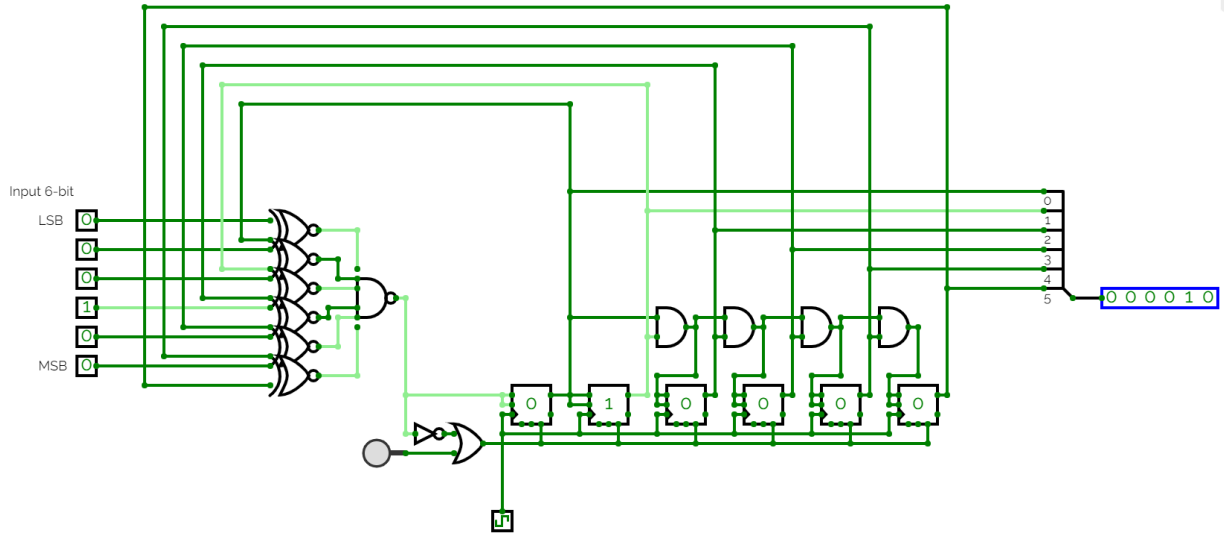
Keeping measurement of passing time is a common issue that can be solved by developing and designing a device which measures for you as time passes. Hence the original design of a timer. These timers were mechanical devices and used clockwork mechanisms as a means of keeping a regular time. After a few years came the electromechanical timer designs which allowed for more precise time measurement. However, both mechanical and electromechanical timers suffered from maintenance and longevity issues. Over time, the mechanical materials used such as gears would degrade and result in timer failures or inaccurate measurements. To fix this, we proposed creating a digital timer which is based on logic circuits and an accurate and regular clock signal, rather than analog mechanical components, to accurately measure time and eliminate all negative aspects of the past mechanical and electromechanical designs.

The general idea of the Digital design is to use the source of clock pulses to drive a subsequent timer circuit. The IC will be configured to give an astable, period output.

Circuit Design: (link)

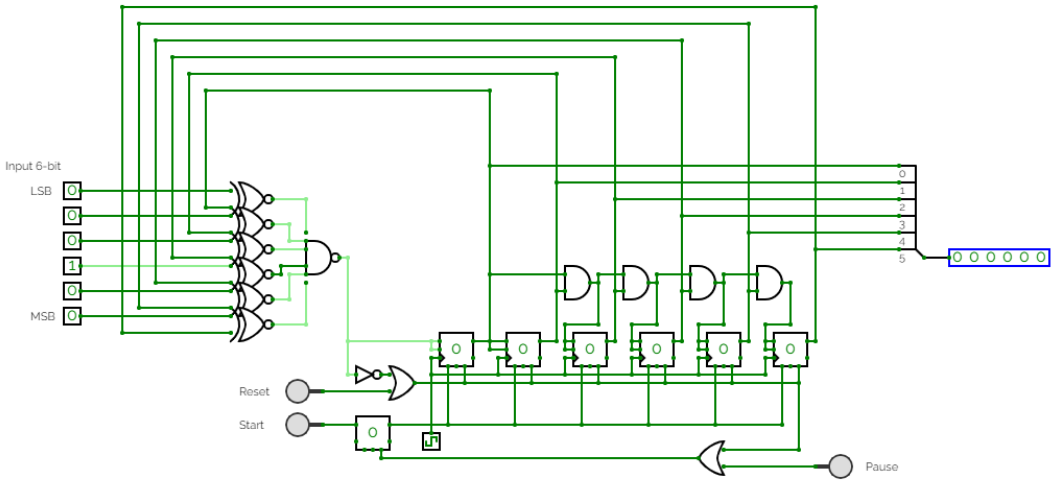
The first, and most important problem we needed to solve was how we were going to keep track of time and count upwards until our input value was reached. To do this, we needed to develop a

counter that would iterate forwards until the output value is equal to the input value, then reset itself back to its initial value (0). With this solution in mind, we developed the following circuit:



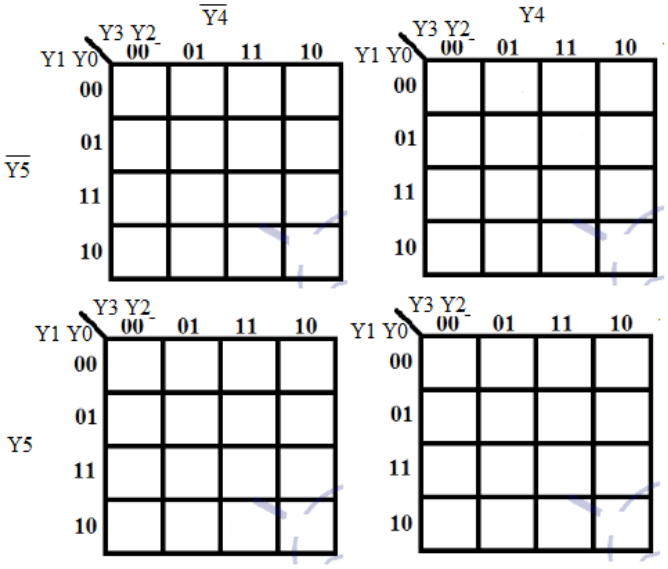
According to its truth table, XNOR gates output a HIGH value when both input values are equal, and a LOW value otherwise. Our counter utilizes the XNOR gate truth table to continue counting upwards until both the output and input values are equal. Once the input value is reached, reset the counter using the reset input on the JK-FlipFlops and start the counter again. Our circuit only needs to count until 60 (1 minute), thus we only needed 6 flip flops (one for each bit) and an input of 6 bits.

Outside of the main counter, we needed a way to gather the inputs and add our timer features (such as the start button, pause button and reset button). Thus, through the addition of an SR-Flip Flop and 2 buttons, we updated the circuit to the following:



The start button toggles the SR-Flip Flop (which is connected to the counter flip flop' enable bits on and begins the timer, whereas the "Pause" button resets the flip-flop to its initial state (0) and stops sending the HIGH signal to the enable bits.

As seen in the 7-segment-display tab of our CircuitVerse link, we also converted the timer outputs into a 2 digit 7-segment display output. We did this by creating truth tables for each segment of both displays and simplifying the expressions using 6-bit k-maps.



Although there are some logic mistakes, the display properly displays (most of) the numbers and successfully counts to 60 before it is reset. (.csv file containing truth tables for displays included in submission).

Implementation using VHDL:

In VHDL the digital timer can be implemented by first using an entity to specify the circuit's external interface along with the ports or input signals it can use.

```
library ieee;
use ieee.std_logic_1164.all;

entity digital_timer is
    port(
        count   :in std_logic_vector(6 down 0);
        display :out std_logic_vector(6 down 0);
        clock   :in std_logic;
```

```
        start   :in std_logic;
        pause   :in std_logic;
        reset   :in std_logic;

    );
end digital_timer;
```

The internal architecture handles the inner workings of the circuit with multiple processes to represent each component within the circuit. The main behaviour process of our circuit has a sensitivity list to make sure the clock input is detected.

```
architecture behavior of digital_timer is
    --Inputs
    signal count    :std_logic_vector(6 downto 0);
    signal clock    :std_logic;
    signal start    :std_logic;
    signal pause    :std_logic;
    signal reset    :std_logic;

    -- Outputs
    signal display  :std_logic_vector(6 downto 0);
begin
    process(clock)
    begin
        if clock'event and clock='1' then

            if count='0' then
                tmp <= tmp;
                elsif T='1' then
                    tmp <= not (tmp);
                end if;
            end if;
            end process;
end behavior
```

Simulations and Discussion:

As far as performance is concerned, our circuit design functions in the way it was expected to perform, with the exception of human errors (such as improperly simplified expressions). During development and testing, we have not encountered any noticeable time delays or glitches.

Conclusion

In conclusion, our chosen digital system of a timer has countless applications and can be used to solve numerous issues. Our implementation of a digital timer accepts an input from the user, converts it to seconds, waits for the start button to be pushed and then begins the count.

Throughout the creation of this timer we investigated many different digital circuit components. The components investigated that are included in our implementation of the timer are; Multiplexers, Counters, SR flip-flops and T flip-flops. The functionality of these components can be seen in our circuit.

Based on our investigations we found that with the chosen components we were able to successfully achieve the functionality required for a digital timer. In the future we hope to improve on our existing implementation by adding previously investigated components with the proper functionality, this includes 7 segment displays with the proper BCD (Binary-coded decimal) conversions applied.

References

Brown and Vranesic, *"Fundamentals of Digital Logic with VHDL Design"*. 3rd Edition, McGraw-Hill Education, 2008, ISBN 0077221435

Harris and Harris, *"Digital Design and Computer Architecture"*. 2nd Edition, Morgan Kaufmann, 2012, ISBN 0123944244

CircuitVerse. (2022). Version (Simulator). *CircuitVerse* . Retrieved December 16, 2022, from https://circuitverse.org/.