

Lab 06



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Ex. 1

- Cortex-M4 instruction set contains the following instruction:

UADD8 <Rd>, <Rn>, <Rm>

- UADD8 sums corresponding bytes of Rn and Rm, storing the result in Rd.
- Example:
Rn = 0x 7A 30 45 8D
Rm = 0x C3 15 9E AA
Rd = 0x 3D 45 E3 37
- Please note the absence of carry between bytes in Rd.

Ex. 1 (cont.)

- UADD8 is not present in Cortex-M3 instruction set.
- Write instructions for Cortex-M3 equivalent to
UADD8 r4, r0, r1.

Ex. 2

- Cortex-M4 instruction set contains the following instruction:

USAD8 <Rd>, <Rn>, <Rm>

- Each byte of R_n and R_m is a pure binary number.
- USAD8 calculates the absolute value of the difference between each byte in R_n and R_m .
- After that, USAD8 sums the four absolute values, storing the result in R_d .

Ex. 2 (cont.)

- Example: $R_n = 0x\ 7A\ 30\ 45\ 8D$
 $R_m = 0x\ C3\ 15\ 9E\ AA$

1. $|0x8D - 0xAA| = 0x1D$

2. $|0x45 - 0x9E| = 0x59$

3. $|0x30 - 0x15| = 0x1B$

4. $|0x7A - 0xC3| = 0x49$

$$R_d = 0x1D + 0x59 + 0x1B + 0x49 = 0xDA$$

- Note: the value in R_d can be on more than 8 bit

Ex. 2 (cont.)

- USAD8 is not present in Cortex-M3 instruction set.
- Write instructions for Cortex-M3 equivalent to
USAD8 r5, r0, r1.

Ex. 3

- Cortex-M4 instruction set contains the following instruction:

SMUAD <Rd>, <Rn>, <Rm>

SMUSD <Rd>, <Rn>, <Rm>

- Both instructions multiply the lower halfword of R_n times the lower halfword of R_m , and the higher halfword of R_n times the higher halfword of R_m .

Ex. 3 (cont.)

- Halfwords are considered in two's complement.
- SMUAD sums the two products and stores the result in R_d .
- SMUSD subtracts the product of high halfwords from the product of low halfwords, storing the result in R_d .

Ex. 3 (cont.)

- Example: $R_n = 0x7A30\ 458D$
 $R_m = 0xC315\ 9EAA$
- $0x458D * 0x9EAA = 0xE58E35A2$
- $0x7A30 * 0xC315 = 0xE2EC95F0$
- With SMUAD, $R_d = 0xC87ACB92$
- With SMUSD, $R_d = 0x02A19FB2$

Ex. 3 (cont.)

- SMUAD and SMUSD are not present in Cortex-M3 instruction set.
- Write instructions for Cortex-M3 equivalent to

SMUAD r6, r0, r1

SMUSD r7, r0, r1

Ex. 3 (cont.)

- The sign of halfwords has to be extended before multiplication.
- Example in pure binary:
 - $0x458D = 17805$
 - $0x9EAA = 40618$
 - $0x458D * 0x9EAA = 0x2B1B35A2 = 723.203.490$
- In two's complement:
 - $0x9EAA = -24918$
 - $0x458D * 0x9EAA = 0xE58235A2 = -443.664.990$

Ex. 4

- Create a new project selecting a board with Cortex-M4 core, for instance NXP LPC4072.

Write instructions:

```
UADD8  r4, r0, r1
```

```
USAD8  r5, r0, r1
```

```
SMUAD  r6, r0, r1
```

```
SMUSD  r7, r0, r1
```

- Verify that results are coherent with the ones obtained in the previous exercises.