14-Bit CCD Signal Processor with *Precision Timing*™ Generator

AD9970

FEATURES

- 1.8 V analog and digital core supply voltage
- Serial data link with reduced range LVDS outputs
- Correlated double sampler (CDS) with −3 dB, 0 dB, +3 dB, and +6 dB gain
- 6 dB to 42 dB, 10-bit variable gain amplifier (VGA)
- 14-bit, 65 MHz ADC
- Black level clamp with variable level control
- Complete on-chip timing generator
- *Precision Timing* core with 240 ps resolution @ 65 MHz
- On-chip, 3 V horizontal and RG drivers
- 5 mm × 5 mm, 32-lead LFCSP_VQ

APPLICATIONS

- Professional HDTV camcorders
- Professional/high end digital cameras
- Broadcast cameras
- Industrial high speed cameras
- High speed data acquisition systems

GENERAL DESCRIPTION

The AD9970 is a highly integrated CCD signal processor for high speed digital video camera applications. Specified at pixel rates of up to 65 MHz, the AD9970 consists of a complete analog front end with analog-to-digital conversion combined with a programmable timing driver. The *Precision Timing* core allows adjustment of high speed clocks with 240 ps resolution at 65 MHz operation. The AD9970 also contains a reduced range LVDS interface for data outputs.

The analog front end includes black level clamping, CDS, VGA, and a 65 MSPS, 14-bit ADC. The timing driver provides the high speed CCD clock drivers for RG, HL, and H1 to H4. Operation is programmed using a 3-wire serial interface.

Packaged in a space-saving 5 mm × 5 mm, 32-lead LFCSP_VQ, the AD9970 is specified over an operating temperature range of −25°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

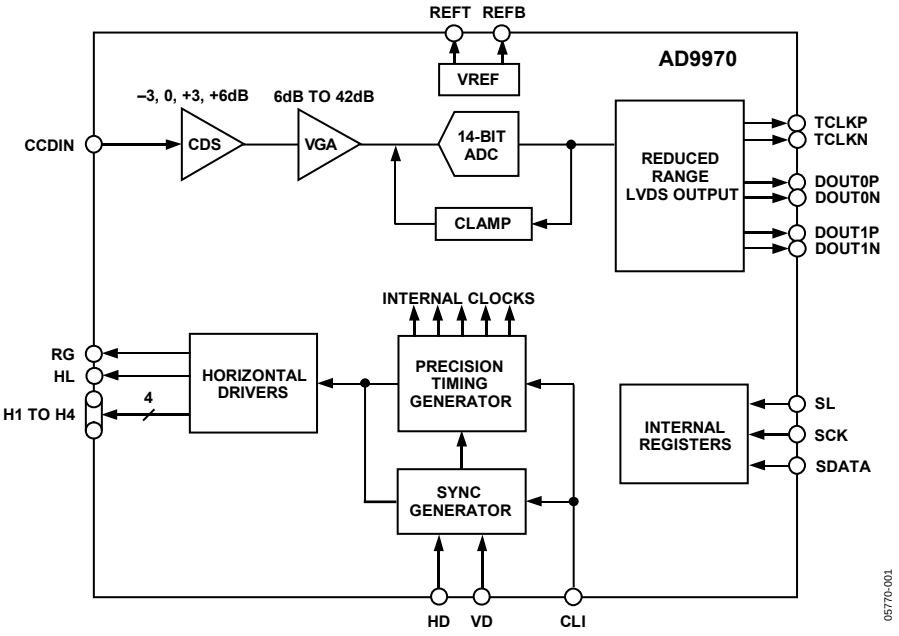

Figure 1.

Rev. SpB

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10/05—Revision Sp0: Initial Version

SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating	–25		+85	°C
Storage	–65		+150	°C
POWER SUPPLY VOLTAGE				
AVDD, (AFE, Timing Core)	1.6	1.8	2.0	V
RGVDD (RG Driver)	2.7	3.0	3.6	V
HVDD (H1 to H4 Drivers)	2.7	3.0	3.6	V
DVDD (Internal Digital Supply)	1.6	1.8	2.0	V
LVDD (LVDS Output Drivers)	1.6	1.8	2.0	V
IOVDD (I/O Supply for HD, VD, SCK, SL, SDATA, CLI)	1.6	1.8	3.6	V
POWER SUPPLY CURRENTS—65 MHz OPERATION				
AVDD (1.8 V)		55		mA
RGVDD (3.3 V, 20 pF RG Load, 20 pF HL Load)		8		mA
HVDD[1] (3.3 V, 200 pF Total Load on H1 to H4)		40		mA
DVDD (1.8 V)		18		mA
LVDD (1.8 V)		17		mA
IOVDD (1.8 V)		2		mA
POWER SUPPLY CURRENTS—STANDBY MODE OPERATION				
Reference Standby		10		mA
Total Shutdown		0.5		mA
MAXIMUM CLOCK RATE (CLI)	65			MHz
MINIMUM CLOCK RATE (CLI)	8			MHz

[1] The total power dissipated by the HVDD or RGVDD supply can be approximated using the equation

Total HVDD Power = [C_{LOAD} × *HVDD* × *Pixel Frequency*] × *HVDD*

Reducing the capacitive load and/or reducing the HVDD supply reduces the power dissipation. C_{LOAD} is the total capacitance seen by all H-outputs.

DIGITAL SPECIFICATIONS

IOVDD = 1.6 V to 3.6 V, RGVDD = HVDD = 2.7 V to 3.6 V, C_L = 20 pF, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	IOVDD – 0.6			V
Low Level Input Voltage	V_{IL}			0.6	V
High Level Input Current	I_{IH}		10		µA
Low Level Input Current	I_{IL}		10		µA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS					
High Level Output Voltage, I_{OH} = 2 mA	V_{OH}	IOVDD – 0.5			V
Low Level Output Voltage, I_{OL} = 2 mA	V_{OL}			0.5	V
CLI INPUT					
High Level Input Voltage	V_{IHCLI}	IOVDD/2 + 0.5			V
Low Level Input Voltage	V_{ILCLI}			IOVDD/2 – 0.5	V
H-DRIVER OUTPUTS					
High Level Output Voltage @ Maximum Current	V_{OH}	HVDD – 0.5			V
Low Level Output Voltage @ Maximum Current	V_{OL}			0.5	V
Maximum Output Current (Programmable)			30		mA
Maximum Load Capacitance		100			pF

ANALOG SPECIFICATIONS

AVDD = 1.8 V, f_{CLI} = 65 MHz, typical timing specifications, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CDS[1]					
Allowable CCD Reset Transient		0.5	0.8	V	
CDS Gain Accuracy					
−3.0 dB CDS Gain	−3.2	−2.7	−2.2	dB	
0 dB CDS Gain (Default)	−0.5	0	+0.5	dB	
+3 dB CDS Gain	+2.4	+2.9	+3.4	dB	
+6 dB CDS Gain	+4.5	+5	+5.5	dB	
Maximum Input Voltage					VGA gain = 5.6 dB (Code 15, default value)
−3 dB CDS Gain		1.4		V p-p	
0 dB CDS Gain (Default)		1.0		V p-p	
+3 dB CDS Gain		0.7		V p-p	
+6 dB CDS Gain		0.5		V p-p	
Allowable OB Pixel Amplitude[1]					
0 dB CDS Gain (Default)	−100		+200	mV	
+6 dB CDS Gain	−50		+100	mV	
VARIABLE GAIN AMPLIFIER (VGA)					
Gain Control Resolution		1024		Steps	
Gain Monotonicity		Guaranteed			
Low Gain Setting (VGA Code 15, Default)		5.6		dB	
Maximum Gain Setting (VGA Code 1023)		41.8		dB	
BLACK LEVEL CLAMP					
Clamp Level Resolution		1024		Steps	
Minimum Clamp Level (Code 0)		0		LSB	Measured at ADC output
Maximum Clamp Level (Code 1023)		1023		LSB	Measured at ADC output
ADC					
Resolution	14			Bits	
Differential Nonlinearity (DNL)	−1.0	±0.5	+1.2	LSB	
No Missing Codes		Guaranteed			
Integral Nonlinearity (INL)		5	16	LSB	
Full-Scale Input Voltage		2.0		V	
VOLTAGE REFERENCE					
Reference Top Voltage (REFT)		1.4		V	
Reference Bottom Voltage (REFB)		0.4		V	
SYSTEM PERFORMANCE					Specifications include entire signal chain
VGA Gain Accuracy					0 dB CDS gain (default)
Low Gain (Code 15)	5.1	5.6	6.1	dB	Gain = (0.0359 × code) + 5.1 dB
Maximum Gain (Code 1023)	41.3	41.8	42.3	dB	
Peak Nonlinearity, 500 mV Input Signal		0.1	0.4	%	12 dB total gain applied
Total Output Noise		2		LSB rms	AC grounded input, 6 dB total gain applied
Power Supply Rejection (PSR)		45		dB	Measured with step change on supply

[1] Input signal characteristics are defined as shown in Figure 2. Note that OB refers to optical black.

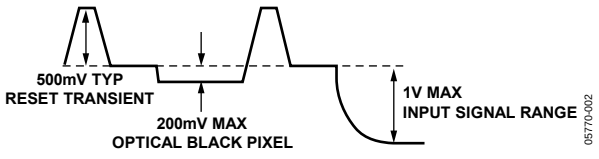


Figure 2. Input Signal Characteristics

TIMING SPECIFICATIONS

C_L = 20 pF, AVDD = DVDD = 1.8 V, f_{CLI} = 65 MHz, CLI_BIAS disabled (0x15[0] = 0x0), unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
MASTER CLOCK (CLI)					
CLI Clock Period	t_{CLI}	15.38			ns
CLI High/Low Pulse Width	t_{ADC}	6.9	7.7	8.9	ns
Delay from CLI Rising Edge to Internal Pixel Position 0	t_{CLIDLY}		5		ns
AFE					
SHP Rising Edge to SHD Rising Edge (See Figure 23)	t_{S1}	6.9	7.7	8.5	ns
AFE Pipeline Delay (See Figure 24)			18		Cycles
CLPOB Pulse Width (Programmable) [1]		2	20		Pixels
SERIAL INTERFACE (See Figure 65)					
Maximum SCK Frequency (Must Not Exceed CLI Frequency)	f_{SCLK}	40			MHz
SL-to-SCK Setup Time	t_{LS}	10			ns
SCK-to-SL Hold Time	t_{LH}	10			ns
SDATA Valid-to-SCK Rising Edge Setup	t_{DS}	10			ns
SCK Falling Edge-to-SDATA Valid Hold	t_{DH}	10			ns
H-COUNTER RESET SPECIFICATIONS (See Figure 61)					
HD Pulse Width		t_{CONV}			ns
VD Pulse Width		1 HD period			ns
VD Falling Edge to HD Falling Edge	t_{VDHD}	0		VD period − t_{CONV}	ns
HD Falling Edge to CLI Rising Edge	t_{HDCLI}	3		t_{CONV} − 2	ns
CLI Rising Edge to SHPLOC (Internal Sample Edge)	T_{CLISHP}	3		t_{CONV} − 2	ns
TIMING CORE SETTING RESTRICTIONS (See Figure 23)					
Inhibited Region for SHP Edge Location [2]	t_{SHPINH}	50		64/0	Edge location
Inhibited Region for SHP or SHD With Respect to H-Clocks [3,4,5,6]					
RETIME = 0, MASK = 0	t_{SHDINH}	HxNEGLOC − 15		HxNEGLOC − 0	Edge location
RETIME = 0, MASK = 1	t_{SHDINH}	HxPOSLOC − 15		HxPOSLOC − 0	Edge location
RETIME = 1, MASK = 0	t_{SHPINH}	HxNEGLOC − 15		HxNEGLOC − 0	Edge location
RETIME = 1, MASK = 1	t_{SHPINH}	HxPOSLOC − 15		HxPOSLOC − 0	Edge location
Inhibited Region for DOUTPHASE Edge Location	$t_{DOUTINH}$	SHDLOC + 0		SHDLOC + 15	Edge location

[1] Minimum CLPOB pulse width is for functional operation only. Wider typical pulses are recommended to achieve good clamp performance.
[2] Only applies to slave mode operation. The inhibited area for SHP is needed to meet the timing requirements for T_{CLISHP} for proper H-counter reset operation.
[3] When 0x34[2:0] HBLKRETIME bits are enabled, the inhibit region for SHD location changes to the inhibit region for the SHP location.
[4] When sequence register 0x09[23:21] HBLK masking registers are set to 0, the H-edge reference becomes HxNEGLOC.
[5] The H-clock signals that have SHP/SHD inhibit regions depend on the HCLK mode:
Mode 1 = H1
Mode 2 = H1, H2
Mode 3 = H1, H3
[6] These specifications apply when H1POL, H2POL, RGPOL, and HLPOL are all set to 1 (default setting).

LVDS SPECIFICATIONS

R_L = 100 Ω, LVDD = 1.8 V, f_{CLI} = 65 MHz, f_{TCLK} = 260 MHz, unless otherwise noted.

Table 5. Reduced Range LVDS Driver Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Output Voltage High, V_{OA} or V_{OB}	R_{LOAD} = 100 Ω ± 1%	V_{OH}			1400	mV
Output Voltage Low, V_{OA} or V_{OB}	R_{LOAD} = 100 Ω ± 1%	V_{OL}	1000			mV
Output Differential Voltage	R_{LOAD} = 100 Ω ± 1%	$\|V_{OD}\|$	120		290	mV
Output Offset Voltage	R_{LOAD} = 100 Ω ± 1%	V_{OS}	1075		1350	mV
Change in $\|V_{OD}\|$ Between 0 and 1	R_{LOAD} = 100 Ω ± 1%	$\|V_{OD}\|$			25	mV
Change in V_{OS} Between 0 and 1	R_{LOAD} = 100 Ω ± 1%	V_{OS}			25	mV

Table 6. LVDS Driver AC Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Clock Signal Duty Cycle		t_{CYCLE}	40		60	%
TCLK Frequency		f_{TCLK}			260	MHz
V_{OD} Fall Time, 20% to 80%	R_{LOAD} = 100 Ω ± 1%	t_{FALL}		140		ps
V_{OD} Rise Time, 20% to 80%	R_{LOAD} = 100 Ω ± 1%	t_{RISE}		140		ps
Differential Skew	Any differential pair	t_{SKEW1}		25		ps
Channel-to-Channel Skew	Any two signals	t_{SKEW2}		30		ps

TIMING DIAGRAMS

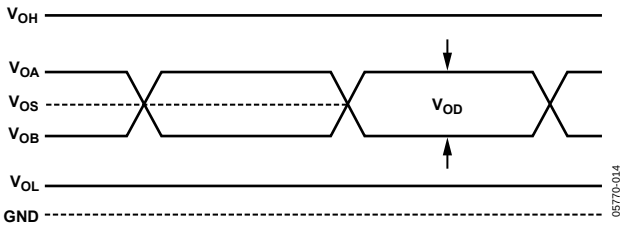


Figure 3. LVDS Driver Waveform

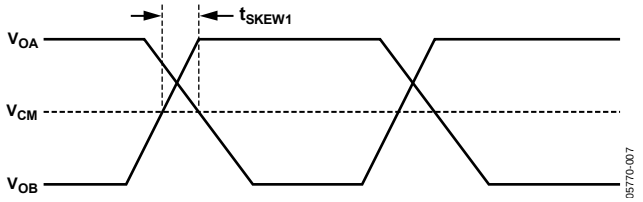


Figure 5. Definition of t_{SKEW1}

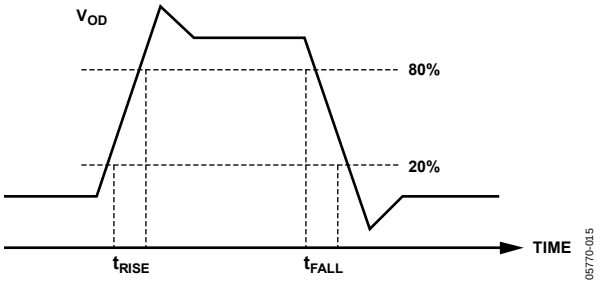


Figure 4. Driver Rise and Fall Times

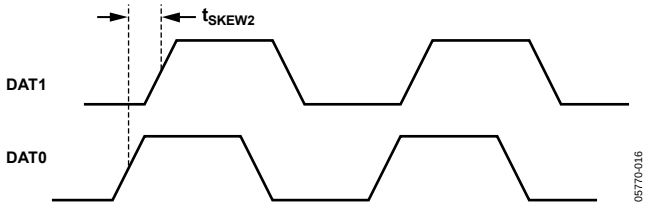


Figure 6. Definition of t_{SKEW2}

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	With Respect To	Rating
AVDD	AVSS	–0.3 V to +2.2 V
DVDD	DVSS	–0.3 V to +2.2 V
LVDD	LVSS	–0.3 V to +2.2 V
IOVDD	DVSS	–0.3 V to +3.9 V
HVDD	HVSS	–0.3 V to +3.9 V
RGVDD	RGVSS	–0.3 V to +3.9 V
Any VSS	Any VSS	–0.3 V to +0.3 V
RG Output	RGVSS	–0.3 V to RGVDD + 0.3 V
H1 to H4, HL Output	HVSS	–0.3 V to HVDD + 0.3 V
Digital Output	IOVSS	–0.3 V to IOVDD + 0.3 V
Digital Input	IOVSS	–0.3 V to IOVDD + 0.3 V
SCK, SL, SDATA	IOVSS	–0.3 V to IOVDD + 0.3 V
LVDS Outputs	LVSS	–0.3 V to LVDD + 0.3 V
REFT, REFB, CCDIN	AVSS	–0.3 V to AVDD + 0.3 V
Junction Temperature		150°C
Lead Temperature, 10 sec		350°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

θ_{JA} is measured using a 4-layer PCB with the exposed paddle soldered to the board.

Table 8. Thermal Resistance

Package Type	θ_{JA}	Unit
32-Lead, 5 mm × 5 mm, LFCSP_VQ	27.7	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

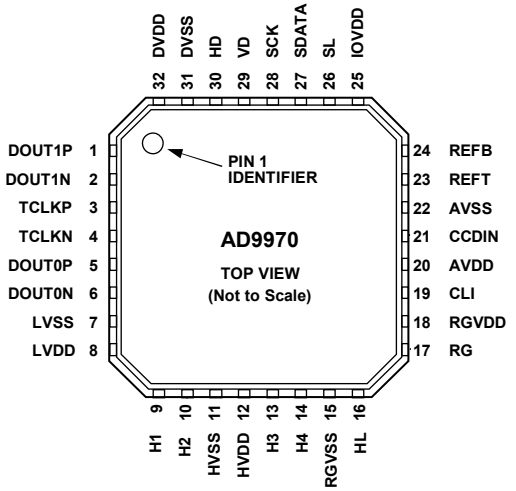


Figure 7. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	DOUT1P	DO	Data Output 1, Positive Output.
2	DOUT1N	DO	Data Output 1, Negative Output.
3	TCLKP	DO	Transmit Clock, Positive Output.
4	TCLKN	DO	Transmit Clock, Negative Output.
5	DOUT0P	DO	Data Output 0, Positive Output.
6	DOUT0N	DO	Data Output 0, Negative Output.
7	LVSS	P	LVDS Output Ground.
8	LVDD	P	LVDS Output Supply: 1.8 V.
9	H1	DO	CCD Horizontal Clock 1.
10	H2	DO	CCD Horizontal Clock 2.
11	HVSS	P	Horizontal Driver Ground.
12	HVDD	P	Horizontal Driver Supply: 3.0 V.
13	H3	DO	CCD Horizontal Clock 3.
14	H4	DO	CCD Horizontal Clock 4.
15	RGVSS	P	RG Driver Ground.
16	HL	DO	CCD Horizontal HL Clock.
17	RG	DO	CCD Reset Gate Clock.
18	RGVDD	P	RG Driver Supply: 3.0 V.
19	CLI	DI	Master Clock Input.
20	AVDD	P	Analog Supply for AFE: 1.8 V.
21	CCDIN	AI	Analog Input for CCD Signal. Connect through series 0.1 µF capacitor.
22	AVSS	P	Analog Ground for AFE.
23	REFT	AO	Reference Top Decoupling. Bypass with 0.1 µF to AVSS.
24	REFB	AO	Reference Bottom Decoupling. Bypass with 0.1 µF to AVSS.
25	IOVDD	P	Digital I/O Supply: 3.0 V (HD, VD, SL, SCK, SDATA).
26	SL	DI	3-Wire Serial Load.
27	SDATA	DI	3-Wire Serial Data Input.
28	SCK	DI	3-Wire Serial Clock.
29	VD	DI	Vertical Synchronization Pulse.
30	HD	DI	Horizontal Synchronization Pulse.
31	DVSS	P	Digital Ground.
32	DVDD	P	Digital Internal Logic Supply: 1.8 V.

[1] AI = analog input, AO = analog output, DI = digital input, DO = digital output, P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

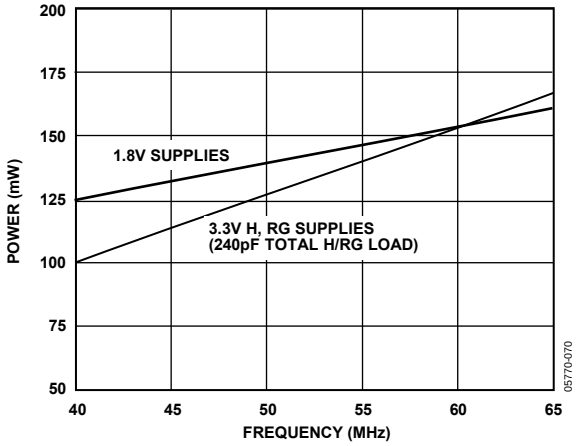


Figure 8. Power vs. Sample Rate

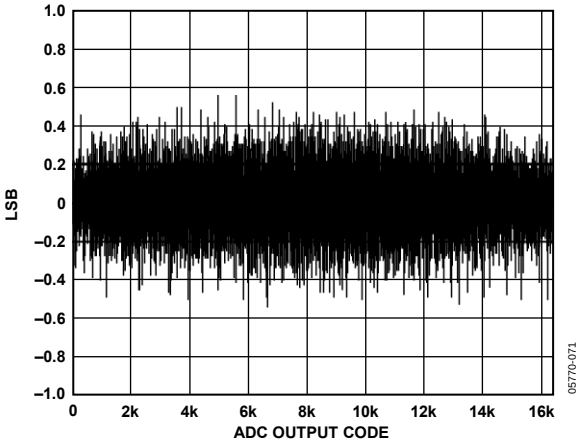


Figure 10. Differential Nonlinearity (DNL)

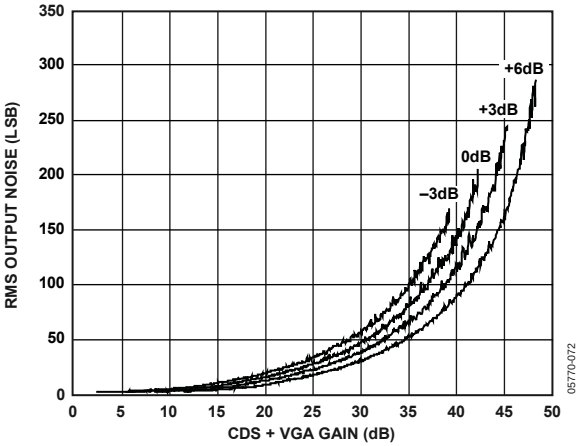


Figure 9. Noise vs. CDS + VGA Gain

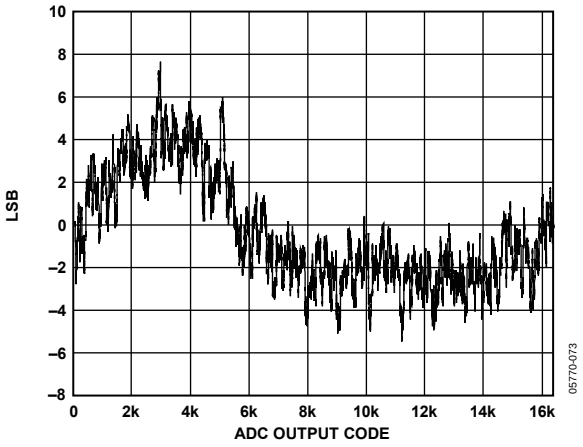


Figure 11. System Integral Nonlinearity (INL)

EQUIVALENT INPUT/OUTPUT CIRCUITS

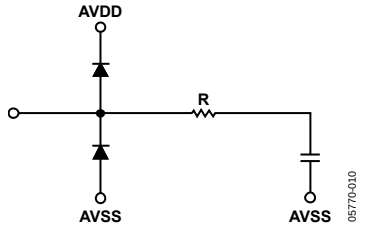


Figure 12. CCDIN Input

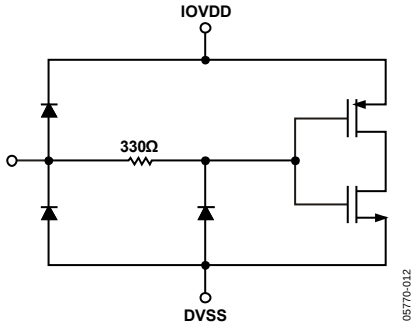


Figure 14. Digital Inputs

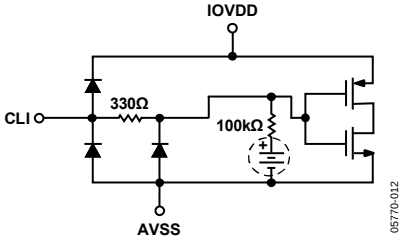


Figure 13. CLI Input, Register 0x15[0] = 1
(Enables the Internal Bias Voltage for AC-Coupled CLI Application Only)

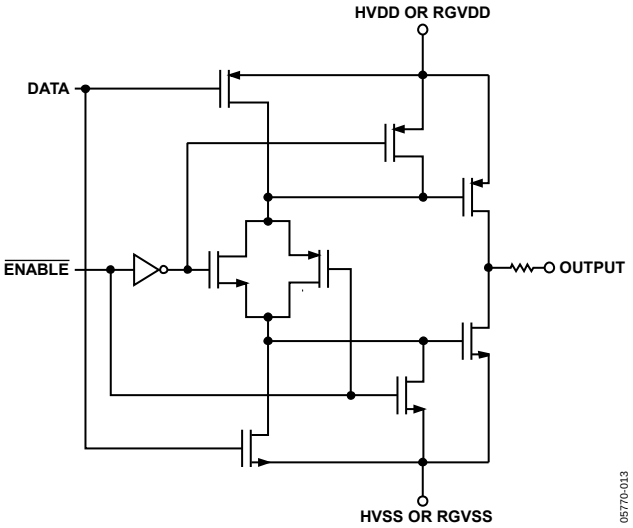


Figure 15. H1 to H4, HL and RG Outputs

TERMINOLOGY

Differential Nonlinearity (DNL)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore, every code must have a finite width. No missing codes guaranteed to 14-bit resolution indicates that all 16,384 codes, each for its respective input, must be present over all operating conditions.

Peak Nonlinearity
Peak nonlinearity, a full signal chain specification, refers to the peak deviation of the output of the AD9970 from a true straight line. The point used as zero scale occurs 0.5 LSB before the first code transition. Positive full scale is defined as a level 1 LSB and 0.5 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the true straight line. The error is then expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always gained appropriately to fill the ADC full-scale range.

Total Output Noise
The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage using the relationship

$$1\ \text{LSB} = (\textit{ADC Full Scale}/2^{n}\ \textit{Codes})$$

where n is the bit resolution of the ADC. For the AD9970, 1 LSB is approximately 122.0 μV.

Power Supply Rejection (PSR)
The PSR is measured with a step change applied to the supply pins. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.

THEORY OF OPERATION

Figure 16 shows the typical system block diagram for the AD9970. The CCD output is processed by the AFE circuitry of the AD9970 consisting of a CDS, VGA, black level clamp, and ADC. The digitized pixel information is sent to the digital image processor chip that performs the postprocessing and compression. To operate the CCD, all CCD timing parameters are programmed into the AD9970 from the system ASIC, through the 3-wire serial interface. From the system master clock, CLI, provided by the image processor or external crystal, the AD9970 generates the horizontal clocks of the CCD and all internal AFE clocks.

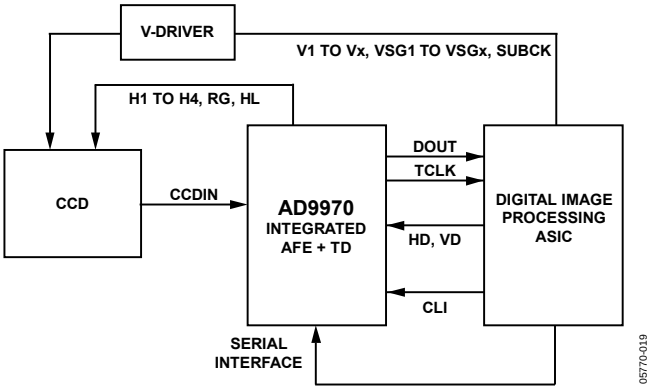


Figure 16. Typical Application

All AD9970 clocks synchronize with VD and HD inputs. All AD9970 horizontal pulses (CLPOB, PBLK, and HBLK) are programmed and generated internally.

The H-drivers for H1 to H4 and RG are included in the AD9970, allowing these clocks to be directly connected to the CCD. H-drive voltage of 3 V is supported in the AD9970.

Figure 17 and Figure 18 show the maximum horizontal and vertical counter dimensions for the AD9970. All internal horizontal and vertical clocking is controlled by these counters to specify line and pixel locations. Maximum HD length is 8192 pixels per line, and maximum VD length is 8192 lines per field.

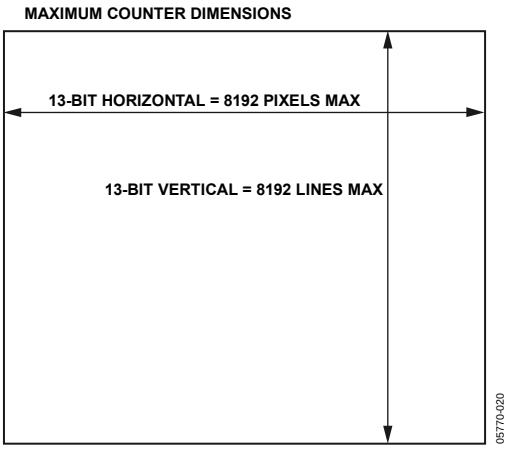


Figure 17. Vertical and Horizontal Counters

H-Counter Behavior

In the AD9970, the internal H-counter holds at its maximum count of 8191 pixels instead of rolling over. This feature allows the AD9970 to be used in applications containing a line length greater than 8192 pixels. Although no programmable values for the horizontal blanking or clamping are available beyond pixel 8191, the H, RG, and AFE clocking continues to operate, sampling the remaining pixels on the line.

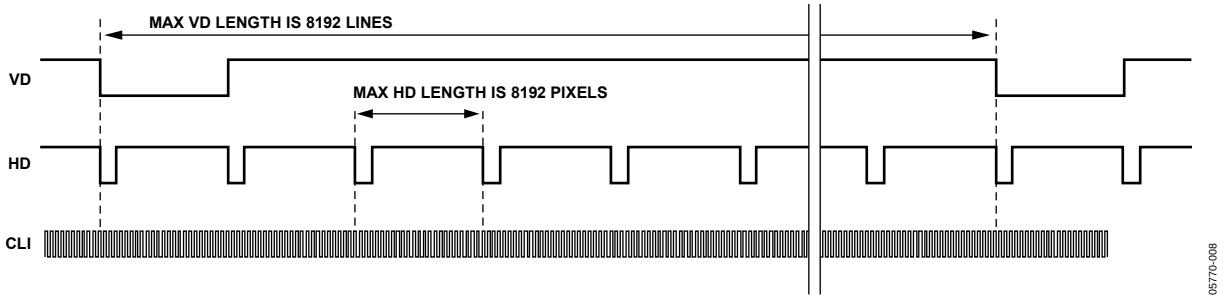


Figure 18. Maximum VD/HD Dimensions

PROGRAMMABLE TIMING GENERATION

PRECISION TIMING HIGH SPEED TIMING CORE

The AD9970 generates flexible high speed timing signals using the *Precision Timing* core. This core is the foundation for generating the timing for both the CCD and the AFE, the Reset Gate RG, HL, Horizontal Driver H1 to Horizontal Driver H4, and the SHP/SHD sample clocks. A unique architecture makes it routine for the system designer to optimize image quality by providing precise control over the horizontal CCD readout and the AFE correlated double sampling.

Timing Resolution

The *Precision Timing* core uses a master clock input (CLI) as a reference. This clock should be the same as the CCD pixel clock frequency. Figure 19 illustrates how the internal timing core divides the master clock period into 64 steps or edge positions. Therefore, the edge resolution of the *Precision Timing* core is (t_{CLI}/64). For more information on using the CLI input, refer to the Applications Information section.

Using a 65 MHz CLI frequency, the edge resolution of the *Precision Timing* core is approximately 240 ps. If a 1× system clock is not available, it is also possible to use a 2× reference clock by programming the CLIDIVIDE register (Address 0x0D). The AD9970 then internally divides the CLI frequency by 2.

High Speed Clock Programmability

Figure 20 shows how the high speed clocks, RG, HL, H1 to H4, SHP, and SHD are generated. The RG pulse has programmable rising and falling edges, and can be inverted using the polarity control. The HL, H1, and H2 horizontal clocks have separate programmable rising and falling edges, and polarity control. The AD9970 provides additional HCLK-mode programmability, as described in Table 10.

The edge location registers are each six bits wide, allowing the selection of all 64 edge locations. Figure 23 shows the default timing locations for all of the high speed clock signals.

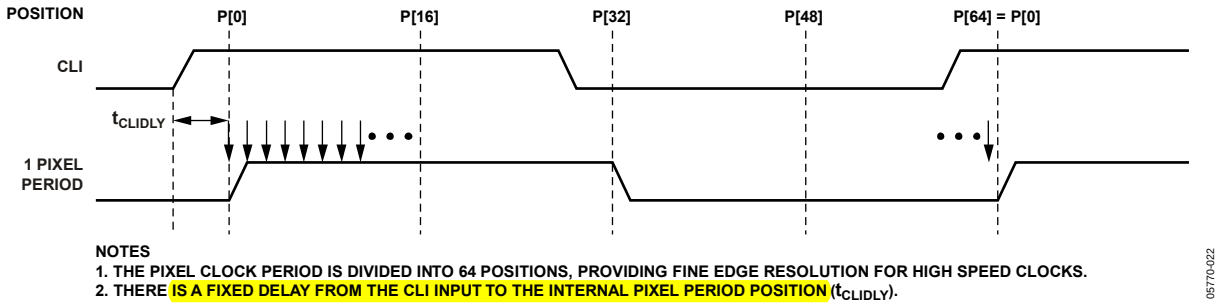


Figure 19. High Speed Clock Resolution from CLI Master Clock Input

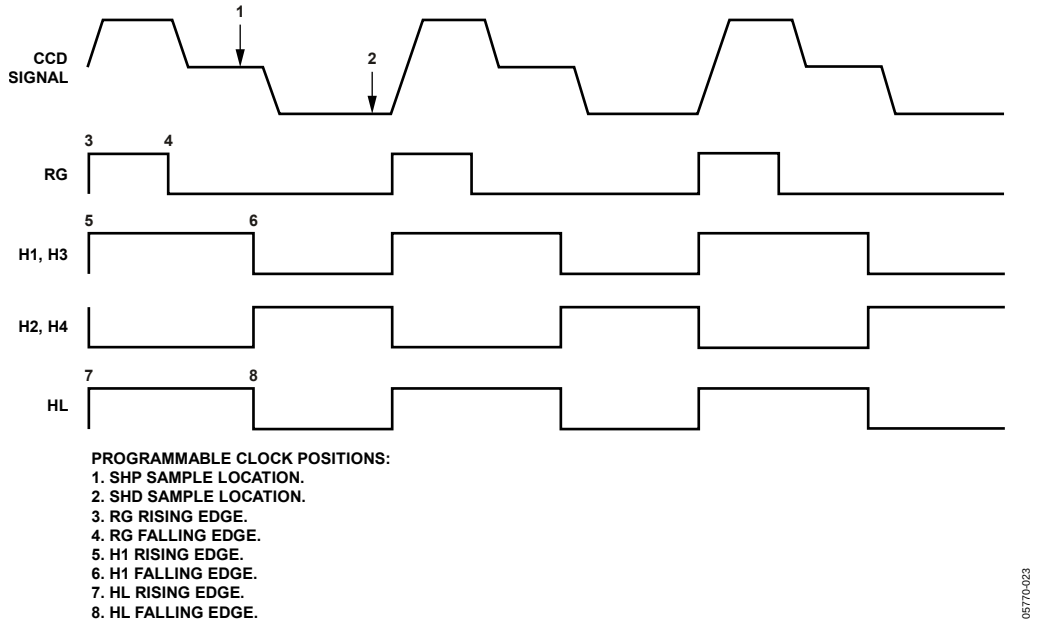


Figure 20. High Speed Clock Programmable Locations (HCLKMODE 1)

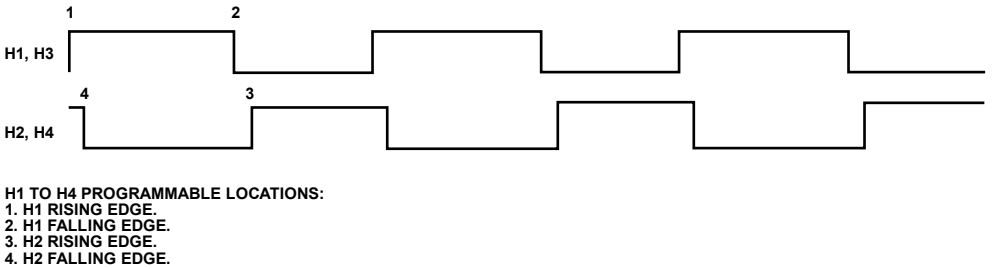


Figure 21. HCLKMODE 2 Operation

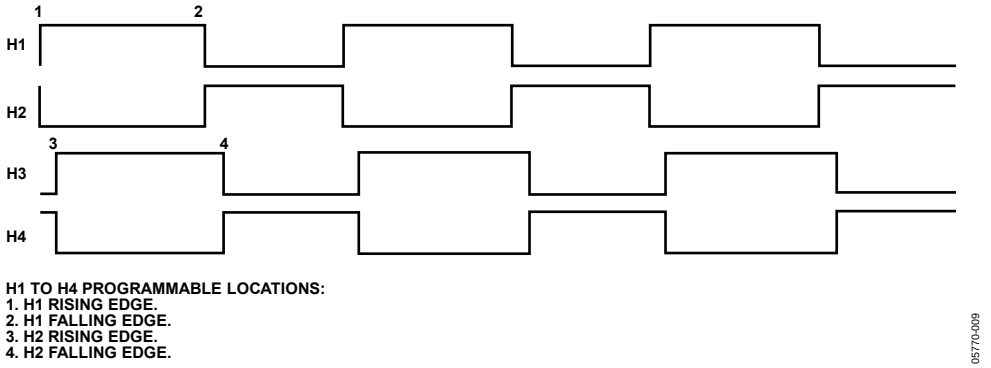


Figure 22. HCLKMODE 3 Operation

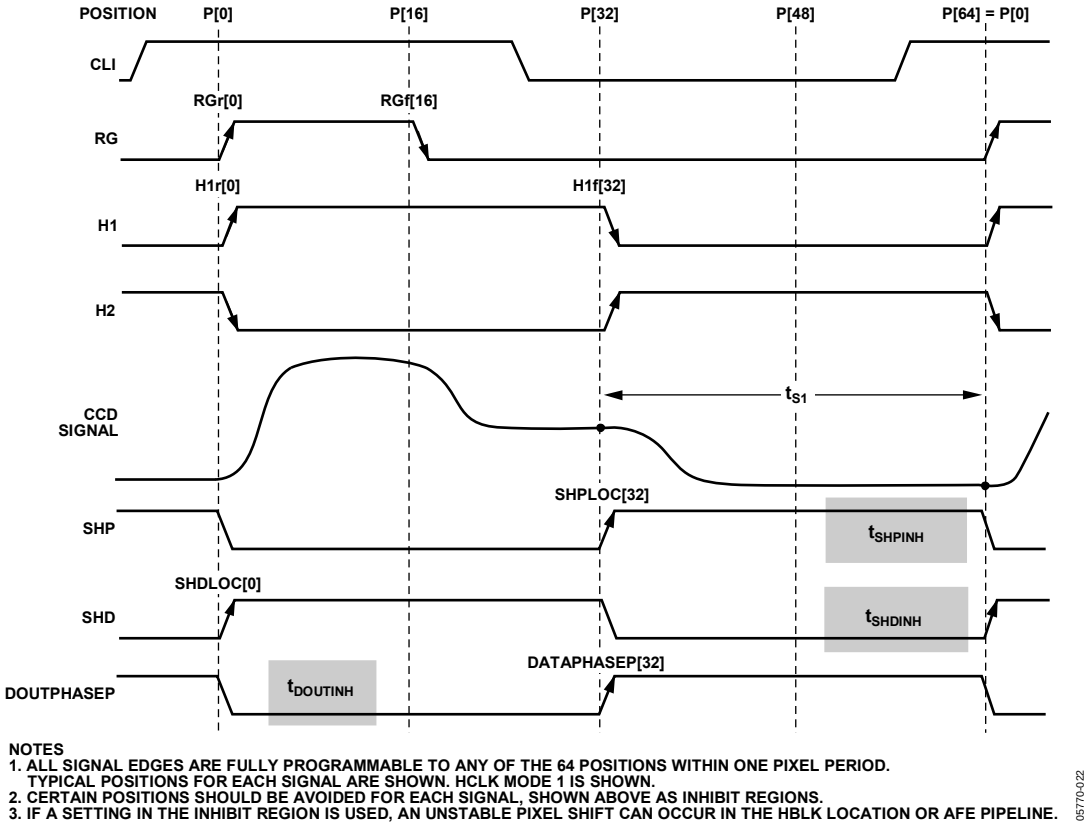


Figure 23. High Speed Timing Default Locations

Table 10. HCLK Modes, Selected by Register 0x23, Bits[7:5]

HCLK Mode	Register Value	Description
Mode 1	001	H1 edges are programmable with H3 = H1, H2 = H4 = inverse of H1.
Mode 2	010	H1 edges are programmable with H3 = H1. H2 edges are programmable with H4 = H2.
Mode 3	100	H1 edges are programmable with H2 = inverse of H1. H3 edges are programmable with H4 = inverse of H3.
Invalid Selection	000, 011, 101, 110, 111	Invalid register settings.

Table 11. H1, H2, H3, HLCONTROL, RGCONTROL, DRVCONTROL, and SAMPCONTROL Register Parameters

Parameter	Length	Range	Description
Polarity	1 bit	High/low	Polarity control for H1/H3 and RG. 0 = no inversion. 1 = inversion.
Positive Edge	6 bits	0 to 63 edge location	Positive edge location for H1/H3 and RG.
Negative Edge	6 bits	0 to 63 edge location	Negative edge location for H1/H3 and RG.
Sample Location	6 bits	0 to 63 sample location	Sampling location for SHP and SHD.
Drive Control	3 bits	0 to 7 current steps	Drive current for H1 to H4 and RG outputs, 0 to 7 steps of 4.1 mA each.

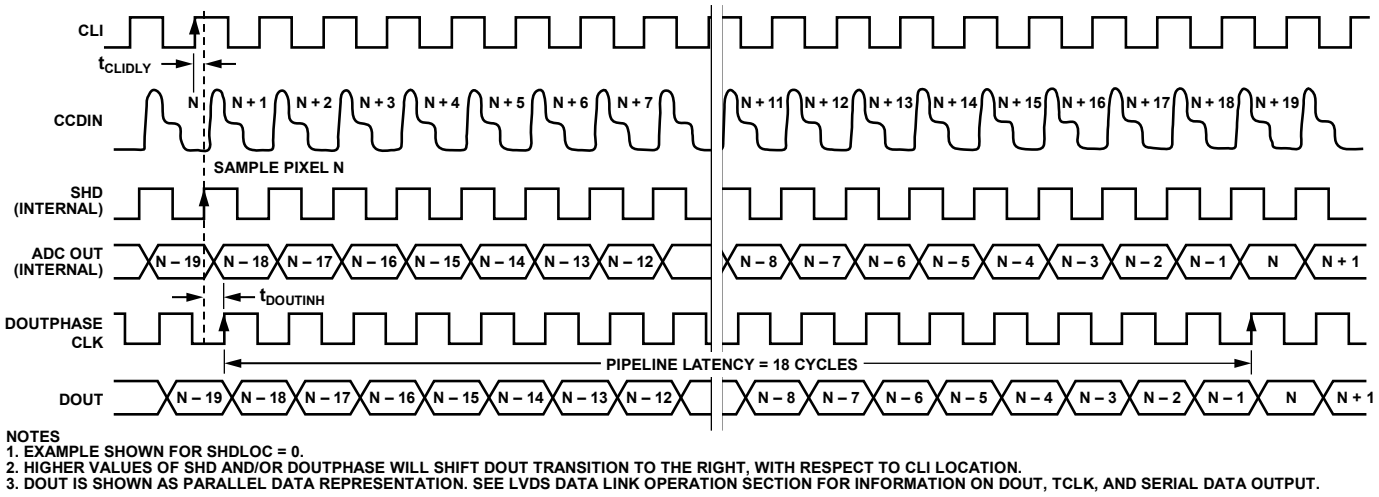


Figure 24. Pipeline Delay of AFE Data Outputs

H-Driver and RG Outputs

In addition to the programmable timing positions, the AD9970 features on-chip output drivers for the HL, RG, and H1 to H4 outputs. These drivers are powerful enough to directly drive the CCD inputs. The H-driver and RG-driver currents can be adjusted for optimum rise/fall times into a particular load by using the drive strength control registers (Address 0x35). Use the registers to adjust the drive strength in 4.3 mA increments. The minimum setting of 0 is equal to off or three-state, and the maximum setting of 7 is equal to 30.1 mA.

Digital Data Outputs

For maximum system flexibility, the AD9970 uses the DOUTPHASE register (Address 0x37, Bits[11:0]) to select the location for the start of each new pixel data value. Any edge location from 0 to 63 can be programmed. This register determines the start location of the data output and TCLK rising edge with respect to the Master Clock Input CLI. For more information, see the Programmable Data Delay section.

The pipeline delay through the AD9970 is shown in Figure 24. After the CCD input is sampled by SHD, there is an 18-cycle delay until the data is available.

HORIZONTAL CLAMPING AND BLANKING

The horizontal clamping and blanking pulses of the AD9970 are fully programmable to suit a variety of applications. Individual control is provided for CLPOB, PBLK, and HBLK during the different regions of each field. This allows the dark pixel clamping and blanking patterns to be changed at each stage of the readout to accommodate different image transfer timing and high speed line shifts.

Individual CLPOB and PBLK Patterns

The AFE horizontal timing consists of CLPOB and PBLK, as shown in Figure 25. These two signals are independently programmed using the registers in Table 12. POL is the start polarity for the signal, and TOG1 and TOG2 are the first and second toggle positions of the pulse. Both signals are active low, and need to be programmed accordingly.

Two separate patterns for CLPOB and PBLK can be programmed for each H-pattern, CLPOB0, CLPOB1, PBLK0, and PBLK1. The CLPOB_PAT and PBLK_PAT field registers select which of the two patterns are used in each field.

Figure 36 shows how the sequence change positions divide the readout field into different regions. By assigning a different H-pattern to each region, the CLPOB and PBLK signals can change with each change in the vertical timing.

CLPOB and PBLK Masking Area

Additionally, the AD9970 allows the CLPOB and PBLK signals to be disabled during certain lines in the field, without changing any of the existing pattern settings. There are three sets of start and end registers for both CLPOB and PBLK that allow the creation of up to three masking areas for each signal.

For example, to use the CLPOB masking, program the CLPOBMASKSTART and CLPOBMASKEND registers to specify the starting and ending lines in the field where the CLPOB patterns are to be ignored. Figure 26 illustrates this feature.

The masking registers are not specific to a certain H-pattern; they are always active for any existing field of timing. To disable the CLPOB and PBLK masking feature, set these registers to the maximum value of 0x1FFF.

Note: During power-up, the recommended settings to disable CLPOB and PBLK masking are MASKSTART = 8191 and MASKEND = 0. This prevents any accidental masking caused by different register update events.

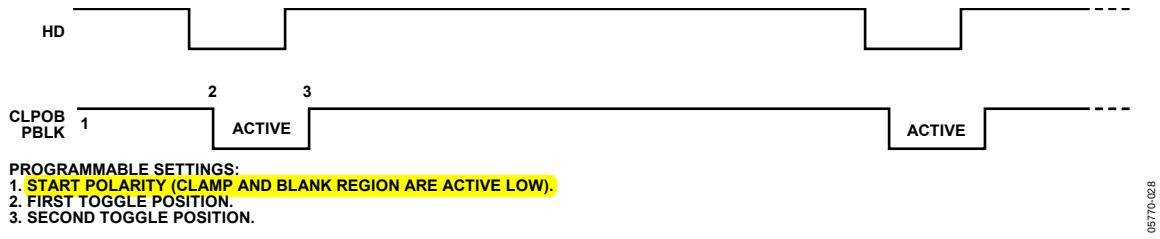


Figure 25. Clamp and Preblank Pulse Placement

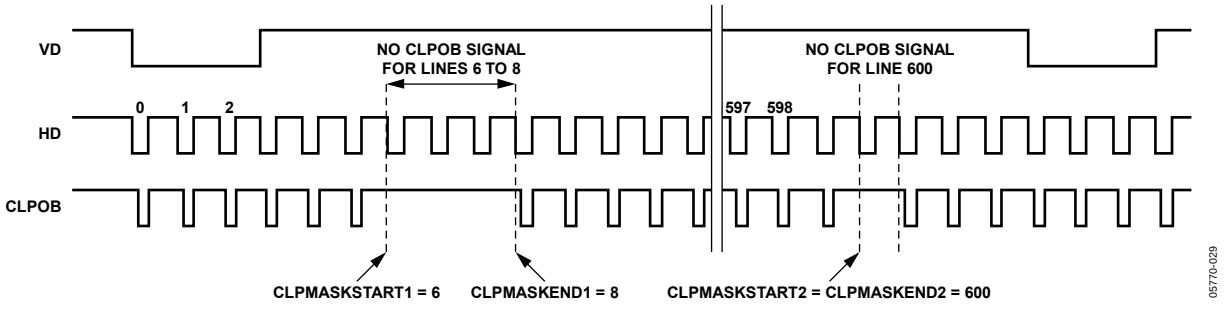


Figure 26. CLPOB Masking Example

Table 12. CLPOB and PBLK Parameters

Parameter	Length	Range	Description
CLPOB0_TOG1	13 bits	0 to 8191 pixel location	First CLPOB0 toggle position within the line for each V-sequence.
CLPOB0_TOG2	13 bits	0 to 8191 pixel location	Second CLPOB0 toggle position within the line for each V-sequence.
CLPOB1_TOG1	13 bits	0 to 8191 pixel location	First CLPOB1 toggle position within the line for each V-sequence.
CLPOB1_TOG2	13 bits	0 to 8191 pixel location	Second CLPOB1 toggle position within the line for each V-sequence.
CLPOB_POL	9 bits	High/low	Starting polarity of CLPOB for each V-Sequence[8:0] (in field registers).
CLPOB_PAT	9 bits	0 to 9 settings	CLPOB pattern selection for each V-Sequence[8:0] (in field registers).
CLPOBMASKSTART	13 bits	0 to 8191 pixel location	CLPOB Mask Start Position. Three values available (in field registers).
CLPOBMASKEND	13 bits	0 to 8191 pixel location	CLPOB Mask End Position. Three values available (in field registers).
PBLK0_TOG1	13 bits	0 to 8191 pixel location	First PBLK0 toggle position within the line for each V-sequence.
PBLK0_TOG2	13 bits	0 to 8191 pixel location	Second PBLK0 toggle position within the line for each V-sequence.
PBLK1_TOG1	13 bits	0 to 8191 pixel location	First PBLK1 toggle position within the line for each V-sequence.
PBLK1_TOG2	13 bits	0 to 8191 pixel location	Second PBLK1 toggle position within the line for each V-sequence.
PBLK_POL	9 bits	High/low	Starting polarity of PBLK for each V-Sequence[8:0] (in field registers).
PBLK_PAT	9 bits	0 to 9 settings	PBLK pattern selection for each V-Sequence[8:0] (in field registers).
PBLKMASKSTART	13 bits	0 to 8191 pixel location	PBLK Mask Start Position. Three values available (in field registers).
PBLKMASKEND	13 bits	0 to 8191 pixel location	PBLK Mask End Position. Three values available (in field registers).

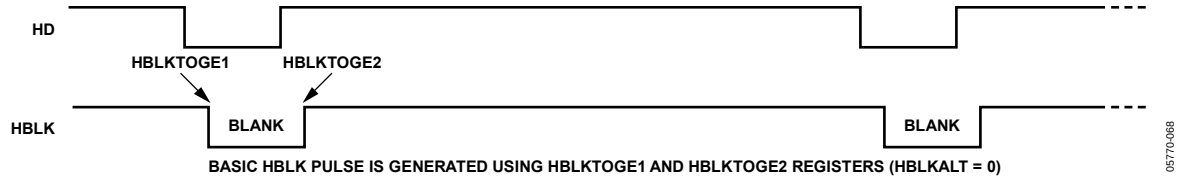


Figure 27. Typical Horizontal Blanking Pulse Placement (HBLKMODE = 0)

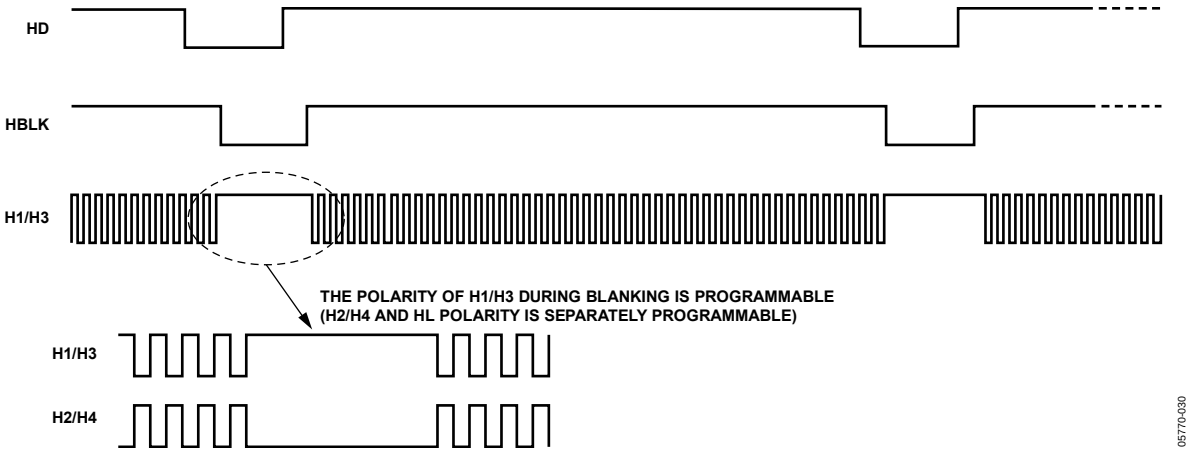


Figure 28. HBLK Masking Control

Individual HBLK Patterns

The HBLK programmable timing shown in Figure 27 is similar to CLPOB and PBLK; however, there is no start polarity control. Only the toggle positions designate the start and the stop positions of the blanking period. Additionally, as shown in Figure 28, there is a polarity control, HBLKMASK, for H1/H3, H2/H4 and HL that designates the polarity of the horizontal clock signals during the blanking period. Setting HBLKMASK high sets H1 = H3 = low, and H2 = H4 = high during the blanking.

As with the CLPOB and PBLK signals, HBLK registers are available in each H-pattern group allowing unique blanking signals to be used with different vertical timing sequences.

The AD9970 supports three different modes for HBLK operation. HBLK Mode 0 supports basic operation and some support for special HBLK patterns. HBLK Mode 1 supports pixel mixing HBLK operation. HBLK Mode 2 supports advanced HBLK operation. The following sections describe each mode. Register parameters are detailed in Table 13.

HBLK Mode 0 Operation

There are six toggle positions available for HBLK. Normally, only two of the toggle positions are used to generate the standard HBLK interval. However, the additional toggle positions can be used to generate special HBLK patterns, as shown in Figure 29. The pattern in this example uses all six toggle positions to generate two extra groups of pulses during the HBLK interval. Different patterns can be created by changing the toggle positions.

Separate toggle positions are available for even and odd lines. If alternation is not needed, load the same values into both the HBLKTOGE and HBLKTOGO registers.

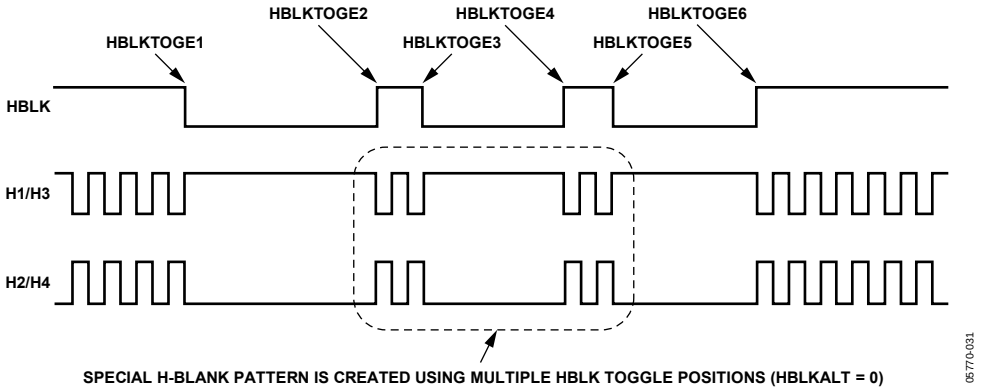


Figure 29. Generating Special HBLK Patterns

Table 13. HBLK Pattern Registers

Register	Length	Range	Description
HBLKMODE	2 bits	0 to 2 HBLK modes	Enables different HBLK toggle position operation. 0: Normal mode. Six toggle positions available for even and odd lines. If even/odd alternation is not needed, set toggles for even/odd the same. 1: Pixel mixing mode. Instead of only six toggle positions, use the HBLKSTART, HBLKEND, HBLKLEN, and HBLKREP registers, along with TOG1 to TOG6. If even/odd alternation is not needed, set toggles for even/odd the same. 2: Advanced HBLK mode. Divides HBLK interval into six different repeat areas Uses HBLKSTARTA, HBLKSTARTB, HBLKSTARTC, and RAxHxREPABC registers. 3: Test mode only. Do not access.
HBLKSTART	13 bits	0 to 8191 pixel location	Start location for HBLK in HBLK Mode 1, Mode 2.
HBLKEND	13 bits	0 to 8191 pixel location	End location for HBLK in HBLK Mode 1, Mode 2.
HBLKLEN	13 bits	0 to 8191 pixels	HBLK length in HBLK Mode 1, Mode 2.
HBLKREP	13 bits	0 to 8191 repetitions	Number of HBLK repetitions in HBLK Mode 1, Mode 2.
HBLKMASK_H1	1 bit	High/low	Masking polarity for H1/H3/H5/H7 during HBLK.
HBLKMASK_H2	1 bit	High/low	Masking polarity for H2/H4/H6/H8 during HBLK.
HBLKMASK_HL	1 bit	High/low	Masking polarity for HL during HBLK.
HBLKTOGO1	13 bits	0 to 8191 pixel location	First HBLK toggle position for odd lines in HBLK Mode 0, Mode 1.
HBLKTOGO2	13 bits	0 to 8191 pixel location	Second HBLK toggle position for odd lines in HBLK Mode 0, Mode 1.
HBLKTOGO3	13 bits	0 to 8191 pixel location	Third HBLK toggle position for odd lines in HBLK Mode 0, Mode 1.
HBLKTOGO4	13 bits	0 to 8191 pixel location	Fourth HBLK toggle position for odd lines in HBLK Mode 0, Mode 1.
HBLKTOGO5	13 bits	0 to 8191 pixel location	Fifth HBLK toggle position for odd lines in HBLK Mode 0, Mode 1.
HBLKTOGO6	13 bits	0 to 8191 pixel location	Sixth HBLK toggle position for odd lines in HBLK Mode 0, Mode 1.
HBLKTOGE1	13 bits	0 to 8191 pixel location	First HBLK toggle position for even lines in HBLK Mode 0, Mode 1.
HBLKTOGE2	13 bits	0 to 8191 pixel location	Second HBLK toggle position for even lines in HBLK Mode 0, Mode 1.
HBLKTOGE3	13 bits	0 to 8191 pixel location	Third HBLK toggle position for even lines in HBLK Mode 0, Mode 1.
HBLKTOGE4	13 bits	0 to 8191 pixel location	Fourth HBLK toggle position for even lines in HBLK Mode 0, Mode 1.
HBLKTOGE5	13 bits	0 to 8191 pixel location	Fifth HBLK toggle position for even lines in HBLK Mode 0, Mode 1.
HBLKTOGE6	13 bits	0 to 8191 pixel location	Sixth HBLK toggle position for even lines in HBLK Mode 0, Mode 1.
RA0H1REPABC	12 bits	0 to 15 HCLK pulses for each A, B, and C	HBLK repeat area 0, number of H1 repetitions for HBLKSTARTA/B/C, for HBLK Mode 2—used for even lines. Odd lines defined using HBLKALT_PAT. [3:0] RA0H1REPA. Number of H1 pulses following HBLKSTARTA. [7:4] RA0H1REPB. Number of H1 pulses following HBLKSTARTB. [11:8] RA0H1REPC. Number of H1 pulses following HBLKSTARTC.

Register	Length	Range	Description
RA1H1REPABC	12 bits	0 to 15 HCLK pulses	HBLK Repeat Area 1. Number of H1 repetitions for HBLKSTARTA/B/C.
RA2H1REPABC	12 bits	0 to 15 HCLK pulses	HBLK Repeat Area 2. Number of H1 repetitions for HBLKSTARTA/B/C.
RA3H1REPABC	12 bits	0 to 15 HCLK pulses	HBLK Repeat Area 3. Number of H1 repetitions for HBLKSTARTA/B/C.
RA4H1REPABC	12 bits	0 to 15 HCLK pulses	HBLK Repeat Area 4. Number of H1 repetitions for HBLKSTARTA/B/C.
RA5H1REPABC	12 bits	0 to 15 HCLK pulses	HBLK Repeat Area 5. Number of H1 repetitions for HBLKSTARTA/B/C.
RA0H2REPABC	12 bits	0 to 15 HCLK pulses for each A, B, and C	HBLK Repeat Area 0. Number of H2 repetitions for HBLKSTARTA/B/C, for HBLK Mode 2—used for even lines. Odd lines defined using HBLKALT_PAT. [3:0] RA0H2REPA. Number of H2 pulses following HBLKSTARTA. [7:4] RA0H2REPB. Number of H2 pulses following HBLKSTARTB. [11:8] RA0H2REPC. Number of H2 pulses following HBLKSTARTC.
RA1H2REPABC	12 bits	0 to 15 HCLK pulses	HBLK Repeat Area 1. Number of H2 repetitions for HBLKSTARTA/B/C.
RA2H2REPABC	12 bits	0 to 15 HCLK pulses	HBLK Repeat Area 2. Number of H2 repetitions for HBLKSTARTA/B/C.
RA3H2REPABC	12 bits	0 to 15 HCLK pulses	HBLK Repeat Area 3. Number of H2 repetitions for HBLKSTARTA/B/C.
RA4H2REPABC	12 bits	0 to 15 HCLK pulses	HBLK Repeat Area 4. Number of H2 repetitions for HBLKSTARTA/B/C.
RA5H2REPABC	12 bits	0 to 15 HCLK pulses	HBLK Repeat Area 5. Number of H2 repetitions for HBLKSTARTA/B/C.
HBLKSTARTA	13 bits	0 to 8191 pixel location	HBLK Repeat Area Start Position A for HBLK Mode 2.
HBLKSTARTB	13 bits	0 to 8191 pixel location	HBLK Repeat Area Start Position B for HBLK Mode 2.
HBLKSTARTC	13 bits	0 to 8191 pixel location	HBLK Repeat Area Start Position C for HBLK Mode 2.
HBLKALT_PAT1	3 bits	0 to 5 even repeat area	HBLK Mode 2. Odd Field Repeat Area 0 pattern, selected from even field repeat areas previously defined.
HBLKALT_PAT2	3 bits	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 1 Pattern.
HBLKALT_PAT3	3 bits	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 2 Pattern.
HBLKALT_PAT4	3 bits	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 3 Pattern.
HBLKALT_PAT5	3 bits	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 4 Pattern.
HBLKALT_PAT6	3 bits	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 5 Pattern.

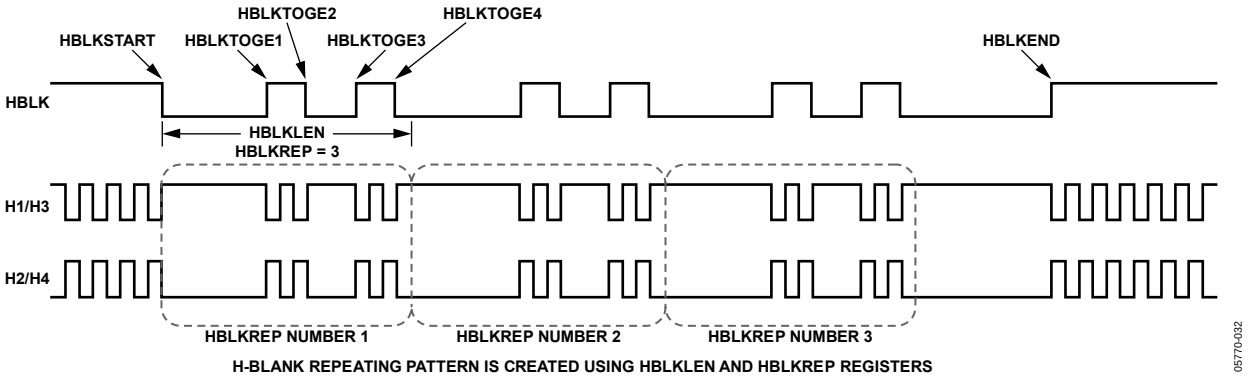


Figure 30. HBLK Repeating Pattern Using HBLKMODE = 1

HBLK Mode 1 Operation

Enable multiple repeats of the HBLK signal by setting HBLKMODE = 1. In this mode, the HBLK pattern is generated using a different set of registers: HBLKSTART, HBLKEND, HBLKLEN, and HBLKREP, along with the six toggle positions (see Figure 30).

Separate toggle positions are available for even and odd lines. If alternation is not needed, load the same values into both the HBLKTOGE and HBLKTOGO registers.

Generating HBLK Line Alternation

HBLK Mode 0 and HBLK Mode 1 provide the ability to alternate different HBLK toggle positions on even and odd lines. Separate toggle positions are available for even and odd lines. If even/odd line alternation is not required, program the same values into the HBLKTOGE and HBLKTOGO registers.

Increasing H-Clock Width During HBLK

HBLK Mode 0 and HBLK Mode 1 allow the H1 to H4 pulse width to be increased during the HBLK interval. As shown in Figure 31, the H-clock frequency can be reduced by a factor of 1/2, 1/4, 1/6, 1/8, 1/10, 1/12, or up to 1/30. To enable this feature, the HCLK_WIDTH register (Address 0x34, Bits[7:4]) is set to a value between 1 and 15. When this register is set to 0, the wide HCLK feature is disabled. The reduced frequency occurs only for H1 to H4 pulses that are located within the HBLK area.

The HCLK_WIDTH feature is generally used in conjunction with special HBLK patterns to generate vertical and horizontal mixing in the CCD.

Note: The wide HCLK feature is available only in HBLK Mode 0 and HBLK Mode 1, and not in HBLK Mode 2.

Table 14. HCLK Width Register

Register	Length	Description
HCLK_WIDTH	4 bits	Controls H1 to H4 width during HBLK as a fraction of pixel rate 0: same frequency as pixel rate 1: 1/2 pixel frequency, that is, doubles the HCLK pulse width 2: 1/4 pixel frequency 3: 1/6 pixel frequency 4: 1/8 pixel frequency 5: 1/10 pixel frequency … 15: 1/30 pixel frequency

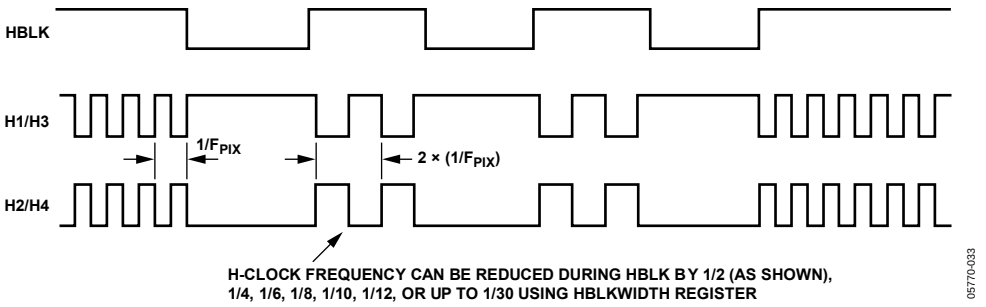


Figure 31. Generating Wide H-Clock Pulses During HBLK Interval

HBLK Mode 2 Operation

HBLK Mode 2 allows more advanced HBLK pattern operation. If unevenly spaced, multiple areas of HCLK pulses are needed, use HBLK Mode 2. Using a separate set of registers, HBLK Mode 2 can divide the HBLK region into up to six different repeat areas (see Table 13). As shown in Figure 33, each repeat area shares a common group of toggle positions: HBLKSTARTA, HBLKSTARTB, and HBLKSTARTC. However, the number of toggles following each STARTA, STARTB, and STARTC position can be unique in each repeat area by using the RAH1REP and RAH2REP registers. As shown in Figure 32, setting the RAH1REPA/RAH1REPB/RAH1REPC or RAH2REPA/RAH2REPB/RAH2REPC registers to 0 masks the HCLK groups from appearing in a particular repeat area. Figure 33 shows only two repeat areas being used, although six are available. It is possible to program a separate number of repeat area repetitions for H1 and H2, but generally, the same value is used for both H1 and H2.

Figure 33 shows the example

RA0H1REPA/RA0H1REPB/ RA0H1REPC =
RA0H2REPA/RA0H2REPB/RA0H2REPC =
RA1H1REPA/RA1H1REPB/RA1H1REPC =
RA1H2REPA/ RA1H2REPB/RA1H2REPC = 2

Furthermore, HBLK Mode 2 allows a different HBLK pattern on even and odd lines. The HBLKSTARTA, HBLKSTARTB, and HBLKSTARTC registers, as well as the RAH1REPA/RAH1REPB/RAH1REPC and RAH2REPA/RAH2REPB/RAH2REPC registers, define operation for the even lines. For separate control of the odd lines, the HBLKALT_PAT registers specify up to six repeat areas on the odd lines by reordering the repeat areas used for the even lines. New patterns are not available, but the order of the previously defined repeat areas on the even lines can be changed for the odd lines to accommodate advanced CCD operation.

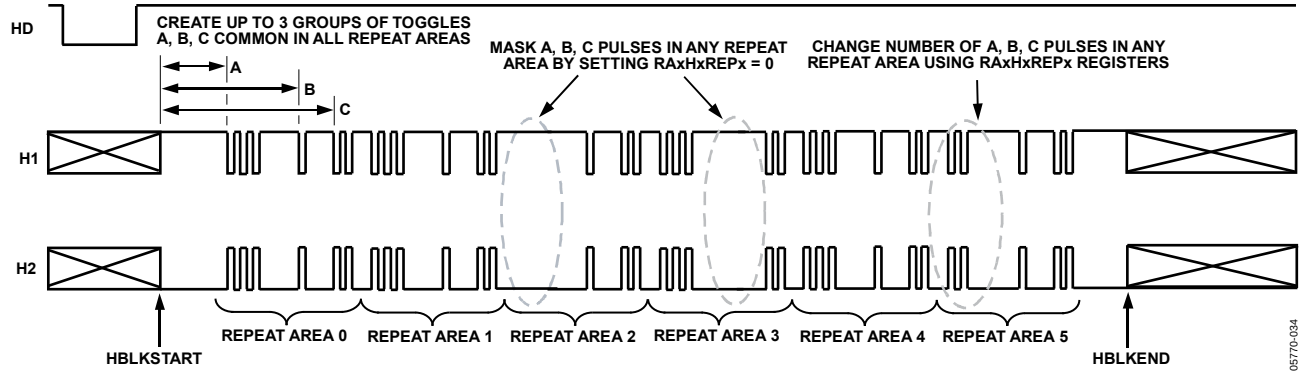


Figure 32. HBLK Mode 2 Operation

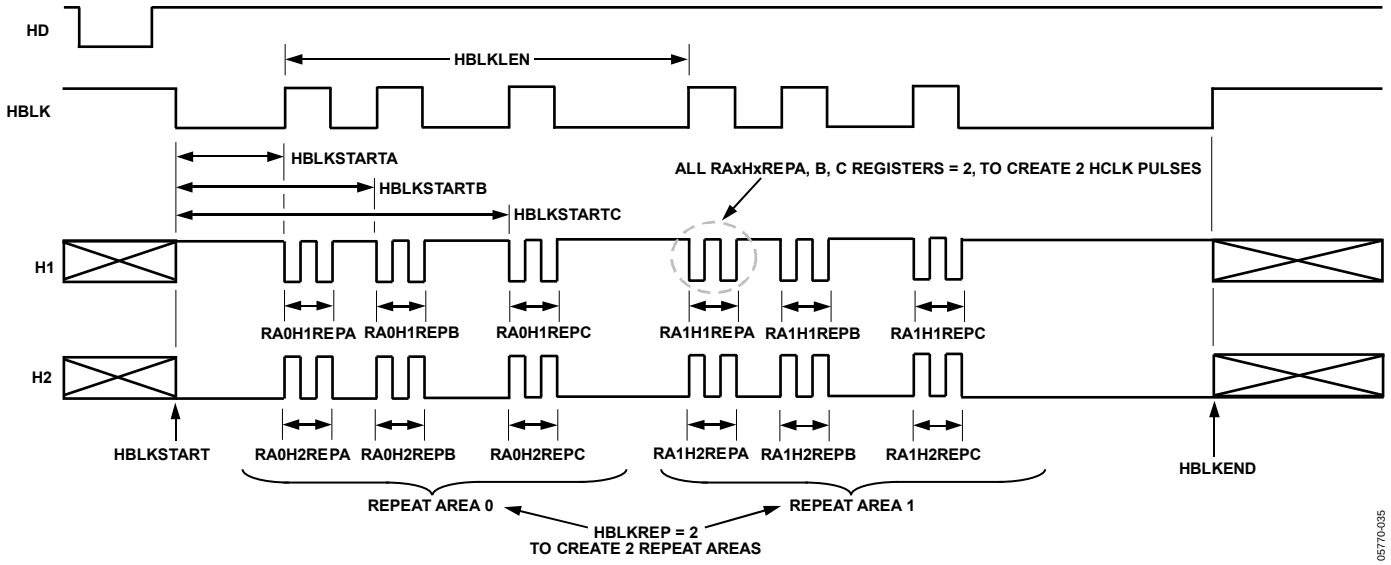


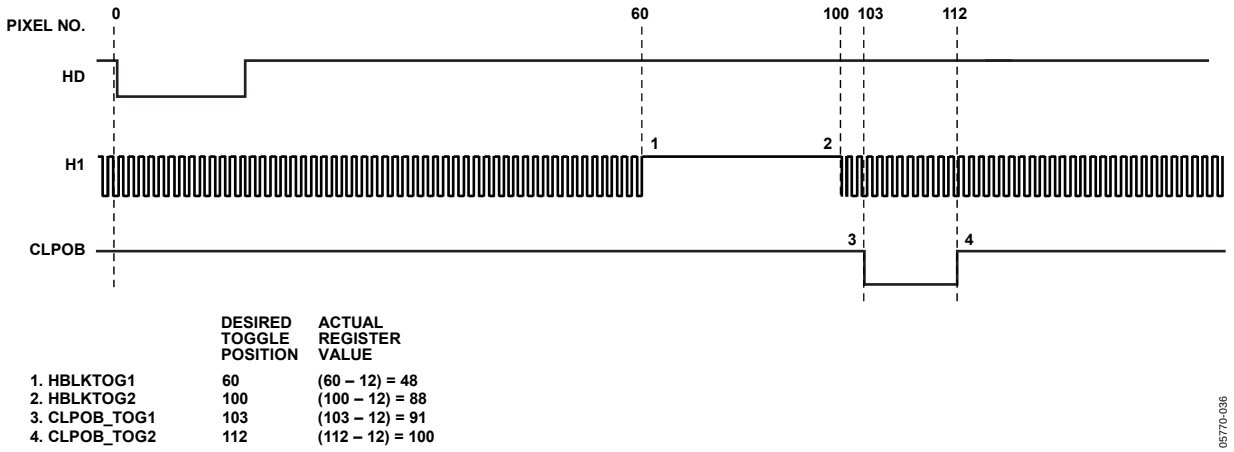
Figure 33. HBLK Mode 2 Registers

HBLK, PBLK and CLPOB Toggle Positions

The AD9970 uses an internal horizontal pixel counter to position the HBLK, PBLK, and CLPOB toggle positions. Ideally, this counter resets to zero on the falling edge of HD. The actual operation contains an internal pipeline delay associated with the counter. The horizontal counter does not reset to zero until 12 CLI periods after the falling edge of HD. This 12-cycle pipeline delay has to be considered when determining the register toggle positions. For example, if CLPOB_TOG1 = 100 and the pipeline delay is not considered, the final toggle position is applied at 112. To obtain the correct toggle positions, the toggle position registers have to be set to the desired toggle position minus 12. For example, if the desired toggle position is 100, CLPOBTOG should be set to (100 – 12) = 88. Figure 61 shows the 12-cycle pipeline delay referenced to the falling edge of HD. Figure 34 compares the toggle position values for desired and actual toggle positions.

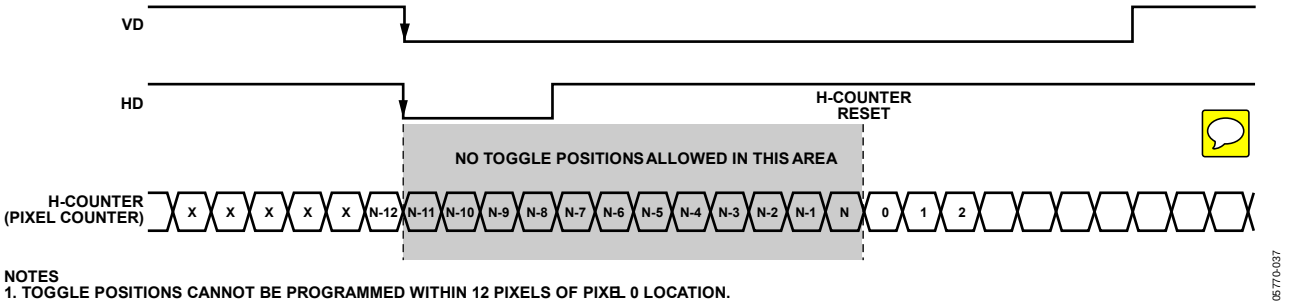
CAUTION

Toggle positions cannot be programmed during the 12-cycle delay from the HD falling edge until the H-counter has reset. See Figure 35 for an example of this restriction.



	DESIRED TOGGLE POSITION	ACTUAL REGISTER VALUE
1. HBLKTOG1	60	(60 – 12) = 48
2. HBLKTOG2	100	(100 – 12) = 88
3. CLPOB_TOG1	103	(103 – 12) = 91
4. CLPOB_TOG2	112	(112 – 12) = 100

Figure 34. Example of Actual Register Settings to Obtain Desired Toggle Positions



NOTES
1. TOGGLE POSITIONS CANNOT BE PROGRAMMED WITHIN 12 PIXELS OF PIXEL 0 LOCATION.

Figure 35. Restriction for Toggle Position Placement

COMPLETE FIELD—COMBINING H-PATTERNS

Once created, the H-patterns are combined to create different readout fields. A field consists of up to nine different regions determined by the SCP registers, and within each region, a different H-pattern group can be selected up to a maximum of 31 groups. Registers to control the H-patterns are located in the field registers.

Table 32 describes the field registers.

H-Pattern Selection

The H-patterns are summarized in Table 15 and are stored in the HPAT memory as described in Table 32. The user decides how many H-pattern groups are required up to a maximum of 31, and then uses the HPAT_SEL registers to select which H-pattern group is output in each region of the field. Figure 36 shows how to use the HPAT_SEL and SCP registers. The SCP registers create the line boundaries for each region.

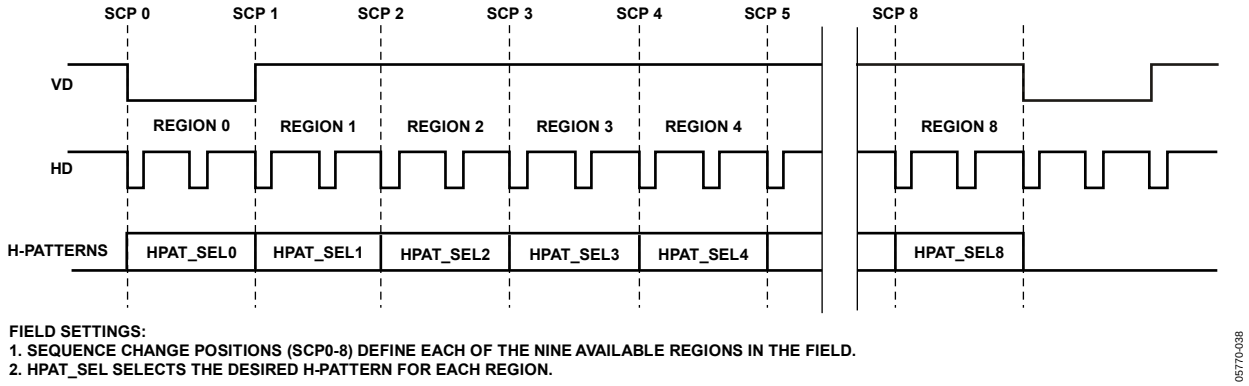


Figure 36. Complete Field Divided into Regions

Table 15. Field Registers

Register	Length	Range	Description
SCP	13 bits	0 to 8191 line number	Sequence change position for each region; selects an individual line.
HPAT_SEL	5 bits	0 to 31 H-patterns	Selected H-pattern for each region of the field.
CLPOB_POL	9 bits	High/low	CLPOB start polarity settings for each region of the field.
CLPOB_PAT	9 bits	0 to 9 patterns	CLPOB pattern selector for each region of the field.
CLPOBMASK	13 bits	Number of lines	CLPOB mask positions for up to three masking configurations.
PBLK_POL	9 bits	High/low	PBLK start polarity settings for each region of the field.
PBLK_PAT	9 bits	0 to 9 patterns	PBLK pattern selector for each region of the field.
PBLKMASK	13 bits	Number of lines	PBLK mask positions for up to three masking configurations.

MODE REGISTERS

The mode register contains registers to select the final field timing of the AD9970. Typically, all of the field and H-pattern group information is programmed into the AD9970 at startup. During operation, the mode register allows the user to select any combination of field timing to meet the current requirements of the system.

The advantage of using the mode register in conjunction with preprogrammed timing is that it greatly reduces the system programming requirements during camera operation. Only a few register writes are required when the camera operating mode is changed, rather than having to write in all of the vertical timing information with each camera mode change.

A basic still camera application can require five different fields of horizontal timing: one for draft mode operation, one for autofocusing, and three for still image readout. With the AD9970, all of the register timing information for the five fields load at startup. Then, during camera operation, the mode register selects which field timing to activate depending on how the camera is being used.

The AD9970 supports up to seven field sequences selected from up to 31 preprogrammed field groups using the FIELD_SEL registers. When FIELDNUM is greater than 1, the AD9970 starts with Field 1 and increments to each Field N at the start of each VD.

Figure 37 provides examples of mode register configuration settings. This example assumes four field groups, Field Group 0 to Field Group 3, are stored in memory.

Table 16. Mode Registers

Register	Length	Range	Description
HPATNUM	5 bits	0 to 31 H-pattern groups	Total number of H-pattern groups starting at Address 0x800
FIELDNUM	3 bits	0 to 7 fields	Total number of applied fields (set = 1 for single field operation)
FIELD_SEL1	5 bits	0 to 31 field groups	Selected 1st field
FIELD_SEL2	5 bits	0 to 31 field groups	Selected 2nd field
FIELD_SEL3	5 bits	0 to 31 field groups	Selected 3rd field
FIELD_SEL4	5 bits	0 to 31 field groups	Selected 4th field
FIELD_SEL5	5 bits	0 to 31 field groups	Selected 5th field
FIELD_SEL6	5 bits	0 to 31 field groups	Selected 6th field
FIELD_SEL7	5 bits	0 to 31 field groups	Selected 7th field

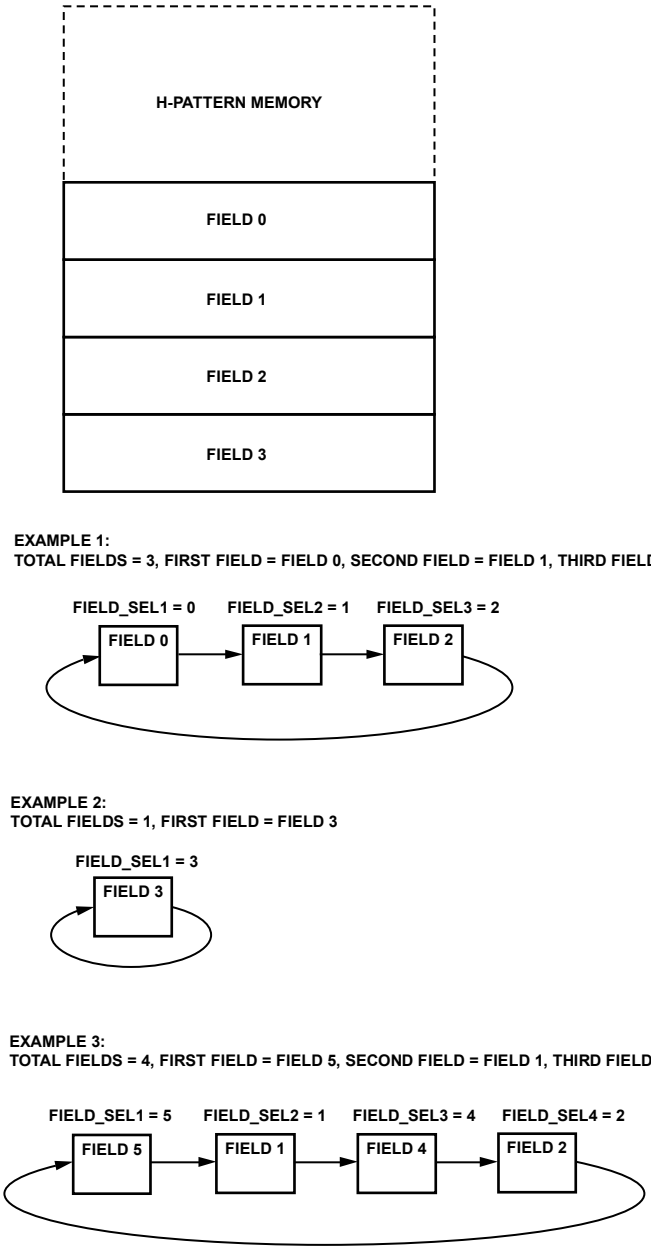


Figure 37. Example of Mode Register Configurations

HORIZONTAL TIMING SEQUENCE EXAMPLE

Figure 38 shows an example of a CCD layout. The horizontal register contains 28 dummy pixels that occur on each line clocked from the CCD. In the vertical direction, there are 10 optical black (OB) lines at the front of the readout and two at the back of the readout. The horizontal direction has four OB pixels in the front and 48 in the back.

Figure 39 shows the basic sequence layout to use during the effective pixel readout. The 48 OB pixels at the end of each line are used for the CLPOB signals. PBLK is optional and is often used to blank the digital outputs during the HBLK time. HBLK is used during the vertical shift interval.

Because PBLK is used to isolate the CDS input (see the Analog Front End Description and Operation section), do not use the PBLK signal during CLPOB operation. The change in the offset behavior that occurs during PBLK impacts the accuracy of the CLPOB circuitry.

The HBLK, CLPOB, and PBLK parameters are programmed in the V-sequence registers. More elaborate clamping schemes can be used, such as adding in a separate sequence to clamp in the entire shielded OB lines. This requires configuring a separate H-Pattern for clocking out the OB lines.

The CLPOBMASK registers are also useful for disabling the CLPOB on a few lines without affecting the setup of the clamping sequences. It is important to use CLPOB only during valid OB pixels. During other portions on the frame timing, such as vertical blanking or SG line timing, the CCD does not output valid OB pixels. Any CLPOB pulses occurring during this time cause errors in the clamping operation and, therefore, cause changes in the black level of the image.

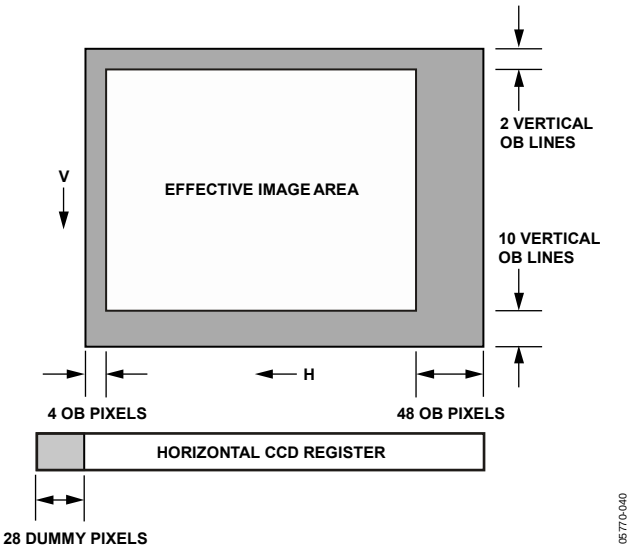


Figure 38. CCD Configuration Example

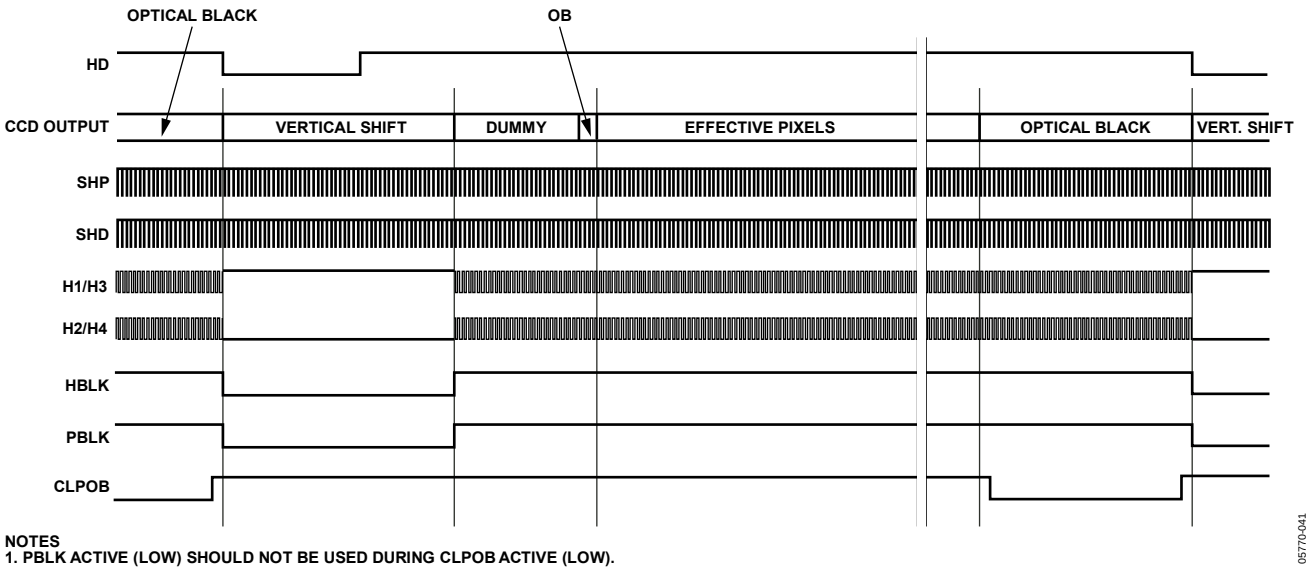


Figure 39. Horizontal Sequence Example

LVDS SERIAL DATA INTERFACE

As digital imaging products such as digital still cameras, camcorders, and scanners have become more prevalent in the market, designers of these systems have driven the demand for both higher speed and higher resolution analog front ends (AFE) in the ongoing pursuit for better image quality.

The AFE (which includes the analog-to-digital converter) needs to be able to drive receiving logic and the accompanying PCB trace capacitance. The combination of the increase in data lines and of higher speed signals presents the system designer with issues in EMI emissions, larger board area (due to the increase in data lines), higher power, and more current transients. This last issue can create kickback noise, a phenomenon wherein transients created by driving the load are coupled back to the ADC analog front end, manifesting in the image as noise or distortion. The previously listed issues present a daunting challenge to users attempting to develop a high performance imaging application.

A configurable low voltage differential signaling (LVDS) serial data interface offers another approach to provide high speed data outputs while minimizing performance limitations in AFE applications. LVDS, as the name implies, is a differential signaling scheme using a low voltage swing.

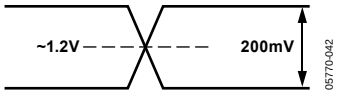


Figure 40. LVDS Output Levels

The LVDS offers the following advantages over the conventional parallel interface:

- Reduced kickback noise: LVDS outputs are current output stages requiring a 100 Ω terminating resistor at the receiver, differing from CMOS outputs that generally do not require termination (see Figure 41).

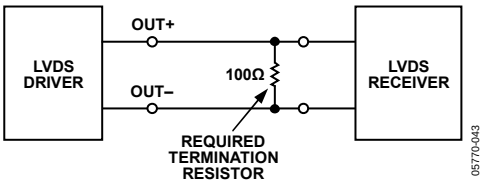


Figure 41. LVDS Requires Far End Termination

  To avoid current spikes on the supply that can couple to the sensitive analog front end (resulting in kickback noise), the current output results in a fixed dc load current on the output supplies.

- Fewer data lines: With a serial data output, the number of data lines is reduced significantly. This is important in applications that require multiple channels, such as higher speed imaging applications needing a small form factor. LVDS serial data outputs dramatically reduce kickback noise due to the limited number of data output switching compared to a 14-bit or 16-bit parallel output bus switching simultaneously.
- Reduced EMI emissions: Because two balanced signals of the same magnitude transmit through the line in opposite directions, the electromagnetic field from each signal is radiated in the opposing direction, effectively canceling each other's EMI emissions. This reduces shielding, lowering overall system cost. It also reduces RF interference critical in wireless enabled systems.

In addition to the inherent benefits of LVDS, a configurable transmitter enables the AFE to support a wide variety of different LSI receivers, enabling the system designer to implement a receiver that optimizes system performance. The configurable LVDS transmitter enables the user to adjust the following parameters:

- Number of output ports to accommodate higher speed outputs. This allows the designer to use the same device to upgrade the system for higher speed applications.
- Configurable current values to adjust for varying capacitive loads.
- Test pattern generation for simpler verification of functionality.
- Phase delay and trigger adjustment for better synchronization.
- Control word configuration to accommodate varying system protocols for data synchronization.
- Configurable data formatting with single and double data port options.

For LVDS layout recommendations, see the LVDS PCB Design Considerations section.

LVDS SERIAL DATA LINK OPERATION

The LVDS registers for serial register programming are described in Table 17. The configuration of these registers determines the LVDS configuration and operation mode. The serial data link output consists of three pairs of differential output signals, as shown in Figure 42. The DOUT0 and DOUT1 are each 8-bit or 16-bit data outputs that can be configured to operate in different modes by using the TX_CTRL register. The TCLK is the data transmit clock corresponding to valid output data on both rising and falling edges.

Note: Although the DOUT0 and DOUT1 data outputs can be 16 bits in length for single data port mode, the ADC output data is only 14 bits. The two LSBs of the 16-bit output are always set to zero.

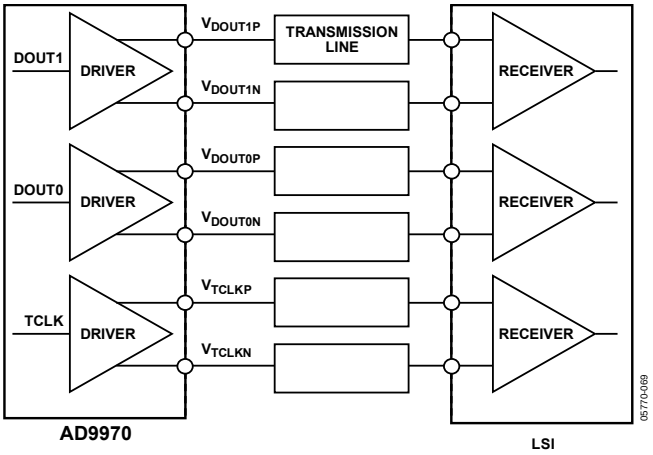


Figure 42. LVDS Serial Data Output

Table 17. LVDS Registers

Register	Length	Range	Description
TCLK_PDN	1 bit	High/low	TCLK output enable 0 = normal operation 1 = power down
DOUT0_PDN	1 bit	High/low	DOUT0 output enable 0 = normal operation 1 = power down
DOUT1_PDN	1 bit	High/low	DOUT1 output enable 0 = normal operation 1 = power down
TX_CTRL	2 bits	4 settings	Serial data transmit control 00 = single port mode with data on DOUT0 10 = single port mode with data on DOUT1 01 = double port mode with low byte on DOUT0 and high byte on DOUT1 11 = double port mode with low byte on DOUT1 and high byte on DOUT0
TCLK_DELAY	4 bits	0 to15 settings	TCLK rising edge delay 0 = default with no delay 1 LSB = 1/16 cycle of internal TCLK when operating in double port mode 1 LSB = 1/8 cycle of internal TCLK when operating in single port mode
LVDS_LSB_ALIGN	1 bit	High/low	LVDS LSB align control 0 = MSB first 1 = LSB first
CLIP_ZS	1 bit	High/low	Data clip operation for ADC zero-scale output data 0 = clip disabled, ADC zero scale = 0x0000 1 = clip function enabled, ADC zero scale = 0x0001
CLIP_FS	1 bit	High/low	Data clip operation for ADC full-scale output data 0 = clip disabled, ADC full scale = 0x3FFF 1 = clip function enabled, ADC full scale = 0x3FFE
LVDS_TEST_EN	2 bits	0 to 3 settings	LVDS data input test enable 0 = disable 1 = enable
LVDS_PATTERN	16 bits		Pattern of the TCLK signal when the TCLK pattern mode is enabled
TCLK_PAT_MODE	1 bit	High/low	0 = disable TCLK pattern mode 1 = enable TCLK pattern mode
LVDS_PATTERN_EN	1 bit	High/low	0 = disable LVDS test pattern 1 = enable LVDS test pattern

CONFIGURABLE DATA FORMATTING

The serial data outs can be configured to operate in single data port or double data port modes to support different LSI receiver capabilities. In both single and double data port modes, double data rate is used with respect to TCLK rising and falling timing.

Note: Although the DOUT0 and DOUT1 data outputs can be 16 bits in length for single data port mode, the ADC output data is only 14 bits. The two LSBs of the 16-bit output are always set to zero.

Single Data Port Mode

Single data port operation outputs the entire 16-bit word on only one data port. The DOUT0 or DOUT1 data port is selected to output the data by using the TX_CTRL register.

During single data port operation, the TCLK runs at the maximum allowable data rate of 260 MHz resulting in the TCLK frequency being eight times the CLI input pixel clock (see Figure 43). This implies that a maximum 32.5 MHz CLI clock frequency can be supported while operating in this mode.

260 MHz/8 = 32.5 MHz

Double Data Port Mode

Double data port operation uses both DOUT0 and DOUT1 to output the 16-bit word at double the single port data rate. Apply the upper and lower bytes to either port using the TX_CTRL register. During double port operation, the TCLK runs at only four times the CLI input pixel clock as shown in Figure 44. Because the maximum allowable data rate is 260 MHz, the double port operation allows for faster AFE operation of up to 65 MHz (260 MHz/4).

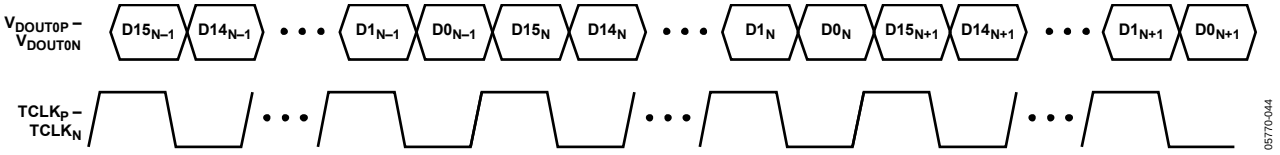


Figure 43. Data and Clock Format for Single Data Port Operation (Using DOUT0, MSB First)

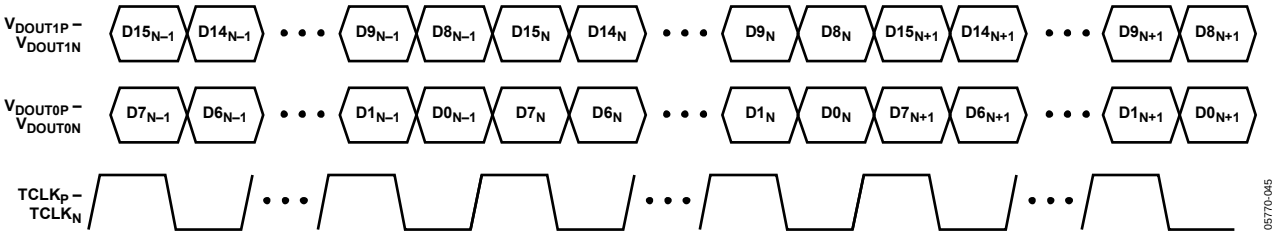


Figure 44. Data and Clock Format for Double Data Port Operation (Using Upper Byte on DOUT1, MSB First)

PROGRAMMABLE DATA DELAY

The AD9970 also provides programmable delay for the serial data outputs allowing fine adjustment with the LVDS receiver. Two levels of programmability are provided: one at the pixel clock rate (DOUTPHASE), and one at the serial data clock rate (TCLK).

TCLK Delay Adjustment

Additional features provide the ability to delay the TCLK phase relative to the starting location of each data bit by using the TCLK_DELAY register. This feature optimally positions the rising edge of TCLK to the center of the data bit at the receiver input as shown in Figure 47. The TCLK adjustment range differs between the single data port and double data port modes as illustrated in Figure 45 and Figure 46. As shown, there are eight adjustment range positions for the single port mode and 16 adjustment range positions during operation in the double port mode.

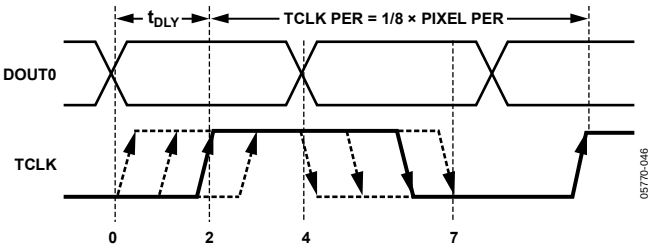


Figure 45. TCLK Delay for Single Data Port Mode

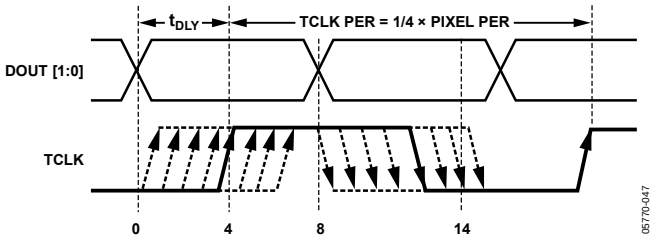


Figure 46. TCLK Delay for Double Data Port Mode

DOUTPHASE Control

Use the DOUTPHASEP register to skew the TCLK and DOUT phases with respect to the rising edge of the CLI master clock. The value of the DOUTPHASEN register is dependent on the DOUTPHASEP value. DOUTPHASEN must always be set as follows: DOUTPHASEN = DOUTPHASEP + 0x20. This maintains a 50% internal DOUTPHASE clock. Figure 48 shows the internal DOUTPHASE clock with respect to CLI and the DOUTPHASEP register setting.

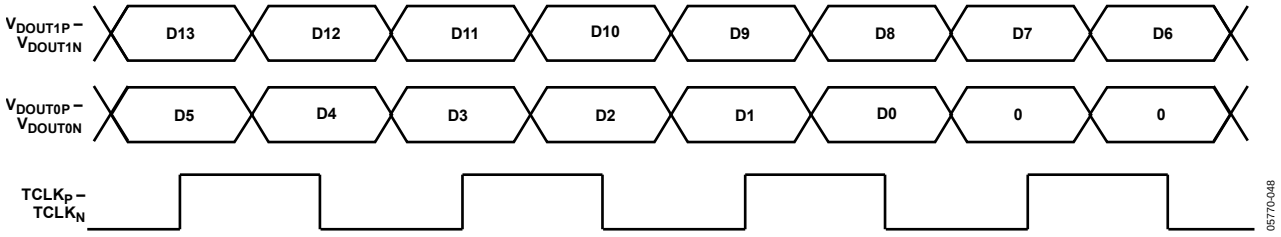


Figure 47. Ideal TCLK Phase Location Centered (TCLK Delay = 4)

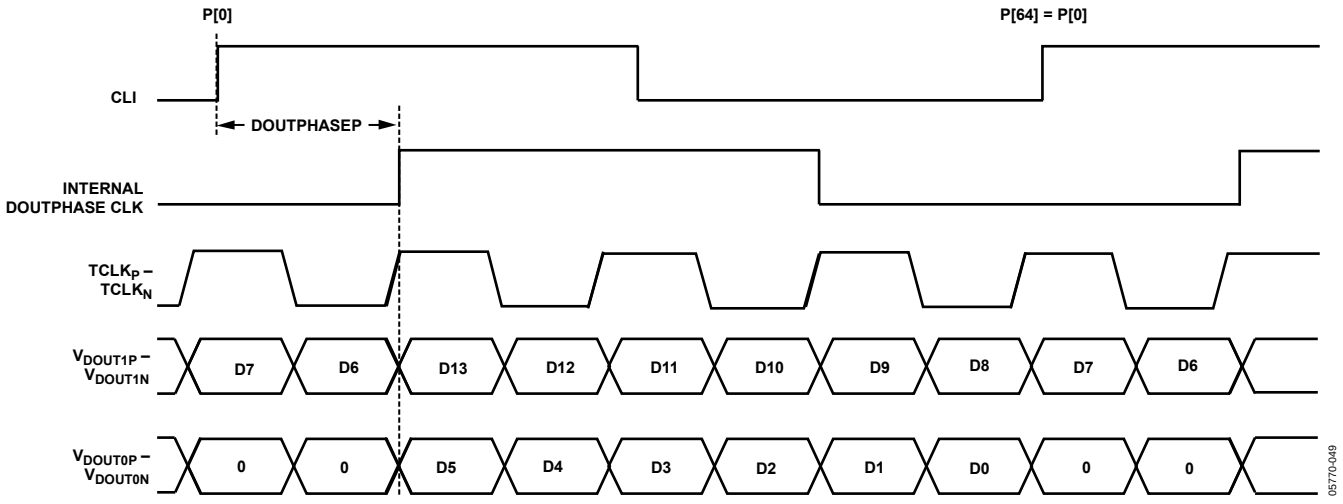


Figure 48. DOUTPHASEP Operation (TCLK Delay = 0 is shown)

TCLK Pattern

By enabling the LVDS_PATTERN_EN register, it is possible to generate a unique TCLK pattern. When the LVDS_PATTERN_EN register is enabled, each of the LVDS_PATTERN register bits [15:0] determine the polarity of 1/16th of one CLI period respectively, MSB first.

For example, to generate a TCLK pattern with the same period as the CLI, the LVDS_PATTERN is set to 0xFF00 as shown in Figure 49. In the dual port mode, eight MSBs of the LVDS_PATTERN register are used to output a desired TCLK pattern as shown in Figure 50. The eight LSBs are ignored.

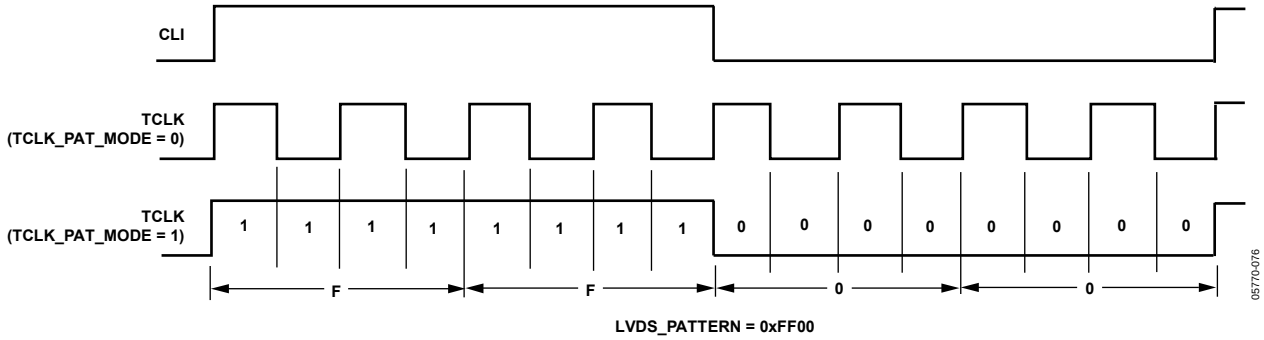


Figure 49. Using TCLK Pattern Function to Create Frame Clock Signal, in Single Port Mode

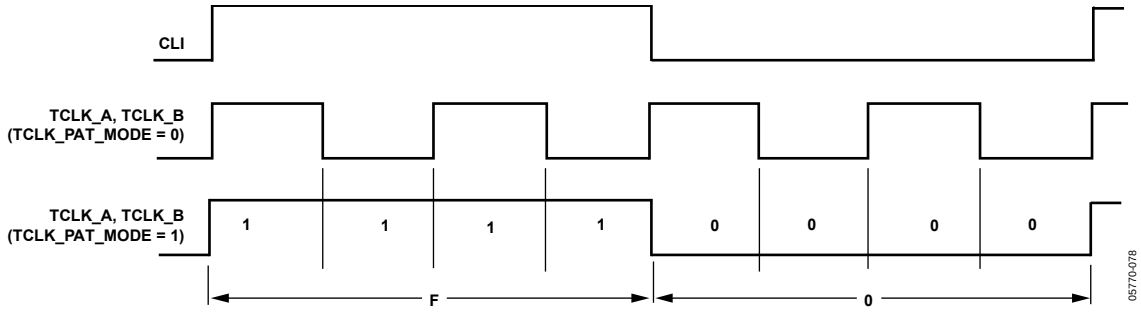


Figure 50. Using TCLK Pattern Function to Create Frame Clock Signal, in Double Port Mode

LVDS Test Pattern Insertion

A special test pattern insertion feature can be enabled to output a 16-bit data-word programmed in the LVDS_PATTERN register. The 16-bit pattern programmed in this register is output by setting the LVDS_PATTERN_EN register = 1. Use this feature to assist with the initial LVDS serial interface system development. Figure 51 shows the mux operation that enables the test pattern mode.

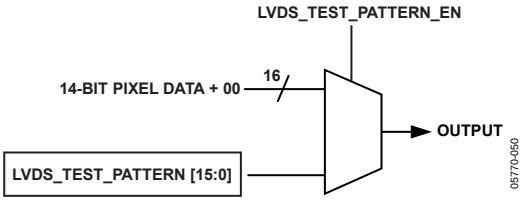


Figure 51. LVDS Test Pattern Mux Control

CONFIGURABLE SERIAL DATA SYNCHRONIZATION PROTOCOLS

Configurable synchronization programmability is provided while operating in single data port and double data port modes. The host processor uses these synchronization features to automatically track pixel data with respect to the start of each field and line position. Table 18 describes the synchronization registers.

Up to seven configurable synchronization words followed by one configurable control word are supported, as shown in Figure 52. The multiple preprogrammed synchronization words are available to eliminate the risk of synchronization errors between the LVDS serializer and the receiver. The synchronization and control words always replace the preceding pixel data.

Table 18. Synchronization Registers

Register	Length	Range	Description
SYNCWORDNUM	3 bits	0 to 7 sync words	Total number of synchronization words.
CONTROLWORD_EN	1 bit	High/low	Control word enable.
SYNC_WORD0	16 bits	0 to 15 sync word bits	Synchronization Word 0 data bits.
SYNC_WORD1	16 bits	0 to 15 sync word bits	Synchronization Word 1 data bits.
SYNC_WORD2	16 bits	0 to 15 sync word bits	Synchronization Word 2 data bits.
SYNC_WORD3	16 bits	0 to 15 sync word bits	Synchronization Word 3 data bits.
SYNC_WORD4	16 bits	0 to 15 sync word bits	Synchronization Word 4 data bits.
SYNC_WORD5	16 bits	0 to 15 sync word bits	Synchronization Word 5 data bits.
SYNC_WORD6	16 bits	0 to 15 sync word bits	Synchronization Word 6 data bits.
SYNC_RISING_EN	8 bits	0 to 7 control word bits	Rising edge synchronization enable.
SYNC_FALLING_EN	8 bits	0 to 7 control word bits	Falling edge synchronization enable.
SYNC_START_LOC	13 bits	0 to 8192 count	Synchronization sequence starting pixel count location.
SYNC_ALIGN_LOC	1 bit	High/low	Synchronization word location.
SYNC_CW_EN	1 bit	High/low	Automatic synchronization and control word enable.
CWB0	4 bits	0 to 15 settings	Control Word Bit 0 Select. Supports seven unique settings (see Table 19).
CWB1	4 bits	0 to 15 settings	Control Word Bit 1 Select. Supports seven unique settings (see Table 19).
CWB2	4 bits	0 to 15 settings	Control Word Bit 2 Select. Supports seven unique settings (see Table 19).
CWB3	4 bits	0 to 15 settings	Control Word Bit 3 Select. Supports seven unique settings (see Table 19).
CWB4	4 bits	0 to 15 settings	Control Word Bit 4 Select. Supports seven unique settings (see Table 19).
CWB5	4 bits	0 to 15 settings	Control Word Bit 5 Select. Supports seven unique settings (see Table 19).
CWB6	4 bits	0 to 15 settings	Control Word Bit 6 Select. Supports seven unique settings (see Table 19).
CWB7	4 bits	0 to 15 settings	Control Word Bit 7 Select. Supports seven unique settings (see Table 19).

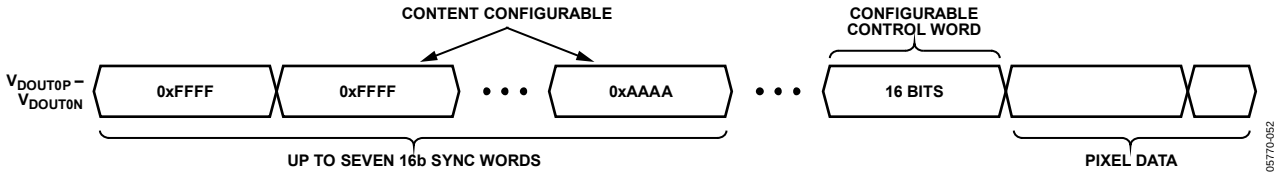


Figure 52. Synchronization and Control Word Output Format

Configurable Control Word

One configurable control word is supported and preprogrammed using the CWB registers. Although the control word is 16 bits, only the lower byte of the control word is configurable. Figure 54 and Figure 53 show the control word configuration for single and double data port operation, respectively. As shown, the upper byte of the control word is always the inverse of the lower byte.

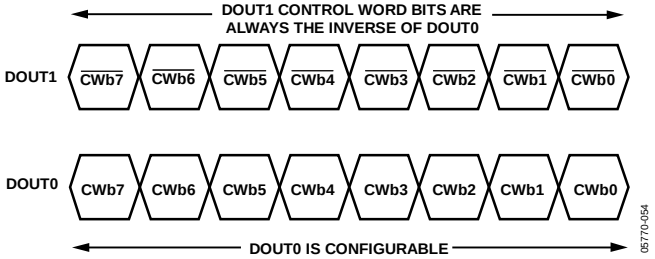


Figure 53. Control Word Configuration for Double Data Port Mode

Triggered Synchronization

A synchronization sequence can be initiated two ways. A triggered synchronization event is initiated by an internal signal transition. The setting programmed for the control word determines the internal signals that trigger a sync sequence.

The synchronization is triggered on either the rising or falling edge of the control word setting by using the SYNC_RISING_EN and SYNC_FALLING_EN registers. Figure 55 shows an example of triggering the synchronization sequence on three occasions. In this example, the sync sequence is triggered at the start of FD0 (1st field), on the rising edge of HD, and also at the end of FD2 (3rd field).

Automatic Synchronization

An automatic synchronization event is initiated at the start of each line. The synchronization sequence can be delayed by a certain number of pixels by using the SYNC_START_LOC register. Additionally, the SYNC_ALIGN_LOC register either starts or ends the synchronization sequence determined by the SYNC_START_LOC setting. Figure 56 and Figure 57 show two examples of using these registers to delay the synchronization sequences after being enabled by the start of the line.

Table 19. CWBx Register Setting vs. Control Word Data for Lower Control Word Byte

CWBx[3:0] Register Setting	1111	1110	1101	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
Control Word Data for Lower Control Word Byte	0	0	0	0	0	0	NA[1]	NA[1]	FD2[2]	FD1[2]	FD0[2]	VD	HD	0	1	0

[1] NA = not available (CWBx values 1001 and 1000 are invalid).
[2] FD0, FD1, and FD2 represent the internal field counter. The CWBx settings can be applied to track the field number. For example, setting register CWB3 = 0110 sets CWB3 of the control word when the second field is active.

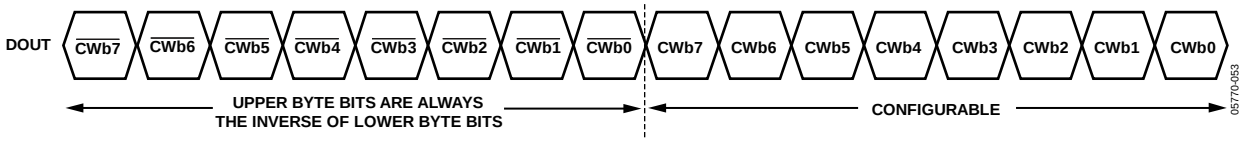


Figure 54. Control Word Configuration for Single Data Port Mode

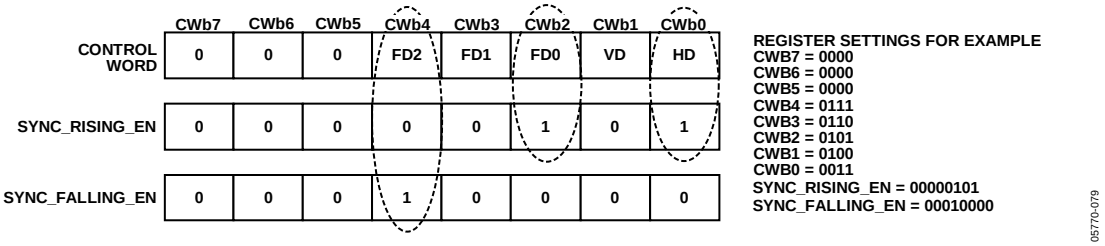


Figure 55. Example of Configuring the Synchronization Register

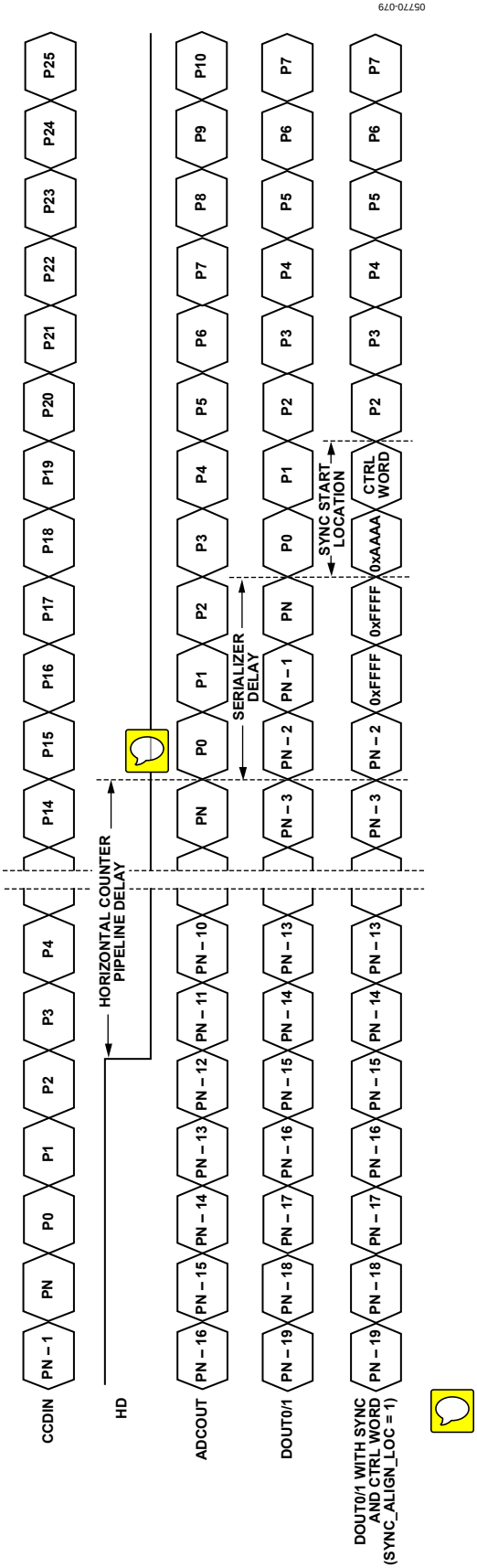


Figure 56. Example of Automatic Synchronization with SYNC_START_LOC =2 and SYNC_ALIGN_LOC =1

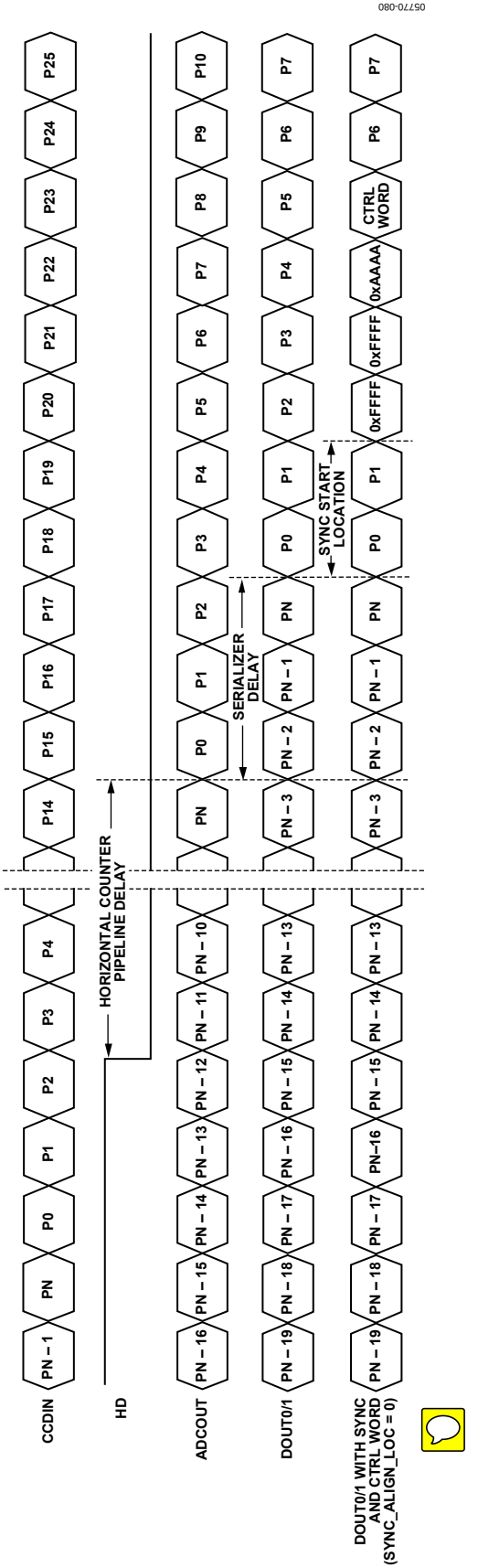


Figure 57. Example of Automatic Synchronization with SYNC_START_LOC = 2 and SYNC_ALIGN_LOC = 0

ANALOG FRONT END DESCRIPTION AND OPERATION

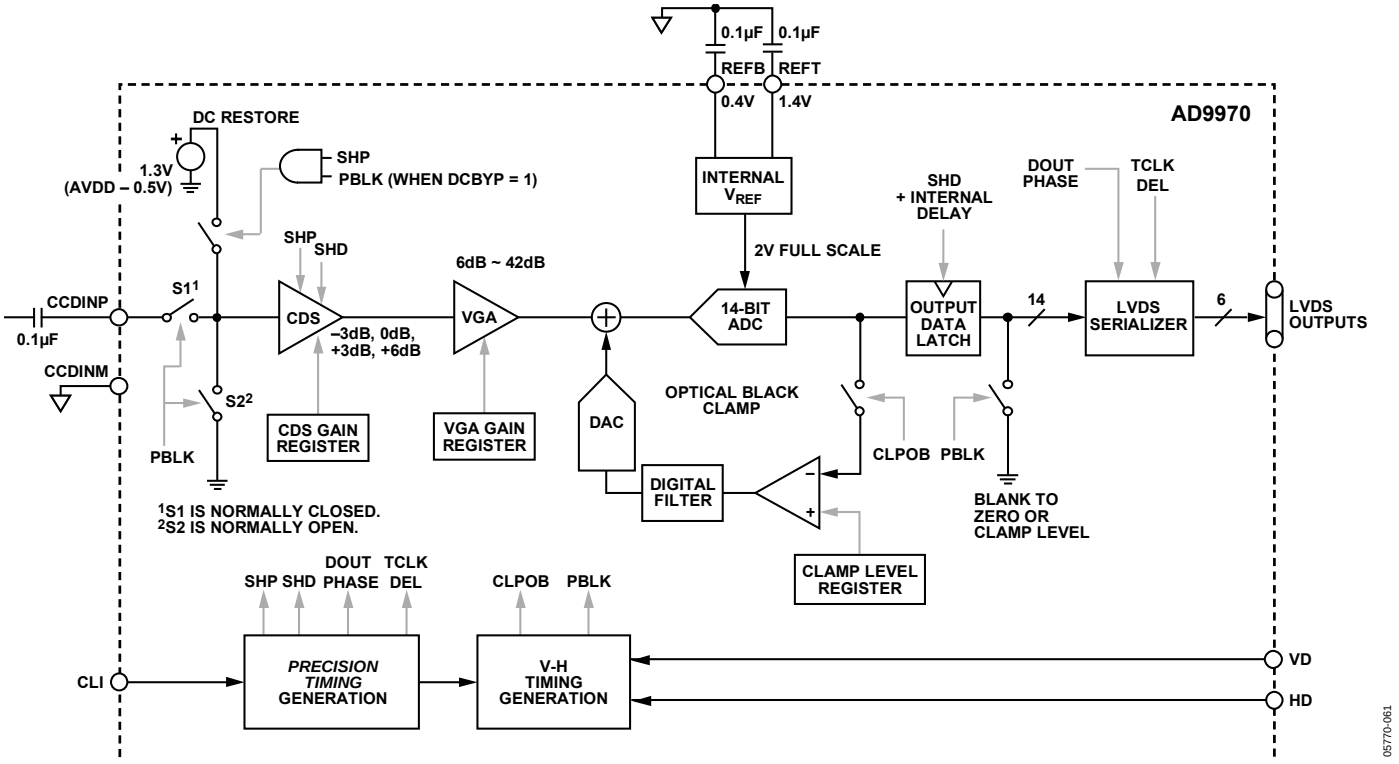


Figure 58. Analog Front End Functional Block Diagram

The AD9970 signal processing chain is shown in Figure 58. Each processing step is essential in achieving a high quality image from the raw CCD pixel data.

DC Restore

To reduce the large dc offset of the CCD output signal, a dc restore circuit is used with an external 0.1 µF series coupling capacitor. This restores the dc level of the CCD signal to approximately 1.3 V (AVDD-0.5V) to be compatible with the 1.8 V core supply voltage of the AD9970. The dc restore switch is active during the SHP sample pulse time.

The dc restore circuit can be disabled when the optional PBLK signal is used to isolate large signal swings from the CCD input (see the Analog Preblanking section). Bit 6 of Address 0x00 controls whether the dc restore is active during the PBLK interval.

Analog Preblanking

During certain CCD blanking or substrate clocking intervals, the CCD input signal to the AD9970 can increase in amplitude beyond the recommended input range. Use the PBLK signal to isolate the CDS input from large signal swings. As shown in Figure 58, when PBLK is active (low), the CDS input is isolated from the CCDIN pin (S1 open) and is internally shorted to ground (S2 closed).

During the PBLK active time, the ADC outputs can be programmed to output all zeros or the programmed clamp level.

Note that because the CDS input is shorted during PBLK, do not use the CLPOB pulse during the same active time as the PBLK pulse.

Correlated Double Sampler (CDS)

The CDS circuit samples each CCD pixel twice to extract the video information and to reject low frequency noise. The timing shown in Figure 23 illustrates how the two internally generated CDS clocks, SHP and SHD, are used to sample the reference level and data level of the CCD signal, respectively. The placement of the SHP and SHD sampling edges is determined by the setting of the SHPLOC and SHDLOC registers located at Address 0x36. Placement of these two clock signals is critical in achieving the best performance from the CCD.

The CDS gain is variable in four steps by using the AFE Address 0x04: –3 dB, 0 dB (default), +3 dB, and +6 dB. Improved noise performance results from using the +3 dB and +6 dB settings, but the input range is reduced (see Table 3).

Variable Gain Amplifier

The VGA stage provides a gain range of approximately 6 dB to 42 dB, programmable with 10-bit resolution through the serial digital interface. A gain of 6 dB is needed to match a 1 V input signal with the ADC full-scale range of 2 V. When compared to 1 V full-scale systems, the equivalent gain range is 0 dB to 36 dB.

The VGA gain curve follows a linear-in-dB characteristic. The exact VGA gain is calculated for any gain register value by

$$Gain\ (\text{dB}) = (0.0359 \times Code) + 5.1\ \text{dB}$$

where *Code* is the range of 0 to 1023.

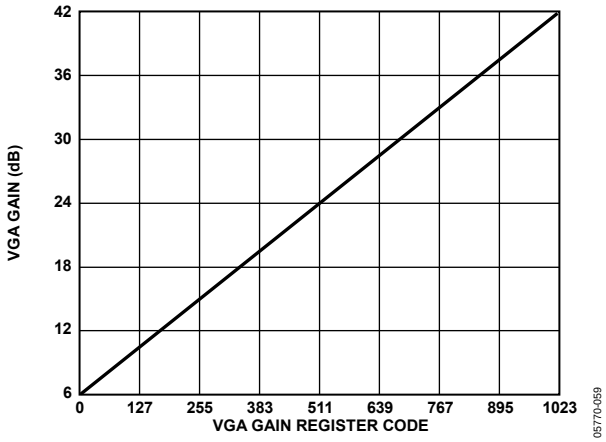


Figure 59. VGA Gain Curve

ADC Architecture

The AD9970 uses high performance ADC architecture optimized for high speed and low power. Differential nonlinearity (DNL) performance is typically better than 0.5 LSB. The ADC uses a 2 V input range. See Figure 9, Figure 10, and Figure 11 for typical linearity and noise performance plots for the AD9970.

Optical Black Clamp

The optical black clamp loop removes residual offsets in the signal chain and tracks low frequency variations in the CCD black level. During the optical black (shielded) pixel interval on each line, the ADC output is compared with a fixed black level reference, selected by the user in the clamp level register. The value can be programmed between 0 LSB and 1023 LSB in 1024 steps. The resulting error signal is filtered to reduce noise, and the correction value is applied to the ADC input through a DAC. Normally, the optical black clamp loop is turned on once per horizontal line, but this loop can be updated more slowly to suit a particular application. If external digital clamping is used during the postprocessing, the AD9970 optical black clamping can be disabled using the AFE register, Address 0x00[3]. When the loop is disabled, the clamp level register can still be used to provide fixed offset adjustment.

Note: If the CLPOB loop is disabled, higher VGA gain settings reduce the dynamic range because the uncorrected offset in the signal path is gained up.

Align the CLPOB pulse with the optical black pixels of the CCD. It is recommended that the CLPOB pulse duration be at least 20 pixels wide. Shorter pulse widths can be used, but the ability for the loop to track low frequency variations in the black level is reduced. See the Horizontal Clamping and Blanking section for more timing information.

Digital Data Outputs

The AD9970 ADC digital output data is latched using the SHDLOC register value, as shown in Figure 58.

For maximum system flexibility, the AD9970 uses the DOUTPHASE register (Address 0x37, Bits[11:0]) to select the location for the start of each new pixel data value. Any edge location from 0 to 63 can be programmed. This register determines the start location of the data output and TCLK rising edge with respect to the master clock input CLI. For more information, see the Programmable Data Delay section.

APPLICATIONS INFORMATION

RECOMMENDED POWER-UP SEQUENCE

The following sequence is recommended to power up the AD9970 (refer to Figure 60 for each step):

1. Turn on the power supplies for the AD9970 and apply the CLI clock. There is no required order for bringing up each supply.
2. Write a 1 to the SW_RST register (Address 0x10) to reset all the internal registers to their default values. This bit is self-clearing and automatically resets back to 0.
3. Configure the STARTUP register with the specified value: STARTUP Address 0x01 [4:3] = 01.
4. Write to the desired registers to configure high speed timing and horizontal timing.
   Note: All TESTMODE registers must be written as described in the Complete Register Listing section.
5. Place the part into normal power operation by writing a 0 to the STANDBY register and the REFBUF_PWRDN register (Address 0x00).
   Note: Wait at least 500 µs before proceeding to Step 6.
6. Reset the *Precision Timing* core by writing a 1 to the TGCORE_RSTB register (Address 0x14). This starts the internal timing core operation.
   Note: Wait at least 100 µs before proceeding to Step 7.
7. Enable the LVDS outputs by writing a 0 to the TCLK_PDN, DOUT0_PDN and DOUT1_PDN registers (Address 0x40). The LVDS outputs should become active.
8. Configure the AD9970 for double data port mode by writing 01 to the TX_CTRL register (Address 0x41 [1:0]), and set the desired TCLK delay setting 0x41[6:3].
9. Write a 1 to the OUT_CONTROL register (Address 0x11).

The next VD/HD falling edge allows register updates to occur, including OUT_CONTROL that enables all clock outputs.

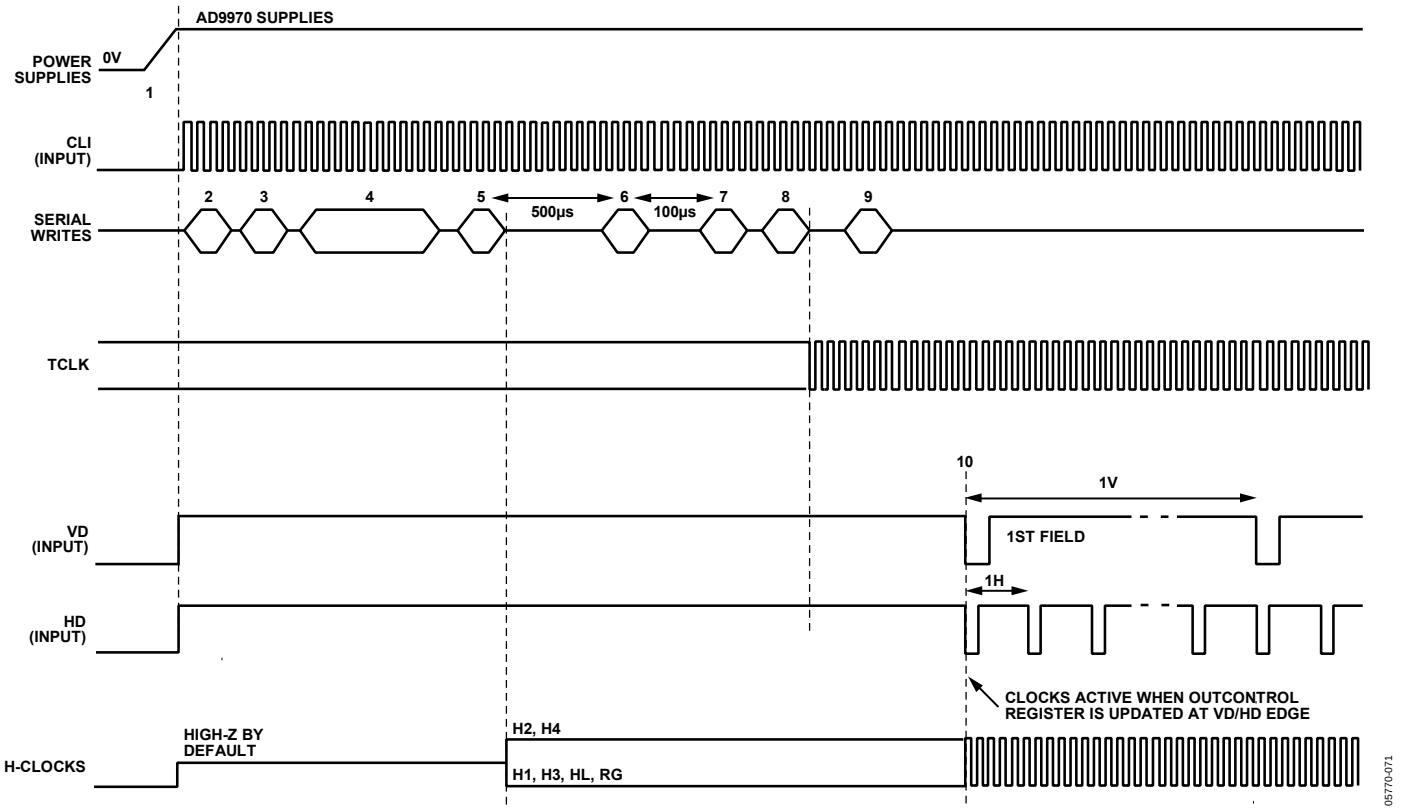


Figure 60. Recommended Power-Up Sequence

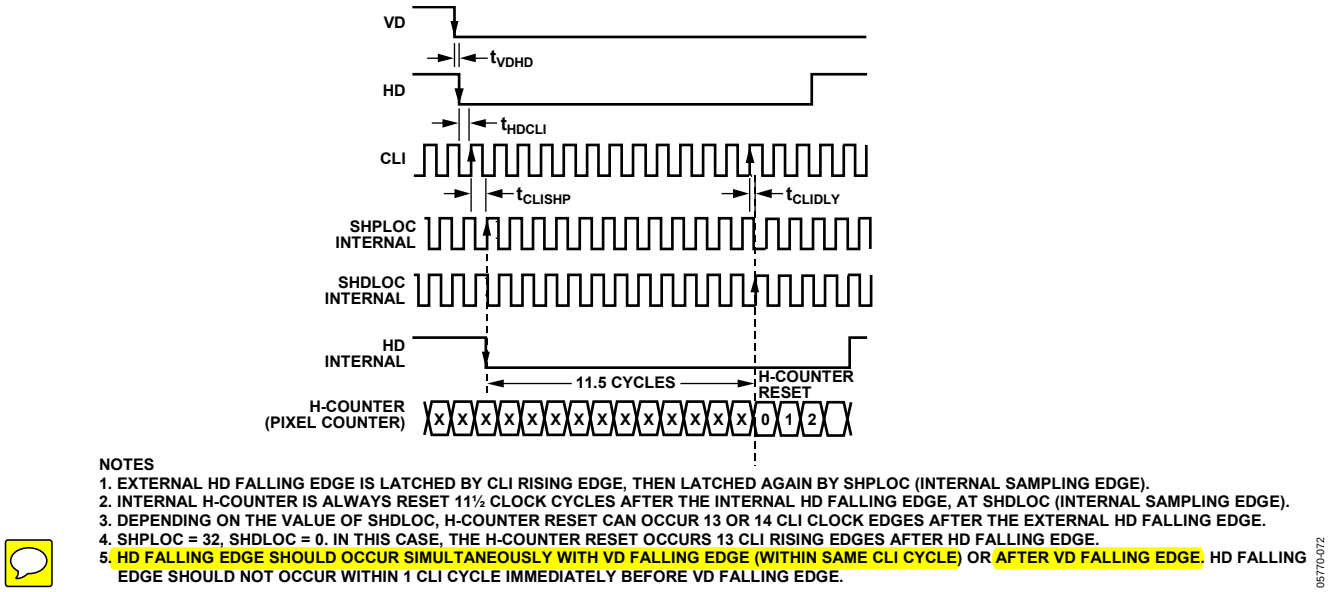


Figure 61. Horizontal Counter Pipeline Delay

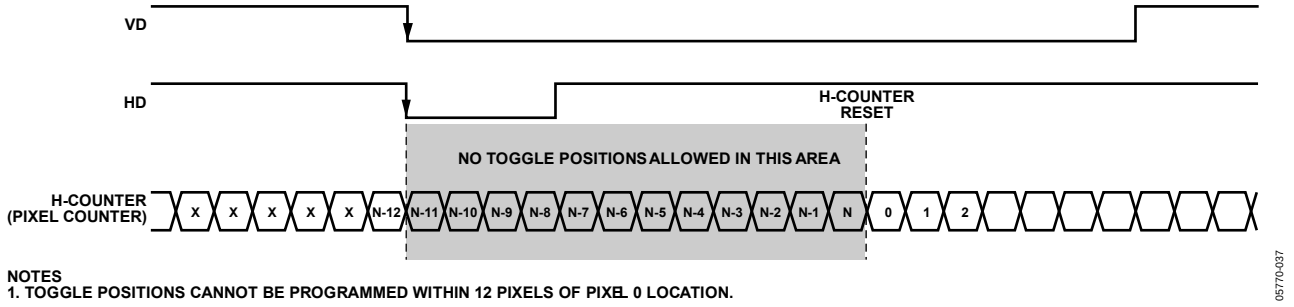


Figure 62. No-Toggle Positions

Additional Restrictions

During operation, note the following restrictions:

- Locate the HD falling edge in the same CLI clock cycle as the VD falling edge, or later than the VD falling edge. The HD falling edge should not be located between one cycle and five cycles prior to the VD falling edge.
- Perform all start-up serial writes with VD and HD disabled, if possible. This prevents unknown behavior caused by partial updating of registers before all information is loaded.

The internal horizontal counter is reset 12 CLI cycles after the falling edge of HD. See Figure 61 and Figure 62 for details on how the internal counter is reset.

STANDBY MODE OPERATION

The AD9970 contains two different standby modes to optimize the overall power dissipation in a particular application. Bits[1:0] of Address 0x00 control the power-down state of the device:

- STANDBY[1:0] = 00 = normal operation (full power)
- STANDBY[1:0] = 01 = reference standby mode
- STANDBY[1:0] = 01 or 11 = total shutdown mode (lowest power)

Table 20 summarizes the operation of each power-down mode. The OUTCONTROL register takes priority over the reference standby mode in determining the digital output states, but total shutdown mode takes priority over OUTCONTROL. Total shutdown mode has the lowest power consumption. When returning from total shutdown mode to normal operation, the timing core must be reset at least 100 µs after the STANDBY register is written to.

There is an additional register to independently disable the internal voltage reference buffer (Address 0x00 [2]). By default, the buffer is disabled, and the buffer must be enabled for normal operation.

CLI FREQUENCY CHANGE

If the input clock, CLI, is interrupted or changes to a different frequency, the timing core must be reset for proper operation. After the CLI clock has settled to the new frequency, or the previous frequency is resumed, write 0 and then 1 to the TGCORE_RSTB register (Address 0x14). This guarantees proper timing core operation. Also, the LVDS interface should be reset by rewriting desired values to address 0x40 and 0x41.

Table 20. Standby Mode Operation

I/O Block	Total Shutdown (Default)[1, 2]	OUTCONTROL = Low[2]	Reference Standby
AFE	Off	No change	Only REFT, REFB on
Timing Core	Off	No change	On
H1	High-Z	Low	Low (4.3 mA)
H2	High-Z	High	High (4.3 mA)
H3	High-Z	Low	Low (4.3 mA)
H4	High-Z	High	High (4.3 mA)
HL	High-Z	Low	Low (4.3 mA)
RG	High-Z	Low	Low (4.3 mA)
TCLK	Low	Running	Running
DOUT0, DOUT1	Low	Low	Low

[1] To exit total shutdown, write 00 to STANDBY (Bits [1:0], Address 0x00), then reset the timing core after 100 µs to guarantee proper settling.
[2] Total shutdown mode takes priority over OUTCONTROL for determining the output polarities.

LVDS PCB DESIGN CONSIDERATIONS

Treat LVDS outputs for high performance AFEs differently than standard LVDS outputs used in digital logic. Although a standard LVDS can drive 1 meter to 10 meters in high speed digital applications (dependent on data rate), it is not recommended to let a high performance AFE drive that distance.

Rather, it is recommended to keep the output trace lengths short (<2 inches), minimizing the opportunity for any noise coupling onto the outputs from the adjacent circuitry that can return to the analog inputs.

Route the differential output traces close together, maximizing common-mode rejection with the 100 Ω termination resistor close to the receiver. Users should pay attention to PCB trace lengths to minimize any delay skew.

A typical differential microstrip PCB trace cross section is shown in Figure 63.

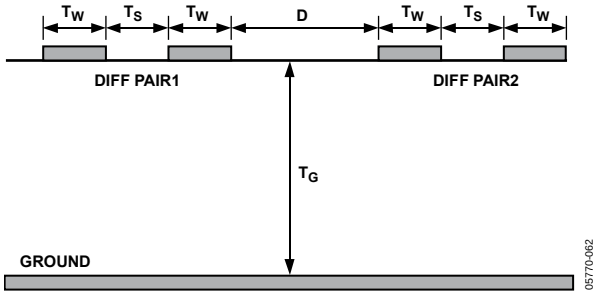


Figure 63. PCB Trace Spacing

Layout Guidelines

What follows is a list of layout guidelines.

- Keep TW, TS, and D constant over the trace length.
- Keep TS ~ < 2 TW.
- Avoid use of vias, where possible.
- Keep D > 2 TS.
- Avoid 90° bends, if possible.
- Design TW and TG for ~50 Ω.

Power supply decoupling is very important with these fast edge rates. Place a low inductance, surface-mount capacitor at every power supply and ground pin, as close to the AFE as possible. Placing the decoupling capacitors on the other side of the PCB is not recommended because the via inductance reduces the effective decoupling.

The differential Z_O tends to be slightly lower than twice the single-ended Z_O of each conductor due to proximity effects—design the Z_O of each line to be slightly higher than 50 Ω. Use simulation in critical applications to verify impedance matching. In short runs, this should not be critical.

CIRCUIT CONFIGURATION

The AD9970 recommended circuit configuration is shown in Figure 64. Achieving good image quality from the AD9970 requires careful attention to PCB layout. Route all signals to maintain low noise performance. Directly route the CCD output signal through a 0.1 µF capacitor to Pin 21. To minimize interference with the CCDIN, REFT, and REFB signals, carefully route the Master Clock CLI to Pin 19.

The H1 to H4, HL and RG traces need low inductance to avoid excessive distortion of the signals. Heavier traces are recommended because of the large transient current demand on H1 to H4 and HL from the capacitive load of the CCD. If possible, physically locating the AD9970 closer to the CCD reduces the inductance on these lines. Make the routing path as direct as possible from the AD9970 to the CCD.

GROUNDING AND DECOUPLING RECOMMENDATIONS

As shown in Figure 64, a single ground plane is recommended for the AD9970. This ground plane should be as continuous as possible, particularly around Pin 19 to Pin 24.

This configuration ensures that all analog decoupling capacitors provide the lowest possible impedance path between the power and bypass pins and their respective ground pins. Locate all high frequency decoupling capacitors as close as possible to the package pins. It is recommended that the exposed paddle on the bottom of the package be soldered to a large pad, with multiple vias connecting the pad to the ground plane.

All the supply pins must be decoupled to ground with good quality, high frequency chip capacitors. In addition, provide a 4.7 µF (or larger) bypass capacitor for each main supply—1.8 V (AVDD, DVDD, LVDD) and 3.3 V (RGVDD, HVDD)—although this is not necessary for each individual pin. In most applications, it is easier to share the supply for RGVDD and HVDD, which can be done as long as the individual supply pins are separately bypassed.

Decouple the reference bypass pins (REFT, REFB) to ground, as close as possible to their respective pins. The bridge capacitor between REFT and REFB is recommended for pixel rates greater than 40 MHz. Also, locate the analog input (CCDIN) capacitor close to the pin.

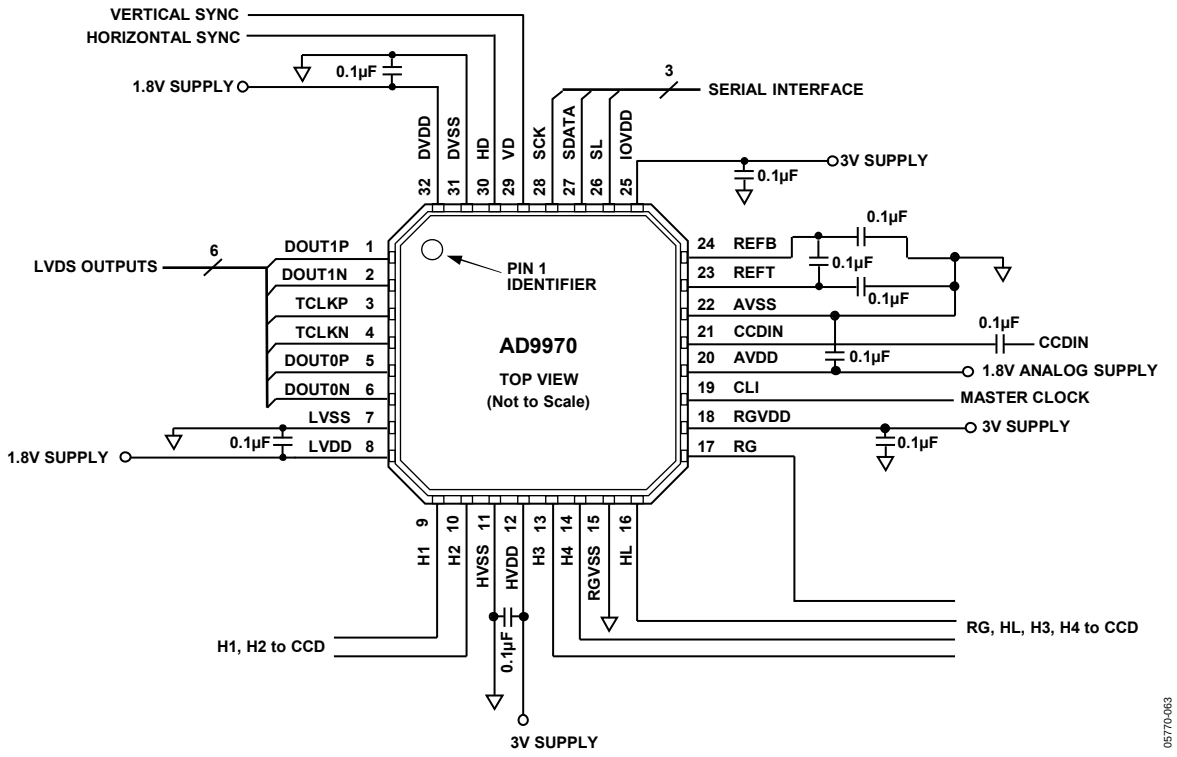
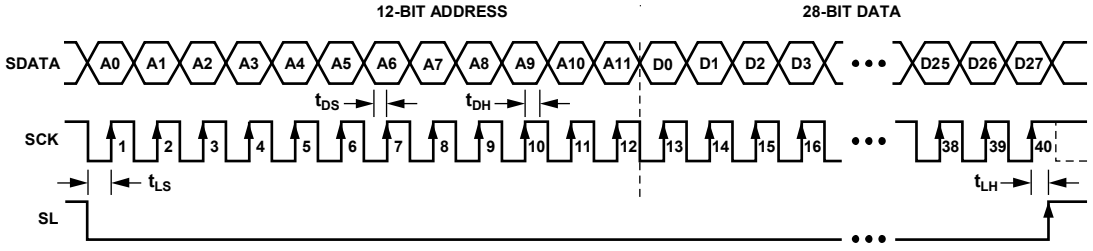


Figure 64. Recommended Circuit Configuration

3-WIRE SERIAL INTERFACE TIMING

All internal registers of the AD9970 are accessed through a 3-wire serial interface. Each register consists of a 12-bit address and a 28-bit data-word. Both the 12-bit address and 28-bit data-word are written starting with the LSB. To write to each register, a 40-bit operation is required, as shown in Figure 65. Although many registers are fewer than 28 bits wide, all 28 bits must be written for each register. For example, if the register is only 20 bits wide, then the upper 8 bits are don't care bits and must be filled with 0s during the serial write operation. If fewer than 28 data bits are written, the register is not updated with new data.

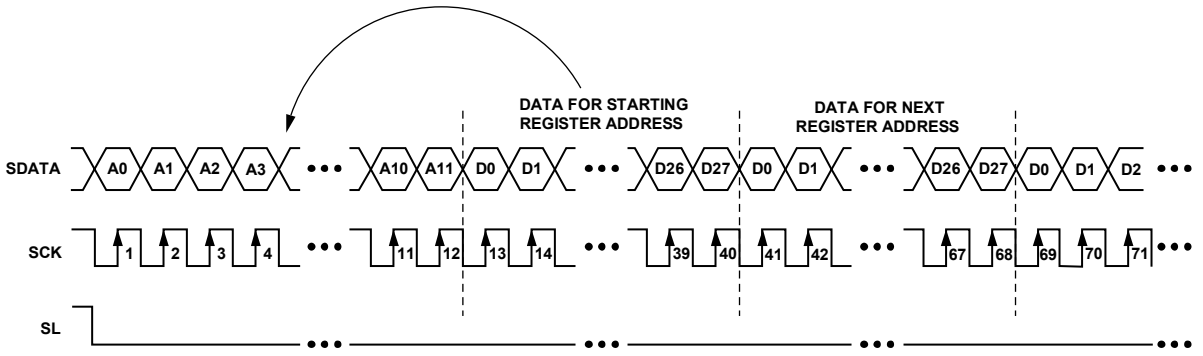
Figure 66 shows a more efficient way to write to the registers, using the AD9970 address auto-increment capability. In this method, the lowest desired address is written first, followed by multiple 28-bit data-words. Each new 28-bit data-word is automatically written to the next highest register address. By eliminating the need to write each 12-bit address, faster register loading is achieved. Continuous write operations can be used starting with any register location.



NOTES
1. SDATA BITS ARE LATCHED ON SCK RISING EDGES. SCK MAY IDLE HIGH OR LOW BETWEEN WRITE OPERATIONS.
2. ALL 40 BITS MUST BE WRITTEN: 12 BITS FOR ADDRESS AND 28 BITS FOR DATA.
3. IF THE REGISTER LENGTH IS < 28 BITS, THEN ZEROS MUST BE USED TO COMPLETE THE 28-BIT DATA LENGTH.
4. NEW DATA VALUES ARE UPDATED IN THE SPECIFIED REGISTER LOCATION AT DIFFERENT TIMES, DEPENDING ON THE PARTICULAR REGISTER WRITTEN TO. SEE THE UPDATING OF NEW REGISTER VALUES SECTION FOR MORE INFORMATION.

05770-064

Figure 65. Serial Write Operation



NOTES
1. MULTIPLE SEQUENTIAL REGISTERS MAY BE LOADED CONTINUOUSLY.
2. THE FIRST (LOWEST ADDRESS) REGISTER ADDRESS IS WRITTEN, FOLLOWED BY MULTIPLE 28-BIT DATA-WORDS.
3. THE ADDRESS WILL AUTOMATICALLY INCREMENT WITH EACH 28-BIT DATA-WORD (ALL 28 BITS MUST BE WRITTEN).
4. SL IS HELD LOW UNTIL THE LAST DESIRED REGISTER HAS BEEN LOADED.

05770-065

Figure 66. Continuous Serial Write Operation

LAYOUT OF INTERNAL REGISTERS

The AD9970 address space is divided into two different register areas, as illustrated in Figure 67. In the first area, Address 0x00 to Address 0x72 contain the registers for the AFE, miscellaneous functions, VD/HD parameters, I/O control, mode control, timing core, LVDS, update control functions, and a special address for LVDS test pattern support. The second area of the address space, beginning at Address 0x800, consists of the registers for the H-pattern groups and fields. This is a configurable set of register space; the user can decide how many H-patterns and fields to use in a particular design. The AD9970 supports up to 32 H-patterns.

Register 0x28 specifies the total number of H-pattern groups. The starting address for the H-pattern groups is always 0x800. The starting address for the field registers is determined by the number of H-pattern groups. Each H-pattern group and field occupies 16 register addresses.

The starting address for the field registers is based on the number of H-pattern groups and is equal to 0x800 plus the number of H-pattern groups times 16.

Note: The H-pattern and field registers must always occupy a continuous block of addresses.

Figure 68 shows an example when three H-pattern groups and two fields are used. The starting address for the H-pattern groups is always 0x800. Because HPAT_NUM = 3, the H-pattern groups occupy 48 address locations; that is, 16 registers × 3 H-pattern groups.

The starting address of the field registers for this example is 0x800 + 48 (decimal) = 0x830. Note the decimal value must be converted to a hexadecimal number before adding it to 0x800.

The AD9970 address space contains many unused addresses. Do not write to any undefined addresses between Address 0x00 and Address 0xFF; otherwise, the AD9970 can operate incorrectly. Carefully perform continuous register writes to avoid writing to undefined registers.

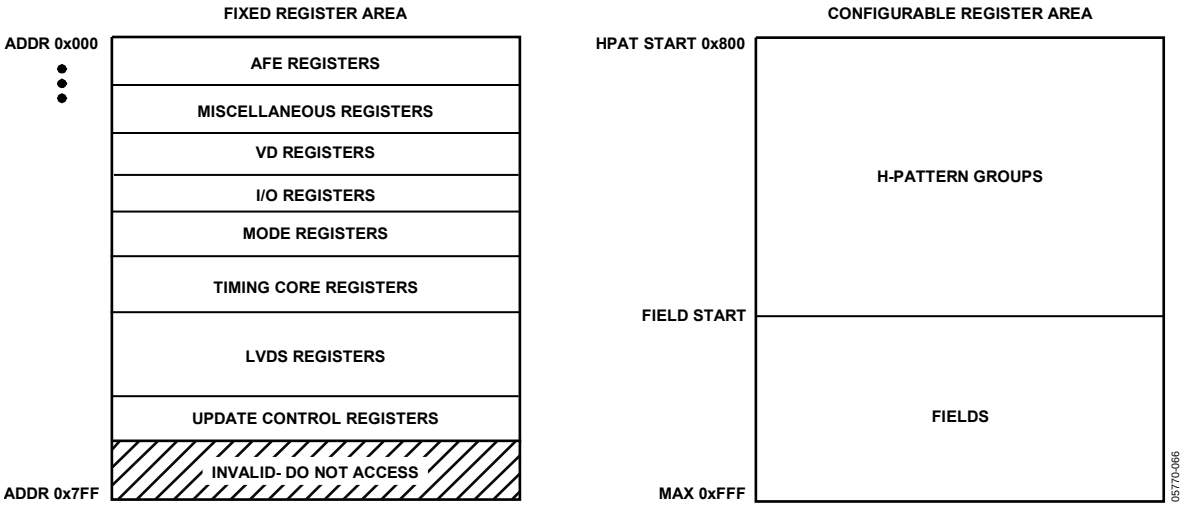


Figure 67. Layout of AD9970 Registers

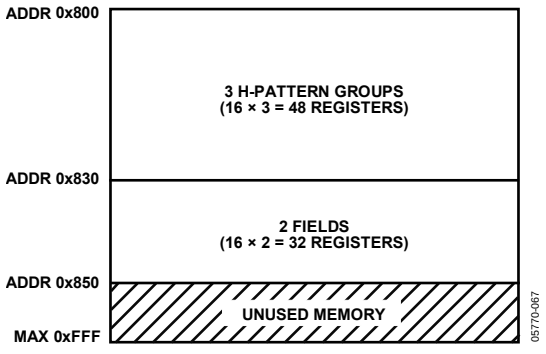


Figure 68. Example of Register Configuration

UPDATING OF NEW REGISTER VALUES

The internal registers of the AD9970 are updated at different times, depending on the particular register. Table 21 summarizes the three different types of register updates. The register listing tables also contain the column, Update Type, to identify when each register is updated:

SCK Updated

Some of the registers are updated immediately, as soon as the 28th data bit (D27) is written. These registers are used for functions that do not require gating with the next VD boundary, such as power-up and reset functions.

VD Updated

Many of the registers are updated at the next VD falling edge. By updating these values at the next VD edge, the current field is not corrupted, and the new register values are applied to the next field. The VD update can be further delayed past the VD falling edge by using the UPDATE register (Address 0x17). This delays the VD-updated register updates to any HD line in the field. Note that the field registers are not affected by the UPDATE register.

SCP Updated

All of the H-pattern group registers are updated at the next SCP where they are used.

Table 21. Register Update Locations

Update Type	Description
SCK Updated	Register is immediately updated when the 28th data bit (D27) is clocked in.
VD Updated	Register is updated at the VD falling edge. VD-updated registers can be delayed further, by using the UPDATE register at Address 0x17. Field registers are not affected by the UPDATE register.
SCP Updated	Register is updated at the next SCP when the register is used.

COMPLETE REGISTER LISTING

All addresses and default values are expressed in hexadecimal. When an address contains less than 28 data bits, all remaining bits must be written as 0s. All TESTMODE registers must be set to the specified values.

Table 22. AFE Registers

Address	Data Bits	Default Value	Update	Name	Description
0x00	[1:0]	3	SCK	STANDBY	Standby modes 0: normal operation 1: reference standby (band gap reference still active) 2/3: total shutdown
	[2]	1		REFBUF_PWRDN	Reference buffer for REFT and REFB power control 0 = REFT/REFB internally driven (normal operation) 1 = REFT/REFB not driven (standby condition)
	[3]	1		CLAMPENABLE	Clamp enable control 0 = disable black clamp 1 = enable black clamp
	[5:4]	0		TESTMODE	Test operation only; set to 0
	[6]	0		PBLK_LVL	PBLK level control 0 = blank to zero 1 = blank to clamp level
	[7]	0		DCBYP	DC restore circuit control 0 = enable dc restore circuit during PBLK 1 = bypass dc restore circuit during PBLK
	[8]	0		TESTMODE	Test operation only; set to 0
	[9]	0		CDSMODE	CDS operation 0 = normal CDS operation 1 = positive CDS operation
	[16:10]	0		TESTMODE	Test operation only; set to 0
	[27:17]			Unused	Set unused bits = 0
0x01	[2:0]	0	SCK	TESTMODE	Test operation only; set to 0
	[4:3]	2		STARTUP	Required start-up register; must be set to 01
	[27:5]			Unused	Set unused bits = 0
0x02	[0]	0	SCK	TESTMODE	Test operation only; set to 0
	[27:1]			Unused	Set unused bits = 0
0x03	[23:0]	FFFFFF	SCK	TESTMODE	Test operation only; set to FFFFFF
	[27:24]			Unused	Set unused bits = 0
0x04	[1:0]	1	VD	CDSGAIN	CDS gain setting 0: −3 dB 1: 0 dB (default) 2: +3 dB 3: +6 dB
	[27:2]			Unused	Set unused bits = 0
0x05	[9:0]	F	VD	VGAGAIN	VGA gain, 6 dB to 42 dB (0.0359 dB per step)
	[27:10]			Unused	Set unused bits = 0
0x06	[9:0]	1EC	VD	CLAMPLEVEL	Optical black clamp level, 0 LSB to 1023 LSB (1 LSB per step)
	[27:10]			Unused	Set unused registers = 0
0x07	[27:0]	0		TESTMODE	Test operation only; set to 0 if this register is accessed
0x08	[27:0]	0		TESTMODE	Test operation only; set to 0 if this register is accessed
0x09	[27:0]	0		TESTMODE	Test operation only; set to 0 if this register is accessed
0x0A	[27:0]	0		TESTMODE	Test operation only; set to 0 if this register is accessed
0x0B	[27:0]	0		TESTMODE	Test operation only; set to 0 if this register is accessed
0x0C	[27:0]	0	VD	TESTMODE	Test operation only; set to 0 if this register is accessed

Address	Data Bits	Default Value	Update	Name	Description
0x0D	[0]	0	VD	CLIDIVIDE	CLI divide. 1 = divide CLI input frequency by 2
	[3:1]	0		TESTMODE	Test operation only; set to 0
	[27:4]			Unused	Set unused bits = 0
0x0E	[27:0]		SCK	Unused	Set unused register = 0 if accessed
0x0F	[27:0]		SCK	Unused	Set unused register = 0 if accessed

Table 23. Miscellaneous Registers

Address	Data Bits	Default Value	Update	Name	Description
0x10	[0]	0	SCK	SW_RST	Software reset, bit self-clears back to 0 when a reset occurs 1: Reset Address 0x00 to Address 0xFF back to default values
	[27:1]			Unused	Set unused bits = 0
0x11	[0]	0	VD	OUT_CONTROL	Output control 0: make all outputs dc inactive 1: enable outputs at next VD edge
	[27:1]			Unused	Set unused bits = 0
0x12	[1:0]	0	SCK	TESTMODE	Test operation only; set to 0
	[27:2]			Unused	Set unused bits = 0
0x13	[0]	0	SCK	TESTMODE	Test operation only; set to 0
	[27:1]			Unused	Set unused bits = 0
0x14	[0]	0	SCK	TGCORE_RSTB	Timing core reset bar 0 = hold in reset 1 = resume operation
				Unused	Set unused bits = 0
0x15	[0]	0	SCK	CLI_BIAS	Enable bias circuit for CLI input (see Figure 13) 0 = disable bias (CLI input is dc coupled) 1 = enable bias (CLI input is ac coupled)
	[27:1]			Unused	Set unused bits = 0
0x16	[0]	0	SCK	TESTMODE	Test operation only; set to 0
	[27:1]			Unused	Set unused bits = 0
0x17	[12:0]	0	SCK	UPDATE	Serial interface update line; sets the line (HD) within the field to update the VD-updated registers; UPDATE is disabled when PREVENTUP = 1
	[13]	0		PREVENTUP	Prevent update; prevents the normal update of the VD-updated registers 0 = normal update at VD 1 = prevent update of VD-updated type registers
	[27:14]			Unused	Set unused bits = 0
0x18	[27:0]	0		TESTMODE	Test operation only; set to 0 if this register is accessed
0x19	[27:0]	0		TESTMODE	Test operation only; set to 0 if this register is accessed

Table 24. VD/HD Registers

Address	Data Bits	Default Value	Update	Name	Description
0x20	[0]	0	SCK	TESTMODE	Test operation only; set to 0
	[27:1]			Unused	Set unused bits = 0
0x21	[0]	0	SCK	VDHDPOL	VD/HD Active Polarity 0 = active low 1 = active high
	[2:1]	0		TESTMODE	Test operation only; set to 0
	[27:3]			Unused	Set unused bits = 0
0x22	[27:0]	0		TESTMODE	Test operation only; set to 0 if this register is accessed

Table 25. I/O Control Registers

Address	Data Bits	Default Value	Update	Name	Description
0x23	[0]	0	SCK	TESTMODE	Test operation only; set to 0
	[1]	0		TESTMODE	Test operation only; set to 0
	[2]	0		IO_NVR	IOVDD voltage range for VD, HD, SCK, SDATA, SL 0 = 1.8 V 1 = 3.3 V
	[3]	0		TESTMODE	Test operation only; set to 0
	[4]	0		TESTMODE	Test operation only; set to 0
	[7:5]	1		HCLKMODE	Selects HCLK output configuration; see Table 10
	[27:8]			Unused	Set unused bits = 0
0x24	[27:0]	0		TESTMODE	Test operation only; set to 0 if this register is accessed
0x25	[27:0]	0		TESTMODE	Test operation only; set to 0 if this register is accessed
0x26	[27:0]	0		TESTMODE	Test operation only; set to 0 if this register is accessed
0x27	[27:0]	0		TESTMODE	Test operation only; set to 0 if this register is accessed

Table 26. Mode Registers

Address	Data Bits	Default Value	Update	Name	Description
0x28	[4:0]	0	VD	HPAT_NUM	Total number of H-pattern groups
	[27:5]			Unused	Set unused bits = 0
0x29	[27:0]			Unused	Set unused register = 0 if accessed
0x2A	[2:0]	0	VD	FIELDNUM	Total number of fields (set = 1 for single field operation)
	[27:3]			Unused	Set unused bits = 0
0x2B	[4:0]	0	VD	FIELD_SEL1	Selected 1st field
	[9:5]	0	VD	FIELD_SEL2	Selected 2nd field
	[14:10]	0		FIELD_SEL3	Selected 3nd field
	[19:15]	0		FIELD_SEL4	Selected 4th field
	[24:20]	0		FIELD_SEL5	Selected 5th field
	[27:25]			Unused	Set unused bits = 0
0x2C	[4:0]	0	VD	FIELD_SEL 6	Selected 6th field
	[9:5]	0		FIELD_SEL 7	Selected 7th field
	[27:10]			Unused	Set unused bits = 0
0x2D	[27:0]		SCK	Unused	Set unused register = 0 if this register is accessed
0x2E	[27:0]		SCK	Unused	Set unused register = 0 if this register is accessed
0x2F	[27:0]		SCK	Unused	Set unused register = 0 if this register is accessed

Table 27. Timing Core Registers

Address	Data Bits	Default Value	Update	Name	Description
0x30	[5:0]	0	SCK	H1POSLOC	H1 rising edge location
	[7:6]			Unused	Set unused bits = 0
	[13:8]	20		H1NEGLOC	H1 falling edge location
	[15:14]	0		TESTMODE	Test operation only; set to 0
	[16]	1		H1POL	H1 Polarity Control 0 = inverse of Figure 23 1 = no inversion; recommended setting
	[27:17]			Unused	Set unused bits = 0
0x31	[5:0]	0	SCK	H2POSLOC	H2 rising edge location
	[7:6]			Unused	Set unused bits = 0
	[13:8]	20		H2NEGLOC	H2 falling edge location
	[15:14]	0		TESTMODE	Test operation only; set to 0
	[16]	1		H2POL	H2 polarity control 0 = inverse of Figure 23 1 = no inversion; recommended setting
	[27:17]			Unused	Set unused bits = 0
0x32	[5:0]	0	SCK	HLPOSLOC	HL rising edge location
	[7:6]			Unused	Set unused bits = 0
	[13:8]	20		HLNEGLOC	HL falling edge location
	[15:14]	0		TESTMODE	Test operation only; set to 0
	[16]	1		HLPOL	HL polarity control 0 = inverse of Figure 23 1 = no inversion; recommended setting
	[27:17]			Unused	Set unused bits = 0
0x33	[5:0]	0	SCK	RGPOSLOC	RG rising edge location
	[7:6]			Unused	Set unused bits = 0
	[13:8]	10		RGNEGLOC	RG falling edge location
	[15:14]	0		TESTMODE	Test operation only; set to 0
	[16]	1		RGPOL	RG polarity control 0 = inverse of Figure 23 1 = no inversion; recommended setting
	[27:17]			Unused	Set unused bits = 0
0x34	[0]	0	SCK	H1BLKRETIME	Retime H1 HBLK to internal SHP clock 0 = no retime 1 = enable SHP retime Recommended setting is retime enabled for H1 and HL; enabling retime adds one half cycle delay to HBLK positions
	[1]	0		H2BLKRETIME	Retime H2 HBLK to internal SHP. Used in HCLK 2 and HCLK 3 modes.
	[2]	0		HLBLKRETIME	Retime HL HBLK to internal SHP clock
	[3]	0		HL_HBLK_EN	Enable HBLK for HL output 0 = disable 1 = enable
	[7:4]	0		HCLK_WIDTH	Enable wide H-clocks during HBLK interval; see Table 14 0 = disable
	[27:8]			Unused	Set unused bits = 0

Address	Data Bits	Default Value	Update	Name	Description
0x35	[2:0]	1	SCK	H1DRV	H1: drive strength 0 = off 1 = 4.3 mA 2 = 8.6 mA 3 = 12.9 mA 4 = 17.2 mA 5 = 21.5 mA 6 = 25.8 mA 7 = 30.1 mA
	[3]			Unused	Set unused bits = 0
	[6:4]	1		H2DRV	H2: drive strength
	[7]			Unused	Set unused bits = 0
	[10:8]	1		H3DRV	H3: drive strength
	[11]			Unused	Set unused bits = 0
	[14:12]	1		H4DRV	H4: drive strength
	[15]			Unused	Set unused bits = 0
	[18:16]	1		HLDRV	HL: drive strength
	[19]			Unused	Set unused bits = 0
	[22:20]	1		RGDRV	RG: drive strength
	[27:23]			Unused	Set unused bits = 0
0x36	[5:0]	0	SCK	SHDLOC	SHD sampling edge location
	[11:6]	20		SHPLOC	SHP sampling edge location
	[17:12]	10		SHPWIDTH	SHP width; controls input DC restore switch active time
	[27:18]			Unused	Set unused bits = 0
0x37	[5:0]	0	SCK	DOUTPHASEP	DOUTP phase control
	[11:6]	20		DOUTPHASEN	DOUTN phase control (Set DOUTPHASEN = DOUTPHASEP + 0x20)
	[12]	0		TESTMODE	Test operation only; set to 0
	[14:13]	2		TESTMODE	Test operation only; set to 2
	[15]	0		TESTMODE	Test operation only; set to 0
	[27:16]			Unused	Set unused bits = 0
0x38	[27:0]			Unused	Set unused register = 0 if this register is accessed
0x39	[27:0]			Unused	Set unused register = 0 if this register is accessed
0x3A	[27:0]			Unused	Set unused register = 0 if this register is accessed
0x3B	[27:0]			Unused	Set unused register = 0 if this register is accessed
0x3C	[27:0]			Unused	Set unused register = 0 if this register is accessed
0x3D	[27:0]			Unused	Set unused register = 0 if this register is accessed

Table 28. LVDS Registers

Address	Data Bits	Default Value	Update	Name	Description
0x3E	[18:0]	4B020	SCK	TESTMODE	Test operation only; set to 0x4B020
	[27:19]			Unused	Set unused bits = 0
0x40	[0]	1	SCK	TCLK_PDN	0 = normal operation, 1= power down
	[1]	1		TESTMODE	Test operation only, set to 1
	[2]	1		DOUT0_PDN	0 = normal operation, 1= power down
	[3]	1		DOUT1_PDN	0 = normal operation, 1= power down
	[9:4]	0		TESTMODE	Test operation only; set to 0
	[27:10]			Unused	Set unused bits = 0

Address	Data Bits	Default Value	Update	Name	Description
0x41	[1:0]	0	SCK	TX_CTRL	Serial Data Transmit Control 00 = single data port mode with data on DOUT0 10 = single data port mode with data on DOUT1 01 = double data port mode with low byte on DOUT0, high byte on DOUT1 11 = double data port mode with low byte on DOUT1, high byte on DOUT0
	[2]	0		TESTMODE	Test operation only; set to 0
	[6:3]	0		TCLK_DELAY	TCLK rising edge delay 0 = default with no delay 1 LSB = 1/16 cycle of internal TCLK in double data port mode 1 LSB = 1/8 cycle of internal TCLK in single data port mode
	[7]	0		LVDS_LSB_ALIGN	0 = MSB first, 1 = LSB first
	[8]	0		TESTMODE	Test operation only; set to 0
	[10:9]	01		TESTMODE	Test operation only; must be set to 01
	[11]	0		CLIP_ZS	Data clip operation for ADC zero-scale output data 0 = clip disabled; ADC zero scale = 0x0000 1 = clip function enabled; ADC zero scale = 0x0001
	[12]	0		CLIP_FS	Data clip operation for ADC full-scale output data 0 = clip disabled; ADC full scale = 0x3FFF 1 = clip function enabled; ADC full scale = 0x3FFE
	[27:13]			Unused	Set unused bits = 0
0x42	[0]	0	SCK	TESTMODE	Test operation only; set to 0
	[27:1]			Unused	Set unused bits = 0
0x43	[2:0]	0	SCK	SYNCWORDNUM	Number of SYNC words
	[3]	0		CONTROLWORD_EN	Control word enable 0 = disable control word 1 = enable control word
	[27:4]			Unused	Set unused bits = 0
0x44	[15:0]	0	SCK	SYNC_WORD0	Sync word 0
	[27:16]			Unused	Set unused bits = 0
0x45	[15:0]	0	SCK	SYNC_WORD1	Sync word 1
	[27:16]			Unused	Set unused bits = 0
0x46	[15:0]	0	SCK	SYNC_WORD2	Sync word 2
	[27:16]			Unused	Set unused bits = 0
0x47	[15:0]	0	SCK	SYNC_WORD3	Sync word 3
	[27:16]			Unused	Set unused bits = 0
0x48	[15:0]	0	SCK	SYNC_WORD4	Sync word 4
	[27:16]			Unused	Set unused bits = 0
0x49	[15:0]	0	SCK	SYNC_WORD5	Sync word 5
	[27:16]			Unused	Set unused bits = 0
0x4A	[15:0]	0	SCK	SYNC_WORD6	Sync word 6
	[27:16]			Unused	Set unused bits = 0
0x4B	[0]		SCK	TESTMODE	Test operation only; set to 0
	[1]	0		LVDS_TEST_EN	LVDS data input test enable 0 = disable 1 = enable
	[5:2]	0		TESTMODE	Test only; set to 0x0
	[27:6]			Unused	Set unused register = 0 if this register is accessed
0x4C	[7:0]	0	SCK	SYNC_RISING_EN	Rising synchronization enable for control word bit[7:0]
	[15:8]	0		SYNC_FALLING_EN	Falling synchronization enable for control word bit[7:0]
	[27:16]			Unused	Set unused bits = 0

Address	Data Bits	Default Value	Update	Name	Description
0x4D	[12:0]	0	SCK	SYNC_START_LOC	Sync sequence start location in each line
	[13]	0		SYNC_ALIGN_LOC	0 = synchronization word inserted after SYNC_DELAY 1 = synchronization word inserted before SYNC_DELAY
	[14]	0		SYNC_CW_EN	1 = synchronization word and control word are applied at location of SYNC_START_LOC register
	[27:15]			Unused	Set unused bits = 0
0x4E	[3:0]	0	SCK	CWB0	Control word bit 0 select
	[7:4]	0		CWB1	Control word bit 1 select
	[11:8]	0		CWB2	Control word bit 2 select
	[15:12]	0		CWB3	Control word bit 3 select
	[19:16]	0		CWB4	Control word bit 4 select
	[23:20]	0		CWB5	Control word bit 5 select
	[27:24]			Unused	Set unused bits = 0
0x4F	[3:0]	0	SCK	CWB6	Control word bit 6 select
	[7:4]	0		CWB7	Control word bit 7 select
	[27:8]			Unused	Set unused bits = 0
0x50 to 0x5F	[27:0]		SCK	Unused	Address 50 through Address 5F are unused; set = 0 if accessed

Table 29. Update Control Registers

Address	Data Bits	Default Value	Update	Name	Description
0x60	[15:0]	1803	SCK	AFE_UPDT_SCK	Enable SCK update of AFE registers; each bit corresponds to one address location AFE_UPDT_SCK[0] = 1, update Address 0x00 on SL rising edge AFE_UPDT_SCK[1] = 1, update Address 0x01 on SL rising edge … AFE_UPDT_SCK[15] = 1, update Address 0x0F on SL rising edge
	[27:16]			Unused	Set unused register = 0 if accessed
0x61	[15:0]	E7FC	SCK	AFE_UPDT_VD	Enable VD update of AFE registers; each bit corresponds to one address location AFE_UPDT_VD[0] = 1, update Address 0x00 on VD rising edge AFE_UPDT_VD[1] = 1, update Address 0x01 on VD rising edge … AFE_UPDT_VD[15] = 1, update Address 0x0F on VD rising edge
	[27:16]			Unused	Set unused register to 0 if accessed
0x62	[15:0]	F8FD	SCK	MISC_UPDT_SCK	Enable SCK update of miscellaneous registers Address 0x10 to Address 0x1F
	[27:0]			Unused	Set unused register to 0 if accessed
0x63	[15:0]	0702	SCK	MISC_UPDT_VD	Enable VD update of miscellaneous registers Address 0x10 to Address 0x1F
	[27:0]			Unused	Set unused register to 0 if accessed
0x64	[15:0]	FFF9	SCK	VDHD_UPDT_SCK	Enable SCK update of VDHD registers, Address 0x20 to Address 0x22
	[27:0]			Unused	Set unused register to 0 if accessed
0x65	[15:0]	0006	SCK	VDHD_UPDT_VD	Enable VD update of VDHD registers, Address 0x20 to Address 0x22
	[27:16]			Unused	Set unused register to 0 if accessed
0x66 to 0x71	[27:0]		SCK	Unused	Set unused register to 0 if accessed

Table 30. Special Test Pattern Registers

Address	Data Bits	Default Value	Update	Name	Description
0x72	[15:0]	0		LVDS_PATTERN	Dual purpose register; 16-bit LVDS test pattern; to apply the LVDS test pattern also set Bit 24 of Address 0x72 = 1 and Bits[1:0] of Address 0x4B = 1 When TCLK_PAT_MODE is enabled, this register is used to set the TCLK output pattern
	[16]	0		TCLK_PAT_MODE	TCLK Pattern enable 0 = disable TCLK pattern mode 1 = enable TCLK pattern mode
	[23:17]	0		TESTMODE	Always set = 0
	[24]	0		LVDS_PATTERN_EN	LVDS test pattern enable 0 = disable 1 = enable
	[27:25]			Unused	Set unused bits = 0

Table 31. HPAT Registers (HPAT Registers Always Start at Address 0x800)

Address	Data Bits	Default Value	Update	Name	Description
0x00	[12:0]	X	SCP	HBLKTOGO1	1st HBLK toggle position for odd lines or RA0H1REPABC
	[25:13]	X		HBLKTOGO2	2nd HBLK toggle position for odd lines or RA1H1REPABC
	[27:26]	X		Unused	Set unused bits = 0
0x01	[12:0]	X	SCP	HBLKTOGO3	3rd HBLK toggle position for odd lines or RA2H1REPABC
	[25:13]	X		HBLKTOGO4	4th HBLK toggle position for odd lines or RA30H1REPABC
	[27:26]	X		Unused	Set unused bits = 0
0x02	[12:0]	X	SCP	HBLKTOGO5	5th HBLK toggle position for odd lines or RA4H1REPABC
	[25:13]	X		HBLKTOGO6	6th HBLK toggle position for odd lines or RA5H1REPABC
	[27:26]	X		Unused	Set unused bits = 0
0x03	[12:0]	X	SCP	HBLKTOGE1	1st HBLK toggle position for even lines or RA0H2REPABC
	[25:13]	X		HBLKTOGE2	2nd HBLK toggle position for even lines or RA1H2REPABC
	[27:26]	X		Unused	Set unused bits = 0
0x04	[12:0]	X	SCP	HBLKTOGE3	3rd HBLK toggle position for even lines or RA2H2REPABC
	[25:13]	X		HBLKTOGE4	4th HBLK toggle position for even lines or RA3H2REPABC
	[27:26]	X		Unused	Set unused bits = 0
0x05	[12:0]	X	SCP	HBLKTOGE5	5th HBLK toggle position for even lines or RA4H2REPABC
	[25:13]	X		HBLKTOGE6	6th HBLK toggle position for even lines or RA5H2REPABC
	[27:26]	X		Unused	Set unused bits = 0
0x06	[12:0]	X	SCP	HBLKSTARTA	HBLK repeat area start Position A for HBLK Mode 2
	[25:13]	X		HBLKSTARTB	HBLK repeat area start position B for HBLK Mode 2
	[27:26]	X		Unused	Set unused bits = 0
0x07	[12:0]	X	SCP	HBLKSTARTC	HBLK repeat area start position C for HBLK Mode 2
	[27:13]	X		Unused	Set unused bits = 0

Address	Data Bits	Default Value	Update	Name	Description
0x08	[2:0]	X	SCP	HBLKALT_PAT1	HBLK pattern 1 order, used during pixel mixing mode
	[5:3]	X		HBLKALT_PAT2	HBLK pattern 2 order, used during pixel mixing mode
	[8:6]	X		HBLKALT_PAT3	HBLK pattern 3 order, used during pixel mixing mode
	[11:9]	X		HBLKALT_PAT4	HBLK pattern 4 order, used during pixel mixing mode
	[14:12]	X		HBLKALT_PAT5	HBLK pattern 5 order, used during pixel mixing mode
	[17:15]	X		HBLKALT_PAT6	HBLK pattern 6 order, used during pixel mixing mode
	[19:18]	X		HBLK_MODE	HBLK mode selection 0 = normal HBLK 1 = pixel mixing mode 2 = special pixel mixing mode 3 = not used
	[20]	X		TESTMODE	Test operation only; set to 0
	[27:21]	X		Unused	Set unused bits = 0
0x09	[12:0]	X	SCP	HBLKLEN	HBLK length in HBLK alteration modes
	[20:13]	X		HBLKREP	Number of HBLK repetitions in HBLK alternation modes
	[21]	X		HBLKMASK_H1	Masking polarity for H1/H3 during HBLK
	[22]	X		HBLKMASK_H2	Masking polarity for H2/H4 during HBLK
	[23]	X		HBLKMASK_HL	Masking polarity for HL during HBLK
	[27:24]	X		Unused	Set unused bits = 0
0x0A	[12:0]	X	SCP	HBLKSTART	HBLK start position used in pixel mixing modes
	[25:13]	X		HBLKEND	HBLK end position used in pixel mixing modes
	[27:26]	X		Unused	Set unused bits = 0
0x0B	[27:0]	X	SCP	TESTMODE	Test operation only; set to 0
0x0C	[12:0]	X	SCP	CLPOB0_TOG1	CLPOB0 toggle Position 1
	[25:13]	X		CLPOB0_TOG2	CLPOB0 toggle Position 2
	[27:26]	X		Unused	Set unused bits = 0
0x0D	[12:0]	X	SCP	CLPOB1_TOG1	CLPOB1 toggle Position 1
	[25:13]	X		CLPOB1_TOG2	CLPOB1 toggle Position 2
	[27:26]	X		Unused	Set unused bits = 0
0x0E	[12:0]	X	SCP	PBLK0_TOG1	PBLK0 toggle Position 1
	[25:13]	X		PBLK0_TOG2	PBLK0 toggle Position 2
	[27:26]	X		Unused	Set unused bits = 0
0x0F	[12:0]	X	SCP	PBLK1_TOG1	PBLK1 toggle Position 1
	[25:13]	X		PBLK1_TOG2	PBLK1 toggle Position 2
	[27:26]	X		Unused	Set unused bits = 0

Table 32. Field Registers

Address	Data Bits	Default Value	Update	Name	Description
0x00	[12:0]	X	VD	SCP0	Sequence change Position 0
	[25:13]	X		SCP1	Sequence change Position 1
	[27:26]	X		Unused	Set unused bits = 0
0x01	[12:0]	X	VD	SCP2	Sequence change Position 2
	[25:13]	X		SCP3	Sequence change Position 3
	[27:26]	X		Unused	Set unused bits = 0
0x02	[12:0]	X	VD	SCP4	Sequence change Position 4
	[25:13]	X		SCP5	Sequence change Position 5
	[27:26]	X		Unused	Set unused bits = 0
0x03	[12:0]	X	VD	SCP6	Sequence change Position 6
	[25:13]	X		SCP7	Sequence change Position 7
	[27:26]	X		Unused	Set unused bits = 0

Address	Data Bits	Default Value	Update	Name	Description
0x04	[12:0]	X	VD	SCP8	Sequence change Position 8
	[27:13]			Unused	Set unused bits = 0.
0x05	[4:0]	X	VD	HPAT_SEL0	Selected H-Pattern for 1st region in field
	[9:5]	X		HPAT_SEL1	Selected H-Pattern for 2nd region in field
	[14:10]	X		HPAT_SEL2	Selected H-Pattern for 3rdt region in field
	[19:15]	X		HPAT_SEL3	Selected H-Pattern for 4th region in field
	[24:20]	X		HPAT_SEL4	Selected H-Pattern for 5th region in field
	[27:25]	X		Unused	Set unused bits = 0
0x06	[4:0]	X	VD	HPAT_SEL5	Selected H-Pattern for 6th region in field
	[9:5]	X		HPAT_SEL6	Selected H-Pattern for 7th region in field
	[14:10]	X		HPAT_SEL7	Selected H-Pattern for 8th Region in field
	[19:15]	X		HPAT_SEL8	Selected H-Pattern for 9th region in field
	[27:20]	X		Unused	Set unused bits = 0
0x07	[27:0]	X	VD	Unused	Set unused bits to 0
0x08	[8:0]	X	VD	CLPOB_POL	CLPOB start polarity settings
	[17:9]		X	CLPOB_PAT	CLPOB Pattern Selector 0 = CLPOB0_TOG registers are used 1 = CLPOB1_TOG registers are used
	[27:18]		X	Unused	Set unused bits = 0
0x09	[12:0]	X	VD	CLPOBMASKSTART1	CLPOB Mask 1 start position
	[25:13]	X		CLPOBMASKEND1	CLPOB Mask 1 end position
	[27:26]			Unused	Set unused bits = 0
0x0A	[12:0]	X	VD	CLPOBMASKSTART2	CLPOB Mask 2 start position
	[25:13]	X		CLPOBMASKEND2	CLPOB Mask 2 end position
	[27:26]	X		Unused	Set unused bits = 0
0x0B	[12:0]	X	VD	CLPOBMASKSTART3	CLPOB Mask 3 start position
	[25:13]	X		CLPOBMASKEND3	CLPOB Mask 3 end position
	[27:26]	X		Unused	Set unused bits = 0
0x0C	[8:0]	X	VD	PBLK_POL	PBLK start polarity settings for sequences 0 to 8
	[17:9]	X		PBLK_PAT	PBLK pattern selector 0 = PBLK0_TOG registers are used 1 = PBLK1_TOG registers are used
	[27:18]	X		Unused	Set unused bits = 0
0x0D	[12:0]	X	VD	PBLKMASKSTART1	PBLK Mask region 1 start position
	[25:13]	X		PBLKMASKEND1	PBLK Mask region 1 end position
	[27:26]	X		Unused	Set unused bits = 0
0x0E	[12:0]	X	VD	PBLKMASKSTART2	PBLK Mask region 2 start position
	[25:13]	X		PBLKMASKEND2	PBLK Mask region 2 end position
	[27:26]	X		Unused	Set unused bits = 0
0x0F	[12:0]	X	VD	PBLKMASKSTART3	PBLK Mask region 3 start position
	[25:13]	X		PBLKMASKEND3	PBLK Mask region 3 end position
	[27:26]	X		Unused	Set unused bits = 0

OUTLINE DIMENSIONS

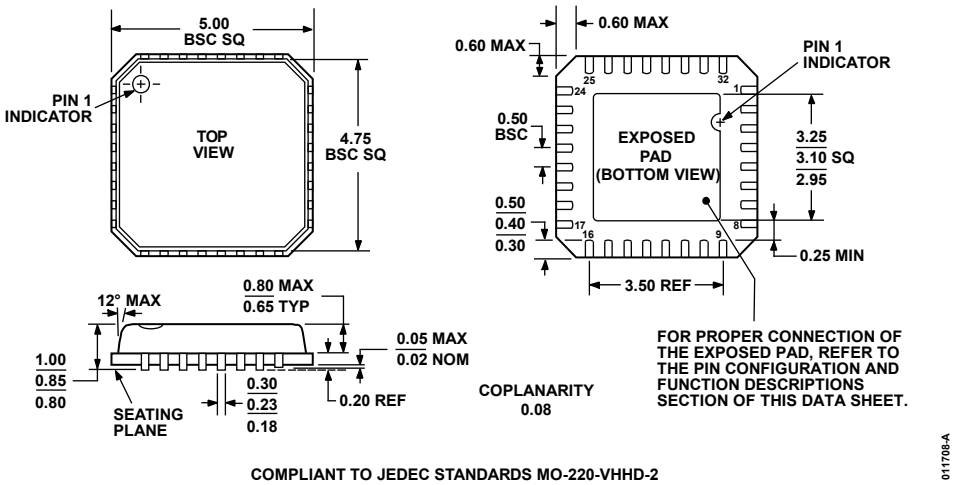


Figure 69. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9970BCPZ[1]	−25°C to +85°C	32-Lead LFCSP_VQ	CP-32-2
AD9970BCPZRL[1]	−25°C to +85°C	32-Lead LFCSP_VQ	CP-32-2
AD9970BCPZRL7[1]	−25°C to +85°C	32-Lead LFCSP_VQ	CP-32-2

[1] Z = RoHS Compliant Part.

D05770-0-8/09(SpB)