ON Semiconductor CMOS IMAGE SENSORS	**Application Note** **Product: VITA Family** **VITA Family Behavioral Model**	Date: Jan 2013 Issue: rev. 4 Page: 1/9

CONTENTS

INTRODUCTION

The VITA model is a VHDL behavioral model. The main objective of this model is to demonstrate the output format and protocol. Upon loading, the model reads an image from file (ppm ASCII format). The model is controlled through its SPI interface. The readout timing is mimicked and the image is transmitted through the LVDS or CMOS interface. The main operation modes, influencing the output protocol, are supported (rolling shutter, global shutter with one or multiple windows, subsampling, etc.).

The primordial purpose of the model is to demonstrate the sensor's interface and frame formatting protocol. The internal latency and timing specifications are not accurate. Additionally, the effect of integration and gain configurations are not modeled.

DIRECTORY STRUCTURE

${MODEL_ROOT} is used in the remainder of the document to denote the path of the directory in which the model has been decompressed. The following directory structure is used:

TABLE 1 DIRECTORY STRUCTURE

Directory	Description
`${MODEL_ROOT}/src/`	Contains the model's source files (VHDL)
`${MODEL_ROOT}/tb/`	Contains example testbenches, instantiating the model's toplevel
`${MODEL_ROOT}/doc/`	Contains this document

TOPLEVEL ENTITY, CONFIGURATION AND LIBRARY

TABLE 2 MODEL ENTITY AND CONFIGURATION NAMES

Entity	VHDL Configuration	Description
noiv1sn1300a	cfg_noiv1sn1300a_model	VITA1300 Model, LVDS Outputs
noiv2sn1300a	cfg_noiv2sn1300a_model	VITA1300 Model, CMOS Outputs
noiv1sn2000a	cfg_noiv1sn2000a_model	VITA2000 Model, LVDS Outputs
noiv2sn2000a	cfg_noiv2sn2000a_model	VITA2000 Model, CMOS Outputs
noiv1sn5000a	cfg_noiv1sn5000a_model	VITA5000 Model, LVDS Outputs
noiv1sn025ka	cfg_noiv1sn025ka_model	VITA25k Model, LVDS Ouputs

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COMPILATION ORDER

The model is written in VHDL-93 and needs to be compiled into different libraries. The compilation order, together with the target libraries is shown below.

```
lib_vita_hdl   ${MODEL_ROOT}/src/pck_vita_model.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/pck_vita_seq.vhd
lib_model      ${MODEL_ROOT}/src/pck_frame_format.vhd
lib_model      ${MODEL_ROOT}/src/pck_calc.vhd
lib_model      ${MODEL_ROOT}/src/pck_file_io.vhd
lib_model      ${MODEL_ROOT}/src/pck_ppm.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/pck_vita_spi.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/vita_imc.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/vita_spi.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/vita_io.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/vita_pll.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/vita_mux.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/vita_rgen.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/vita_adc.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/vita_seq.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/vita_db_sync.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/pck_crc.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/vita_db_data.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/vita_db.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/vita_clkgen.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/vita_ser_channel.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/vita_ser_par_mux.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/vita_ser.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/vita.vhd
```

Sensor Specific Compilation (select the file corresponding to the desired VITA model):

```
lib_vita_hdl   ${MODEL_ROOT}/src/noiv1sn1300a.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/noiv2sn1300a.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/noiv1sn2000a.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/noiv2sn2000a.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/noiv1sn5000a.vhd
lib_vita_hdl   ${MODEL_ROOT}/src/noiv1sn25ka.vhd
```


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IMAGE FILES

The VITA model uses a ppm format input file, which is an uncompressed ASCII format.

The name of the model's input file is defined by means of the generic *G_IMG_NAME*. The default name is *input.ppm* and the file shall be searched for in the directory from which the simulator is invoked.

Note that the value of generics can be redefined when invoking the simulator. Note that *G_IMG_NAME* contains the image file name, without the extension (.ppm). Optionally a path can be included in the file name.

The size of the image file must correspond with the resolution of the sensor model. The following table lists the required resolution for each model.

TABLE 3 MODEL IMAGE RESOLUTION

Model	y-resolution [pixels]	x-resolution [pixels]
noiv1sn1300a noiv2sn1300a	1024	1280
noiv1sn2000a noiv2sn2000a	1200	1920
noiv1sn5000a	2048	2592
noiv1sn25ka	5120	5120

PPM File Format

A ppm file contains a three lines header, followed by the pixel values in decimal numbers (0-255). The header contains the following information:

TABLE 4 PPM FILE HEADER

Line Number	Description	Example
1	File type (e.g. *P2*)	P2
2	Resolution	1280 1024
3	Maximum pixel value Only 255 is supported by the model – this is upscaled to 10-bit as needed.	255

Each pixel of a monochrome image is represented by one 8-bit integer value. Color pixels are represented by three 8-bit values (Red, Green, Blue). The sensor model supports both monochrome and color images and the selection is made by means of the generic G_COLOR (false = monochrome, true = color). This generic has to be set according to the image file format used (default configuration is monochrome).

Note: Some editors add comment lines (i.e. lines starting with the '#' symbol). Comment lines are not supported by the model's parser. Make sure to remove these lines before starting a simulation.

EXAMPLE TESTBENCHES

Testbenches and test cases are included as example in the tb directory. The sensor uploads correspond to the datasheet's values, except for the 'Required Uploads', which are not required for the the model and have been omitted in the example test scenario.

The example test case configures the model for readout of multiple windows in global shutter mode.

In order to simulate the model with the provided examples, one need to compile the following files in the mentioned library, in addition to the model's source).

```
lib_tb_vita_hdl   ${MODEL_ROOT}/tb/src/pck_spi_upload_model.vhd
lib_tb_vita_hdl   ${MODEL_ROOT}/tb/src/pck_tb_vita_model.vhd
lib_tb_vita_hdl   ${MODEL_ROOT}/tb/src/spi_upload_model.vhd

lib_tb_vita_hdl   ${MODEL_ROOT}/tb/noivXsnYYYYa/src/tb_noivXsnYYYYa.vhd
lib_tb_vita_tc    ${MODEL_ROOT}/tb/noivXsnYYYYa/tests/test001/stimuli.vhd
```

Note: Replace X and YYYY with the corresponding values for the desired model.

Simulation can be started for the by loading the following configuration in the simulator:

```
lib_tb_vita.hdl.cfg_tb_noivXsnYYYYa_model
```


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SUPPORTED FUNCTIONALITY AND LIMITATIONS

Supported:

- SPI read/write with defaults
- Rolling Shutter Mode – 1 window inclusive black and dummy line generation
- Global Shutter Mode – multiple windows, ev. overlapping, inclusive black line generation
- Triggered Global Shutter
- Subsampled and Binned Readout
- Monochrome and Color readout
- Black Level: set to target level, no auto black level calibration
- 10 bit and 8 bit mode
- Testpattern generation (fixed, incremental, PRBS)
- PLL: basic model regenerating a clock with 5x/4x input clock frequency (no modeling of jitter, startup effects,..)
- Output Format and Protocol
- LVDS Output Mode
- CMOS Output Mode

Limitations:

The following features are not modeled, or modeled with the described limitations.

- Integration Time Control. Integration time can be set, but has no impact on the image data sent out.
- Gains
- AEC
- Black Level Calibration: black level is set to target level, no automatic black level calibration
- Datapath latency (i.e. latency of trigger/sequencer enable to image out)

- FOT/ROT/line duration: these may deviate from the recommended sensor configuration
- Electro-Optical Artifacts
- Startup Requirements/Upload Sequence: No explicit check
- PLL/Bias/Drivers/… Startup behaviour and transient effects
- Monitor Outputs

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HISTORY

TABLE 5 HISTORY

Version	Date	Description
0	October 2011	First draft of noiv1sn1300a model
1	October 2011	Removed monitor2 pin from toplevel wrapper Created noiv1sn2000a (VITA2000) wrapper
2	October 2011	Remodeled PLL such that frequencies < 62 MHz can be used PLL clock is derived from input clock instead of generating fixed frequency clock Corrected 8 bit operation mode
3	December 2012	Added subsampling and binning modes Added error checking and reporting when ROIs are configured incorrectly Corrected SPI readout Updated PLL for faster lock generation (independent of reset to enable time) Added CMOS output variants of VITA1300/2000 (noiv2sn1300a, noiv2sn2000a) Created VITA5000 model (noiv1sn5000a) Created VITA25k model (noiv1sn25ka) Added support for color images (G_COLOR = true) Reformatted manual/readme
4	January 2013	Corrected length of FOT Added Global Shutter Master Mode Modeled the influence of exposure configurations on frame length (no modeling on image luminance)

PUBLICATION ORDERING INFORMATION

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