Bahir Dar Institute of technology

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Department of Computer Engineering

MSc in Computer Engineering

Advanced VLSI Project On: Digital filter design

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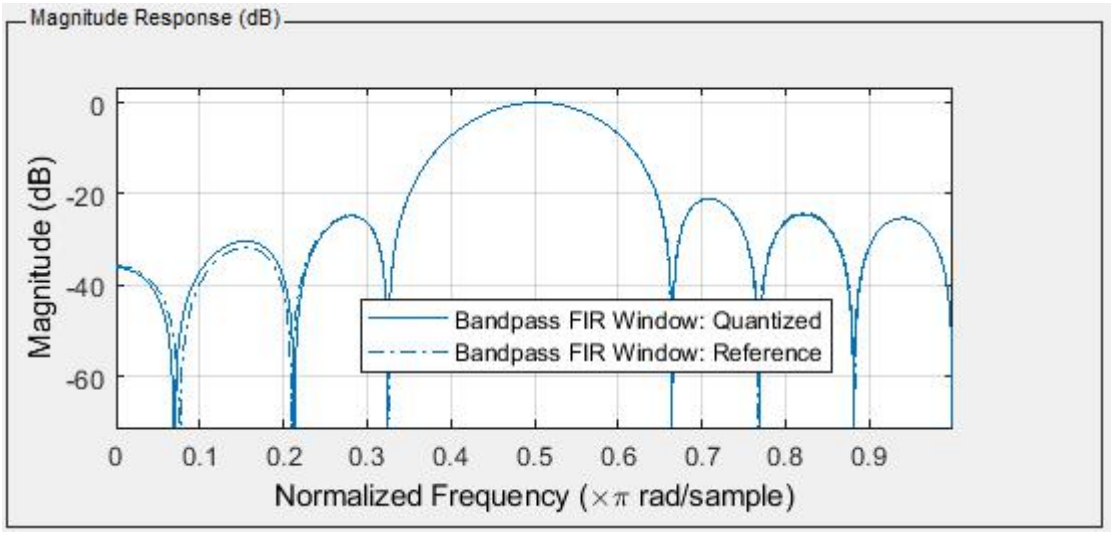
VHDL based Band pass FIR Design

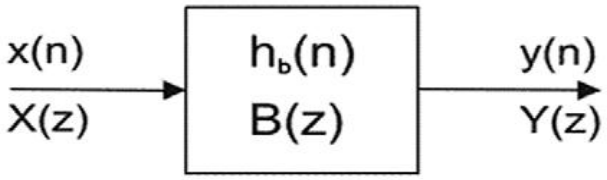
1. Filter Specifications: -

- ✓ FIR impulse response
- ✓ 15 order and single rated filter
- ✓ Its cutoff frequencies are f1=0.4 and f2=0.6
- ✓ It is fixed point Arithmetic filter
- ✓ floor rounding mode and saturated overflow
- ✓ 8-bit input signal word length.
- ✓ 8-bit word length 16 coefficients
- ✓ 16-bit product word length
- ✓ 18-bit accumulator word length
- ✓ 16-bit output word length
- ✓ 16 multiplier
- ✓ Window design method
- ✓ Filter internal specified precision
- ✓ Direct-Form structure
- ✓ Fully parallel architecture
- ✓ Folding factor – 1
- ✓ Internal coefficient source
- ✓ Linear filter adder style
- ✓ Asynchronous reset type
- ✓ Active high reset asserted level
- ✓ Reset remove form – none
- ✓ Real input complexity
- ✓ Magnitude constraint - unconstraint

2. The filter design structure



FIR filters also known as non-recursive digital filters have a finite impulse response because after a finite time the response of FIR filter settles to zero.



The basic structure of FIR filter consists of adders, multipliers and delay elements as shown below.

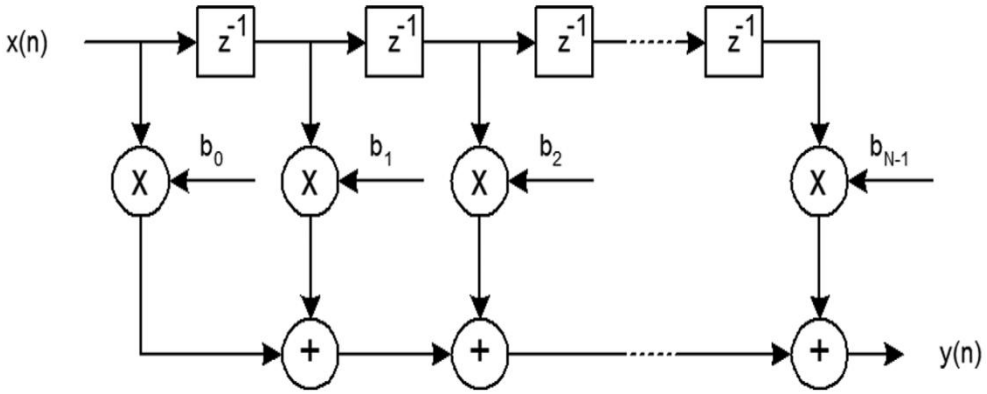


fig: FIR basic operation

Single rate FIR filter -The basic FIR filter core is single rate in which the input and output sample rates are the same. It is the simpler of filter types and is the default in the start of parameter in the core generator software.

The order of the filter determines the number of coefficients. And the higher the order of filter the better is to remove signal noise.

The main advantages of the FIR filter design over their IIR equivalents are:

- ✓ FIR filters with exactly linear phase can easily be designed.
- ✓ There exist computationally efficient realizations for implementing FIR filters.
- ✓ FIR filters realized non-recursively are inherently stable and free of limit cycle oscillations when implemented on a finite-word length digital system.
- ✓ Excellent design methods are available for various kinds of FIR filters with arbitrary specifications.
- ✓ Design and noise issues are less complex than IIR filter.

3. Design stages of digital filters

Filter designing and analysis tool (FDATool) is used for designing the digital filters. It is a powerful user interface for scheming and analyzing the filter's behavior quickly in signal processing. It is used to realize quantized direct-form FIR filters,

Design of a digital filter involves the following five steps:

- ✓ Filter specification
- ✓ Filter coefficient calculation
- ✓ Realization
- ✓ Analysis of finite word length effect and
- ✓ Implementation.

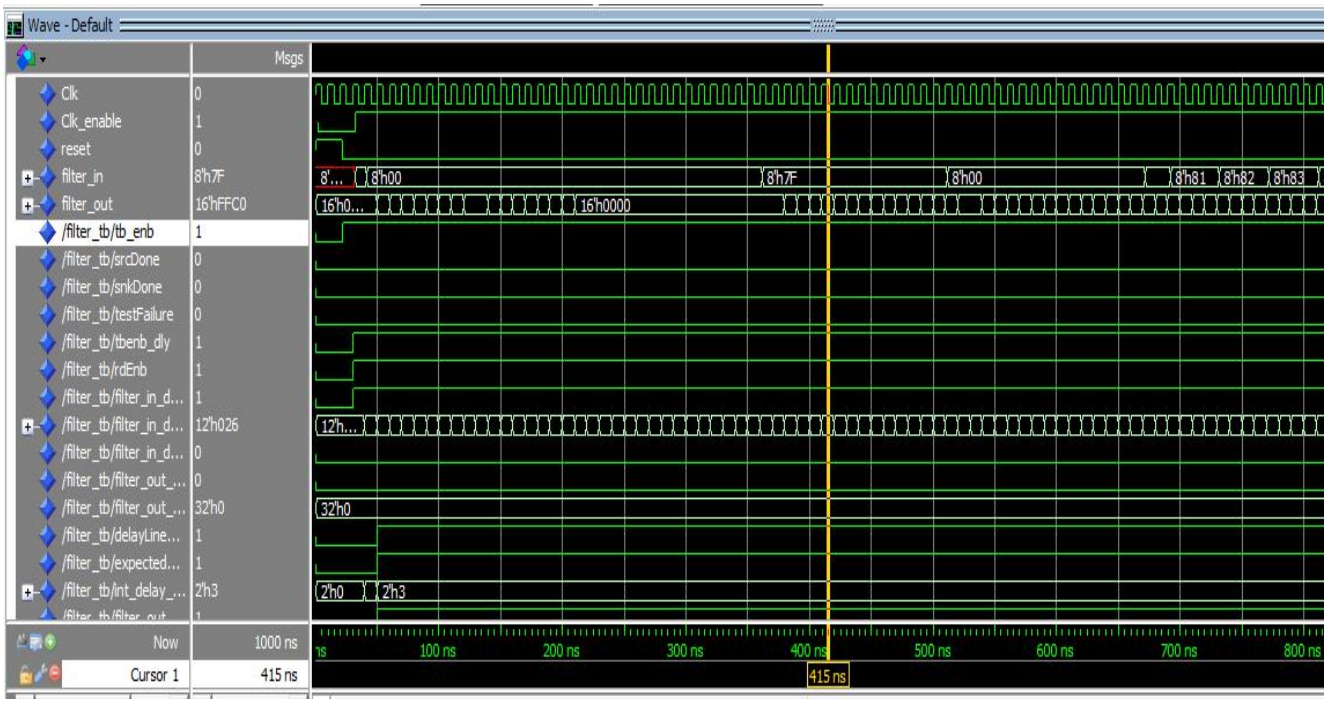
4. Hardware realization

To minimize the hardware implementation cost. For this, the effects of quantization by varying the number of quantization bits. A 15th-order band pass filter using Kaiser window is realized as fixed point precision. it is analyzed that the Kaiser window is more reliable and result in high gain. Generally, the width of the main-lobe determines the transition bandwidth, while the relative heights of the side-lobes control the size of the ripples in the amplitude response. There is abargain between main-lobe width and a height of side-lobe

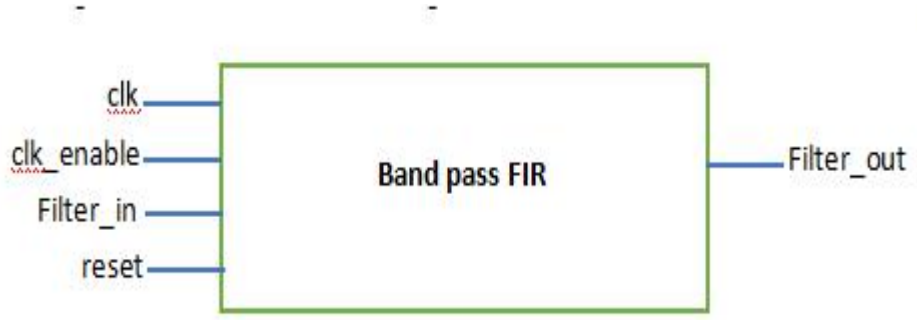
Filter Specifications	
Parameters	**Values**
filter type	band pass
design method	FIR window (β = 0.5 for Kaiser window)
filter order	15
Lower cut off frequency 1	0.4
Lower cut off frequency 2	0.6

5. Simulation

The input output wave form of our filter for the above specification done on MODELSIM from generated HDL test bench. If reset = 1, the filter_out becomes zero and waits until clock enable to be active.



Top module of 15-order band pass filter.



The Coefficients exported from matlab used in our design are:

```
>> Num

Num =

  Columns 1 through 12

    0.0352   -0.0527   -0.0703    0.0859    0.1016   -0.1133   -0.1211    0.1270    0.1270   -0.1211   -0.1133    0.1016

  Columns 13 through 16

    0.0859   -0.0703   -0.0527    0.0352

fx >>
```

We try to test a band pass filter of order 15 almost closer to our mode1 by giving some input signal with noise and plot the two signals together on MATLAB.

```
 t=0:0.1:20;
 s= sin(2*pi*0.25*t);
 n=0.5*randn(size(t));
 x=s + n;
d=designfilt('bandpassfir','Filterorder',15,'cutofffrequency1',
0.4,'cutofffrequency2',0.6,'sampleRate',100);
y=filter(d,x);
plot(x);hold on; plot(y);
```

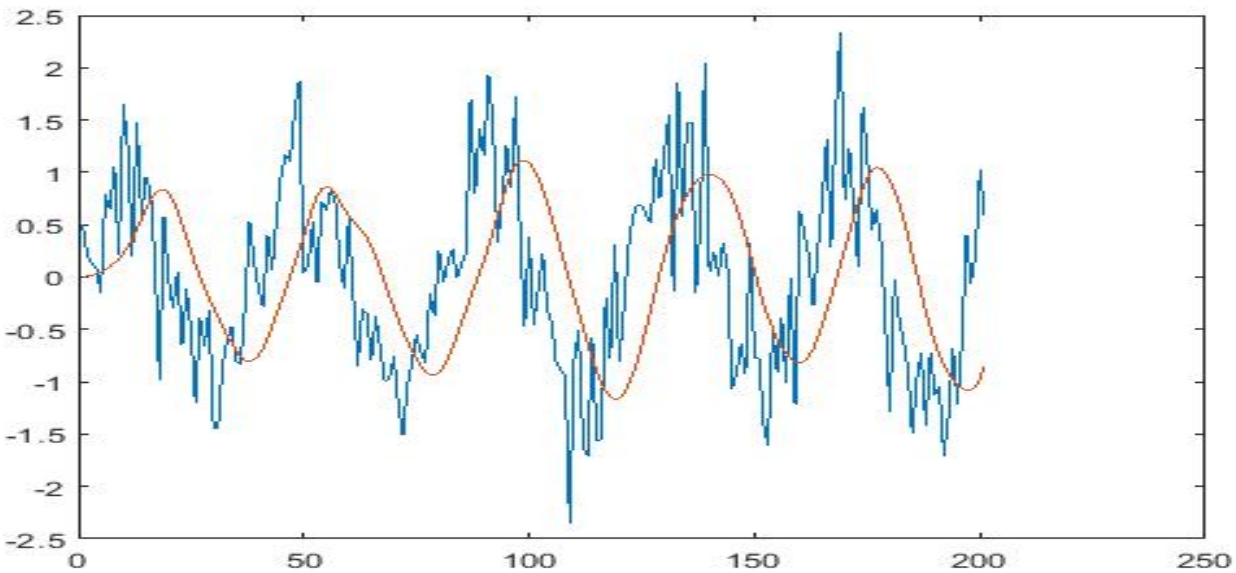


fig:sample band pass filter operation

We have tested our filter to look at its effectiveness after exporting from fdatool and giving it a signal with noise. The we get tangible result indeed as the figure below. The red signal represents after being filtered.

```
t=0:0.1:20;
s= sin(2*pi*0.25*t);
n=0.5*randn(size(t));
x=s + n;
y=filter(Num,1,x);
plot(x);hold on; plot(y);
d=getFilter;
yd=filter(d,x);
plot(t,y,t,yd);
```

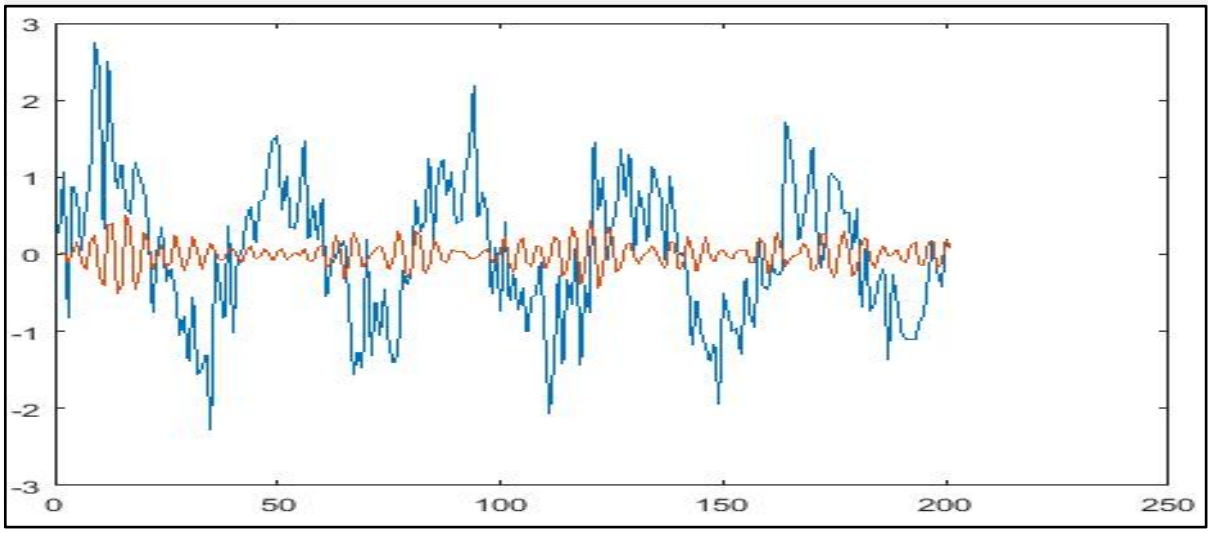


fig : removal of the jitters.

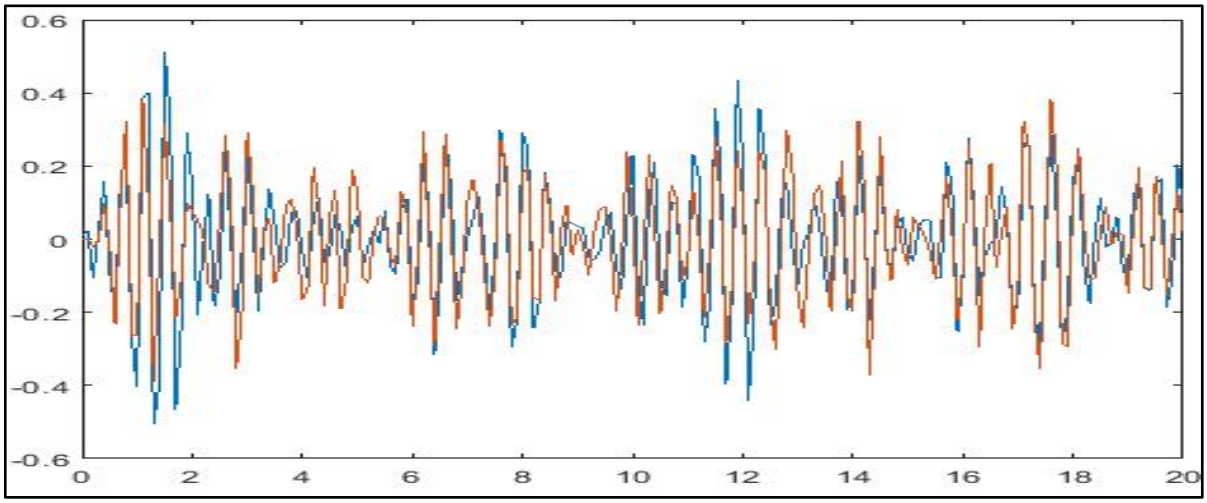


Fig: filtered signal.

The Input and Output Waveform of Simulation

We have used XPAT tools a graphical pattern viewer in alliance. It loads a pattern file (PAT file format) and displays wave forms on a graphical window.

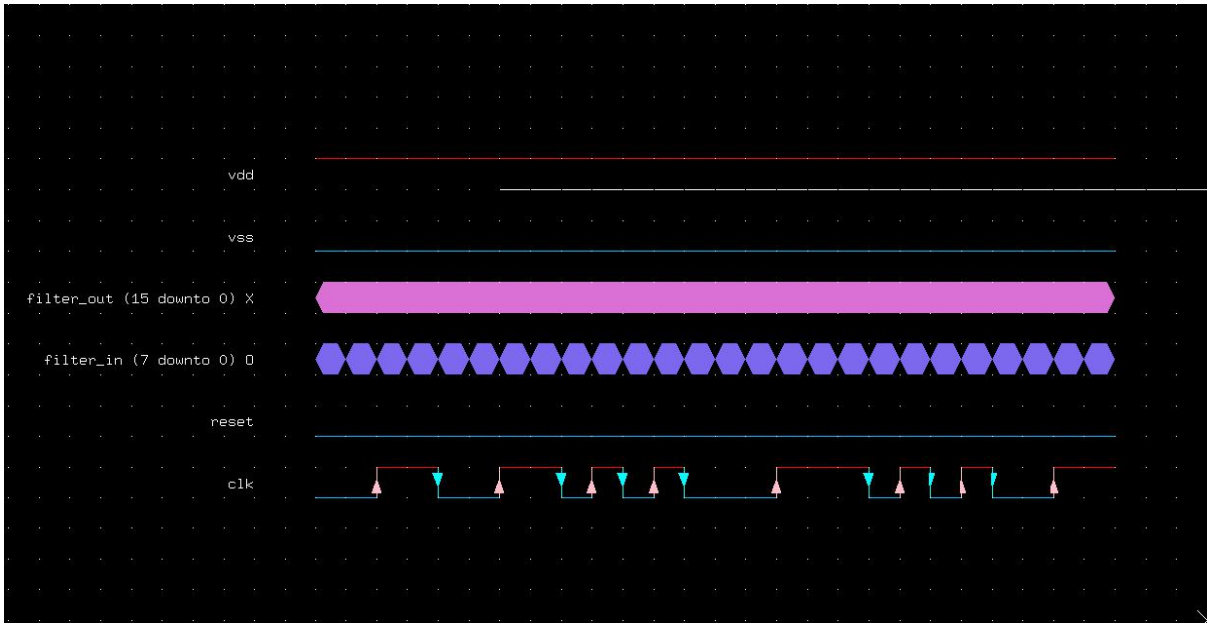


fig: input output wave form of simulation

6. Synthesis

We have verifying and simulate the behavior using alliance tools ,the filter's VHDL code is synthesized into a gate level netlist and represents a new structural VHDL schematic.to generate the filter top module.in Alliance we have use the following tools 'boom','boog'

```
--> Optimization parameters
    Algorithm : simulated annealing
    Keep aux  : no
    Area      : 100 %
    Delay     :   0 %
    Level     :   0

--> Initial cost
    Surface   : 13432000
    Depth     : 51
    Literals  : 11176

--> Translate Abl to Bdd
    Total Bdd nodes 6041

--> Optimization % 100

--> Final cost
    Surface   : 4258250
    Depth     : 32
    Literals  : 3001

--> Post treat figure filter

--> Drive BEH file filter_o
```

fig:optimized parameters

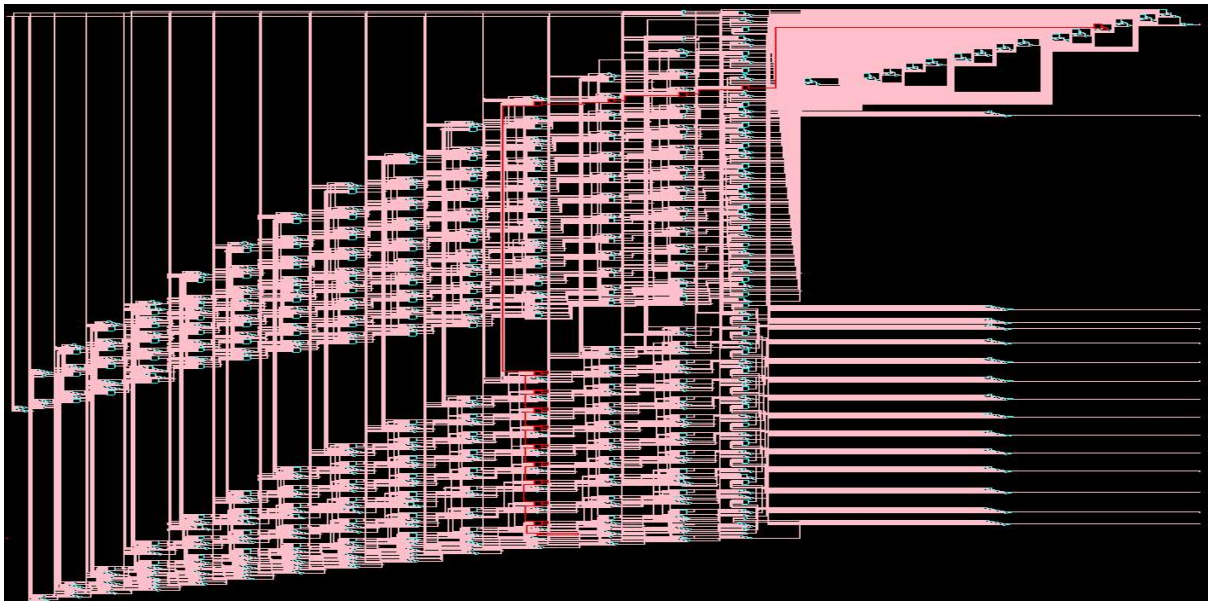


fig : schematic diagram of boolean optimization

Second step of synthesis BOOG is used for the second step of the synthesis process.The report of the design can also be generated using the Boog tool that containing information about the total no. of gates of the filters.

```
Quick estimated critical path (no warranty)...9087 ps from 'product16 0' to 'add_temp_14 15'
Quick estimated area (with over-cell routing)...5682000 lambda◆
Details...
        sff1_x4: 866
        xr2_x1: 515
        oa2ao222_x2: 210
        oa2a22_x2: 20
        buf_x2: 16
        a2_x2: 15
        na2_x1: 10
        no2_x1: 10
        zero_x0: 1
        one_x0: 1
        Total: 1664
Saving critical path in xsch color file 'filter_o.xsc'...
End of boog...
```

fig:generated report of the designed filter

Last step of synthesis Just as BOOG tool, the LOON tool is applied once for each module. loon's file types are very similar to boog's file, but includes some cell buffer types to improve the critical delay paths due to fan-out problems. LOON computes the critical path and performs a gate re powering to decrease its delay and global capacitance.The number of gates used in the system are 1664.

```
Details...
        sff1_x4: 866 (68%)
        xr2_x1: 515 (20%)
        oa2ao222_x2: 210 (9%)
        oa2a22_x2: 20 (0%)
        buf_x2: 16 (0%)
        a2_x2: 15 (0%)
        na2_x1: 10 (0%)
        no2_x1: 10 (0%)
        zero_x0: 1 (0%)
        one_x0: 1 (0%)
        Total: 1664
```

fig:optimized net list

physical implementation of the design: Once the circuit netlist has been captured and validated, each leaf of the hierarchy has to be physically implemented. netlist and a placement. physical symbolic layout file with physical connectors and placed cells. now ready to take our design into the layout phase in the design process, The placement system is based on simulated annealing.

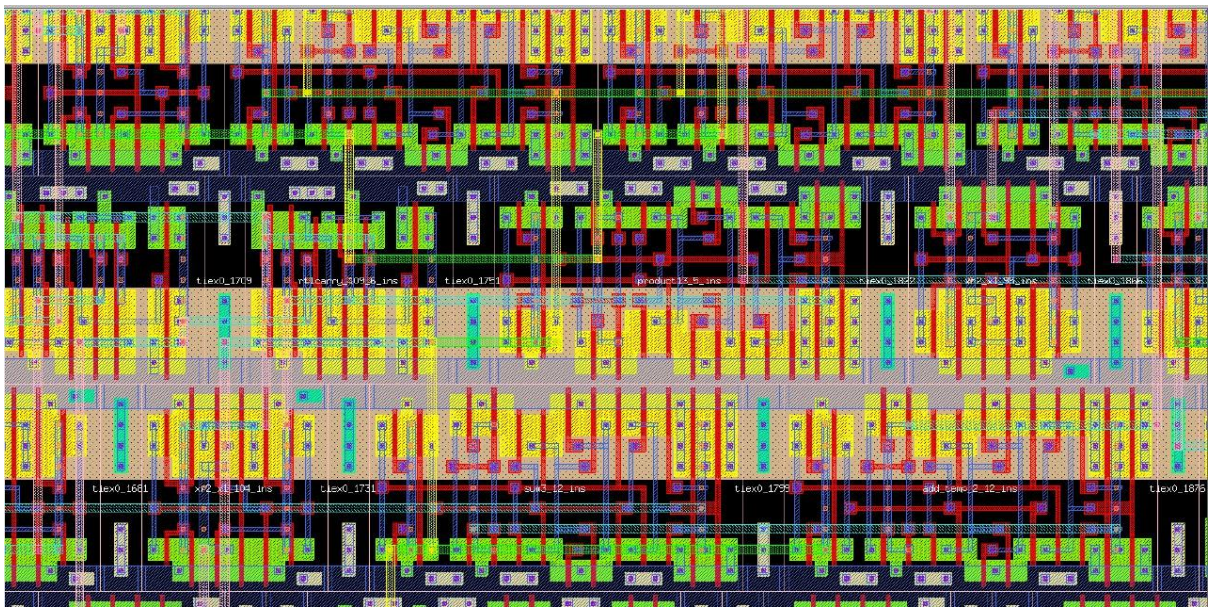


fig:Physical Layaout

Mechanisms to improve performance of the system.

Choosing appropriate specifications results better performance than ever before. The filter word length and size of filter order have valuable effect on FIR performance. And the kaiser window method found to be the best and easiest model than other common structures . The use of the appropriate quantization scheme can result in a reduction in the arithmetic complexity of FIR filtering to thus minimizing the FIR filter area and hardware resources. Many common hardware optimization techniques such as coefficient representation in canonic signed digit (CSD) or minimum sign digit (MSD) and common sub expression Elimination (CSE) techniques can also be used in further reduction in hardware resources and ADC converter can be interfaced within the design (ASIC).