# milling machine

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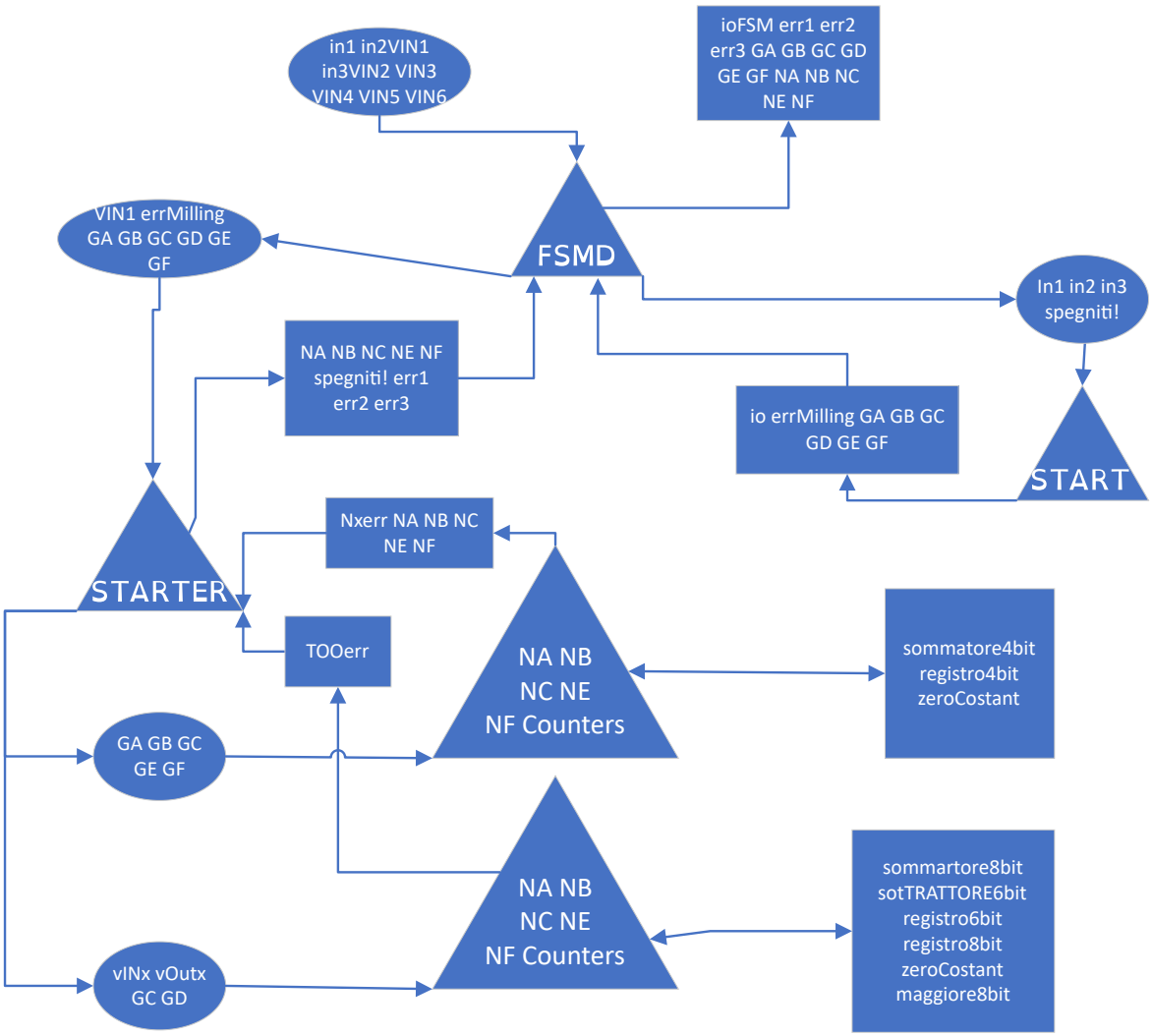
**read README.blif first**

The implementation of the machine control system had required five states, two of them are for the starting point of the machine and other three for each section. When turned on the machine require three consecutive bit T taken to the FSM, which will respond with the correct gates opening. The data path analyzes gates to open the correct registers. On overflow error registers will reset. from the second cycle and on, the first state will require only one T bit to proceed (the 5th state).

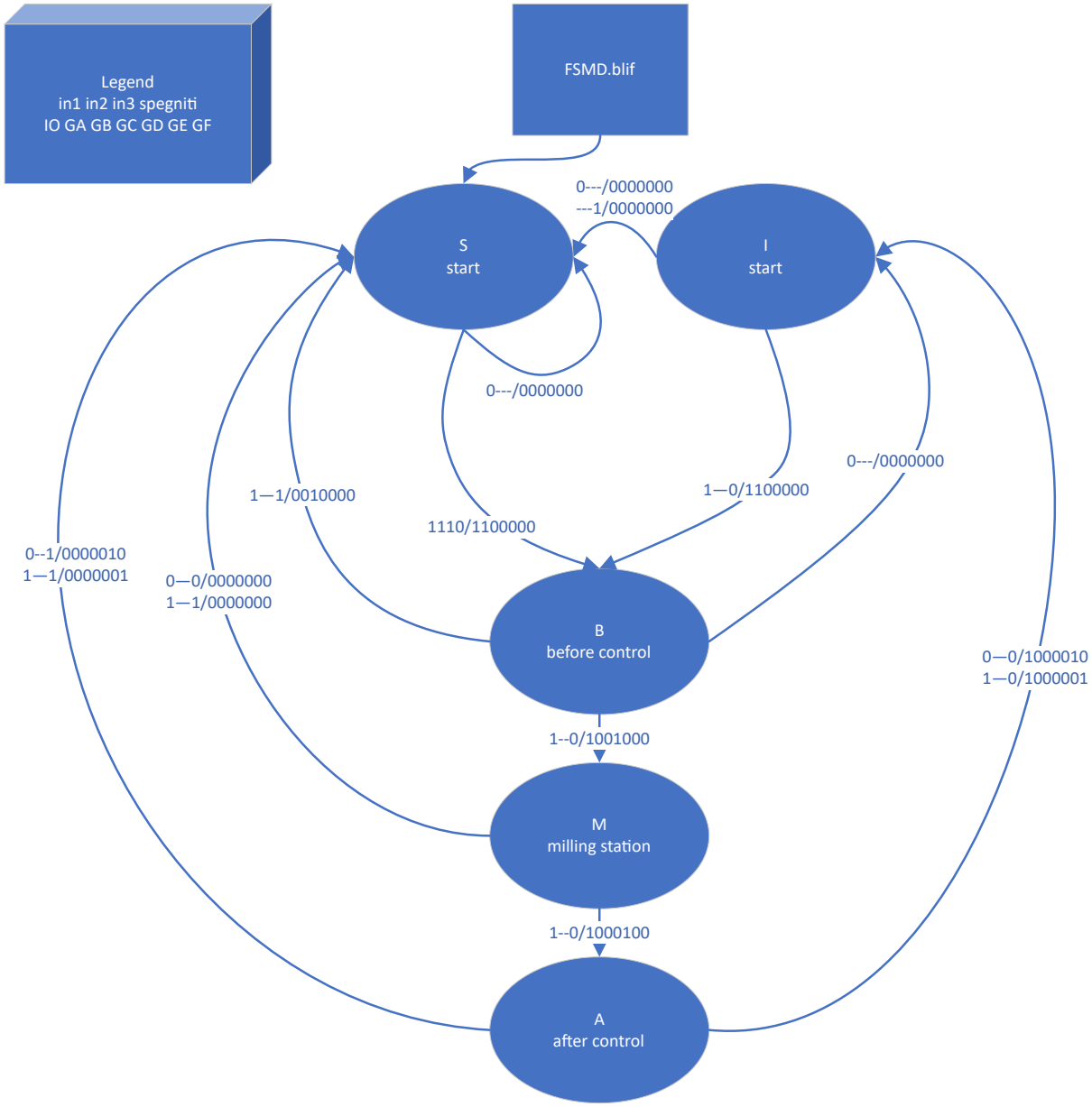


## Here the stg:

FSM is composed of 5 states: S / I,B,M,A. Each of them represents different switch-on / off states.

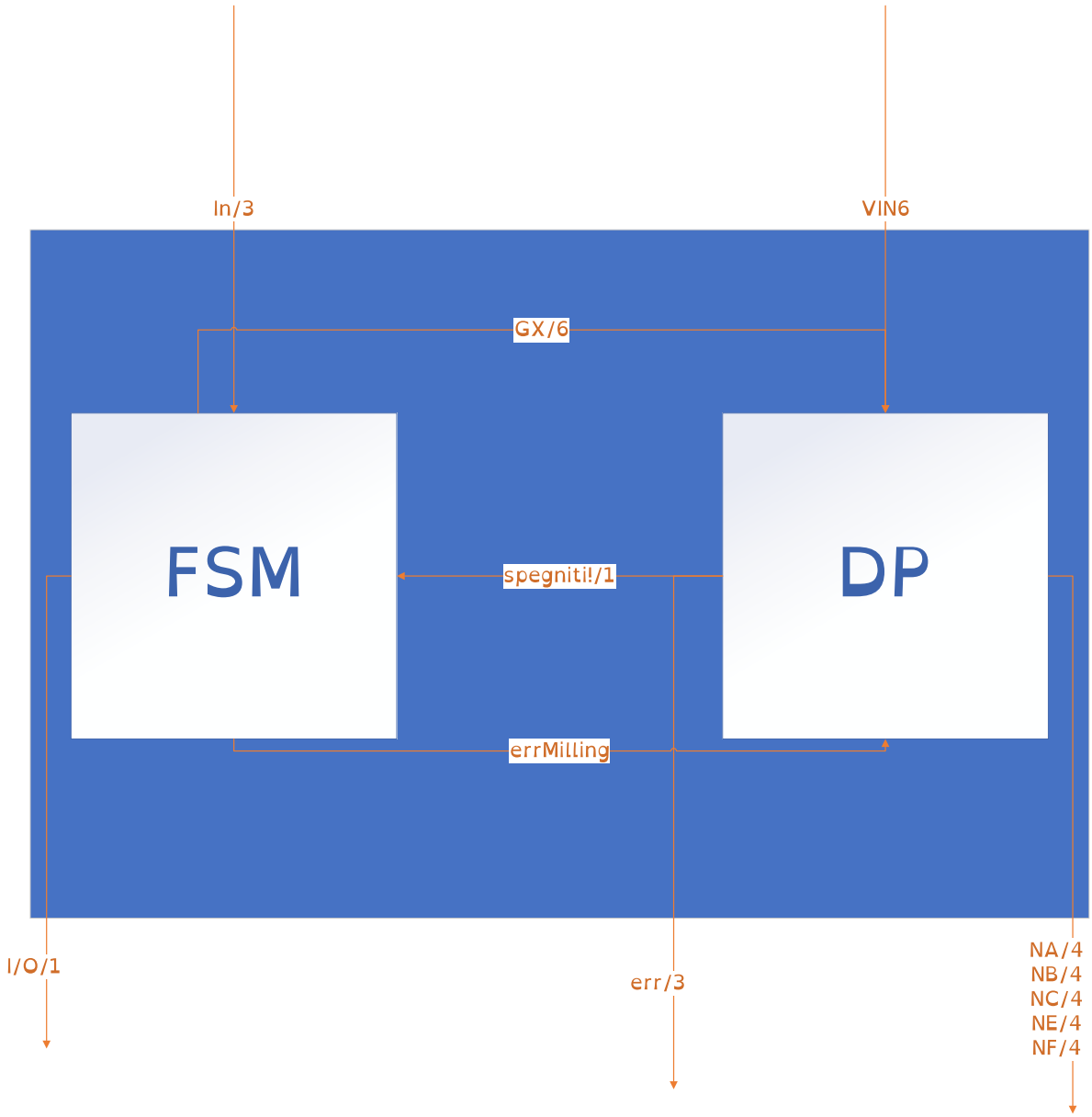
```
inputs: in1 in2VIN1 in3VIN2 VIN3 VIN4 VIN5 VIN6
outputs: ioFSM err1 err2 err3 GA GB GC GD GE GF NA1 NA2 NA3 NA4 NB1 NB2 NB3 NB4 NC1 NC2 NC3 NC3 NC4 NE1
NE2 NE3 NE4 NF1 NF2 NF3 NF4.
```

Following a flow chart of each file with relative variables between them:




## FSMD:

The system is divided into FSM (finite state machine) and DP (Data path).
The FSM acquires the signals to shut down the machine on errors, and the first three inputs bits; it takes care of switching the machines on and off and what decide what to do with inputs and gates.
The DP takes the current state throw opened gate. It takes directly load bits and arrange counters.




**statistiche generali dell'ottimizzazione**

| | prima | dopo |
|---|---|---|
| input | 7 | 7 |
| outputs | 30 | 30 |
| nodes | 164 | 164 |
| latch | 37 | 37 |
| lits (sop) | 681 | 362 |
| gates | 9056 | 8896 |
| ritardo | 38.00 | 35.40 |