One hour

Special instructions:

- You are expected to complete the exam independently and not confer with anyone during the examination.
- You must not make copies of any of the questions (either written or screenshot)
- You must not share the details of this assessment with anyone
- You must not approach or ask anyone for support with this assessment
- The answers you provide must be your own work and by submitting your answers you are confirming that it is your own work.
- Remember the University's rules on plagiarism and academic malpractice (see: http://www.regulations.manchester.ac.uk/guidance-to-students-on-plagiarism-and-other-forms-of-academic-malpractice/).
- If you are undertaking a professionally regulated degree programme, you'll also be bound by their code of conduct.

THE UNIVERSITY OF MANCHESTER

Faculty of Science and Engineering

School of Engineering

Department of Electrical and Electronic Engineering

Computer Systems Architecture

Answer **all** questions

Your answers should be handwritten in black and submitted to Blackboard as a single document

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Question 1

(a) A processor uses the 5-stage pipeline architecture presented in the lectures. The pipeline includes interlock and forwarding logic. The processor stores data and instructions in a single memory device and the pipeline accesses this memory through a single memory interface without caches.

(i) Write a short ARMv8 assembly language program to illustrate how a structural hazard can arise in the operation of the pipeline. Show how your program executes using a pipeline diagram, and clearly identify the source of the structural hazard and the action taken by the interlock logic. Use the standard pipeline notation presented in the lectures.

(ii) Write a short ARMv8 assembly language program to illustrate how a data hazard can arise in the operation of the pipeline and how forwarding can minimise the impact of the hazard on performance. Show how your program executes using a pipeline diagram, and clearly identify the source of the data hazard and the action taken by the interlock and forwarding logic. Use the standard pipeline notation presented in the lectures.

[6, 6 marks]

(b) A processor with a Load/Store architecture has 4 general purpose registers, R0, R1, R2 and R3, and instructions with the following formats:

```
LOAD    Ra, X        Ra = [X]
STORE   Ra, X        [X] = Ra
OP      Ra, Rb       Ra = Ra <OP> Rb
```

Question 1 continues over the page.

Question 1 continued.

(i) Derive a sequence of instructions for this processor to implement the high-level language arithmetic statement given below without using any temporary memory locations. Define the function of all arithmetic instructions that you use and include comments to explain the operation of your program.

$Z = (A + B + Z) / (A + Z)$

(iii) Assuming that 6 bits are required to encode an instruction operation (including load and store) and that Load and Store instructions must be capable of addressing all words in a 128 Ki word address space, determine the minimum number of bits required to encode each of the three instruction types.

[8, 5 marks]

[Total 25 marks]

Question 2

(a) The execution times for a set of five benchmark programs executing on two different computer systems are given in the table Q2.1.

The geometric mean of the execution times of the five benchmark programs executing on the benchmarking reference computer system is 1200 s.

	Execution Time (s)	
	Computer System A	Computer System B
Program 1	1000	1500
Program 2	150	200
Program 3	250	400
Program 4	1500	1000
Program 5	1500	200

Table Q2.1

(i) Explain why the geometric mean is frequently used when compiling benchmark metrics.

(ii) Determine the performance ratios (relative to the benchmark computer system) for the two computer systems being evaluated.

[3, 6 marks]

(b) A given embedded processor has a 32-bit address bus and a 16-bit data bus for interfacing to external memory. The external memory is addressed as 16-bit words. The embedded processor contains a 64 KiB 8-way set associative data cache memory with a block size of 512 (16-bit) words.

(i) Determine the number of blocks in the cache memory.

(ii) Determine the number of sets in the cache memory.

Question 2 continues over the page.

Question 2 continued.

(iii) Determine the number of tag bits associated with each cache line.

(iv) Determine the set number and cache tag bits that correspond to the memory address 0xFC1C033F.

(v) Explain the practical reasons why the cache would not be implemented as 64-way set associative.

[2, 3, 3, 4, 4 marks]

[Total 25 marks]

END OF EXAMINATION PAPER