Exam answering time: 1 hour

Technical processing time: 1 hour

Total time available: 2 hours

Special instructions:

- Please refer to the detailed test instructions that were presented on Blackboard before you started this examination.

THE UNIVERSITY OF MANCHESTER

Faculty of Science and Engineering

School of Engineering

Department of Electrical and Electronic Engineering

Computer Systems Architecture

26 May 2021

Time Window 09:00 – 16:00 (UK Time)

Answer **all** questions

Your answers should be handwritten in black and submitted to Blackboard as a single document

Question 1

(a) A computer system executes a signal processing task using instructions from five instruction categories. Table Q1.1 lists the instruction categories, the number of instructions executed from each category, and the average Cycles per Instruction (CPI) for each category.

The computer system operates at a clock frequency of 3.2 GHz.

Category	**Number of Occurrences**	**CPI**
Load	15,000	2
Store	20,000	2
FPADD	4,000	3
FPSUB	6,000	3
FPMUL	10,000	6

Table Q1.1

(i) Determine the overall execution time of the signal processing task.

(ii) Determine the average CPI for execution of the signal processing task.

(iii) What is the maximum speedup factor that could be achieved by optimising the implementation of both the FPADD and FPSUB instructions?

[3, 3, 4 marks]

Question 1 continues over the page.

Question 1 continued.

(b) Presented below is a fragment of an ARMv8 assembly language program. The program is to be executed on a processor using the 5-stage pipeline architecture with interlock logic presented in the lectures. The processor accesses the instruction memory and the data memory through separate memory interfaces.

```
LDUR X5, [X3, #100]

ADD  X2, X5, X6

ORR  X8, X5, X1
```

(i) Draw a pipeline diagram to show how the assembly language program would execute **without** data forwarding. Use the pipeline diagram notation presented in the lectures.

(ii) Draw a pipeline diagram to show how the assembly language program would execute **with** data forwarding. Use the pipeline diagram notation presented in the lectures. Clearly annotate the diagram to show the data forwarding.

(iii) The program fragment is extended as shown below. Demonstrate how the program can be rewritten to avoid pipeline stalls with data forwarding. It is not necessary to draw a pipeline diagram.

```
LDUR X5, [X3, #100]

ADD  X2, X5, X6

ORR  X8, X5, X1

ADD  X4, X6, X6
```

[6, 6, 3 marks]

Total [25 marks]

Question 2

(a) A given embedded processor has a 24-bit address bus and a 16-bit data bus for interfacing to external memory. The external memory is addressed as 16-bit words. The embedded processor contains a 128 KiB direct mapped data cache memory with a block size of 64 (16-bit) words.

(i) Determine the number of blocks in the cache memory.

(ii) Determine the number of tag bits associated with each cache block.

(iii) Determine the cache block ID of the cache block that will hold the main memory location with the address 0x3F2B7E. State your answer in hexadecimal.

(iv) Determine the highest address in the main memory that maps to the cache block with ID = 0x14. State your answer in hexadecimal.

[2, 2, 3, 4 marks]

(b) The high-level language statement below is to be implemented on a zero-address (stack) processor.

A = (A + B + C) × (A + C)

The processor has the following characteristics:

- the stack is implemented in the data memory,
- the read and write access time of the data memory is 50 ns,
- the read access time of the instruction memory is 50 ns, and each instruction requires a single fetch from instruction memory,
- ALU operations execute in 5 ns,
- instruction opcodes are encoded in 8 bits,
- data operands are 32 bits,
- memory addresses are 32 bits.

Question 2 continues over the page.

Question 2 continued.

(i) Derive a sequence of assembly language instructions that implement the high-level language statement on the zero-address processor. Define the operation of all instructions used and include comments to explain the operation of your program by showing the contents of the stack.

(ii) What is the maximum number of bytes required to implement the stack in data memory for this specific program?

(iii) Calculate the execution time of the sequence of instructions.

[7, 2, 5 marks]

Total [25 marks]

END OF EXAMINATION PAPER