



MANGALORE INSTITUTE OF TECHNOLOGY & ENGINEERING

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(A Unit of Rajalaxmi Education Trust®, Mangalore - 575001)

Affiliated to V.T.U., Belagavi, Approved by AICTE, New Delhi.

DEPARTMENT OF ELECTRONICS & COMMUNICATION

ENGINEERING

(Accredited by NBA)

“DESIGN AND IMPLEMENTATION OF 6T SRAM CELL”

Project Associates:

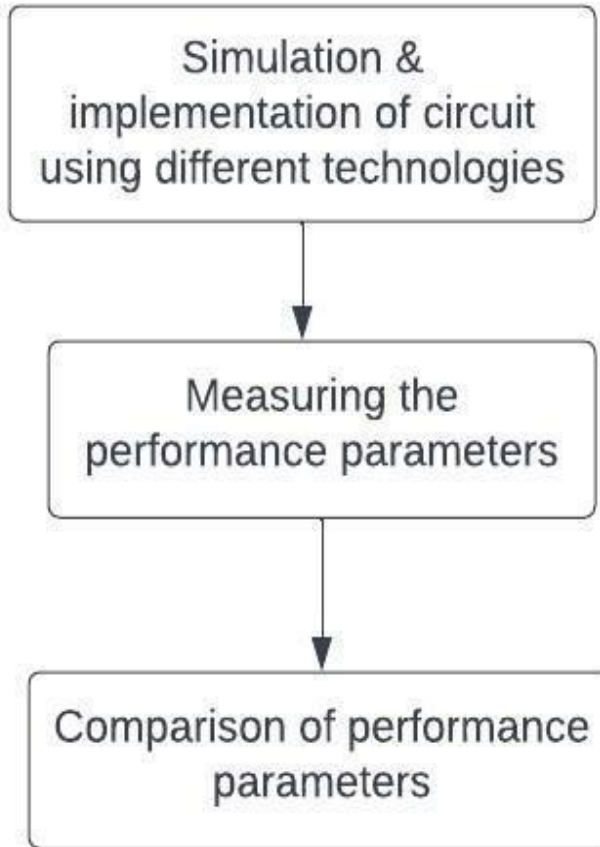
- | | |
|--------------------------------|------------|
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Assistant Professor
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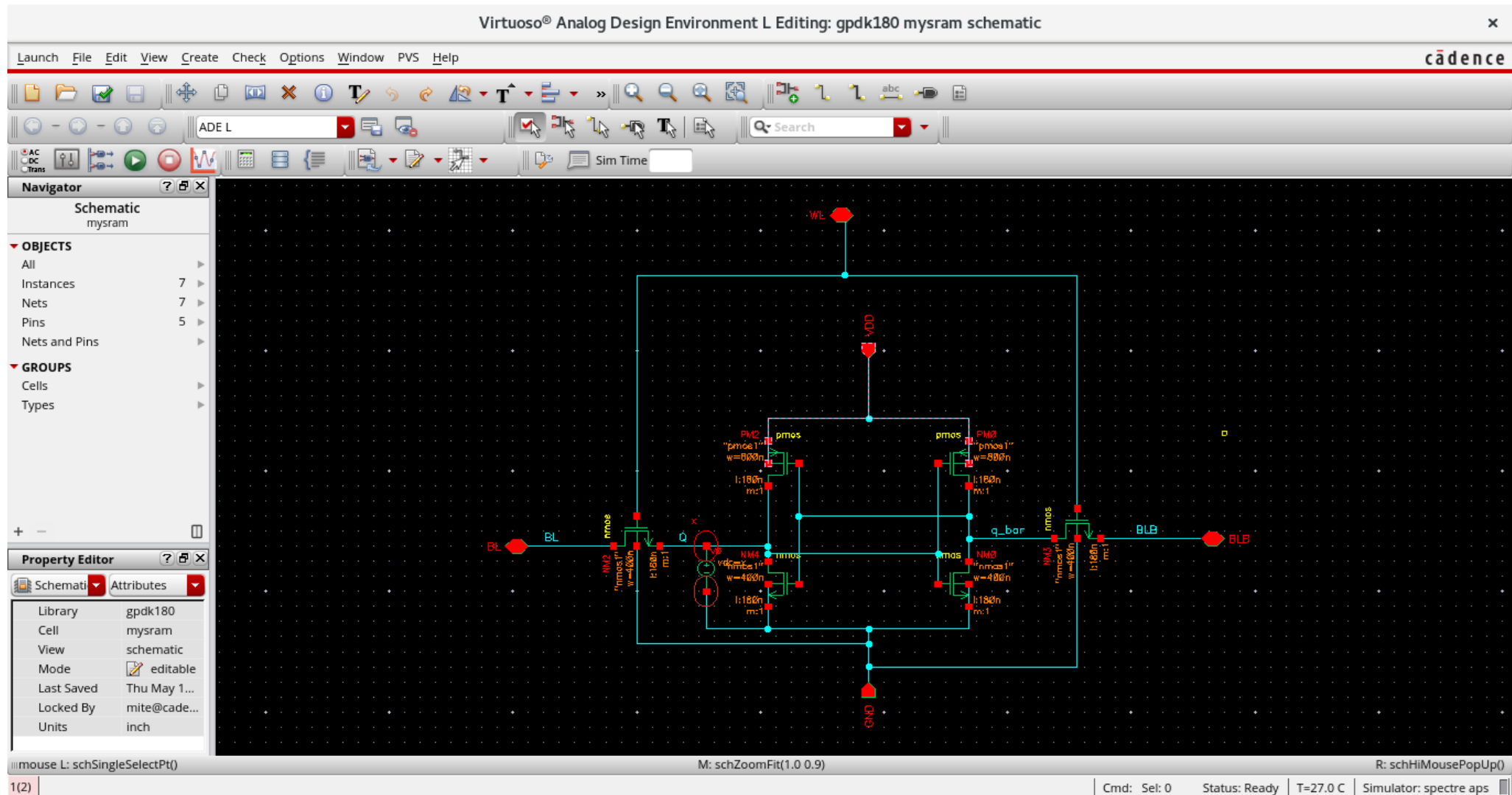
Problem Statement

- To design a low-power 6T SRAM that is suitable for use in energy-efficient electronic systems.
- The challenge is to reduce the power consumption of the 6T SRAM while maintaining high performance and reliability, to achieve a balance between power consumption and operational stability, as well as to improve the energy efficiency of devices that use 6T SRAM, such as mobile devices, IoT applications, and wearable devices.

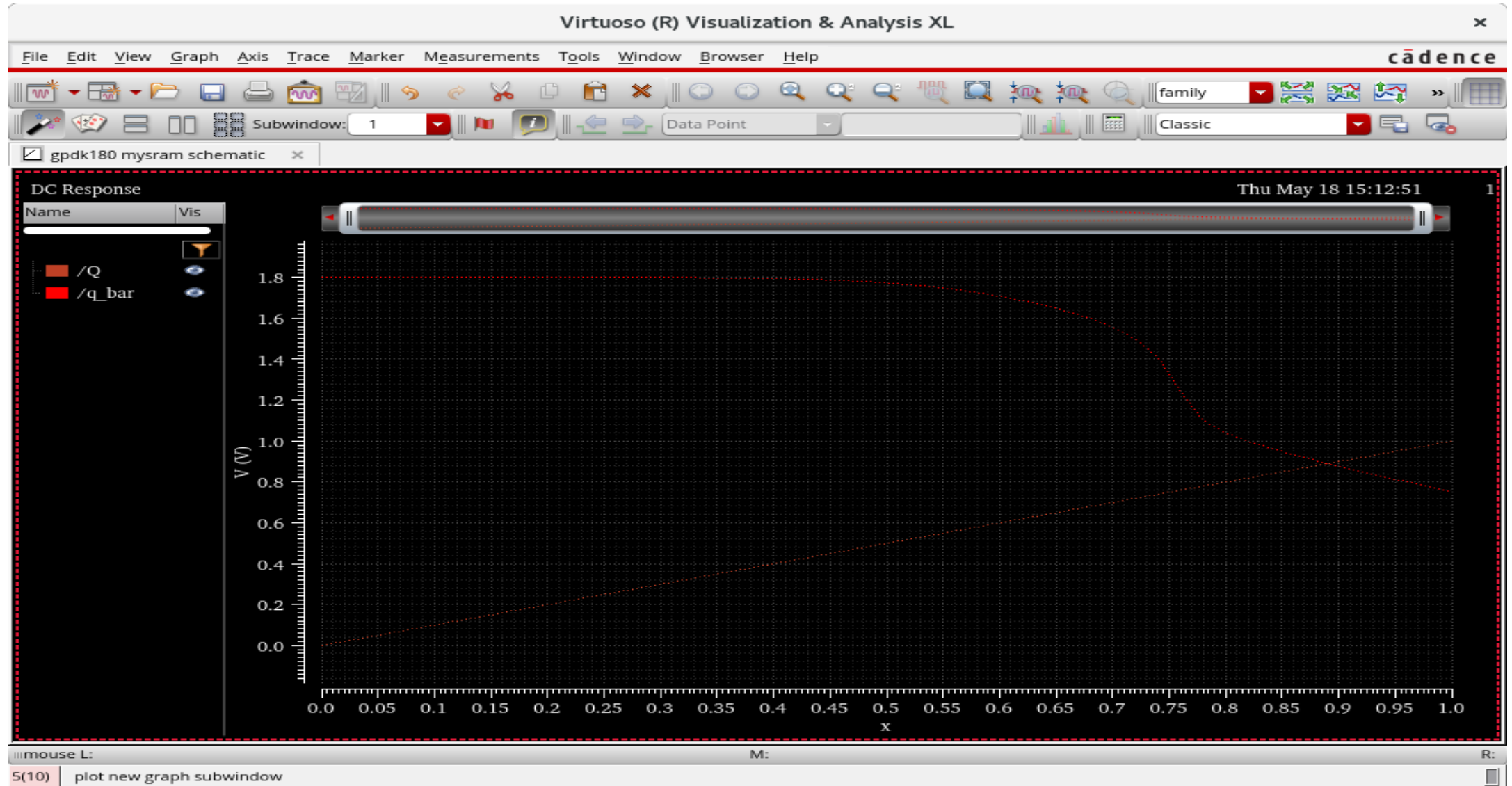
Methodology / Block Diagram/ Flowchart



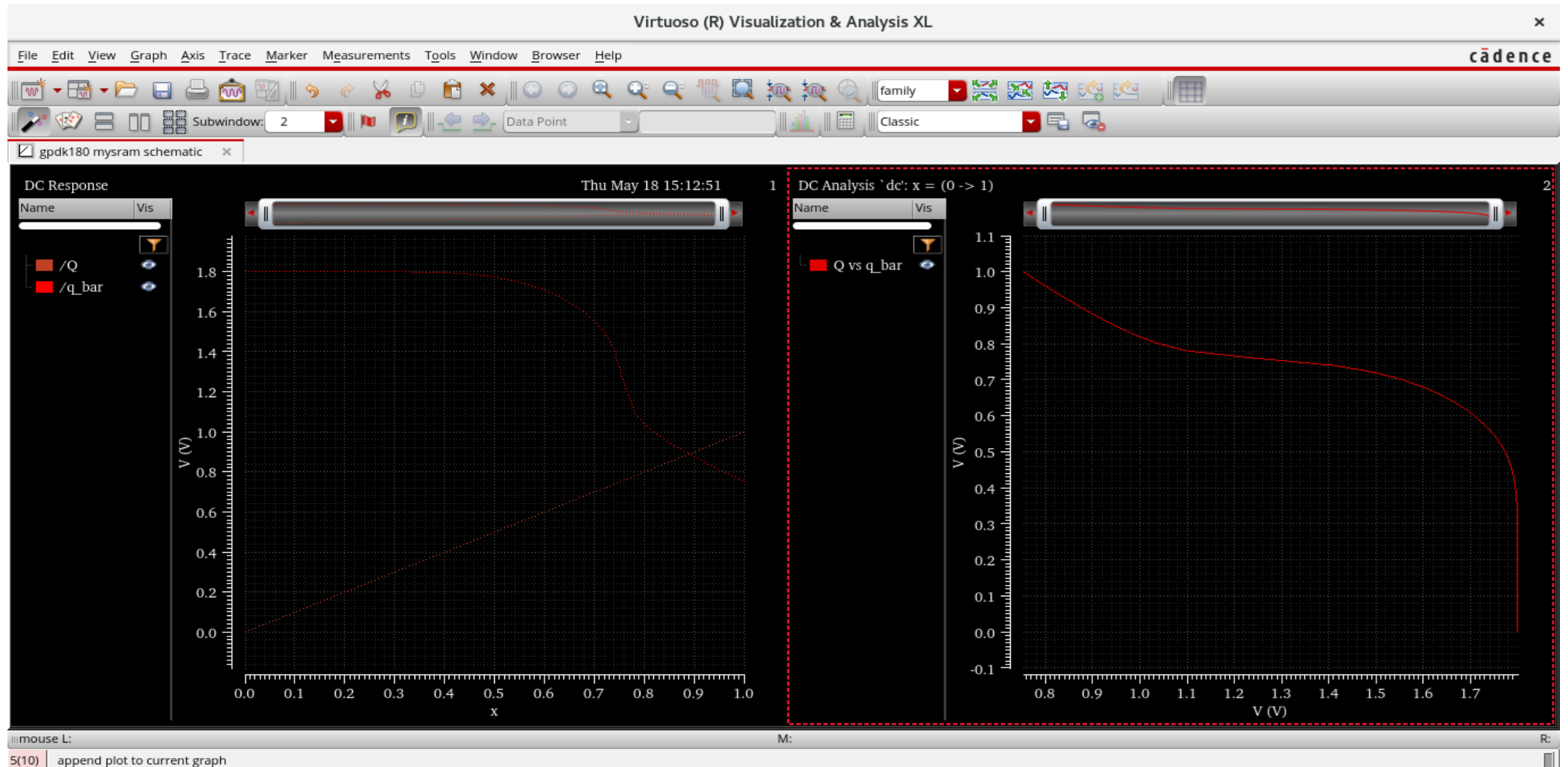
6T SRAM 180nm CIRCUIT



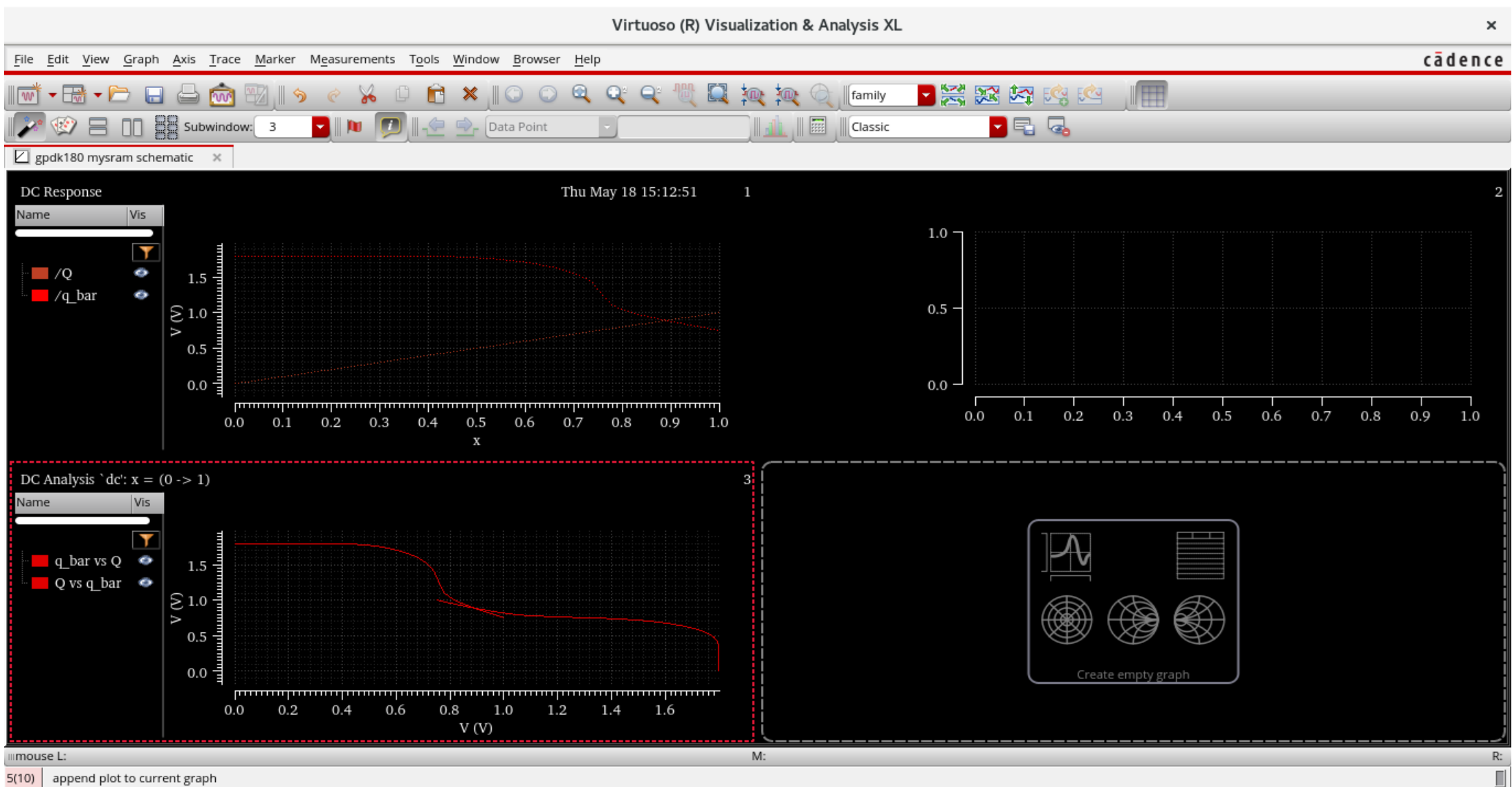
DC response



DC RESPONSE & DC ANALYSIS



BUTTERFLY CURVE



TEMPERATURE

Parametric Analysis - spectre(0): gpd180 mysram schematic

File Analysis Help

Parametric Simulation Completed.

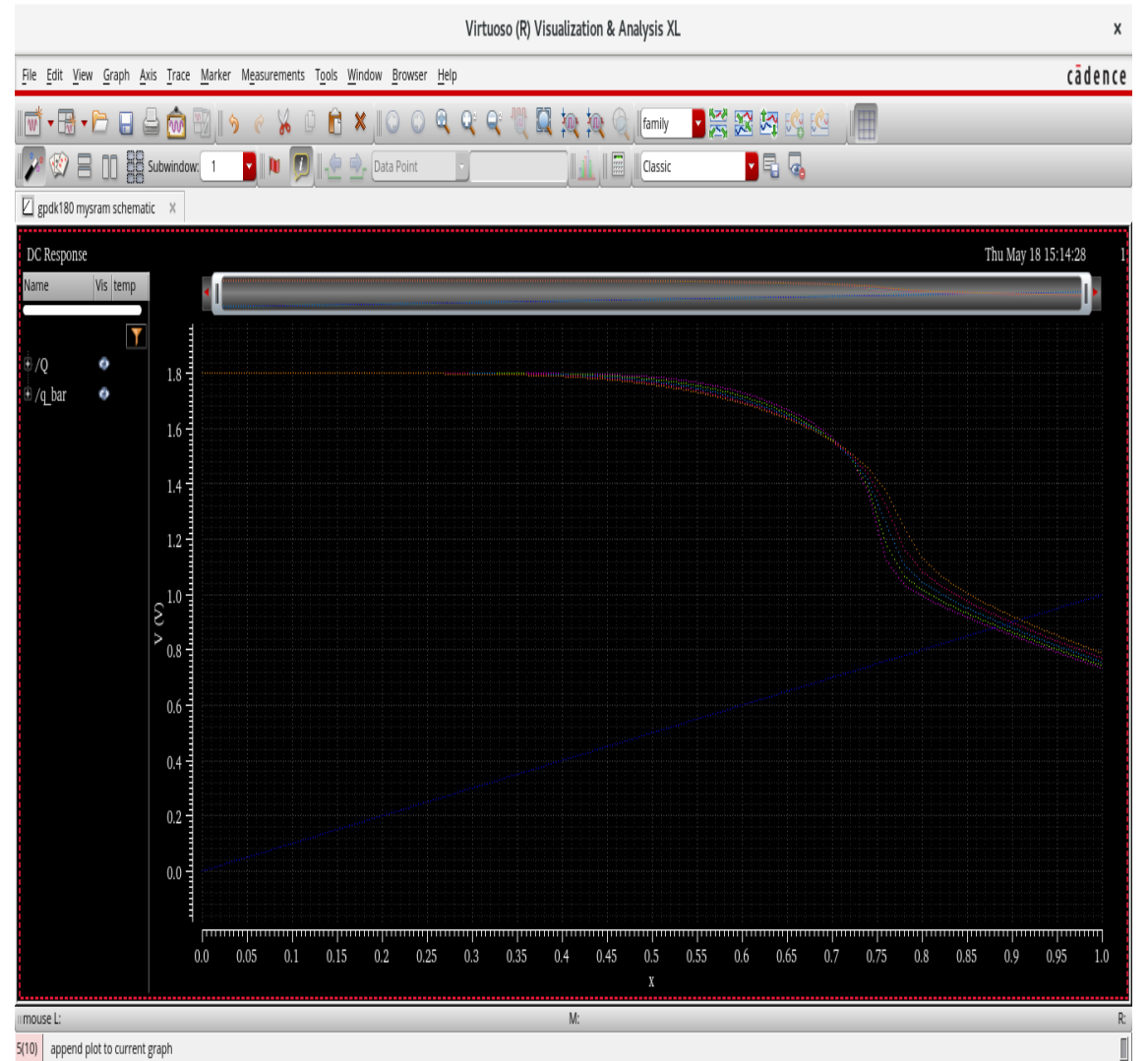
Run Mode: Sweeps & Ranges

Variable	Value	Sweep?	Range Type	From	To	Step Mode	Total Steps	Inclusion List	Exclusion List
temp	27	<input checked="" type="checkbox"/>	From/To	-55	125	Auto			

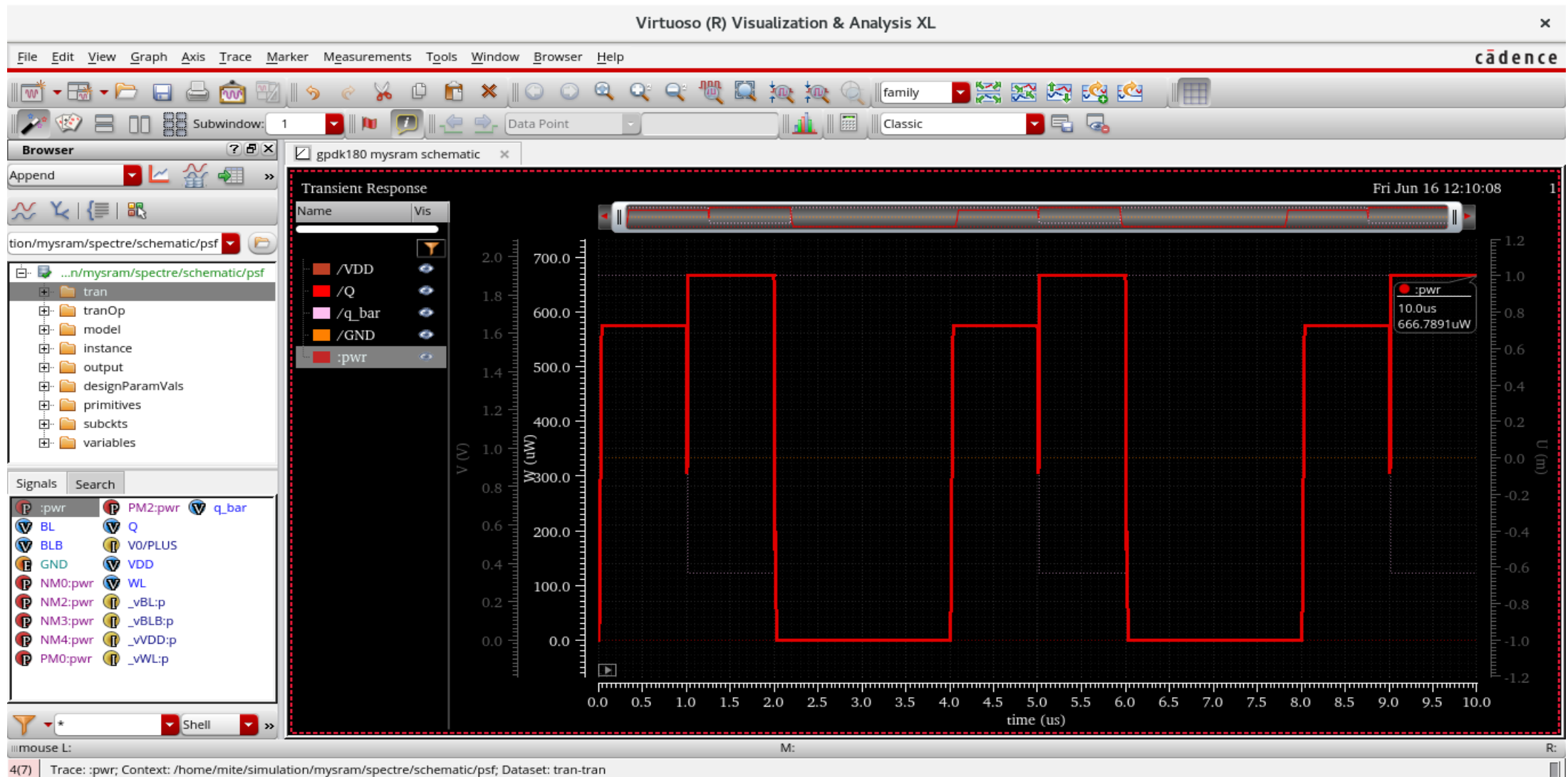
100%

Info: Parametric Simulation Completed

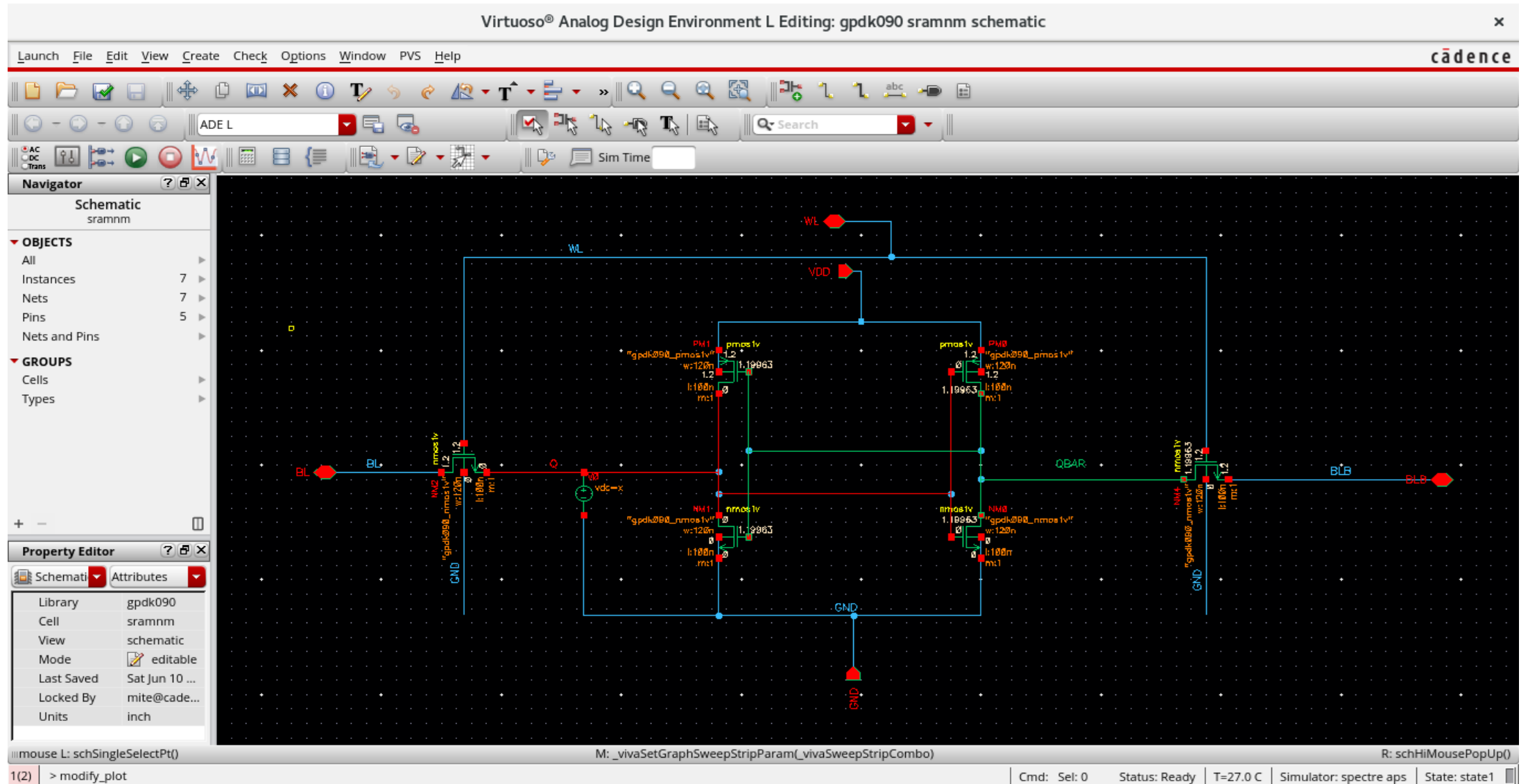
9 Run Selected Sweeps



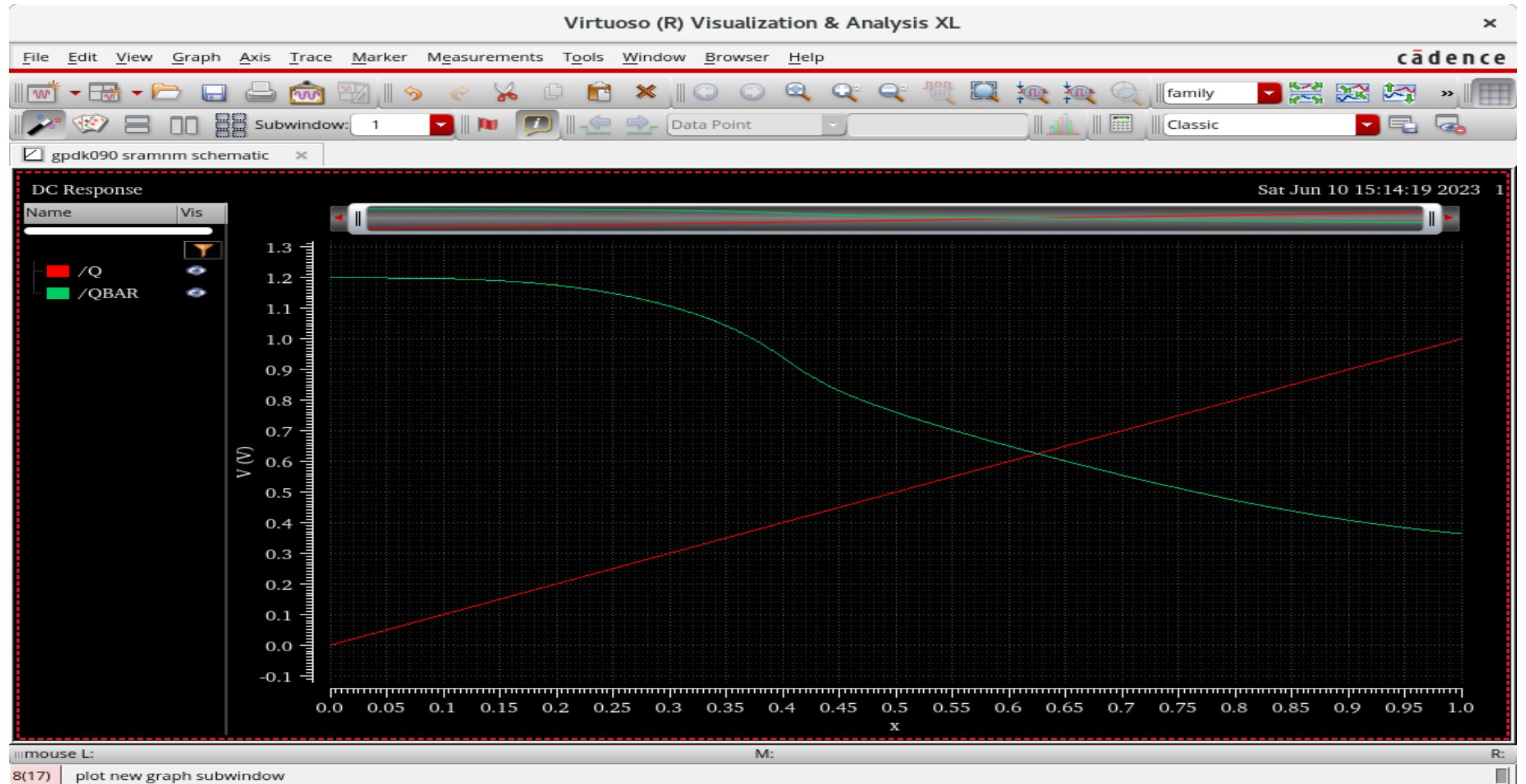
POWER



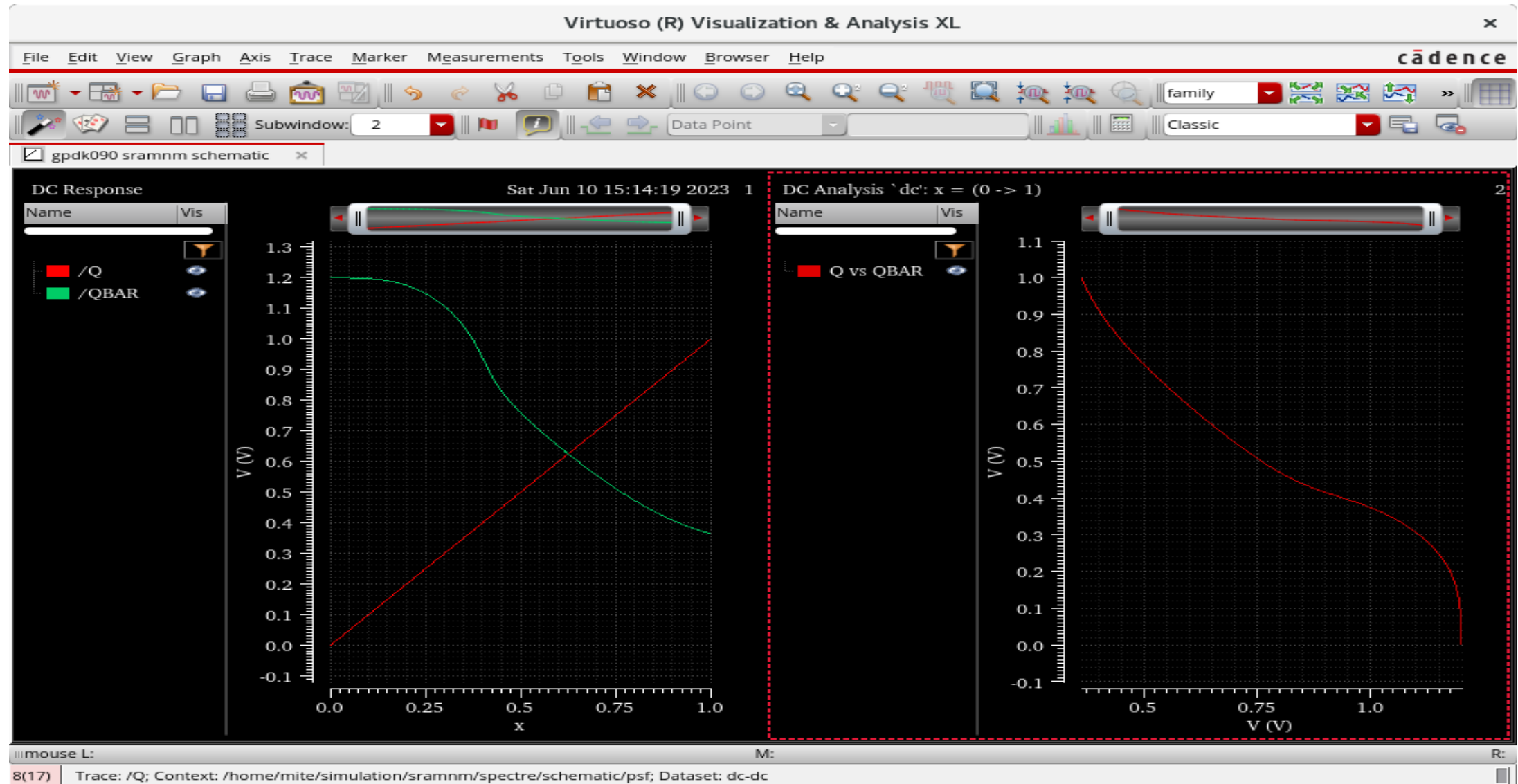
6T SRAM 90nm CIRCUIT



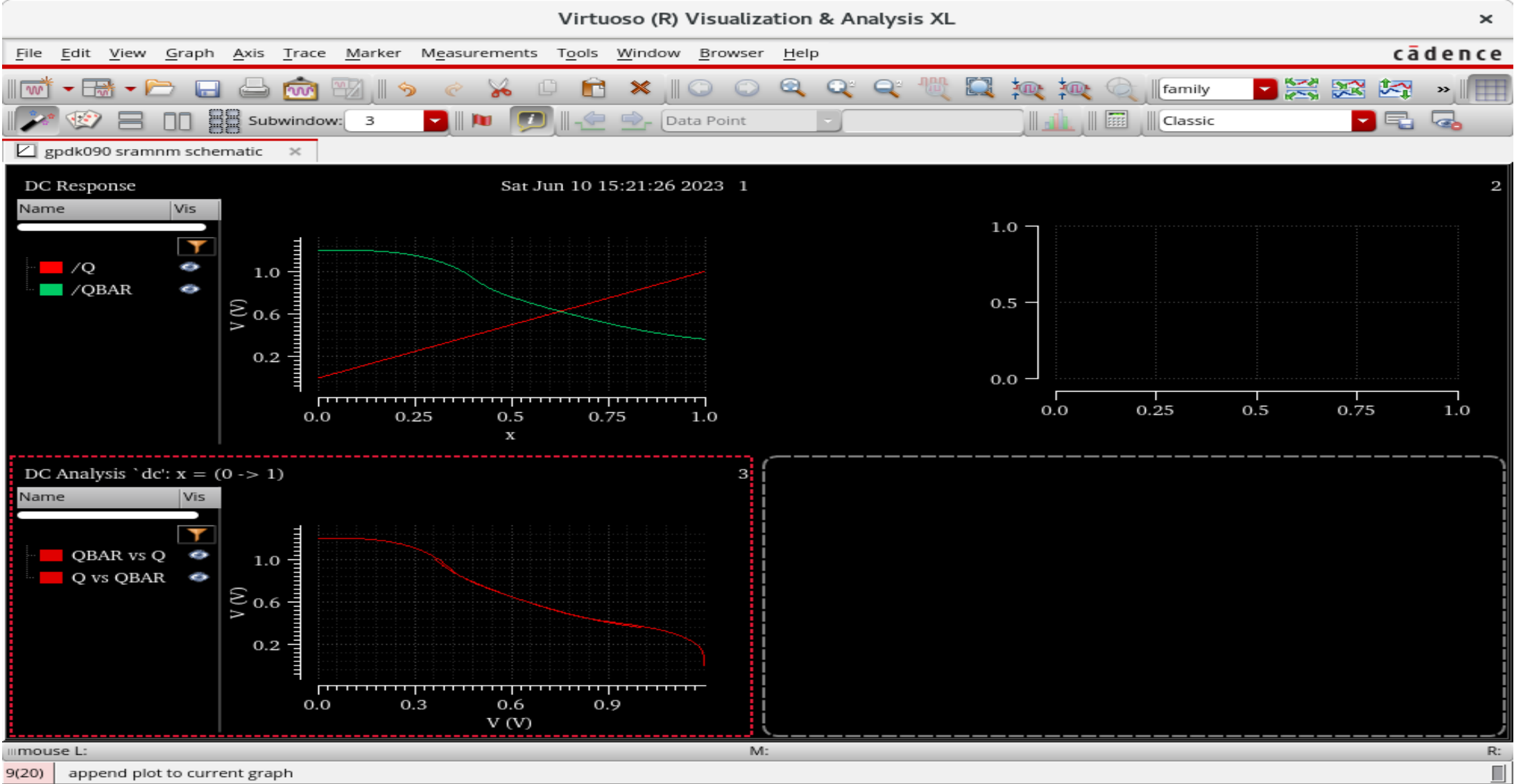
DC RESPONSE



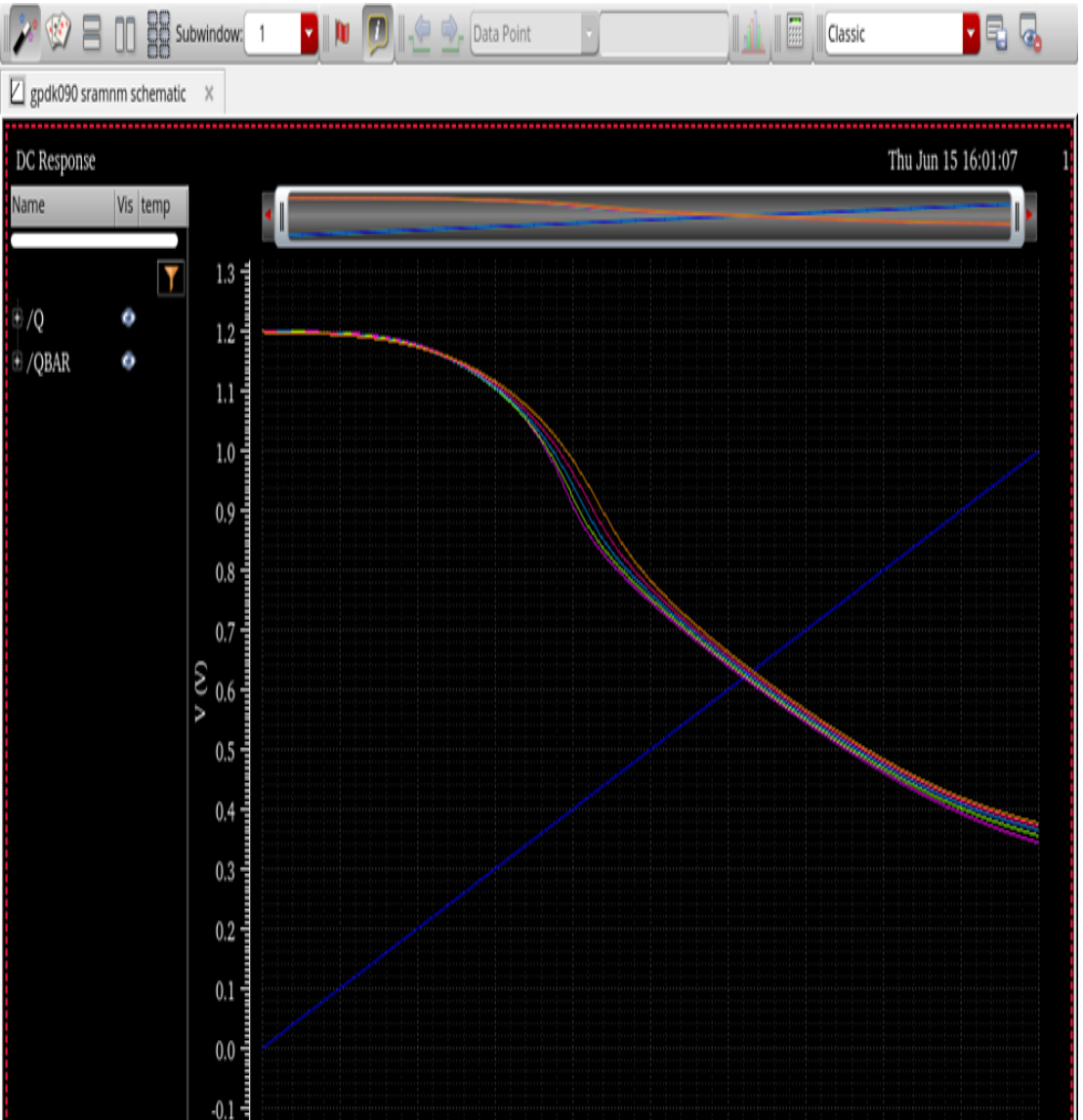
DC RESPONSE & DC ANALYSIS



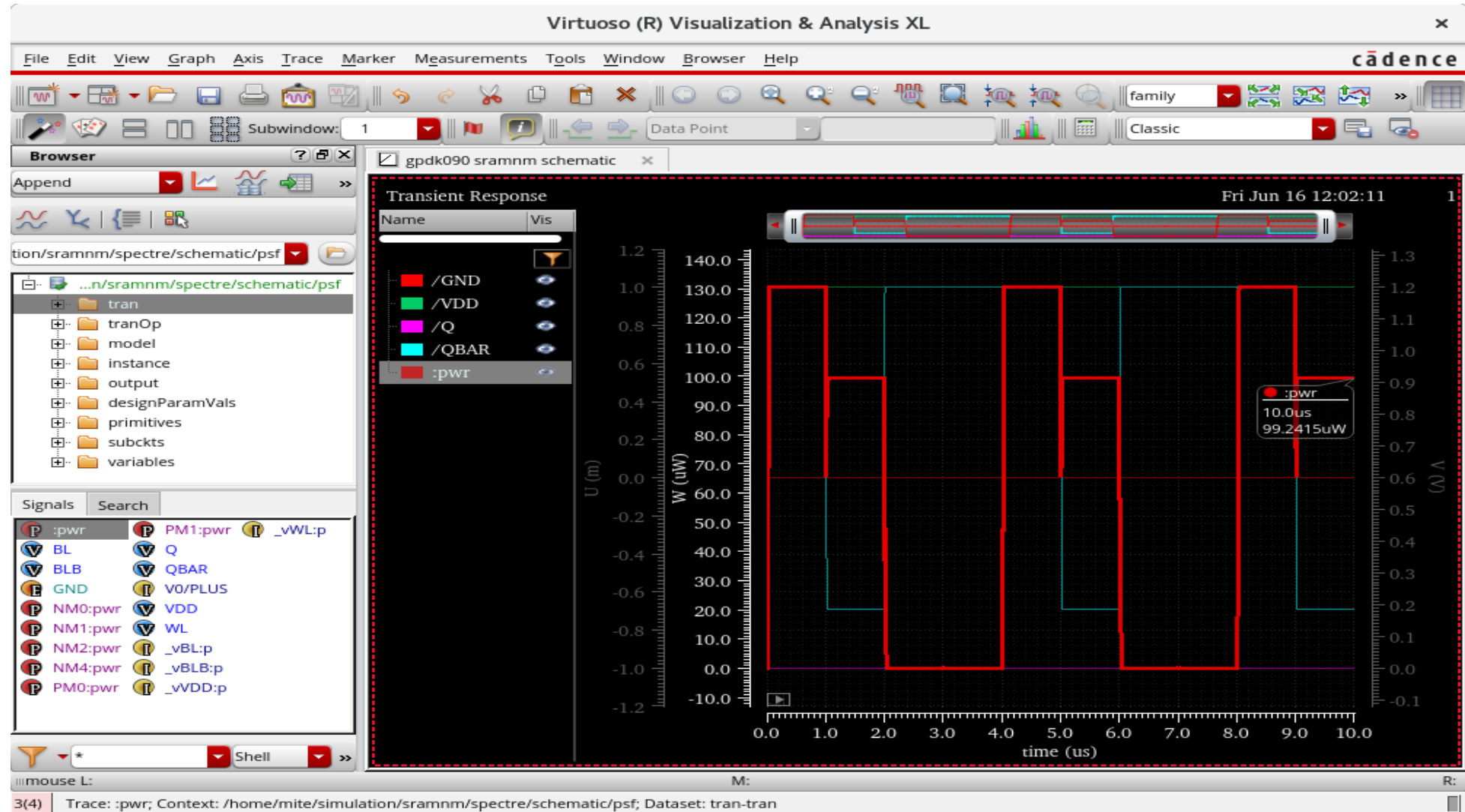
BUTTERFLY CURVE



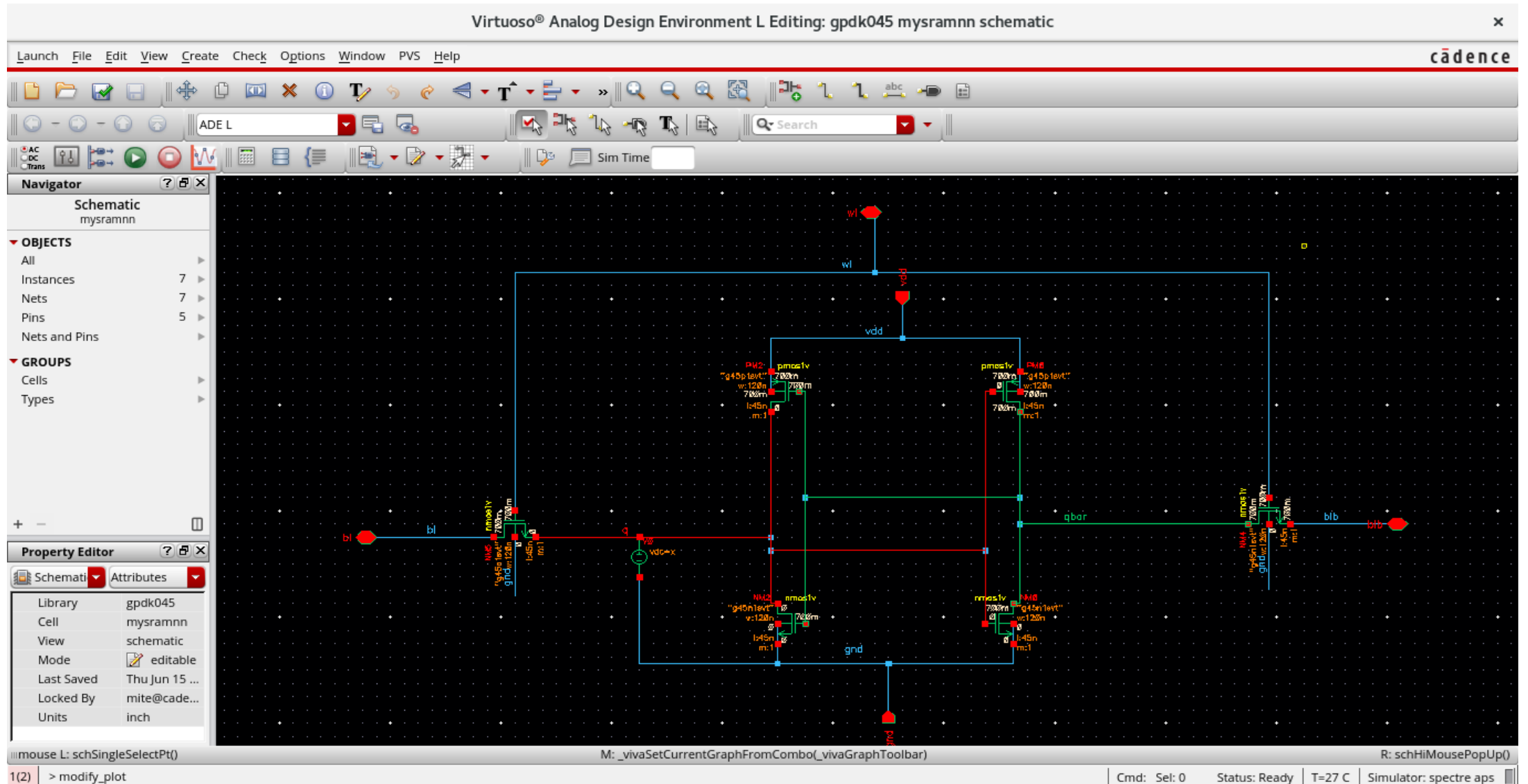
TEMPERATURE



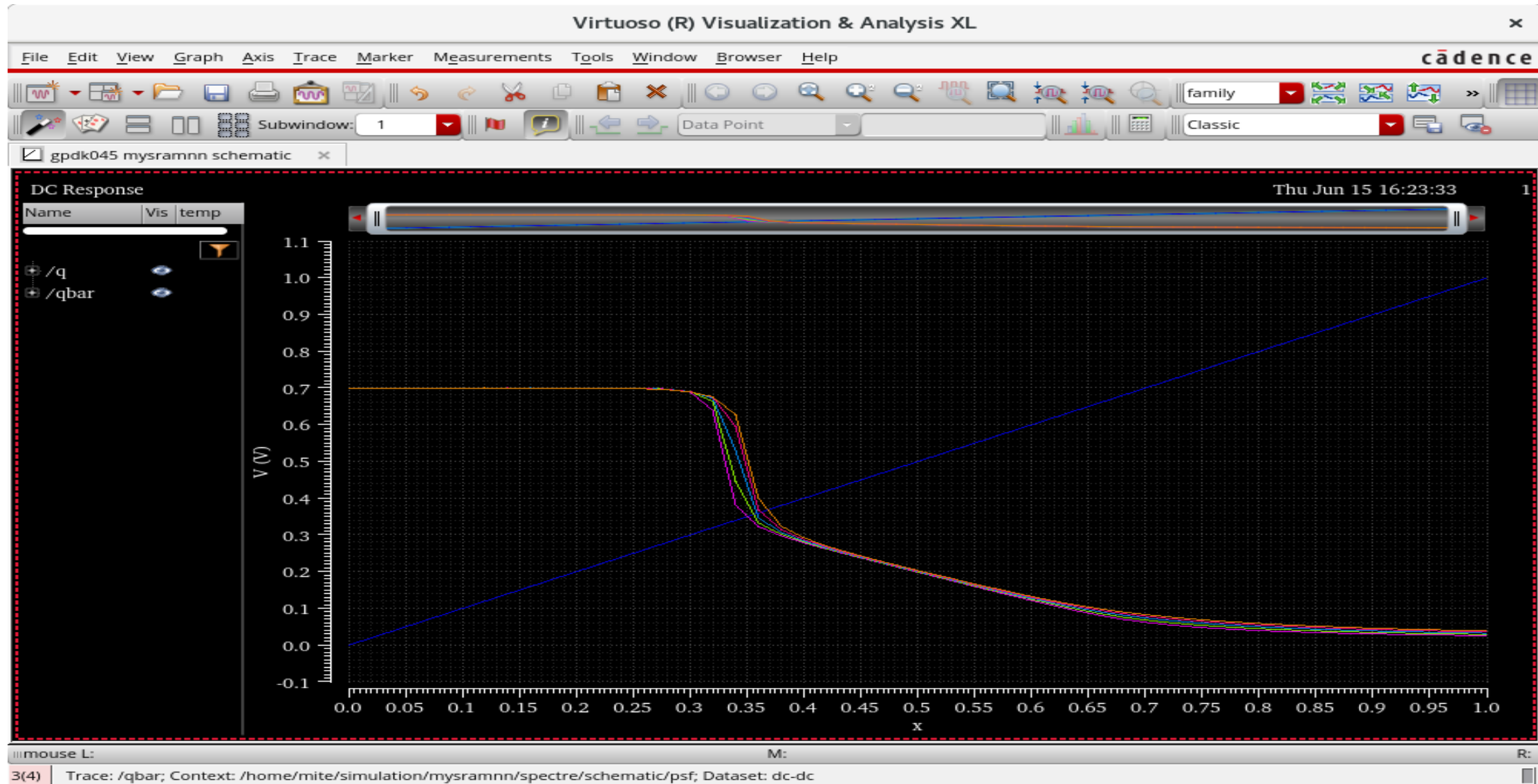
POWER



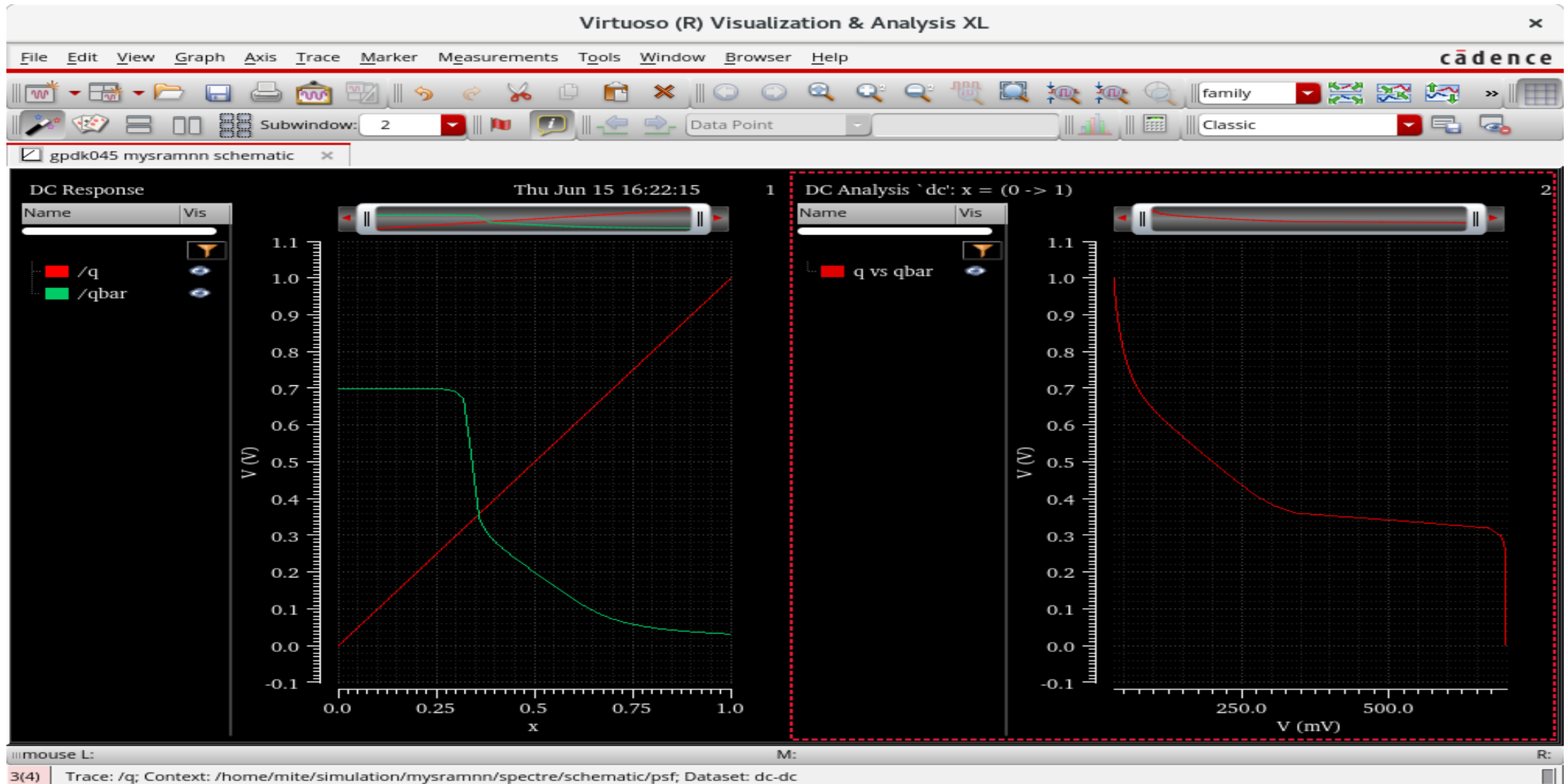
6T SRAM 45nm CIRCUIT



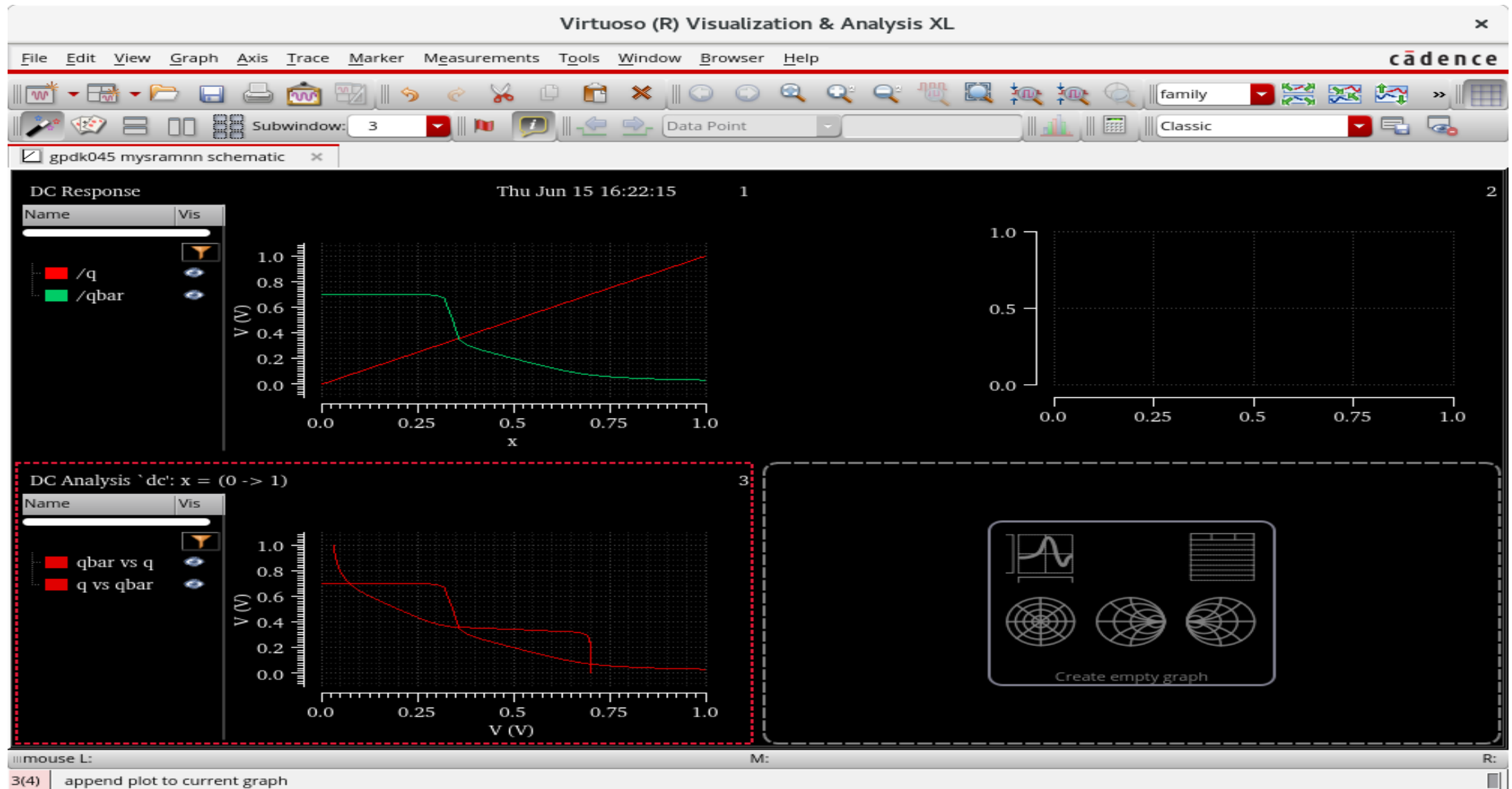
DC RESPONSE



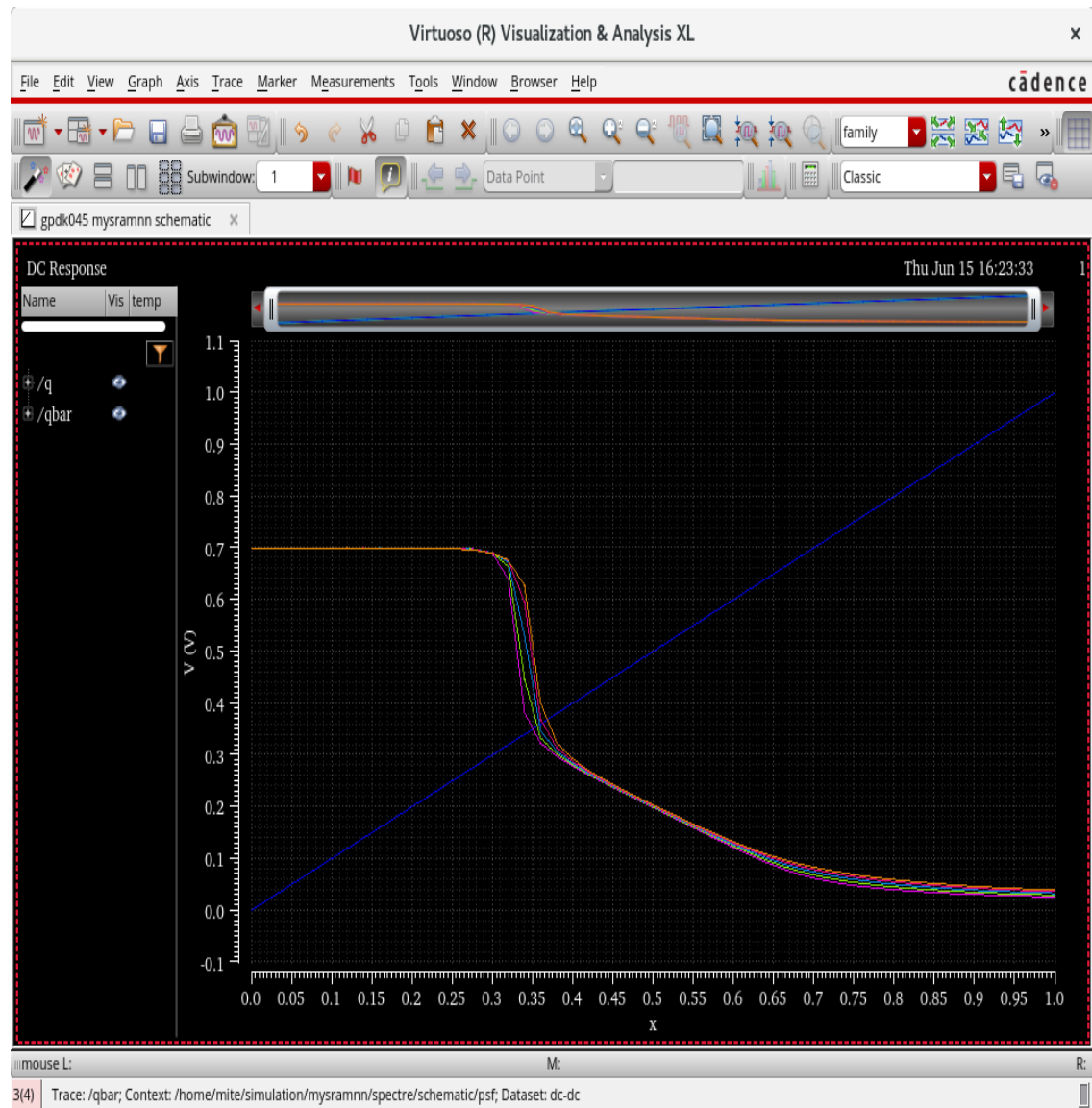
DC RESPONSE & DC ANALYSIS



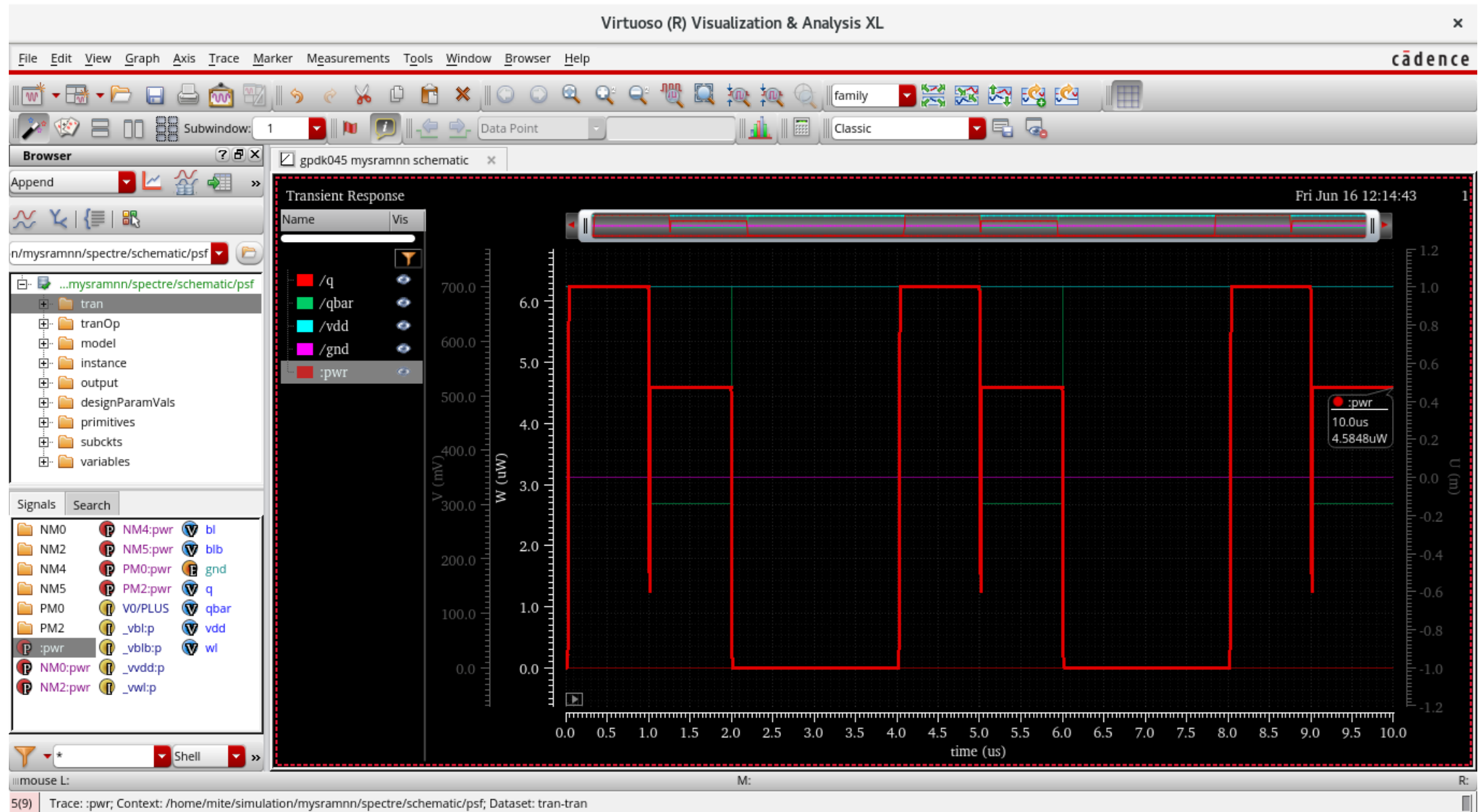
BUTTERFLY CURVE



TEMPERATURE



POWER



Work to be done

Task description	Start date	End Date	Status
Reviewed IEEE paper related to present project, exposure to Cadence Tool and implementation of basic circuits.	1/04/2023	30/04/2023	Completed.
Design and implementation of 6T SRAM cell and measuring the performance parameters.	1/05/2023	31/05/2023	Completed..
Comparison of performance parameters & review paper.	1/06/2023	30/06/2023	Completed.

References

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2. Keerthi R, Chen H. “*Stability and SNM analysis of low power SRAM*”, IEEE International Instrumentation and Measurement Technology Conference, Victoria Canada; 2008 May. p.1541–4.
3. Christensen D.C. Arandilla, Anastacia B. Alvarez, and Christian Raymund K. Roque ,“*Static Noise Margin of 6T SRAM Cell in 90-nm CMOS*”, IEEE UKSim 13th International Conference on Modelling and Simulation, pp534-539, 2011.
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6. Arora G, Poonam, Singh A, “*SNM Analysis of SRAM Cells at 45nm, 32nm and 22nm technology*”, International Journal of Engineering Research and General Science. 2014 Jun–Jul; 2(4):785–9.
7. Hiroyuki Yamauchi, “A Discussion on SRAM Circuit Design Trend in Deeper Nanometre-Scale Technologies”, in IEEE TRANSACTIONS ON VERY LARGE-SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 18, NO. 5, MAY 2010.
8. Abhishek Agal et al, “6T SRAM Cell: Design and Analysis in Int. Journal of Engineering Research and Applications”, www.ijera.com ISSN: 2248-9622, Vol. 4, Issue 3(Version1), March 2014, pp.574-57.
9. Arvind Kumar Nigam et. Al, “6T SRAM Cell: Design and Analysis”, in Intl JEngg Sci Adv Research 2015 June ;1(2):27-29.
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