VISVESVARAYA TECHNOLOGICAL UNIVERSITY

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Mini Project Synopsis (18ECMP68)

On

"DESIGN AND IMPLEMENTATION OF 6T SRAM CELL"

By

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ABSTRACT

Static Random Access Memory (SRAM) is one of the core components in the digital world. Generally, it consumes enormous amount of power and die area. Thereby extensive research in SRAM is in progress related power dissipation, memory chip area and supply voltage requirement. In this paper SRAM analysis in terms of Static Noise Margin, Data Retention Voltage, Read Margin (RM) and Write Margin (WM) for low power application is considered. Static Noise Margin (SNM) is one of the most essential parameters for memory design because it affects both read and write margin. SNM is related to the threshold voltages of the Negative Metal Oxide Semiconductor (NMOS) and Positive Metal-Oxide Semiconductor (PMOS) devices of the SRAM cell. High Read and Write Noise Margin are also significant challenges in the design of SRAM. Performance analysis is estimated in 6T-SRAM designed and implemented using Cadence Virtuoso Tool.

INTRODUCTION

SRAM is a type of Random Access Memory (RAM) that retains data bits in its memory as long as power is being supplied. Unlike Dynamic RAM (DRAM), which must be continuously refreshed, SRAM does not have this requirement, resulting in better performance and lower power usage. However, SRAM is also more expensive than DRAM, and it requires a lot more space. Stability in SRAM when designed using the Complementary Metal–Oxide– Semiconductor (CMOS) technologies generally depend on the SNM. SRAM memory technology is used because of its speed and robustness. As the device is scaled down in sizes several design challenges arise in the nanometre size SRAM design. In an SRAM cell operation generally supply voltage scaling is performed. Reducing the VDD reduces subthreshold leakage current and gate leakage. For analysing high speed SRAM calculation of read margin and WM is necessary. Nowadays focus is on low supply voltage which reduces the SNM. The stability of SRAM cell can be analysed based on the SNM value because performance is proportional to the SNM.

LITERATURE SURVEY

Changhwan Shin *et al.,* [1]- Reviewed a detailed discussion about the performance and threshold voltage variability of fully depleted silicon-on-insulator (FD-SOI) MOSFETs are compared against those of conventional bulk MOSFETs via 3-D device simulation with atomistic doping profiles. Compact (analytical) modelling is then used to estimate six-transistor SRAM cell performance metrics (i.e., read and write margins, and read current) at the 22 nm CMOS technology node. The dependences of these metrics on cell ratio, pull-up ratio, and operating voltage are analysed for FD-SOI versus bulk SRAM cells.

Keerthi R *et al.*, [2]- Have proposed a method to overcome the read data destruction and to gain stability at IOWVDD a seven-transistor (7T) SRAM cell is implemented and compared with the conventional six-transistor (6T) SRAM cell. To illustrate the robust performance of an 8-bit SRAM statistical simulation and data analysis by considering the process variations and mismatch was conducted for every operation of the SRAM. The measurement results show that the static noise margin (SNM) of the 7T SRAM cell is better than that of the 6T SRAM cell. The stability of the 8-bit 7T SRAM at IOW-VDD is also proved by testing the SRAM at 720 mV.

Christiensen D.C *et al.*, [3]- Have discussed to examines the factors that affect the Static Noise Margin (SNM) of a 6T Static Random Access Memory (SRAM) cell designed in 90-nm CMOS. In this paper, the SRAM cell is simulated and noise margins are obtained while varying several parameters that affect SRAM operations. These parameters are temperature, threshold voltage, supply voltage, cell ratio, pull-up ratio, and process corner variations.

Prajna Mishra *et al.*, [4]- Have analysed about Static Random Access Memory (SRAM) and CMOS technology, which necessitates new SRAM design innovations. SRAM bit cells are formed of lowest geometry devices in order to achieve high density and stay up with CMOS technology scaling; as a consequence, they are the first to feel the consequences of technological scaling. Simultaneously, the success of next generation technology is dependent on the effective realization of SRAM. As a result, to deal with the nano-regime issues, numerous SRAM bit cell topologies and array layouts have recently been suggested. Poor stability, process variation tolerance, device deterioration due to ageing, and soft mistakes are some of the primary issues in SRAM design.

Calhoun, B.H. *et al.*, [5]- Have examined about the increased importance of lowering power in memory design has produced a trend of operating memories at lower supply voltages. Recent explorations into sub-threshold operation for logic show that minimum energy operation is possible in this region. These two trends suggest a meeting point for energy-constrained applications in which SRAM operates at sub-threshold voltages compatible with the logic. Since sub-threshold voltages leave less room for large static noise margin (SNM), a thorough understanding of the impact of various design decisions and other parameters becomes critical. This paper analyzes SNM for subthreshold bit cells in a 65-nm process for its dependency on sizing, DD, temperature, and local and global threshold variation.

Gourav Arora1 *et al.*, [6]- Reviewed a detailed discussion about High Read and Write Noise Margin is one of the important challenges of SRAM design. This paper analyzes the read stability and write ability of 6T and 7T SRAM cell structures at different technologies. SRAM cell stability analysis is typically based on Static Noise Margin (SNM) investigation and SNM affects both read and write margin.

Hiroyuki Yamauchi *et al.*,[7]- Have detailed discussion about area scaling capabilities of many kinds of SRAM margin-assist solutions for variability issues, which are based on various efforts by not only the cell topology changes from 6T to 8T and 10T but also incorporation of multiple voltage supply for cell terminal biasing and timing sequence controls of read and write. The various SRAM solutions are analyzed considering an impact on the required area overhead for each design solution given by ever-increasing random variation.

Abhishek Agal *et al.*,[8]- Have researched about "SRAM has become a major component in many VLSI Chips due to their large storage density and small access time. SRAM has become the topic of substantial research due to the rapid development for low power, low voltage memory design during recent years due to increase demand for notebooks, laptops, IC memory cards and hand-held communication devices. SRAMs are widely used for mobile applications as both on chip and off chip memories, because of their ease of use and low standby leakage.

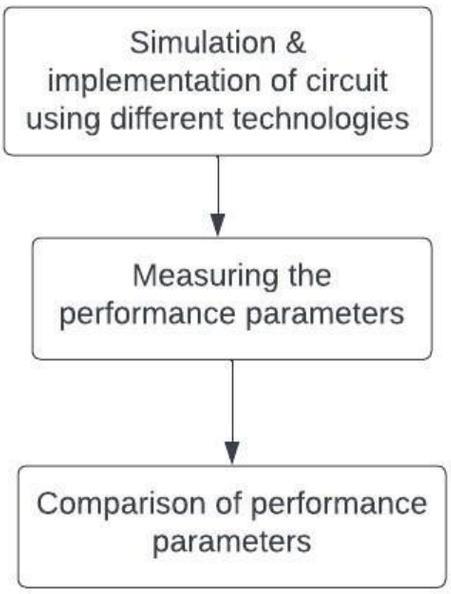
Manoj Padmanabha Murthy. T1 *et al.*,[9]- Reviewed a detail discussion about SRAM is a type of semiconductor memory uses bi-stable circuit to store 1 bit of data. SRAM cell don't require refresh circuits just like DRAM, The power consumed by single cell varies on the operations they perform. SRAM is a high speed memory it takes less time to access the data. Hence, it is used as a cache memory in processors and controllers. DRAM is denser compared to SRAM, they are used in main memories, where speed is not a higher part of importance. The applications of SRAM are growing wider and they are extended to industrial and automotive electronics as well. In this thesis SRAM cell is designed in two different technologies.

K. Dhananjay *et al.*,[10]- Have developed about SRAM is designed to provide an interface with CPU and to replace DRAMs in systems that require very low power consumption. Low power SRAM design is crucial since it takes a large fraction of total power and die area in high performance processors. A SRAM cell must meet the requirements for the operation in submicron/nano ranges. The scaling of CMOS technology has significant impacts on SRAM cell – random fluctuation of electrical characteristics and substantial leakage current. The random fluctuation of electrical property causes the SRAM cell to have high voltage.

METHODOLOGY

Static Random Access Memory (SRAM)- Much digital architecture consists of SRAM. In digital architectures, the density of the design and speed of execution is the most criticized element. Devices are scaled to achieve less complexity, supply voltages and threshold voltages. The 6-Transistor memory cell which is widely accepted as the standard memory cell. To achieve high density, the memory cells should be sized properly a conventional 6T SRAM configuration is considered. If the supply voltage applied to the operation of SRAM is low, then power consumption is also scaled down.

FLOWCHART



TIME SCHEDULE

April	Reviewed IEEE paper related to present project, exposure to Cadence Tool and implementation of basic circuits.
May	Design and implementation of 6T SRAM cell and measuring the performance parameters .
June	Comparison of performance parameters.

ESTIMATED BUDGET

- Miscellaneous
- **Software used-** Cadence Virtuous Tool.

REFERENCE

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