

How to crack CLD?

Here, I am suggesting some of the guide line, which may help you to crack CLD.



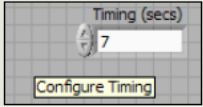
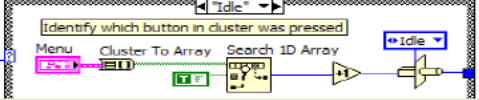
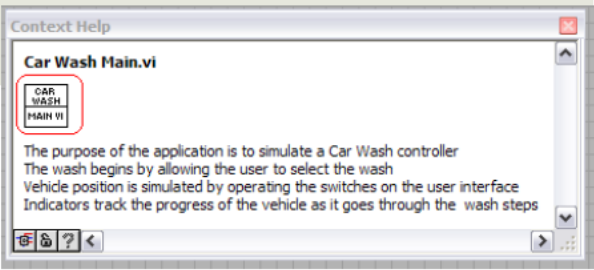


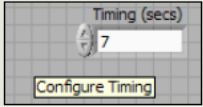
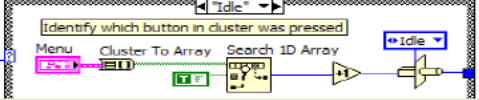
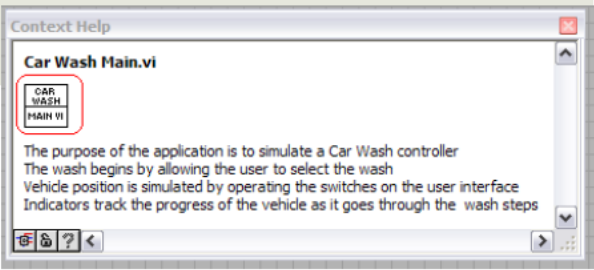


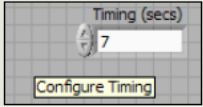
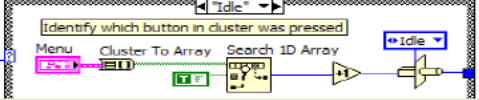
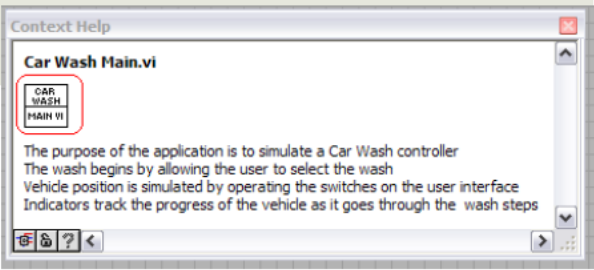
Just follow some simple steps during the exam because you have some limitation and goals.

Time target : 04 Hours(Limitation)

Passing Grade : 75% (Goal)

Step 1.	Leave the habits of “ Re-inventing the wheels ” means if you have available functions or VIs then don’t regenerate. If not available then find similar function and modified it as per your needs.
Step 2.	Practice all CLD examples with in time frame. Because CLD exam will be similar to these examples as per CLD holders <i>comments</i> .
Step 3.	What efficient method you have to use during exam?
	Ans : When you get the question , do immediately following steps
	<ul style="list-style-type: none"> - Read problem in quick and understand the scenario. - Open labview - Open a labview project and save it in a folder - Make different folders at same time like SubVIs, Typedef, Reports, Documents etc.. - Press CTRL+N (Open new VI) - Press CTRL+H (Labview Help to see comments) - Turn off Automatic tool selection - Select nothing on the front panel and change the font style to bold. This makes all subsequent creations boldface. - Open the Block diagram and then open function palate and search for something, it take some time to populating - At mean time read problem carefully, after opening - Open Labview icon editor - Press Ctrl+SPACE to open Quick Drop(to easily search any function), it takes time to populate.(Ctrl+Space and then Ctrl+D -> Automatic wiring , Ctrl+Space and then Ctrl+R -> Removing wiring , Ctrl+Space and then Ctrl+T -> Labeling Alignment). - At mean time read problem carefully

	<ul style="list-style-type: none"> - Select Labview design pattern as per question.
Step 4.	Style checklist : (Small things that make a Big Difference !!) <ul style="list-style-type: none"> ✓ Avoid the use of local variables when you can use a wire ✓ Use property nodes to modify control attributes and control values but not indicator values ✓ Typedefine reused enums and data structures ✓ Close references if opened explicitly ✓ Avoid data coercion and default tunnels ✓ Avoid copies of code -Develop SubVI if code is reused ✓ Create readable block diagram ✓ Avoid unnecessary bends, overlapping objects, wires
Step 5.	Error handling: <ul style="list-style-type: none"> ✓ Wire error terminals. ✓ Wire error clusters to “no error” case. ✓ Stop top level VI on error (all loops)! ✓ Use simple error handler on program exit. ✓ Monitor errors from parallel loops. <p>Wire error terminals</p> <p>Wire Error clusters to Connector pane</p> <p>Stop VI on error when specified</p> <p>Use Simple error handler</p>

Step 6.	Documentation : <ul style="list-style-type: none"> ✓ Documentation for the VI & subVIs. ✓ Free labels on wires. ✓ Labels on block diagram items. ✓ Label the actual loops (yes you can). ✓ Label constants. ✓ Tip strips on GUI. ✓ Consistent icon scheme. ✓ Be brief & to the point <table border="1"> <thead> <tr> <th>Documentation</th><th>Example</th></tr> </thead> <tbody> <tr> <td>Label wires to identify their use</td><td></td></tr> <tr> <td>Label constants</td><td></td></tr> <tr> <td>Description and tool tips for UI controls</td><td></td></tr> <tr> <td>Block diagram comments</td><td></td></tr> <tr> <td>VI / SubVI Properties » Documentation</td><td></td></tr> </tbody> </table>	Documentation	Example	Label wires to identify their use		Label constants		Description and tool tips for UI controls		Block diagram comments		VI / SubVI Properties » Documentation	
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Step 7.	Test : <ul style="list-style-type: none"> ✓ Functionality ✓ Weird behavior from user 												
Step 8.	Final check through <ul style="list-style-type: none"> ✓ Close the project. ✓ Reopen it. ✓ Open the top level. ✓ Make sure there are no errors. ✓ Verify that it runs correctly. ✓ Double check documentation on every VI. ✓ Make important terminals on subVIs required. ✓ Run VI Analyzer if time permits 												