FIR Filter using adders to meet tight constraints

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Abstract—this is an IP design for a FIR Filter using only 2 input adders

In my design I used adders to replace the multipliers to meet the area and time contraints and i added a register at the end to fix the slack time it was really strange for me that when i added a register at the ouput the slack time was fixed and equall to zero !

I looked in the internet and found that the wires has a big propagation delay so I added a register at the end that fixed it .

Wires have an approximate propagation delay of 1 ns for every 6 inches (15 cm) of length. Logic gates can have propagation delays ranging from more than 10 ns down to the picosecond range, depending on the technology being used.

```
--------------------------------------------------------------
  data required time                              7.72
  data arrival time                              -7.72
--------------------------------------------------------------
  slack (MET)                                     0.00

****************************************
Report : area
Design : fir_sol_wrapper
Version: E-2010.12-SP5-3
Date   : Mon Apr 28 13:29:00 2014
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Library(s) Used:

    saed90nm_typ (File: /opt/synopsys/SAED/SAED_EDK90nm
    /Digital_Standard_cell_Library/synopsys/models/saed90nm_typ.db)

Number of ports:                   66
Number of nets:                   395
Number of cells:                   19
Number of combinational cells:      8
Number of sequential cells:         0
Number of macros:                   0
Number of buf/inv:                  8
Number of references:              13

Combinational area:       40227.840145
Noncombinational area:     8784.691093
Net Interconnect area:     2872.294229

Total cell area:          49012.531239
Total area:               51884.825468
```
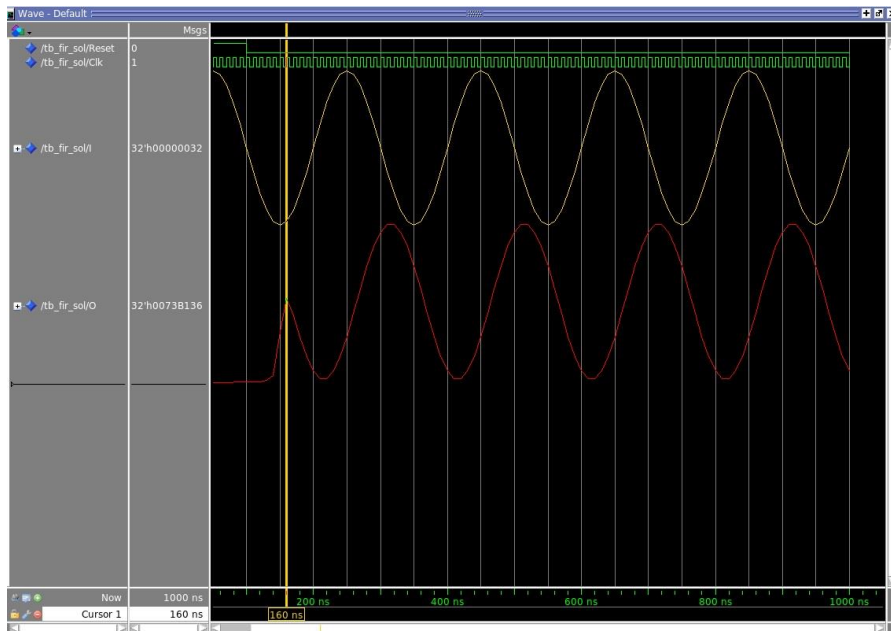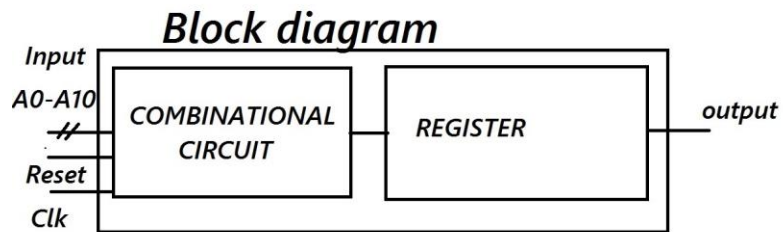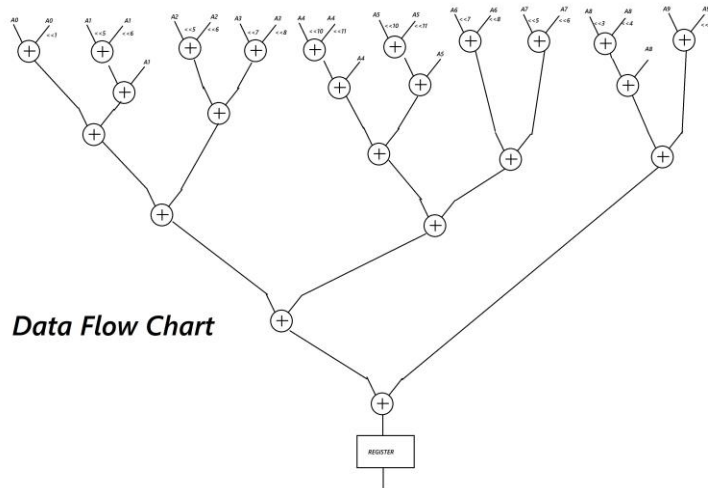
Data Flow Chart

Block diagram

Reference

http://en.wikipedia.org/wiki/Propagation_dela