

## PIC32MM0256GPM064 Family Silicon Errata and Data Sheet Clarification

The PIC32MM0256GPM064 family devices that you have received conform functionally to the current Device Data Sheet (DS60001387C), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).


The errata described in this document will be addressed in future revisions of the PIC32MM0256GPM064 silicon.

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (A2).

Data Sheet clarifications and corrections start on [page 8](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site ([www.microchip.com](http://www.microchip.com)).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
  - a) For MPLAB IDE 8, select *Programmer > Reconnect*.
  - b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon (  ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

**Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC32MM0256GPM064 silicon revisions are shown in [Table 1](#).

**TABLE 1: SILICON DEVREV VALUES**

Part Number	Device ID <sup>(1)</sup>	Revision ID for Silicon Revision <sup>(2)</sup>		Part Number	Device ID <sup>(1)</sup>	Revision ID for Silicon Revision <sup>(2)</sup>	
		A1	A2			A1	A2
PIC32MM0064GPM028	0x7708	01h	02h	PIC32MM0064GPM048	0x772C	01h	02h
PIC32MM0128GPM028	0x7710			PIC32MM0128GPM048	0x7734		
PIC32MM0256GPM028	0x7718			PIC32MM0256GPM048	0x773C		
PIC32MM0064GPM036	0x770A			PIC32MM0064GPM064	0x770E		
PIC32MM0128GPM036	0x7712			PIC32MM0128GPM064	0x7716		
PIC32MM0256GPM036	0x771A			PIC32MM0256GPM064	0x771E		

- Note 1:** The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".
- 2:** Refer to the "PIC32MM Families Flash Programming Specification" (DS60001364) for detailed information on Device and Revision IDs for your specific device.

# PIC32MM0256GPM064

**TABLE 2: SILICON ISSUE SUMMARY**

Module	Feature	Item Number	Issue Summary	Affected Revisions	
				A1	A2
ADC	12-Bit Conversion	1.	ADC may miss codes near the $\frac{1}{4}$ (1023), $\frac{1}{2}$ (2047) and $\frac{3}{4}$ (3071) scale transitions in 12-bit mode.	X	X
ADC	Format Options	2.	32-bit signed format option is the same as the 16-bit signed format option.	X	X
UART	Receive Buffer Overflow Disable	3.	Overflow disable feature controlled by the OVFDIS bit is not functional.	X	
MCCP	OCM3A Output	4.	The OCM3A output for MCCP3 is not functional.	X	X
Primary Oscillator	Primary Oscillator Start-up Timer (OST)	5.	The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use and set the POSCRDY (CLKSTAT<2>) bit too early.	X	X
Reset	Reset	6.	Current consumption in Reset is high.	X	X
Timer1	External Clock Mode	7.	Timer1 does not overflow in External Clock mode when PR1 = 1 and the prescaler is 1:1.	X	X
Timer1	External Clock Mode	8.	The first increment value is not visible when using External Clock mode and a 1:1 prescaler.	X	X
I <sup>2</sup> C Slave	I <sup>2</sup> C Slave	9.	I <sup>2</sup> C line does not return to Idle after receiving a NACK from the Master. Writes to I2CxTRN are not ignored in this condition.	X	X
I <sup>2</sup> C Slave	I <sup>2</sup> C Slave	10.	Slave reports a Bus Collision (BLC) for every transaction when SBCDE is enabled.	X	X
I <sup>2</sup> C Slave	I <sup>2</sup> C Slave	11.	When BOEN = 0, RBF = 0, and I2COV = 1, a NACK is generated but the address is not received.	X	X
I <sup>2</sup> C Slave	I <sup>2</sup> C Slave	12.	The Slave may ACK subsequent data after it has gone Idle after a NACK.	X	X
I <sup>2</sup> C Slave	I <sup>2</sup> C Slave	13.	The Slave will not Acknowledge reserved addresses in the '111_10xx' range regardless of the STRICT setting.	X	X
Power	Retention Sleep	14.	When the device wakes up from Retention Sleep mode, a device Reset may occur. The BOR, POR and EXTR bits in the RCON register are set erroneously for this Reset.	X	
Programming	Programming	15.	The JTAG TDO (RC9) pin toggles during programming when using the PGEC1/PGED1 or PGEC2/PGED2 pairs.	X	
Oscillator	Secondary Oscillator (SOSC)	16.	Enabling POSC in XT or HS mode may inhibit SOSC operation.	X	
ADC	ADC Performance	17.	Enabling POSC in XT or HS mode may degrade ADC performance.	X	
Power	BOR	18.	BOR: The main BOR may not function.	X	X
I/O	Schmitt Trigger Inputs	19.	Schmitt Trigger inputs may have glitches with slow signal rise/fall times.	X	X
SPI	SRMT Bit	20.	In SPI Slave mode, the SRMT bit may be set if the FIFO or Shift register is not empty.	X	X
ICSP™ Programming	Programming	21.	Programming in Retention Sleep.	X	X
ICSP Programming	Programming	22.	Self-programming after a POR or $\overline{\text{MCLR}}$ Reset.	X	X

## Silicon Errata Issues

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

### 1. Module: ADC

The ADC may miss codes near the  $\frac{1}{4}$  (1023),  $\frac{1}{2}$  (2047) and  $\frac{3}{4}$  (3071) scale transitions in 12-bit mode.

#### Work around

There is no work around in 12-bit mode. If all codes are desired in the application, use 10-Bit Operating mode.

#### Affected Silicon Revisions

A1	A2						
X	X						

### 2. Module: ADC

The 32-bit signed format option is the same as the 16-bit signed format option.

#### Work around

Use software to correct the output format. Sign-extend the ADC module's 16-bit signed integer output to a 32-bit signed integer. Using the MPLAB® XC32 C compiler, this can be accomplished by casting the ADC1BUFx SFR contents to a volatile short type, followed by a cast to a volatile int type.

#### Affected Silicon Revisions

A1	A2						
X	X						

### 3. Module: UART

The overflow disable feature controlled by the OVFDIS bit is not functional.

#### Work around

None.

#### Affected Silicon Revisions

A1	A2						
X							

### 4. Module: MCCP

The OCM3A output for MCCP3 is not functional.

#### Work around

Select the OCM3B, OCM3C, OCM3D output, or use MCCP1 OCM1A or MCCP2 OCM2A output.

#### Affected Silicon Revisions

A1	A2						
X	X						

### 5. Module: Primary Oscillator

The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use and set the POSCRDY (CLKSTAT<2>) bit too early. Clocking the device before the oscillator is ready may result in incorrect execution and exceptions.

#### Work around

Make sure that the Primary Oscillator clock is ready before using it by following these steps:

1. Running on non-POSC source, request the POSC clock using a peripheral such as REFO.
2. Provide a delay to stabilize POSC.
3. Switch to the POSC source.

[Example 1](#) shows a work around for the device power-on and [Example 2](#) shows the work around when the device wakes from Sleep.

# PIC32MM0256GPM064

## EXAMPLE 1: USING POSC AT POWER-ON

```
#pragma config FNOSC = FRCDIV          // Oscillator Selection bits (Fast RC oscillator (FRC))
// Clock Switching Enabled (Failsafe Clock Monitor can be enabled or disabled)
#pragma config FCKSM = CSECMD
-----
void main()
{
    // configure REFO to request POSC
    REFO1CONbits.ROSEL = 2;             // POSC = 2
    REFO1CONbits.OE = 0;                // disable output
    REFO1CONbits.ON = 1;                // enable module
    // wait for POSC stable clock
    // this delay may vary depending on different application conditions
    // such as voltage, temperature, layout, XT or HS mode and components
    { // delay for 9 ms
        unsigned int start = __builtin_mfc0(_CP0_COUNT, _CP0_COUNT_SELECT);
        while((__builtin_mfc0(_CP0_COUNT, _CP0_COUNT_SELECT)) - start < (unsigned int)(0.009*8000000/2));
    }
    // unlock OSCCON
    SYSKEY = 0;
    SYSKEY = 0xAA996655;
    SYSKEY = 0x556699AA;
    // switch to POSC = 2
    OSCCONCLR = _OSCCON_NOSC_MASK | _OSCCON_CLKLOCK_MASK | _OSCCON_OSWEN_MASK;
    OSCCONSET = (2<<_OSCCON_NOSC_POSITION) | _OSCCON_OSWEN_MASK;
    while(OSCCONbits.OSWEN == 1);      // wait for switch
```

## EXAMPLE 2: USING POSC WHEN AWAKENED FROM SLEEP

```
// Clock Switching Enabled (Failsafe Clock Monitor can be enabled or disabled)
#pragma config FCKSM = CSECMD
// unlock OSCCON
SYSKEY = 0;
SYSKEY = 0xAA996655;
SYSKEY = 0x556699AA;
// switch to FRC = 0 before entering to sleep
OSCCONCLR = _OSCCON_NOSC_MASK | _OSCCON_CLKLOCK_MASK | _OSCCON_OSWEN_MASK;
OSCCONSET = (0<<_OSCCON_NOSC_POSITION) | _OSCCON_OSWEN_MASK;
while(OSCCONbits.OSWEN == 1);        // wait for switch
// enter sleep mode
asm volatile("wait");
// configure REFO to request POSC
REFO1CONbits.ROSEL = 2;             // POSC = 2
REFO1CONbits.OE = 0;                // disable output
REFO1CONbits.ON = 1;                // enable module
// wait for POSC stable clock
// this delay may vary depending on different application conditions
// such as voltage, temperature, layout, XT or HS mode and components
{ // delay for 9 ms
    unsigned int start = __builtin_mfc0(_CP0_COUNT, _CP0_COUNT_SELECT);
    while((__builtin_mfc0(_CP0_COUNT, _CP0_COUNT_SELECT)) - start < (unsigned int)(0.009*8000000/2));
}
// switch to POSC = 2
OSCCONCLR = _OSCCON_NOSC_MASK | _OSCCON_CLKLOCK_MASK | _OSCCON_OSWEN_MASK;
OSCCONSET = (2<<_OSCCON_NOSC_POSITION) | _OSCCON_OSWEN_MASK;
while(OSCCONbits.OSWEN == 1);        // wait for switch
```

### Affected Silicon Revisions

A1	A2						
X	X						

## 6. Module: Reset

Current consumption in Master Clear Reset is high.

### Work around

Do not use MCLR to hold device in Reset to save power.

### Affected Silicon Revisions

A1	A2						
X	X						

## 7. Module: Timer1

Timer1 does not overflow in External Clock mode when PR1 = 1 and the prescaler is 1:1.

### Work around

Use a PR1 value greater than one.

### Affected Silicon Revisions

A1	A2						
X	X						

## 8. Module: Timer1

The first increment value is not visible when using External Clock mode and a 1:1 prescaler.

### Work around

None.

### Affected Silicon Revisions

A1	A2						
X	X						

## 9. Module: I<sup>2</sup>C Slave

I<sup>2</sup>C line does not return to Idle after receiving a NACK from the Master. Writes to I2CxTRN are not ignored in this condition.

### Work around

Do not write to the I2CxTRN register after a NACK has been received.

### Affected Silicon Revisions

A1	A2						
X	X						

## 10. Module: I<sup>2</sup>C Slave

Slave reports a Bus Collision (BLC) for every transaction when SBCDE is enabled.

### Work around

Do not enable SBCDE.

### Affected Silicon Revisions

A1	A2						
X	X						

## 11. Module: I<sup>2</sup>C Slave

When BOEN = 0, RBF = 0 and I2COV = 1, a NACK is generated but the address is not received.

### Work around

Service the receive buffer to prevent an overflow.

### Affected Silicon Revisions

A1	A2						
X	X						

## 12. Module: I<sup>2</sup>C Slave

The Slave may ACK subsequent data after it has gone Idle after a NACK.

### Work around

The Master should not send data following a NACK without a generating a Start condition

### Affected Silicon Revisions

A1	A2						
X	X						

## 13. Module: I<sup>2</sup>C Slave

The Slave will not Acknowledge reserved addresses in the '111\_10xx' range regardless of the STRICT bit setting.

### Work around

None.

### Affected Silicon Revisions

A1	A2						
X	X						

# PIC32MM0256GPM064

## 14. Module: Power

When the device wakes up from Retention Sleep mode, a device Reset may occur. The BOR, POR and EXTR bits in RCON register are set erroneously for this Reset.

### Work around

To provide a consistent behavior when the device wakes up from the Retention Sleep mode, the software sequence should be performed following the `SLEEP` instruction. In this case, a Reset will always be generated when the device wakes up from Retention Sleep.

### Affected Silicon Revisions

A1	A2						
X							

## 15. Module: Programming

The JTAG TDO (RC9) pin toggles during programming when using the PGEC1/PGED1 or PGEC2/PGED2 pairs.

### Work around

Do not connect external circuitry to the TDO pin that cannot tolerate toggling when programming using the PGEC1/PGED1 or PGEC2/PGED2 pins.

### Affected Silicon Revisions

A1	A2						
X							

## 16. Module: Oscillator

Enabling POSC in XT or HS mode may inhibit SOSC operation.

### Work around

If SOSC operation is required, use FRC or FRCPLL instead of POSC.

### Affected Silicon Revisions

A1	A2						
X							

## 17. Module: ADC

Enabling POSC in XT or HS mode may degrade ADC performance in 10-bit and 12-bit mode.

### Work around

If ADC operation that meets the data sheet specification is required, use FRC or FRCPLL instead of POSC.

### Affected Silicon Revisions

A1	A2						
X							

## 18. Module: Power

The main BOR may not occur when the operating voltage drops below the BOR trip voltage.

### Work around

Ensure the device operating voltage does not violate the specified values.

Use an external supervisor circuit to reset the device if the operating voltage can be outside the specified values.

### Affected Silicon Revisions

A1	A2						
X	X						

## 19. Module: I/O

If the input signal rise or fall time is more than 500 nS, the I/O Schmitt Trigger output may have glitches.

### Work around

The rise/fall time of the input signal must be less than 500 nS.

### Affected Silicon Revisions

A1	A2						
X	X						

## 20. Module: SPI

In SPI Slave mode, the SRMT bit may be set if the FIFO or Shift register is not empty.

### Work around

The following work arounds can be implemented in the application to detect when the FIFO and Shift register are empty:

1. Check the SPITBF bit before checking the SRMT bit. If the SPITBF flag is cleared and the SRMT flag is set, then all data was transmitted. [Example 3](#) demonstrates the SPITBF and SRMT bits polling.
2. Read the SRMT bit twice, back-to-back. If the SRMT bit is set two reads in a row, then the FIFO and Shift register are empty. [Example 4](#) demonstrates the SRMT bit polling using double read.

### EXAMPLE 3: EMPTY STATUS DETECTION USING SPITBF AND SRMT BITS POLLING

```
// Both flags must indicate empty status.
while(SPI1STATLbits.SPITBF);
while(!SPI1STATLbits.SRMT);
```

### EXAMPLE 4: EMPTY STATUS DETECTION USING SRMT BIT POLLING WITH BACK-TO-BACK READS

```
// If SRMT bit is set two reads in a row
then it set correctly.
asm volatile("\n\
la $t0, SPI1STAT;\n
loop:;\n
lw $t1, 0($t0);\n
lw $t2, 0($t0);\n
and $t1, $t1, $t2;\n
andi $t1, $t2, 0x80;\n
beqz $t1, loop;");
```

### Affected Silicon Revisions

A1	A2						
X	X						

## 21. Module: ICSP™ Programming

After a POR or  $\overline{\text{MCLR}}$  Reset, the device may fail to program if Retention Sleep is invoked within 40 ms.

### Work around

Provide a delay in firmware to ensure the device does not enter Retention Sleep within 40 ms of a POR or  $\overline{\text{MCLR}}$  Reset.

### Affected Silicon Revisions

A1	A2						
X	X						

## 22. Module: ICSP Programming

After a POR or  $\overline{\text{MCLR}}$  Reset, the device may fail to program using ICSP if user firmware performs self-programming within 40 ms.

### Work around

Provide a delay in firmware to ensure the device does not perform self-programming within 40 ms of a POR or  $\overline{\text{MCLR}}$  Reset.

### Affected Silicon Revisions

A1	A2						
X	X						

# PIC32MM0256GPM064

## Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001387C):

**Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

### 1. Module: Electrical Characteristics

In [Table 29-20](#), Parameter F20 has been amended with three temperature ranges. The changes are shown below in bold (bold text in original removed for clarity).

**TABLE 29-20: INTERNAL RC ACCURACY**

AC CHARACTERISTICS		Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Characteristic	Min	Typ	Max	Units	Conditions
F20	FRC Accuracy @ 8 MHz	-1.5	—	1.5	%	2.0V ≤ VDD ≤ 3.6V, 0°C ≤ TA ≤ +60°C
		<b>-2.0</b>	—	<b>2.0</b>	%	<b>2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ 0°C,</b> <b>2.0V ≤ VDD ≤ 3.6V, +60°C ≤ TA ≤ +85°C</b>



## APPENDIX A: DOCUMENT REVISION HISTORY

### Rev A Document (3/2017)

Initial release of this document; issued for revision A1.

### Rev B Document (5/2017)

Adds silicon revision **A2**.

Updates [Table 1](#) and [Table 2](#).

Adds new silicon issues 18 ([Power](#)), 19 ([I/O](#)), 20 ([SPI](#)) and 21 ([ICSP™ Programming](#)).

### Rev C Document (6/2017)

Updates [Table 2](#).

Adds new silicon issues 22 ([ICSP Programming](#)).

Adds new data sheet clarification 1 ([Electrical Characteristics](#)).

# PIC32MM0256GPM064

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NOTES:

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**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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