PIC32MZ EF FAMILY

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family Silicon Errata and Data Sheet Clarification

The PIC32MZ Embedded Connectivity with Floating Point Unit (EF) family of devices that you have received conform functionally to the current Device Data Sheet (DS60001320F), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MZ Embedded Connectivity with Floating Point Unit (EF) family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (B2).

Data Sheet clarifications and corrections (if applicable) start on page 13, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select *Window > Dashboard*, and then click the **Refresh Debug Tool Status** icon ( ).
5. The part number and the Device and Revision ID values appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MZ EF Family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)		
		A1	A3	B2
PIC32MZ0512EFE064	0x7201053	0x1	0x3	0x6
PIC32MZ0512EFF064	0x7206053			
PIC32MZ0512EFK064	0x722E053			
PIC32MZ1024EFE064	0x7202053			
PIC32MZ1024EFF064	0x7207053			
PIC32MZ1024EFK064	0x722F053			
PIC32MZ1024EFG064	0x7203053			
PIC32MZ1024EFH064	0x7208053			
PIC32MZ1024EFM064	0x7230053			
PIC32MZ2048EFG064	0x7204053			
PIC32MZ2048EFH064	0x7209053			
PIC32MZ2048EFM064	0x7231053			

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001320F) for detailed information on Device and Revision IDs for your specific device.

TABLE 1: SILICON DEVREV VALUES (CONTINUED)

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)		
		A1	A3	B2
PIC32MZ0512EFE100	0x720B053	0x1	0x3	0x6
PIC32MZ0512EFF100	0x7210053			
PIC32MZ0512EFK100	0x7238053			
PIC32MZ1024EFE100	0x720C053			
PIC32MZ1024EFF100	0x7211053			
PIC32MZ1024EFK100	0x7239053			
PIC32MZ1024EFG100	0x720D053			
PIC32MZ1024EFH100	0x7212053			
PIC32MZ1024EFM100	0x723A053			
PIC32MZ2048EFG100	0x720E053			
PIC32MZ2048EFH100	0x7213053			
PIC32MZ2048EFM100	0x723B053			
PIC32MZ0512EFE124	0x7215053	0x1	0x3	0x6
PIC32MZ0512EFF124	0x721A053			
PIC32MZ0512EFK124	0x7242053			
PIC32MZ1024EFE124	0x7216053			
PIC32MZ1024EFF124	0x721B053			
PIC32MZ1024EFK124	0x7243053			
PIC32MZ1024EFG124	0x7217053			
PIC32MZ1024EFH124	0x721C053			
PIC32MZ1024EFM124	0x7244053			
PIC32MZ2048EFG124	0x7218053			
PIC32MZ2048EFH124	0x721D053			
PIC32MZ2048EFM124	0x7245053			
PIC32MZ0512EFE144	0x721F053	0x1	0x3	0x6
PIC32MZ0512EFF144	0x7224053			
PIC32MZ0512EFK144	0x724C053			
PIC32MZ1024EFE144	0x7220053			
PIC32MZ1024EFF144	0x7225053			
PIC32MZ1024EFK144	0x724D053			
PIC32MZ1024EFG144	0x7221053			
PIC32MZ1024EFH144	0x7226053			
PIC32MZ1024EFM144	0x724E053			
PIC32MZ2048EFG144	0x7222053			
PIC32MZ2048EFH144	0x7227053			
PIC32MZ2048EFM144	0x724F053			

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001320F) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Issue	Issue Summary	Affected Revisions[1]		
				A1	A3	B2
Oscillator	Reference Clock	1.	The Reference Clock cannot divide input frequencies greater than 100 MHz.	X	X	
Oscillator	Primary Oscillator Crystal	2.	**Revision A1 Silicon:** A crystal oscillator cannot be used as an input to the Primary Oscillator (OSC1/ OSC2 pins). **Revision A3 and B2 Silicon:** The Primary Oscillator has been tested in a normal power-up sequence and supports specific crystal operation.	X	X	X
Oscillator	FRC Tuning	3.	The OSCTUN register only increases the frequency of the FRC.	X		
Secondary Oscillator	Crystal Use	4.	The Secondary Oscillator (SOSC) does not support crystal operation.	X	X	
Power-Saving	PMD bits	5.	Turning off REFCLK through the PMD bits causes unpredictable device behavior.	X	X	
I^2C	—	6.	The I^2C module does not function reliably under certain conditions.	X	X	
UART	Auto-baud	7.	The Auto-baud feature does not function to set the baud rate.	X	X	X
UART	Synchronization	8.	On a RX FIFO overflow, shift registers stop receiving data, which causes the UART to lose synchronization.	X	X	X
USB	Suspend Mode	9.	The USB module will not function if the device enters Sleep mode and the USB PHY is turned off by setting the USBSSEN bit in the CFGCON register to ‘1’.	X	X	X
Power-Saving Modes	Sleep Mode	10.	The device may not exit Sleep mode.	X	X	
ADC	Digital Filters	11.	Using multiple digital filters may result in data not being captured accurately.	X	X	
ADC	Level Trigger	12.	The ADC level trigger will not perform burst conversions in Debug mode.	X	X	
ADC	DNL	13.	In Differential mode, DNL for code 3072 is out of specification.	X	X	X
ADC	Low-voltage Operation	14.	When the operating voltage (VDD/AVDD) is below 2.5V (i.e., charge pumps are ON), only one ADC core can be used.	X	X	X
ADC	Turbo Mode	15.	Turbo mode is not functional.	X	X	X
USB	Resume	16.	The USB module does not support remote wake-up.	X	X	X
Oscillator	External Clock Mode	17.	The EC mode timing specifications for the Primary Oscillator (POSC) are not met.	X		
Temperature Sensor	—	18.	The Temperature Sensor does not function.	X	X	X
ICSP	TDO	19.	The TDO pin becomes an output and toggles while programming on any ICSP™ PGECx/PGEDx pair.	X	X	X
DMA	PMD bits	20.	Setting the PMD bit for DMA (PMD7<4>) does not disable clocks or the DMA peripheral.	X	X	X
PMP	Status Bits	21.	The PMP input buffer full flag, IB0F, and the output buffer underflow, OBUF, are set as soon as the PMP is turned on in Slave mode (when TTLEN = 1).	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Issue	Issue Summary	Affected Revisions[1]		
				A1	A3	B2
Sleep	IPD	22.	A 3 mA increase occurs during Sleep mode when PB5DIV is disabled.	X	X	X
SQI	RX/TX FIFO	23.	The SQI may continuously receive invalid data or fail to transmit when the SQICLKDIV is used.	X	X	X
POR	GPIO	24.	Whenever V_{DD} is less than V_{POR}, the I/O pin states may be indeterminate.	X	X	
Crypto	Partial Packet	25.	The cryptographic DMA module does not support partial packet processing.	X	X	X
Crypto	Zero Length Packet	26.	Zero length packets fail to process. The crypto DMA does not support an empty string hash.	X	X	X
SPI	Block Transmission	27.	At the end of a transmission, the SRMT bit can indicate the completion of the transmission for one PBCLK even though the transmission has one block remaining.	X	X	X
SQI	Special Function Registers	28.	The CPU stalls if the SQI Special Function Registers are read before the REFCLKO2 clock is enabled after a Reset.	X	X	X
Sleep	Wake-ups	29.	Multiple sleep attempts which occur before the CPU has fully awakened, may stall the CPU until the next reset event.	X	X	X
Security	System Bus Access	30.	The note at the end of the CFGPG register (Register no. 34-10) indicates that the CPU as system bus initiator is controlled within the CPU core is incorrect. The CPU core internal state will not control the CPU system bus initiator permission group.	X	X	
31. Module:UART	High Speed Mode	31.	The UART Stop bit duration is shorter than expected in High-Speed mode (UxMODE.BRGH =1) for baud rates less than 7.5 Mbps.	X	X	X
32. Module:Reset	NMI Number	32.	The NMICNT bit field in the RNMICON register is 8 bits instead of 16 bits.	X	X	
33. Module:I2C3	I2C3	33.	I2C3 on the A3 revision is non functional.		X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B2**).

1. Module: Oscillator

The Reference Module cannot divide input frequencies greater than 100 MHz. Therefore, SYSCLK cannot be divided if the SYSCLK operates at frequencies greater than 100 MHz.

Work around

Instead of using SYSCLK, use PBCLK1 as the input, which is limited to 100 MHz and is synchronized to SYSCLK.

Alternatively, do not divide the SYSCLK and allow the destination peripheral (i.e., SQI, SPI) to divide it as needed. To do this, set the RODIV<14:0> bits and the ROTRIM<8:0> bits to '0'.

Affected Silicon Revisions

A1	A3	B2					
X	X						

2. Module: Oscillator

Revision A1 Silicon: A crystal oscillator cannot be used as an input to the Primary Oscillator (POSC) pins OSC1 and OSC2.

Silicon Work around

Use an external clock or the Internal FRC Oscillator.

Revision A3 and B2 Silicon: The POSC has been tested in a normal power-up sequence and supports specific crystal operation.

Silicon Work around 1

The Primary Oscillator (POSC) has been characterized to operate at 8 MHz, 12 MHz, and 24 MHz when the circuit in Figure 1 is implemented, and the operating conditions listed in Table 3 are met.

FIGURE 1: POSC CRYSTAL CIRCUIT

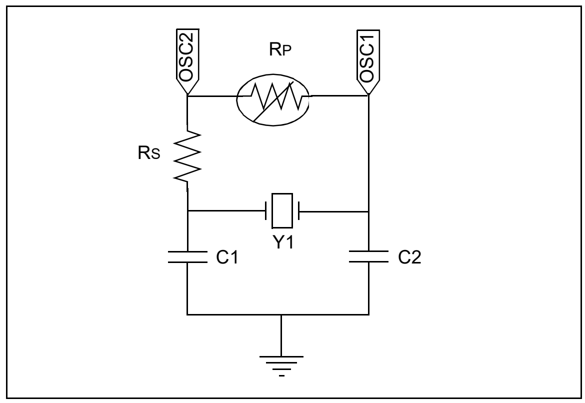

TABLE 3: CRYSTAL SPECIFICATIONS

Crystal Frequency (see Note 1)	Series Resistor (Rs)	Posc Gain Setting POSCGAIN<1:0> (DEVCFG0<20:19>)	Posc Boost Setting POSCBOOST (DEVCFG0<21>)
8 MHz	2 kΩ	'0b00 (GAIN_0)	'0b1 (ON)
12 MHz	1 kΩ	'0b00 (GAIN_0)	'0b1 (ON)
24 MHz	0 kΩ	'0b00 (GAIN_0))	'0b1 (ON)

Note 1: Using any other crystal frequency will require special component selection and characterization.
2: A parallel resistor (RP) should not be used to increase the gain of the POSC.

Silicon Work around 2

Alternatively, use an external clock or the Internal FRC oscillator.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

3. Module: Oscillator

The OSCTUN register only increases the frequency of the FRC, which results in the TUN<5:0> bits (OSCTUN<5:0>) functioning as follows:

TUN<5:0>: FRC Oscillator Tuning bits

111111 = Center frequency +4%

111110 =

•
•
•

000001 =

000000 = Center frequency; Oscillator runs at nominal frequency (8 MHz)

Work around

None.

Affected Silicon Revisions

A1	A3	B2					
X							

4. Module: Secondary Oscillator

A crystal oscillator cannot be used as the input to the Secondary Oscillator (SOSC) pins SOSCI and SOSCO.

Silicon Work around

Use an external clock source (32,768 Hz) applied to the SOSCO pin with the FSOSCEN bit (DEVCFG1<6>) set to '0' (i.e., the SOSC is disabled through the Configuration Word) for a real-time clock base; otherwise, use the internal LPRC for non-precision requirements.

Affected Silicon Revisions

A1	A3	B2					
X	X						

5. Module: Power-Saving

Turning off the REFCLK modules through the PMD bits causes unpredictable behavior.

Work around

None. Do not disable the REFCLK modules through the PMD bits.

Affected Silicon Revisions

A1	A3	B2					
X	X						

6. Module: I^{2}C

Indeterminate I^{2}C module behavior may result when data rates > 100 kHz and/or continuous sequential data transfers > 500 bytes are used.

The potential false intermittent error signals can result in one of the following error conditions, which are listed in order of decreasing frequency:

- **False Error Condition 1:**
  False Master Bus Collision Detect (Master-mode only) – The error is indicated through the BCL bit (I2CxSTAT<10>).
- **False Error Condition 2:**
  Receive Overflow (Master or Slave modes) – The error is indicated through the I2COV bit (I2CxSTAT<20>).
- **False Error Condition 3:**
  Suspended I^{2}C Module Operations (Master or Slave modes) – I^{2}C transactions in progress are inadvertently suspended without error indications.

Note:	All three false error conditions are recoverable in software.

<u>Revision A1 Silicon Work around 1</u>

False Error Condition 1:

Clear the Master Bus Collision Detect (BCL bit (I2CxSTAT<10>), after the bus returns to an Idle state. The software can monitor the S bit (I2CxSTAT<3>) and the P bit (I2CxSTAT<4>) to wait for an Idle bus. When the software services the bus collision Interrupt Service Routine and the I^{2}C bus is free, the software can resume communication by asserting a new Start condition.

False Error Condition 2:

Clear the Receive Overflow Status flag I2COV bit (I2CxSTAT<20>), and then resume normal operation.

False Error Condition 3:

First, initialize a Timer to slightly greater than the worst case I^{2}C transaction cycle, (i.e., from Start-to-Stop, including the sum of all other application PC flow latencies, calls, interrupts, etc.). Exact timing is not required, rather just long enough so that a normal transaction is not interrupted. Prior to the beginning of each transaction, start the timer. Be sure to stop and reset the timer after completion of each successful I^{2}C transaction.

Then, during the Timer interrupt (meaning the I^{2}C transaction has timed out), disable the I^{2}C module by setting the ON bit (I2CxCON<15>) = `0`. After disabling the module, wait 4 instruction cycles, after which time the I2CxSTAT register will automatically be cleared. Then, re-enable the I^{2}C module by setting the ON bit = `1` and resume normal operation.

<u>Revision A1 Silicon Work around 2</u>

Instead of using the hardware I^{2}C module, use a software “bit-bang” implementation.

<u>Revision A3 Silicon Work around</u>

The work arounds described for revision A1 silicon will also work for silicon revision A3, with the exception of I2C3, as I2C3 must use a software “bit-bang” implementation.

<u>Affected Silicon Revisions</u>

A1	A3	B2					
X	X						

7. **Module: UART**

The UART automatic baud rate feature is intended to set the baud rate during run-time based on external data input. However, this feature does not function.

Work around

None.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

8. **Module: UART**

During a RX FIFO overflow condition, the shift register stops receiving data. This causes the UART to lose synchronization with the serial data stream. The only way to recover from this is to turn the UART OFF and ON until it synchronizes. This could require several OFF/ON sequences.

Work arounds

Work around 1:

Avoid the RX overrun condition by ensuring that the UARTx module has a high enough interrupt priority such that other peripheral interrupt processing latencies do not exceed the time to overrun the UART RX buffer based on the application baud rate. Alternately or in addition to, set the URXISEL bits in the UxSTA register to generate an earlier RX interrupt based on RX FIFO fill status to buy more time for interrupt latency processing requirements.

Work around 2:

If avoiding RX FIFO overruns is not possible, implement an ACK/NAK software handshake protocol to repeat lost packet transfers after restoring the UART synchronization.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

9. **Module: USB**

The USB module will not function if the device enters Sleep mode and the USB PHY is turned off by setting the USBSSEN bit in the CFGCON register to '1'.

Work around

Keep the USB PHY operational in Sleep mode by setting the USBSSEN bit to '0'.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

10. **Module: Power-Saving Modes**

The device may not exit Sleep mode when Flash is powered down through the FSLEEP bit in the DEVCFG0/ADEVCFG0 Configuration register.

Work around

Enable Flash in Sleep mode by clearing the Flash Sleep Mode Configuration bit, FSLEEP, in the DEVCFG0/ADEVCFG0 Configuration register.

Affected Silicon Revisions

A1	A3	B2					
X	X						

11. **Module: ADC**

When using multiple digital filters, the filters may not capture data correctly when the assigned data sources are ready at the same time.

Work around

Only one digital filter may be used at a time.

Affected Silicon Revisions

A1	A3	B2					
X	X						

12. **Module: ADC**

The ADC level trigger will not perform burst conversions in Debug mode.

Work around

Do not use Debug mode with the ADC level trigger.

Affected Silicon Revisions

A1	A3	B2					
X	X						

13. **Module: ADC**

In Differential mode, code 3072 has a DNL of +3.

Work around

None.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

14. Module: ADC

When the operating voltage (VDD/AVDD) is below 2.5V (i.e., charge pumps are ON), only one ADC core can be used.

Work around

None.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

15. Module: ADC

Turbo mode is not functional when two channels are linked for the purpose of increasing throughput.

Work around

None.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

16. Module: USB

The USB module does not support remote wakeup through the USBRIE bit (USBCRCON<1>).

Work around

None.

USB descriptors must inform the host that the device does not support remote wake-up.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

17. Module: Oscillator

The Primary Oscillator in EC mode only functions up to 24 MHz

Work around

None.

Affected Silicon Revisions

A1	A3	B2					
X							

18. Module: Temperature Sensor

The temperature sensor does not function.

Work around

None.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

19. Module: ICSP

Regardless of other functions shared on the TDO pin, the TDO function becomes an active output and toggles while programming on any ICSP PGECx/PGEDx pair.

Work around

None.

Affected Silicon Revisions

A1	A3	B2					
X	X	x					

20. Module: DMA

Setting the PMD bit for DMA (PMD7<4>) does not disable clocks or the DMA peripheral.

Work around

None.

A1	A3	B2					
X	X	X					

21. Module: PMP

The PMP input buffer full flag, IB0F, and the output buffer underflow, OBUF, are set as soon as the PMP is turned on in Slave mode (when TTLEN = 1).

Work around

After PMP initial initialization is complete, and before the PMP and interrupts are enabled, clear the TTLEN bits in user software.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

22. Module: Sleep

If the ON bit (PB5DIV<15>) = 0 and PBCLK5 is disabled, a 3mA increase in Sleep IPD current occurs.

Work around

Do not disable PBCLK5 before entering Sleep mode.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

23. Module: SQI

When the SQI clock divider is used (by setting CLKDIV ≠ 0), any one of the following error conditions may occur on some of the devices, which are depending on the DDRMODE setting:

- With DDRMODE = 0, the SQI fails in reception only.
- With DDRMODE = 1, the SQI may fail in both reception and transmission.

Work around

Set the CLKDIV bits to ‘0’ and use the REFCLK02 as the SQI base clock.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

24. Module: POR

Whenever V_{DD} is less than V_{POR}, the I/O pin I/O State and logic level may be indeterminate.

Work around

None.

Affected Silicon Revisions

A1	A3	B2					
X	X						

25. Module: Crypto

Attempting to run part of a cryptographic packet through the peripheral may not result in a usable initial vector for continuing the cryptographic operation.

Work around

Do not interrupt a cryptographic operation with another, instead, always process a hash completely.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

26. Module: Crypto

Using the crypto DMA on an empty hash string will cause the peripheral to time out and not return a valid hash.

Work around

Use the fixed known hash of the empty string.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

27. Module: SPI

Just before the last block of a transmission is shifted out to the SPI pins, the SRMT bit may incorrectly indicate that the transmission is done. However, this does not affect the Transmit Buffer Empty Interrupt (STXISEL = 0).

Work around

Use the interrupt notification rather than polling the SRMT bit to determine when a transmission has completed.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

28. Module: SQI

After a Reset, the first access to the SQI SFRs must be a write. A read access can stall the CPU, requiring a Reset to clear. The typical initialization code may include a write to the SQIEN bit. The SQI1CFGbits.SQIEN=0 instruction is a read, modify, and write sequence. After a Reset, this sequence will stall the CPU. Similarly, only reading the SQI SFRs will also stall the CPU if that read is the first access after a Reset.

Work around

Be sure to enable the REFCLKO2 before reading the registers from the SQI peripheral. Do not use the "SQI1CFGbits.SQIEN=0" instruction to enable the SQI, instead use the "SQI1CFGCLR= "_SQICFG_SQIEN_MASK" instruction.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

29. Module: Sleep

Multiple sleep attempts (WAIT instruction with OSCCON<4>=1) which occur within 20 µs of a wake event, before the CPU has fully awakened, can cause the CPU to stall until a Power-on Reset (POR) event.

Work around

Be sure that at least 20 µs elapse before attempting to put the CPU to sleep (WAIT instruction with OSCCON<4>=1) after it awakens from a previous sleep.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

30. Module: Security

The note at the end of the CFGPG register (Register no. 34-10) indicates that the CPU as a system bus initiator is controlled within the CPU core is incorrect. The CPU core internal state will not control the CPU system bus initiator permission group.

Work around

Use the CFGPG register reserved bits <1:0> to control the permission group ID of the CPU as a system bus initiator.

11 = Initiator is assigned to permission group 3

10 = Initiator is assigned to permission group 2

01 = Initiator is assigned to permission group 1

00 = Initiator is assigned to permission group 0

Also, the reserved bits <:14:12> of the DEVCFG0 and ADEVCFG0 registers can be used to control the permission group ID of the CPU in Debug mode, as in:

- 1xx = Allow CPU access to permission group 2 permission regions
- x1x = Allow CPU access to permission group 1 permission regions
- xx1 = Allow CPU access to permission group 0 permission regions
- 0xx = Deny CPU access to permission group 2 permission regions
- x0x = Deny CPU access to permission group 1 permission regions
- xx0 = Deny CPU access to permission group 0 permission regions

When the CPU is in Debug mode and CFGPG<1:0> are set to a denied permission group as defined by the DEVCFG0<14:12>, the transaction request is assigned Group 3 permissions.

Affected Silicon Revisions

A1	A3	B2					
X	X						

31. Module: UART

The UART TX Stop bit duration is shorter than the expected in High-Speed mode (BRGH (UxMODE<3>) = 1) for baud rates less than 7.5 Mbps.

Work around

For baud rates less than 7.5 Mbps, operate the UART in Standard-Speed mode, that is, BRGH (UxMODE<3>) =0. For baud rates greater than 7.5 Mbps operate the UART in High-Speed mode, that is, BRGH (UxMODE<3>) =1.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

32. Module: Reset

The NMICNT bit field in the RNMICON register is 8 bits instead of 16 bits. It has limited to values 0 through 255.

Work around

The user must update the NMICNT register immediately upon entry into NMI ISR in their code with an 8-bit value not to exceed 0xFF. If the user needs to extend the NMI reset event >257 clock counts, the NMICNT register can be updated many times as required inside the NMI to ensure users NMI routine can complete before the pending reset.

Affected Silicon Revisions

A1	A3	B2					
X	X						

33. Module: I2C3

I2C3 on the A3 revision is non functional.

Work around

Silicon revision A3 I2C3 must use a software “bit-bang” implementation.

Affected Silicon Revisions

A1	A3	B2					
	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001320F):

Note:	Corrections in tables are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Pinout Updates

Updates were done to **TABLE 7: PIN NAMES FOR 144-PIN TFBGA DEVICES** to correct typographical errors. The last row of pins was corrected as follows:

N13	VDD	B13	EBID3/RPE3/PMD3/RE3
K10	**Vss**	**A13**	**EBID4/AN18/PMD4/RE4**

2. Module: DC16 VPOR Specification

Corrections were made to TABLE 37-4 for the DC16 VPOR Specification.

DC CHARACTERISTICS			**Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Operating Voltage							
DC10	VDD	Supply Voltage (Note 1)	2.1	—	3.6	V	—
DC12	VDR	RAM Data Retention Voltage (Note 2)	2.0	—	—	V	—
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal (Note 3)	**—**	—	**VSS + 0.3V**	V	—
DC17	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.000011	—	1.1	V/µs	300 ms to 3 µs @ 3.3V

APPENDIX A: REVISION HISTORY

Rev A Document (7/2015)

Initial release of this document issued for revision A1 silicon, which includes silicon issues 1. Module: (Oscillator), 2. Module: (Oscillator), 3. Module: (Oscillator), 4. Module: (Secondary Oscillator), 5. Module: (Power-Saving), 6. Module: (I^2C), 7. Module: (UART), 8. Module: (UART), 9. Module: (USB), and Power-Saving Modes.

Rev B Document (4/2016)

Added silicon issues 11. Module: (ADC) and 12. Module: (ADC).

Updated silicon issues 2. Module: (Oscillator) and 10. Module: (Power-Saving Modes).

Rev C Document (7/2016)

Updated to include silicon revision A3.

Updated silicon issues 2. Module: (Oscillator), 6. Module: (I^2C), and 11. Module: (ADC).

Added silicon issues 13. Module: (ADC), 14. Module: (ADC), 15. Module: (ADC), and 16. Module: (USB).

Added data sheet clarifications 1. Module: (Resets) and 2. Module: (Interrupt Controller).

Rev D Document (9/2016)

Updated Figure 1 and Table 3 in silicon issue 2. Module: (Oscillator).

Added silicon issues 17. Module: (Oscillator) and 18. Module: (Temperature Sensor).

Added data sheet clarification 3. Module: (External Clock Timing Requirements).

Rev E Document (3/2018)

Internal release, minor content edits gone into this release.

Rev F Document (4/2018)

Added silicon issues: 19. Module: (ICSP), 20. Module: (DMA), 21. Module: (PMP), 22. Module: (Sleep), 23. Module: (SQI), 24. Module: (POR), 25. Module: (Crypto), 26. Module: (Crypto), 27. Module: (SPI), 28. Module: (SQI), and 29. Module: (Sleep).

All data sheet clarifications were removed.

Rev G Document (6/2018)

Updated to include silicon revision B2.

Added silicon issue 30. Module:Security.

Rev H Document (9/2018)

Added Silicon issues: 31. Module:UART.

Rev J Document (03/2019)

Added Silicon Issue 32. Module:Reset.

Added Data Sheet Clarifications: 1. Module:Pinout Updates, 2. Module:DC16 VPOR Specification, and 33. Module:I2C3.

Updated Silicon Issue 2. Module:Oscillator.

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