1-Introduction:

The main idea behind of this project is for us to learn about how to design and implement a finite state machine that models a specified behavior and to use the Xilinx ISE software to design and test these state machines. Finite State Machines (FSMs) are a powerful tool that can be used to model many real-world systems, and are particularly useful for the behavioral modelling of sequential circuits. An FSM has a finite number of 'states' and can be in any one of these states at a given time. The machine transitions from one state to another based on the inputs it receives and the state that it is currently in. There are two kinds of FSM machines: Moore Machine and Mealy Machine. Moore machine is a FSM in which its output only depends on which state it is in, but a Mealy machine its output depends on both the current state and input.

2-Requirement:

For this assignment, we're tasked with designing a vending machine with the following characteristics:

1. Vending machine has 20 different snacks for sale. Each snack has two-digit code (00 to 19).

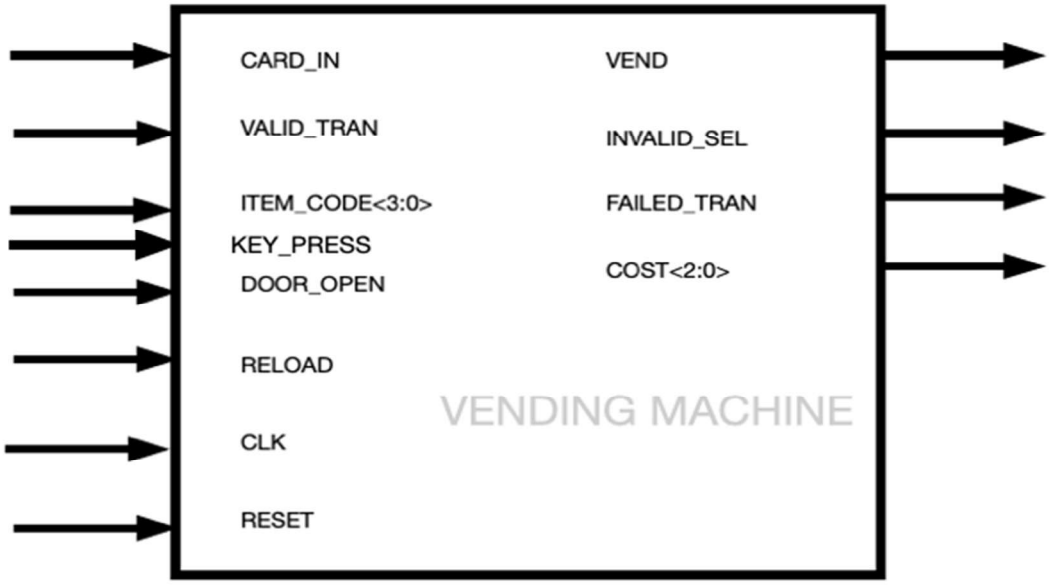
2. Each snack is stored in separate slot. There can be up to 10 units of snack stored in 1 slot.

3. A buyer can purchase only 1 item at a time.

4. The machine only accepts payment by card.

3-Design Description:

For this assignment, I designed my FSM following to the guidance of the lab description. The vending Machine is designed to have the following inputs and outputs:

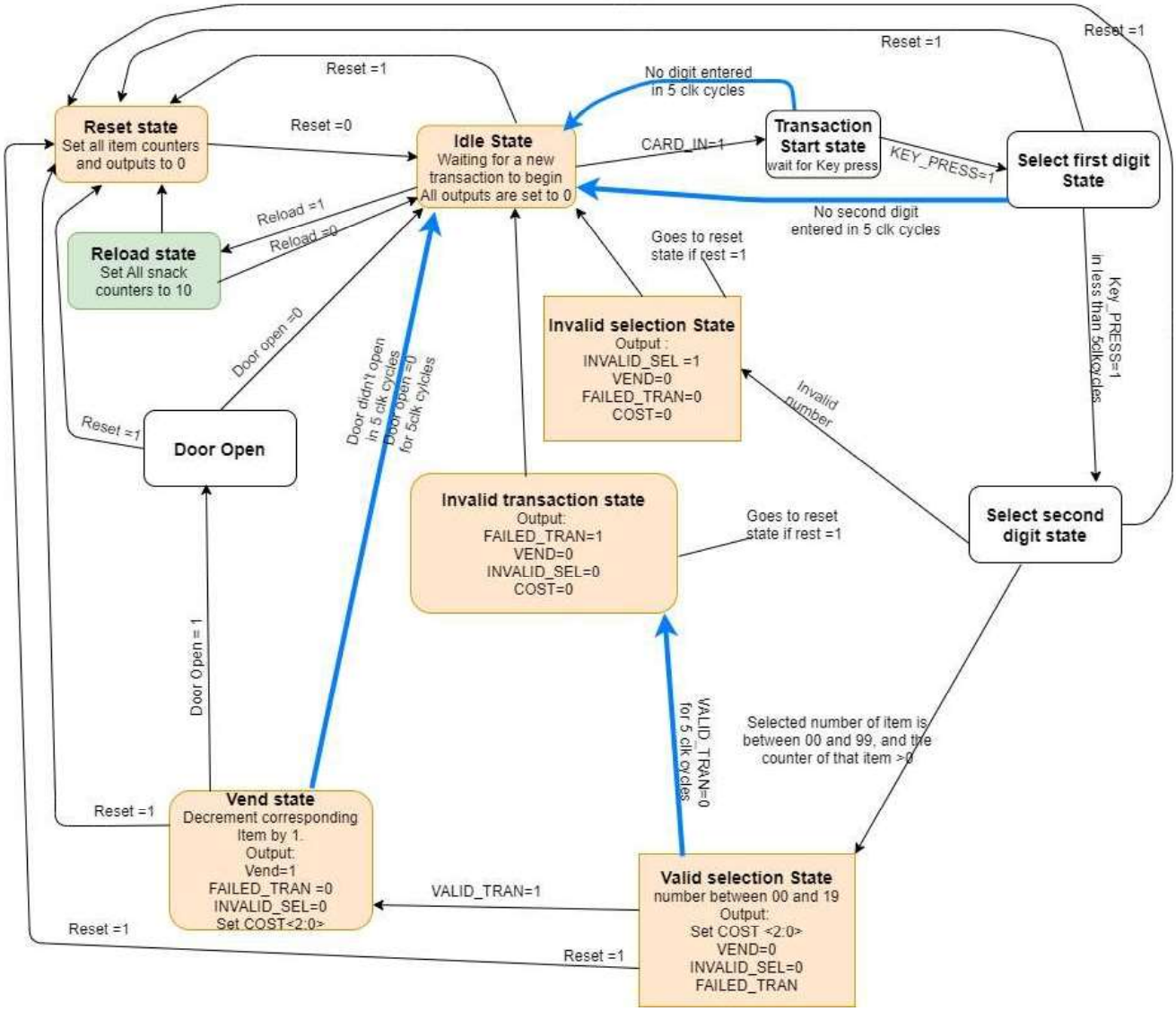


The COST output should be determined based on the user entered ITEM_CODE following this this table:

ITEM CODE	COST ($)	ITEM CODE	COST ($)
00, 01,02,03	1	12,13,14,15	4
04,05,06,07	2	16,17	5
08,09,10,11	3	18,19	6

I designed my vending machine using around 11 states to correctly models the behavior described in the lab requirements.

My states diagram is designed as follow:



State diagram of the vending machine

Descriptions of states and transitions:

In the RESET state all item counters and outputs are set to 0. The FSM transition to this state whenever RST input is set to 1. When RST is set to 0 the FSM transition to IDLE state in which the machine will be waiting for a transaction to start.

When RELOAD input is set to 1 the FSM transition to the reload state where all snack items are set 10 modeling the reload of items' stocks. When RELOAD is set to 0, the machine will transition to IDLE state to wait for a transition to start.

In IDLE state, if the CARD_IN input is set to 1, the FSM will transition to Transaction Start state in which the machine would wait the first digit to be entered. If the first digit is not entered in 5 clocks cycles the machine will return to IDLE state.

If the first digit is entered, the machine would transition to the Select first Digit state in which it would wait for the second digit to be entered. If the second digit is not entered, the machine would transition to IDLE state.

If the second digit is entered, the machine would transition to Select Second Digit state in which the machine would check if the two digits are valid and the stock of the chosen item is greater than 0.

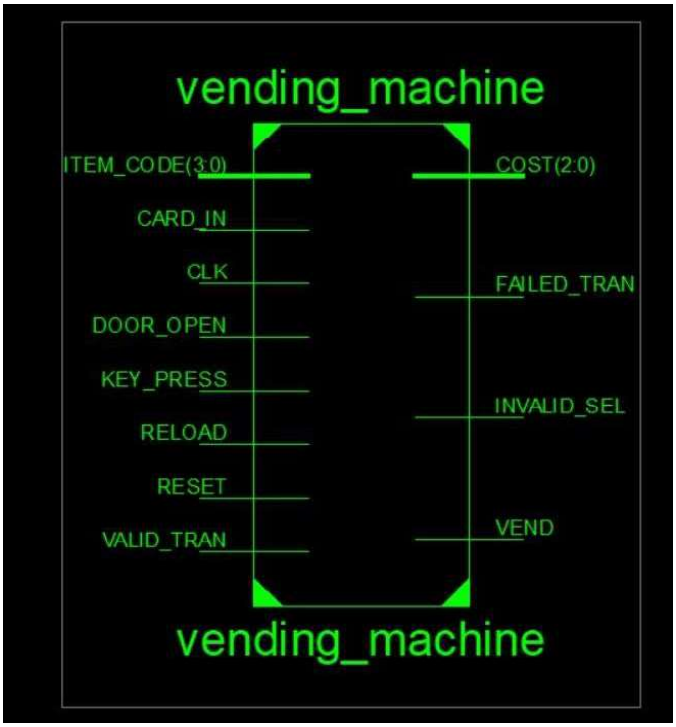
If the two digits are invalid (are not between 00 and 19) or the stock of the chosen item is equal to 0, then the machine would transition to Invalid Selection sate in which the INVALID_SEL output will be set to 1, and then the machine would transition to IDLE to wait for a new state.

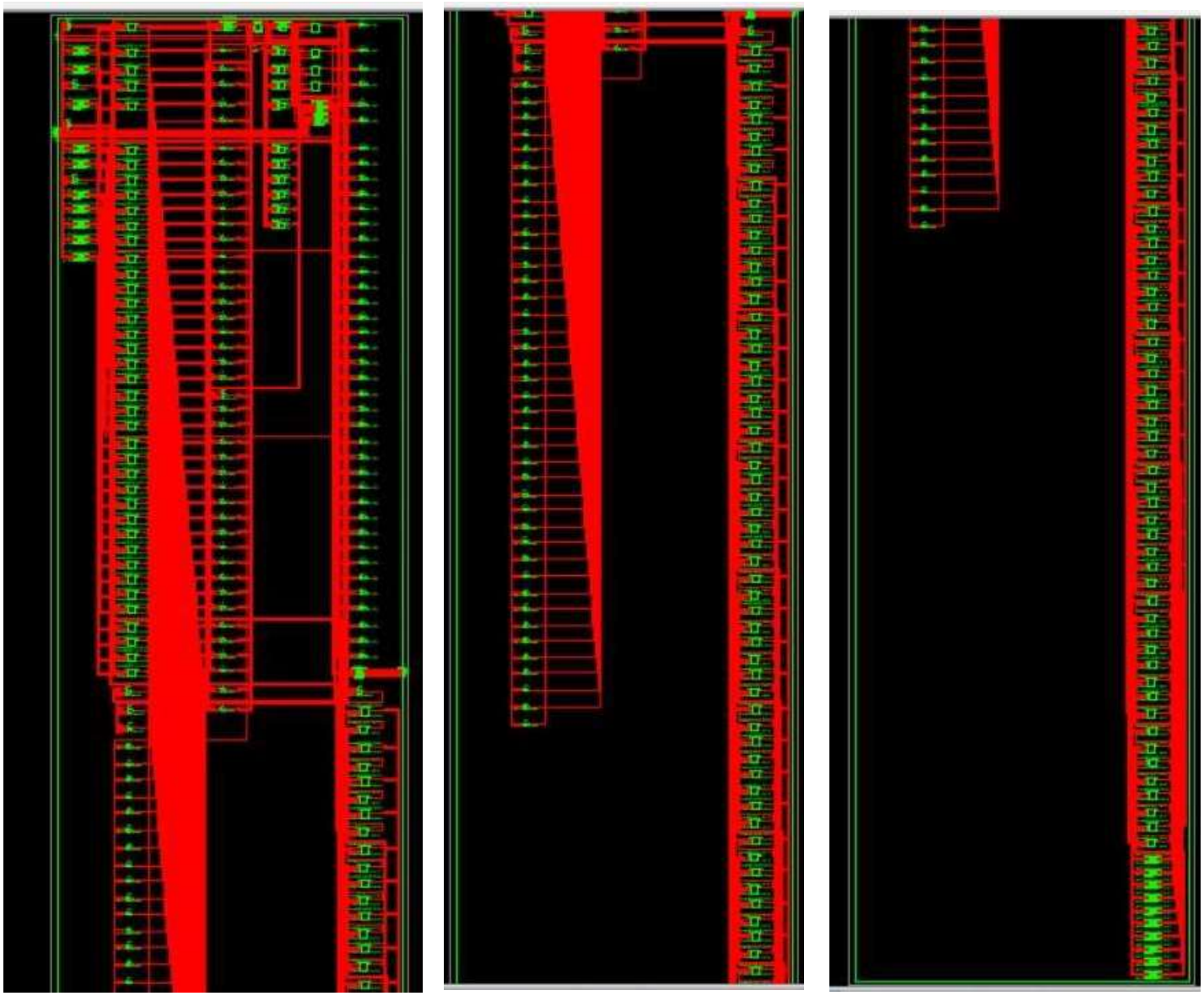
If the two digits are valid and there is enough in stock of the chosen item, the FSM would transition to Valid Selection state in which the COST output will be set with corresponding cost of the chosen item's code. In the state, the machine will wait for VALID_TRAN signal.

If VALID_TRAN is not set to 1 in 5 cycles, the machine would transition to Invalid Transaction state in which the machine would set FAILED-TRAN output to 1, and then it would transition to IDLE to wait for a new transaction.

If the VALID_TRAN is set to 1 in less than 5 cycles, the machine would transition to Vend state in which the VEND output set to 1 and the stock of the corresponding item would decrement by 1. In this state, the machine also wat for DOOR_OPEN to be set to 1 and then to be set to 0 to transition to IDLE state to wait for anew transaction. If the DOOR_OPEN is not set to 1 in 5 clock cycles the machine would transition to IDLE state.

4-The RTL Schematic:





The RTL Schematic divided in thee part top-middle-bottom (first - second -third)

The vending machine as a top module contains three modules:

FiveCounter module: responsible on counting the cycles required to transition to the next state if the required in put is not set to 1.

StateController module: responsible on transitioning the machine from the current state to a specified state based on the current state.

Output module: responsible on setting the output of machine for each state that the machine transition to.

5-Simulation Testbench:

To test if my vending machine works appropriately, I designed the testbench to test all the cases including the tests that would terminate with a successful operation and the others that would fail depending in a given scenario.

As for the successful operations test I created two tests:

One by providing an item code less than 10 and the other by providing an item code more than to test the behavior of the machine on providing the correct cost for both items and show that the operation flow correctly in a successful manner.

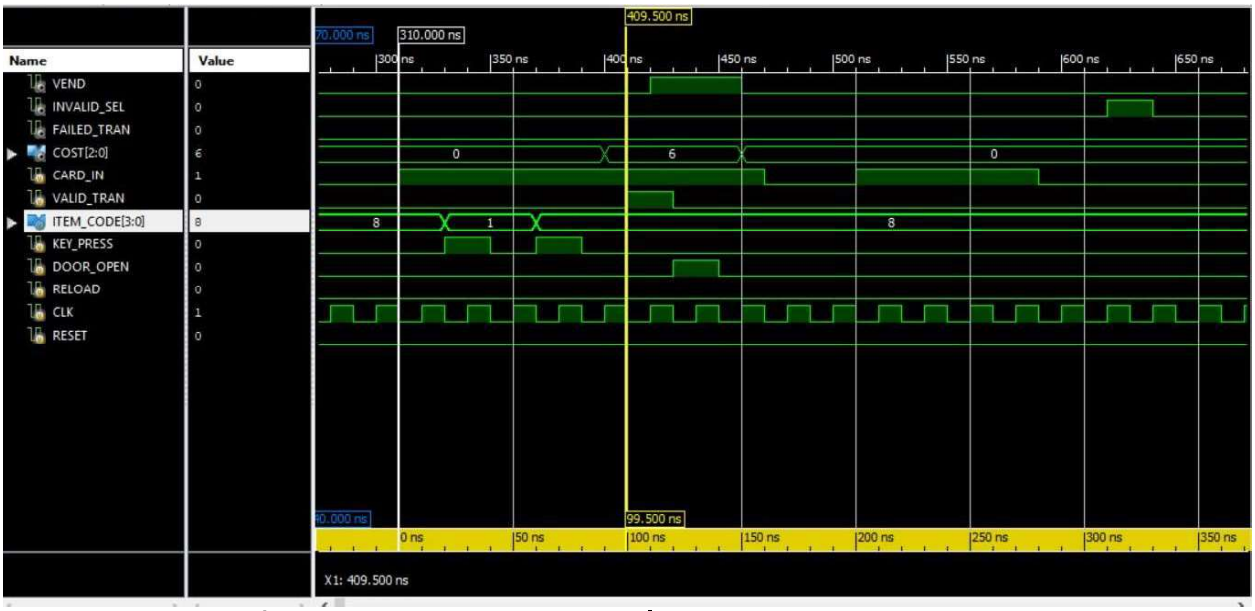
- **Successful operation with code item less than 10**

First, we reset the machine (20ns) to make sure that all items stock, and the outputs are properly set to 0. Then We put the machine in reload state by setting the RELOAD input to 1 at (70ns).

Firstly, at the time 100ns the CARD_IN input is set to high to mimic the card insert. At the time 130ns we submitted the first digit which was 0, and at 170ns we submitted the second digit which was 8. The machine in this state is waiting for valid transaction signal which will occur at the time 210ns (less than 5 clock cycles). Then the machine would transition to VEND state at the time 220ns which will wait for the DOOR OPEN signal to go high and go down to transition to IDLE state. The DOOR_OPEN input will go high at the time 230ns and then will go down at the 250ns, and right after that the machine would transition to IDLE state. At that time, we set the CARD_IN signal to low. This test simulates a successful operation in which our vending machine performed correctly. We also noticed that the output COST in this test after we entered the second digit is 3 which is the correct cost of the item code 08 entered in this test.

- **Successful operation with code item greater than 10:**

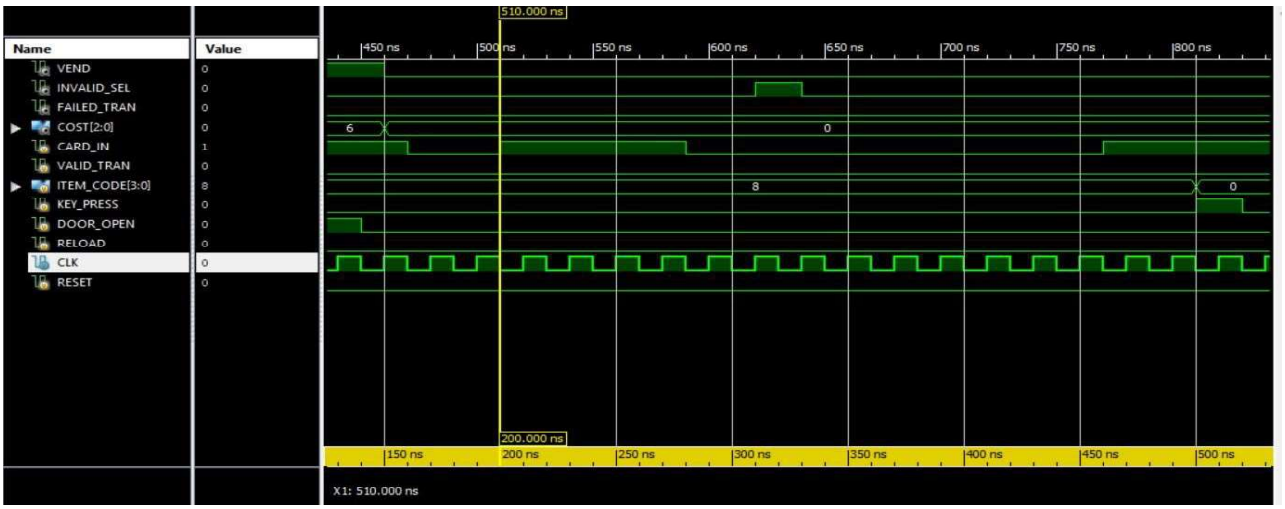
This test is similar to the previous test except is that it is performed to test if the cost output is calculated correctly for items greater than 10.



As we can see that for an entered item code equal to 18 the cost outputted is 6 which is the correct cost corresponding to the item code 18 based on the given table.

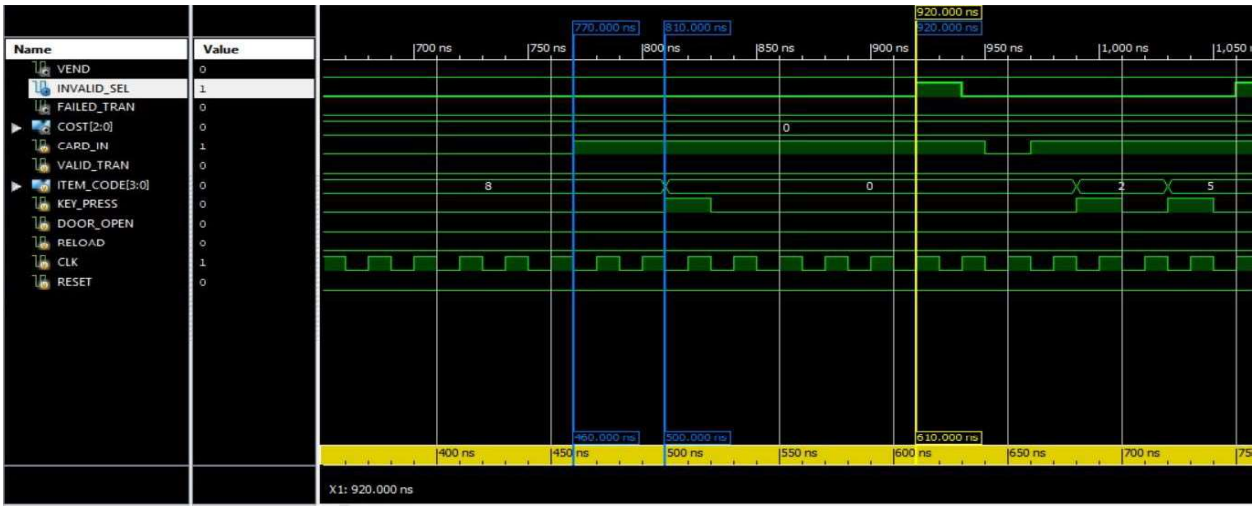
- **Failed Operation test with no digit entered.**

In this case, we set the CARD_IN to high and we didn't enter no digit. The normal flow if the machine indicate that the machine should set the INVALID_SEL output to high and transition to IDLE state. This is exactly what our vending machine did. As at the time 510ns, we set the CARD_IN input to high and we didn't enter any code item. After 5 cycles (at 620ns), INVALID_SEL was set to high and the machine transitioned to IDLE state.



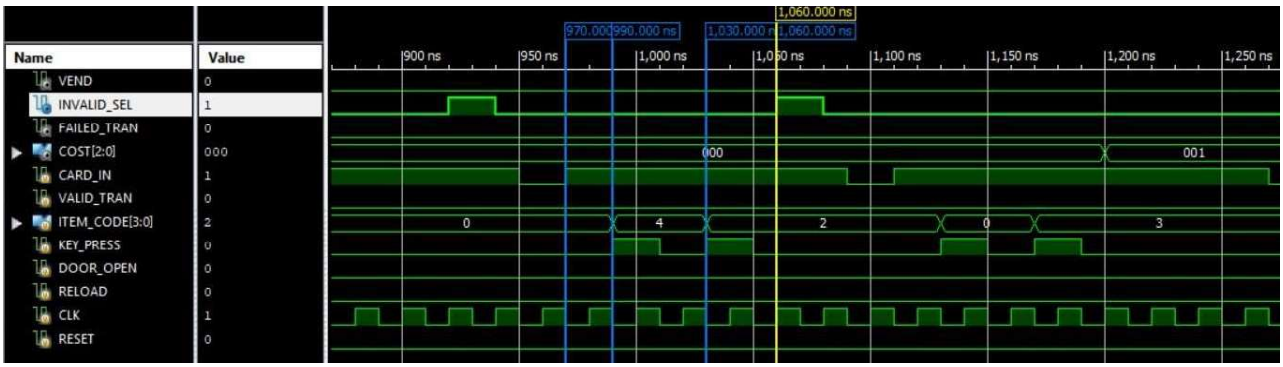
- **Failed Operation with only one digit entered:**

In this case, we simulated the scenario when a user enters his card but it will enter only one digit. In this case, machine would have to wait for the second digit to be entered for 5 clocks cycles. If no digit is entered during that time. The machine would set the INVALID_SEL output to 1 and transition to IDLE state. This is exactly what our machine did. At the time 770ns, we set CARD_IN input to 1 and then at the time 810ns we entered the first digit which was 0. The machine waited for 5 clock cycles and then it set the INVALID_SEL output to 1 at 920ns and transitioned to IDLE state.



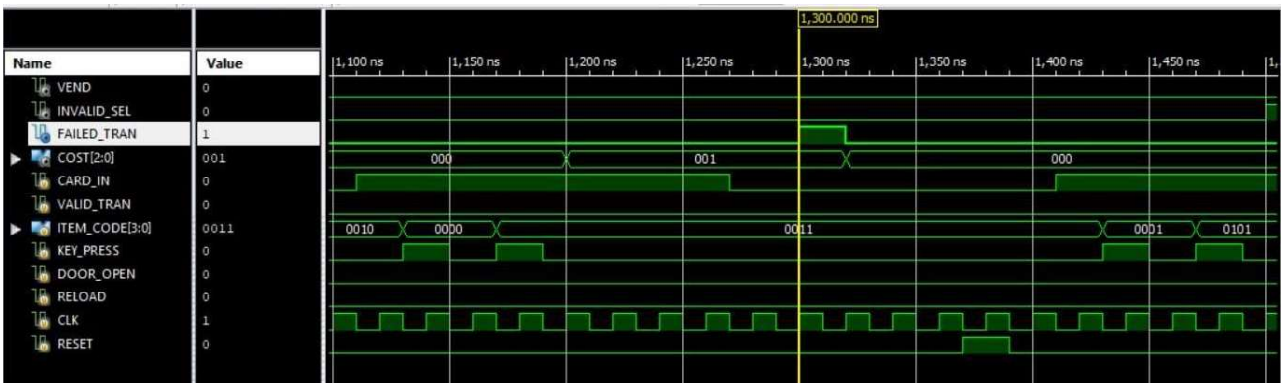
- **Failed operation by entering Invalid digits**

For this case, we entered an item code of 42 which is not within the range 00 to 19. For this case the machine would immediately set the INVALID_SEL output to 1 and transition to IDLE state. And this exactly what our machine did. As at the time 970ns we set CARD_IN to 1 and then we entered the first digit at the time 990ns which was 4. At the time, 1030ns we entered the second digit which was 2. At the time 1060, the machine set the INVALID_SEL output to 1 and transitioned to IDLE state.



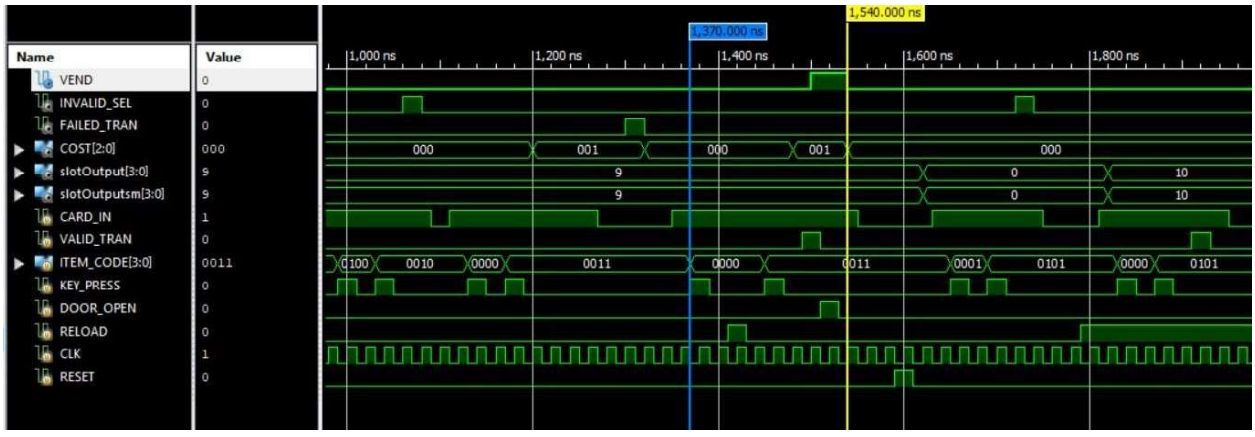
- **Failed Operation with no valid transaction signal.**

For this test I simulated the case where the machine didn't receive a valid transaction signal. After setting CARD_IN to 1 and entering the two digits correctly. The machine is now waiting for VALID_TRAN input signal to be set to 1 to complete the operation. The machine would wait for 5 clock cycles. If the the VALID_TRAN is not set to 1 during that time, the Machine would set the FAILED_TRAN output to 1 and transition to IDLE state. This is exactly what happened in our machine as the FAILED_TRAN output was set to 1 at the time 1300ns and then machine transitioned to IDLE.



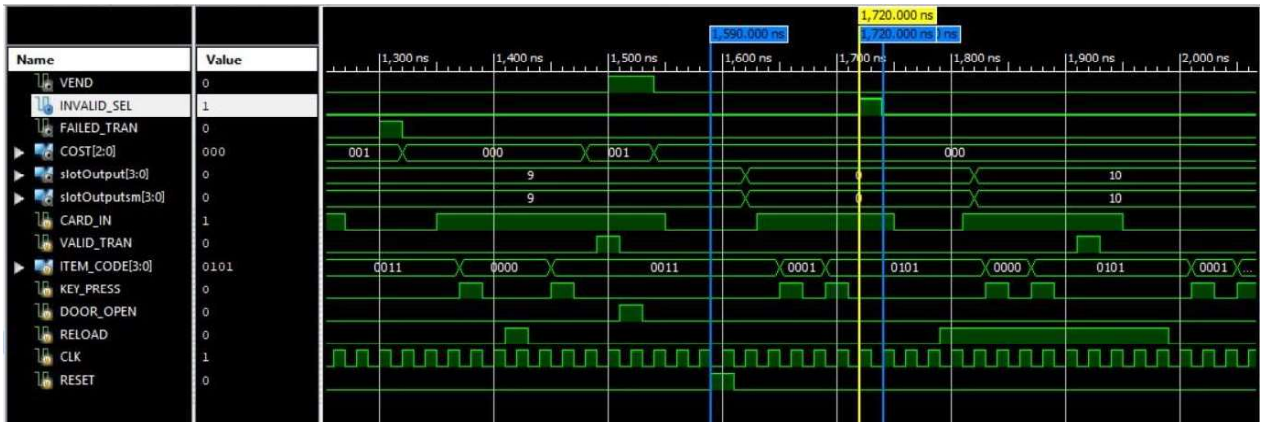
- **Reloading the machine during a transaction.**

As the machine should transition to the reload transition only when it is in IDLE state, the machine should not transition to the reloading state and should continue its transaction. In this test we set the RELOAD input to high just after entering the first digit which didn't affect the machine. The machine continued the transaction successfully and items counters are still at 9 (as the items were purchased in earlier transactions). This test is illustrated between the time frames 1370ns and 1540ns



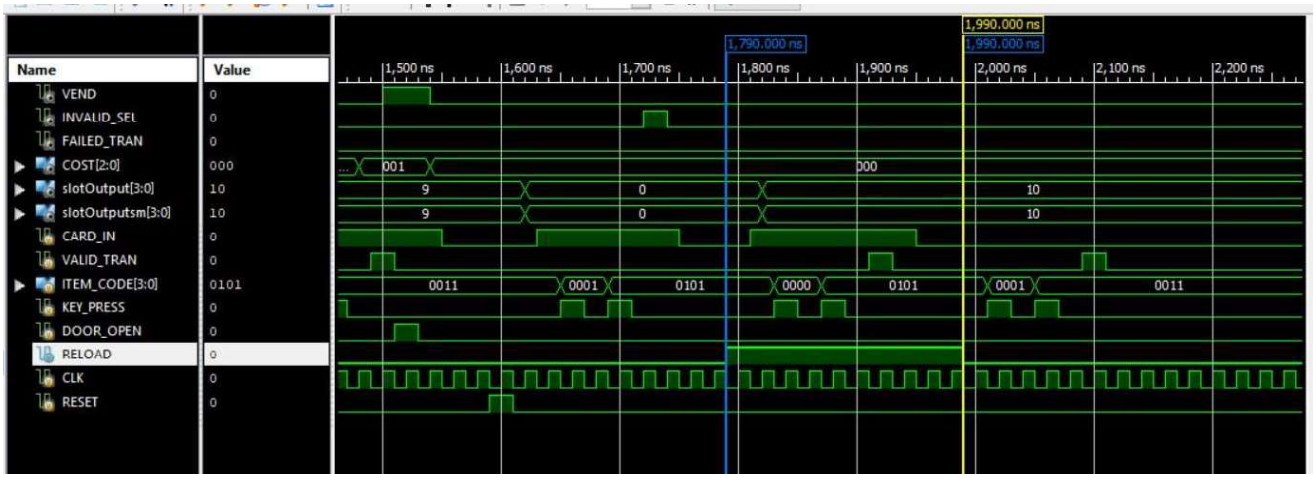
- **Failed Operation when there is no item in stock:**

To simulate this test, we reset the machine to put all items' stock to 0. And the we proceeded with a normal operation by setting the CARD_IN to one and entering the two digits. Right after entering the second digit, the Machine would set INVALID_SEL to 1 at the time 1720ns, and it transitioned to IDLE state.



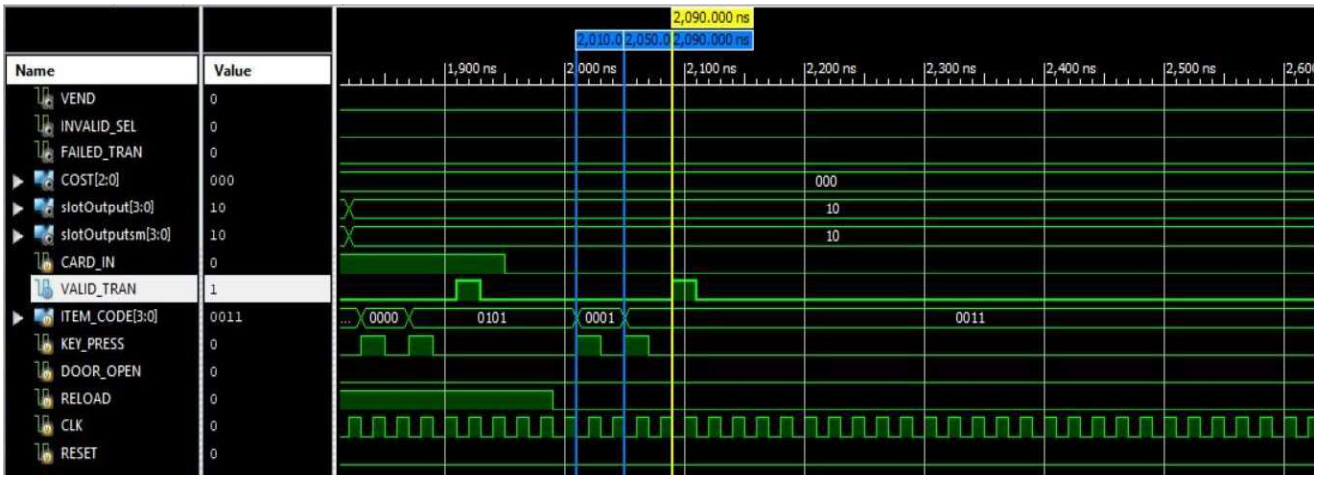
- **Failed transaction when RELOAD is set to 1:**

In this test, we simulated the case where we start an operation while the machine in the reloading state. In this state, the machine should remain in the reloading state and not output should be set illustrating that no transaction has been started. In this case, we proceeded with normal operation by setting CARD_IN to 1 and entering the two digits. After that we set VALID_TRAN to 1, but nothing has been changed in the machine and no out put is set to 1. This what has been shown between the time frames: 1970ns -1990ns



- **Failed Operation without inserting the card.**

We simulated this case by starting an operation without setting the input CARD_IN to 1. We Entered the first digit at the time frame 2010ns the second digit at 2050ns. Then, I set VALID_TRAN to 1 at 2090ns. We see that the machine didn't change the state and remained in the IDLE state and no output was set to 1.



6-Conclusion:

In this assignment, I built a parking meter FSM that models the behavior described in project description. This FSM is built in Moore machine. One of the most difficulties that I encountered in this assignment is how to deal with several states, transition between them, and keep track of the 5 cycles counting. Drawing the state diagram was very useful to overcome these difficulties.

7-Synthesize summary:

```
=========================================================================
*                      Design Summary                   *
=========================================================================

Top Level Output File Name         : vending_machine.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                   : 176
#      INV                : 1
#      LUT2               : 1
#      LUT3               : 3
#      LUT4               : 48
#      LUT5               : 53
```

```
#      LUT6                : 67
#      MUXF7               : 2
#      VCC                 : 1
# FlipFlops/Latches        : 82
#      FD                  : 23
#      FDR                 : 12
#      FDRE                : 25
#      FDS                 : 2
#      LD                  : 14
#      LDC                 : 1
#      LDCE                : 3
#      LDCE_1              : 1
#      LDE_1               : 1
# Clock Buffers            : 1
#      BUFGP               : 1
# IO Buffers               : 24
#      IBUF                : 10
#      OBUF                : 14

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice Registers:            79  out of  18224     0%
 Number of Slice LUTs:                173  out of   9112     1%
    Number used as Logic:             173  out of   9112     1%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:   182
   Number with an unused Flip Flop:    103  out of    182    56%
   Number with an unused LUT:            9  out of    182     4%
   Number of fully used LUT-FF pairs:   70  out of    182    38%
   Number of unique control sets:       12

IO Utilization:
 Number of IOs:                       25
 Number of bonded IOBs:               25  out of    232    10%
    IOB Flip Flops/Latches:           3

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:             1  out of     16     6%
```

Partition Resource Summary:

No Partitions were found in this design.

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Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

Clock Signal	Clock buffer(FF name)	Load
CLK	BUFGP	62
c2/current_state[3]_GND_3_o_MUX_253_o(c2/Mmux_current_state[3]_GND_3_o_MUX_253_o11:O)	NONE(*)(c2/next_state_1)	5
c2/current_state[3]_GND_3_o_equal_1_o(c2/current_state[3]_GND_3_o_equal_1_o1:O)	NONE(*)(c2/firstDigitinputted)	1
c2/current_state[3]_current_state[3]_AND_47_o(c2/current_state[3]_current_state[3]_AND_47_o1:O)	NONE(*)(c2/secondDigit_0)	4
c2/current_state[3]_current_state[3]_AND_17_o(c2/current_state[3]_current_state[3]_AND_17_o1:O)	NONE(*)(c2/firstDigit_0)	4
c3/current_state[3]_GND_18_o_equal_10_o(c3/current_state[3]_GND_18_o_equal_10_o<3>1:O)	NONE(*)(c3/cost_0)	4
c3/current_state[3]_current_state[3]_AND_76_o(c3/current_state[3]_current_state[3]_AND_76_o1:O)	NONE(*)(c3/vend)	1
c3/invalid_G(c3/current_state[3]_current_state[3]_OR_168_o1:O)	NONE(*)(c3/invalid)	1

(*) These 7 clock signal(s) are generated by combinatorial logic,
and XST is not able to identify which are the primary clock signals.
Please use the CLOCK_SIGNAL constraint to specify the clock signal(s) generated by combinatorial logic.
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST with BUFG/BUFR resources. Please use the buffer_type constraint in order to insert these buffers to the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -3

  Minimum period: 3.267ns (Maximum Frequency: 306.119MHz)
  Minimum input arrival time before clock: 4.582ns
  Maximum output required time after clock: 3.820ns
  Maximum combinational path delay: No path found

Timing Details:

All values displayed in nanoseconds (ns)

===
Timing constraint: Default period analysis for Clock 'CLK'
  Clock period: 3.267ns (frequency: 306.119MHz)
  Total number of paths / destination ports: 607 / 95

Delay: 3.267ns (Levels of Logic = 3)
  Source: array4_0_33 (FF)
  Destination: array4_0_34 (FF)
  Source Clock: CLK rising
  Destination Clock: CLK rising

  Data Path: array4_0_33 to array4_0_34
                            Gate   Net
    Cell:in->out   fanout   Delay   Delay Logical Name (Net Name)
    -- ------------
     FDRE:C->Q   5   0.447   0.943 array4_0_33 (array4_0_33)
     LUT6:I3->O   1   0.205   0.580 Mmux_array4[19][3]_array4[19][3]_mux_49_OUT281
(array4[19][3]_array4[19][3]_mux_49_OUT<34>)
     LUT5:I4->O   1   0.205   0.580 array4_0_34_dpot (array4_0_34_dpot)
     LUT4:I3->O   1   0.205   0.000 array4_0_34_rstpot (array4_0_34_rstpot)
     FD:D   0.102   array4_0_34

    Total   3.267ns (1.164ns logic, 2.103ns route)
                              (35.6% logic, 64.4% route)

===
Timing constraint: Default period analysis for Clock 'c2/current_state[3]_GND_3_o_equal_1_o'
  Clock period: 2.537ns (frequency: 394.120MHz)

```
  Total number of paths / destination ports: 1 / 1
-------------------------------------------------------------------
Delay:               2.537ns (Levels of Logic = 1)
  Source:            c2/firstDigitinputted (LATCH)
  Destination:       c2/firstDigitinputted (LATCH)
  Source Clock:      c2/current_state[3]_GND_3_o_equal_1_o rising
  Destination Clock: c2/current_state[3]_GND_3_o_equal_1_o rising

  Data Path: c2/firstDigitinputted to c2/firstDigitinputted
                            Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LDE_1:G->Q           13   0.498   0.933  c2/firstDigitinputted (c2/firstDigitinputted)
     LUT6:I5->O            1   0.205   0.579  c2/current_state[3]_current_state[3]_OR_160_o
(c2/current_state[3]_current_state[3]_OR_160_o)
     LDE_1:GE                  0.322          c2/firstDigitinputted
    ----------------------------------------
    Total                      2.537ns (1.025ns logic, 1.512ns route)
                               (40.4% logic, 59.6% route)

=========================================================================
Timing constraint: Default period analysis for Clock
'c2/current_state[3]_current_state[3]_AND_47_o'
  Clock period: 2.192ns (frequency: 456.223MHz)
  Total number of paths / destination ports: 4 / 4
-------------------------------------------------------------------
Delay:               2.192ns (Levels of Logic = 1)
  Source:            c2/secondDigit_1 (LATCH)
  Destination:       c2/secondDigit_1 (LATCH)
  Source Clock:      c2/current_state[3]_current_state[3]_AND_47_o falling
  Destination Clock: c2/current_state[3]_current_state[3]_AND_47_o falling

  Data Path: c2/secondDigit_1 to c2/secondDigit_1
                            Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q              26   0.498   1.454  c2/secondDigit_1 (c2/secondDigit_1)
     LUT5:I1->O            1   0.203   0.000  c2/Mmux_secondDigit[3]_secondDigit[3]_MUX_382_o11
(c2/secondDigit[3]_secondDigit[3]_MUX_382_o)
     LD:D                      0.037          c2/secondDigit_1
    ----------------------------------------
    Total                      2.192ns (0.738ns logic, 1.454ns route)
                               (33.7% logic, 66.3% route)

=========================================================================
```

```
Timing constraint: Default period analysis for Clock
'c2/current_state[3]_current_state[3]_AND_17_o'
  Clock period: 2.377ns (frequency: 420.757MHz)
  Total number of paths / destination ports: 4 / 4
-------------------------------------------------------------------
Delay:               2.377ns (Levels of Logic = 1)
  Source:            c2/firstDigit_0 (LATCH)
  Destination:       c2/firstDigit_0 (LATCH)
  Source Clock:      c2/current_state[3]_current_state[3]_AND_17_o falling
  Destination Clock: c2/current_state[3]_current_state[3]_AND_17_o falling

  Data Path: c2/firstDigit_0 to c2/firstDigit_0
                          Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q              39   0.498   1.639  c2/firstDigit_0 (c2/firstDigit_0)
     LUT5:I1->O            1   0.203   0.000  c2/Mmux_firstDigit[3]_firstDigit[3]_MUX_344_o11
(c2/firstDigit[3]_firstDigit[3]_MUX_344_o)
     LD:D                      0.037          c2/firstDigit_0
    ----------------------------------------
    Total                      2.377ns (0.738ns logic, 1.639ns route)
                               (31.1% logic, 68.9% route)

=========================================================================
Timing constraint: Default period analysis for Clock 'c3/current_state[3]_GND_18_o_equal_10_o'
  Clock period: 1.585ns (frequency: 630.815MHz)
  Total number of paths / destination ports: 3 / 3
-------------------------------------------------------------------
Delay:               1.585ns (Levels of Logic = 1)
  Source:            c3/cost_2 (LATCH)
  Destination:       c3/cost_2 (LATCH)
  Source Clock:      c3/current_state[3]_GND_18_o_equal_10_o falling
  Destination Clock: c3/current_state[3]_GND_18_o_equal_10_o falling

  Data Path: c3/cost_2 to c3/cost_2
                          Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LDCE:G->Q             2   0.498   0.845  c3/cost_2 (c3/cost_2)
     LUT6:I3->O            1   0.205   0.000  c3/Mmux_cost[2]_cost[2]_MUX_444_o12
(c3/cost[2]_cost[2]_MUX_444_o)
     LDCE:D                    0.037          c3/cost_2
    ----------------------------------------
    Total                      1.585ns (0.740ns logic, 0.845ns route)
                               (46.7% logic, 53.3% route)
```

```
==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'CLK'
  Total number of paths / destination ports: 14 / 14
--------------------------------------------------------------------------
Offset:              2.633ns (Levels of Logic = 1)
  Source:            RESET (PAD)
  Destination:       current_state_0 (FF)
  Destination Clock: CLK rising

  Data Path: RESET to current_state_0
                            Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            15   1.222   0.981  RESET_IBUF (RESET_IBUF)
     FDS:S                     0.430          current_state_0
    ----------------------------------------
    Total                      2.633ns (1.652ns logic, 0.981ns route)
                               (62.7% logic, 37.3% route)

==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock
'c2/current_state[3]_GND_3_o_MUX_253_o'
  Total number of paths / destination ports: 23 / 5
--------------------------------------------------------------------------
Offset:              3.727ns (Levels of Logic = 4)
  Source:            KEY_PRESS (PAD)
  Destination:       c2/next_state_3 (LATCH)
  Destination Clock: c2/current_state[3]_GND_3_o_MUX_253_o falling

  Data Path: KEY_PRESS to c2/next_state_3
                            Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            16   1.222   1.005  KEY_PRESS_IBUF (KEY_PRESS_IBUF)
     LUT6:I5->O            1   0.205   0.924  c2/Mmux_GND_3_o_next_state[3]_mux_88_OUT<0>182
(c2/Mmux_GND_3_o_next_state[3]_mux_88_OUT<0>181)
     LUT6:I1->O            1   0.203   0.000  c2/Mmux_GND_3_o_next_state[3]_mux_88_OUT<0>187_F
(N49)
     MUXF7:I0->O           1   0.131   0.000  c2/Mmux_GND_3_o_next_state[3]_mux_88_OUT<0>187
(c2/GND_3_o_next_state[3]_mux_88_OUT<3>)
     LD:D                      0.037          c2/next_state_3
    ----------------------------------------
    Total                      3.727ns (1.798ns logic, 1.929ns route)
                               (48.2% logic, 51.8% route)
```

```
==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock
'c2/current_state[3]_GND_3_o_equal_1_o'
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------
Offset:              4.582ns (Levels of Logic = 3)
  Source:            KEY_PRESS (PAD)
  Destination:       c2/firstDigitinputted (LATCH)
  Destination Clock: c2/current_state[3]_GND_3_o_equal_1_o rising

  Data Path: KEY_PRESS to c2/firstDigitinputted
                          Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------  ------------
     IBUF:I->O            16   1.222   1.369  KEY_PRESS_IBUF (KEY_PRESS_IBUF)
     LUT6:I0->O            1   0.203   0.684  c2/current_state[3]_current_state[3]_OR_160_o_SW0
(N23)
     LUT6:I4->O            1   0.203   0.579  c2/current_state[3]_current_state[3]_OR_160_o
(c2/current_state[3]_current_state[3]_OR_160_o)
     LDE_1:GE                  0.322          c2/firstDigitinputted
    ----------------------------------
    Total                     4.582ns (1.950ns logic, 2.632ns route)
                              (42.6% logic, 57.4% route)

==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock
'c2/current_state[3]_current_state[3]_AND_47_o'
  Total number of paths / destination ports: 8 / 4
--------------------------------------------------------------------------
Offset:              2.571ns (Levels of Logic = 2)
  Source:            KEY_PRESS (PAD)
  Destination:       c2/secondDigit_0 (LATCH)
  Destination Clock: c2/current_state[3]_current_state[3]_AND_47_o falling

  Data Path: KEY_PRESS to c2/secondDigit_0
                          Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------  ------------
     IBUF:I->O            16   1.222   1.109  KEY_PRESS_IBUF (KEY_PRESS_IBUF)
     LUT5:I3->O            1   0.203   0.000  c2/Mmux_secondDigit[3]_secondDigit[3]_MUX_356_o11
(c2/secondDigit[3]_secondDigit[3]_MUX_356_o)
     LD:D                      0.037          c2/secondDigit_3
    ----------------------------------
    Total                     2.571ns (1.462ns logic, 1.109ns route)
```

(56.9% logic, 43.1% route)

==========

Timing constraint: Default OFFSET IN BEFORE for Clock 'c2/current_state[3]_current_state[3]_AND_17_o'
  Total number of paths / destination ports: 8 / 4

Offset: 2.697ns (Levels of Logic = 2)
  Source: KEY_PRESS (PAD)
  Destination: c2/firstDigit_0 (LATCH)
  Destination Clock: c2/current_state[3]_current_state[3]_AND_17_o falling

  Data Path: KEY_PRESS to c2/firstDigit_0

Cell:in->out	Gate fanout	Net Delay	Delay	Logical Name (Net Name)
IBUF:I->O	16	1.222	1.233	KEY_PRESS_IBUF (KEY_PRESS_IBUF)
LUT5:I2->O	1	0.205	0.000	c2/Mmux_firstDigit[3]_firstDigit[3]_MUX_311_o11 (c2/firstDigit[3]_firstDigit[3]_MUX_311_o)
LD:D		0.037		c2/firstDigit_3
Total		2.697ns (1.464ns logic, 1.233ns route) (54.3% logic, 45.7% route)		

==========

Timing constraint: Default OFFSET IN BEFORE for Clock 'c3/current_state[3]_GND_18_o_equal_10_o'
  Total number of paths / destination ports: 4 / 4

Offset: 3.346ns (Levels of Logic = 2)
  Source: RELOAD (PAD)
  Destination: c3/cost_0 (LATCH)
  Destination Clock: c3/current_state[3]_GND_18_o_equal_10_o falling

  Data Path: RELOAD to c3/cost_0

Cell:in->out	Gate fanout	Net Delay	Delay	Logical Name (Net Name)
IBUF:I->O	6	1.222	0.745	RELOAD_IBUF (RELOAD_IBUF)
LUT5:I4->O	6	0.205	0.744	c3/current_state[3]_current_state[3]_OR_168_o1 (c3/invalid_G)
LDCE:CLR		0.430		c3/cost_2
Total		3.346ns (1.857ns logic, 1.489ns route) (55.5% logic, 44.5% route)		

```
==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock
'c3/current_state[3]_current_state[3]_AND_76_o'
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------
Offset:              3.346ns (Levels of Logic = 2)
  Source:            RELOAD (PAD)
  Destination:       c3/vend (LATCH)
  Destination Clock: c3/current_state[3]_current_state[3]_AND_76_o falling

  Data Path: RELOAD to c3/vend
                          Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------  ------------
     IBUF:I->O             6   1.222   0.745  RELOAD_IBUF (RELOAD_IBUF)
     LUT5:I4->O            6   0.205   0.744  c3/current_state[3]_current_state[3]_OR_168_o1
(c3/invalid_G)
     LDC:CLR                   0.430          c3/vend
    ----------------------------------------
    Total                      3.346ns (1.857ns logic, 1.489ns route)
                               (55.5% logic, 44.5% route)

==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'c3/invalid_G'
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------
Offset:              2.454ns (Levels of Logic = 2)
  Source:            RELOAD (PAD)
  Destination:       c3/invalid (LATCH)
  Destination Clock: c3/invalid_G falling

  Data Path: RELOAD to c3/invalid
                          Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------  ------------
     IBUF:I->O             6   1.222   0.992  RELOAD_IBUF (RELOAD_IBUF)
     LUT5:I1->O            1   0.203   0.000  c3/invalid_D (c3/invalid_D)
     LD:D                      0.037          c3/invalid
    ----------------------------------------
    Total                      2.454ns (1.462ns logic, 0.992ns route)
                               (59.6% logic, 40.4% route)

==========================================================================
```

```
Timing constraint: Default OFFSET OUT AFTER for Clock
'c3/current_state[3]_GND_18_o_equal_10_o'
  Total number of paths / destination ports: 4 / 4
--------------------------------------------------------------------------
Offset:              3.685ns (Levels of Logic = 1)
  Source:            c3/cost_2 (LATCH)
  Destination:       COST<2> (PAD)
  Source Clock:      c3/current_state[3]_GND_18_o_equal_10_o falling

  Data Path: c3/cost_2 to COST<2>
                          Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LDCE:G->Q             2   0.498   0.616  c3/cost_2 (c3/cost_2)
     OBUF:I->O                 2.571          COST_2_OBUF (COST<2>)
    ----------------------------------------
    Total                      3.685ns (3.069ns logic, 0.616ns route)
                               (83.3% logic, 16.7% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'CLK'
  Total number of paths / destination ports: 8 / 8
--------------------------------------------------------------------------
Offset:              3.820ns (Levels of Logic = 1)
  Source:            array4_0_32 (FF)
  Destination:       slotOutput<0> (PAD)
  Source Clock:      CLK rising

  Data Path: array4_0_32 to slotOutput<0>
                          Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q               8   0.447   0.802  array4_0_32 (array4_0_32)
     OBUF:I->O                 2.571          slotOutput_0_OBUF (slotOutput<0>)
    ----------------------------------------
    Total                      3.820ns (3.018ns logic, 0.802ns route)
                               (79.0% logic, 21.0% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock
'c3/current_state[3]_current_state[3]_AND_76_o'
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------
Offset:              3.648ns (Levels of Logic = 1)
  Source:            c3/vend (LATCH)
```

```
  Destination:       VEND (PAD)
  Source Clock:      c3/current_state[3]_current_state[3]_AND_76_o falling

  Data Path: c3/vend to VEND
                          Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LDC:G->Q             1   0.498   0.579  c3/vend (c3/vend)
     OBUF:I->O                2.571          VEND_OBUF (VEND)
    ----------------------------------------
    Total                    3.648ns (3.069ns logic, 0.579ns route)
                               (84.1% logic, 15.9% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'c3/invalid_G'
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------
Offset:              3.648ns (Levels of Logic = 1)
  Source:            c3/invalid (LATCH)
  Destination:       INVALID_SEL (PAD)
  Source Clock:      c3/invalid_G falling

  Data Path: c3/invalid to INVALID_SEL
                          Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q              1   0.498   0.579  c3/invalid (c3/invalid)
     OBUF:I->O                2.571          INVALID_SEL_OBUF (INVALID_SEL)
    ----------------------------------------
    Total                    3.648ns (3.069ns logic, 0.579ns route)
                               (84.1% logic, 15.9% route)

==========================================================================

Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock CLK
---------------------------------------+--------+--------+--------+--------+
                                       | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock                           |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------------------------------+--------+--------+--------+--------+
CLK                                    |   3.267|        |        |        |
c2/current_state[3]_GND_3_o_MUX_253_o  |        |   1.470|        |        |
c2/current_state[3]_current_state[3]_AND_17_o|        |   5.435|        |        |
```

c2/current_state[3]_current_state[3]_AND_47_o| | 5.130| | |

Clock to Setup on destination clock c2/current_state[3]_GND_3_o_MUX_253_o

Source Clock	Src:Rise|Dest:Rise	Src:Fall|Dest:Rise	Src:Rise|Dest:Fall	Src:Fall|Dest:Fall
CLK			10.521	
c2/current_state[3]_GND_3_o_equal_1_o			2.914	
c2/current_state[3]_current_state[3]_AND_17_o			7.008	
c2/current_state[3]_current_state[3]_AND_47_o			4.406	

Clock to Setup on destination clock c2/current_state[3]_GND_3_o_equal_1_o

Source Clock	Src:Rise|Dest:Rise	Src:Fall|Dest:Rise	Src:Rise|Dest:Fall	Src:Fall|Dest:Fall
CLK	4.407			
c2/current_state[3]_GND_3_o_equal_1_o	2.537			

Clock to Setup on destination clock c2/current_state[3]_current_state[3]_AND_17_o

Source Clock	Src:Rise|Dest:Rise	Src:Fall|Dest:Rise	Src:Rise|Dest:Fall	Src:Fall|Dest:Fall
CLK			3.515	
c2/current_state[3]_GND_3_o_equal_1_o			1.775	
c2/current_state[3]_current_state[3]_AND_17_o			2.377	

Clock to Setup on destination clock c2/current_state[3]_current_state[3]_AND_47_o

Source Clock	Src:Rise|Dest:Rise	Src:Fall|Dest:Rise	Src:Rise|Dest:Fall	Src:Fall|Dest:Fall
CLK			3.515	
c2/current_state[3]_GND_3_o_equal_1_o			1.901	
c2/current_state[3]_current_state[3]_AND_47_o			2.192	

Clock to Setup on destination clock c3/current_state[3]_GND_18_o_equal_10_o

```
                                   | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock                       |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
-----------------------------------+---------+---------+---------+---------+
CLK                                |    3.645|         |    3.645|         |
c2/current_state[3]_current_state[3]_AND_17_o|         |         |    3.727|         |
c2/current_state[3]_current_state[3]_AND_47_o|         |         |    3.110|         |
c3/current_state[3]_GND_18_o_equal_10_o     |         |         |    1.585|         |
-----------------------------------+---------+---------+---------+---------+

Clock to Setup on destination clock c3/current_state[3]_current_state[3]_AND_76_o
-------------+---------+---------+---------+---------+
             | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
-------------+---------+---------+---------+---------+
CLK          |         |         |    3.645|         |
-------------+---------+---------+---------+---------+

Clock to Setup on destination clock c3/invalid_G
-------------+---------+---------+---------+---------+
             | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
-------------+---------+---------+---------+---------+
CLK          |         |         |    2.252|         |
-------------+---------+---------+---------+---------+

=================================================================================


Total REAL time to Xst completion: 6.00 secs
Total CPU time to Xst completion: 6.40 secs

-->

Total memory usage is 4510696 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :   61 (   0 filtered)
Number of infos    :    1 (   0 filtered)


 Implementation Summary
Release 14.7 Map P.20131013 (nt64)
Xilinx Mapping Report File for Design 'vending_machine'

Design Information
------------------
```

Command Line : map -filter "C:/Users/kbenl/Desktop/My classes_fall_2020/M152A/Project4/vending_machine/iseconfig/filter.filter" -intstyle ise -p xc6slx16-csg324-3 -w -logic_opt off -ol high -t 1 -xt 0 -register_duplication off -r 4 -global_opt off -mt off -ir off -pr off -lc off -power off -o vending_machine_map.ncd vending_machine.ngd vending_machine.pcf
Target Device : xc6slx16
Target Package : csg324
Target Speed : -3
Mapper Version : spartan6 -- $Revision: 1.55 $
Mapped Date : Sat Dec 12 21:02:02 2020

8-Implementation Summary

Number of errors: 0
Number of warnings: 7
Slice Logic Utilization:
Number of Slice Registers: 79 out of 18,224 1%
Number used as Flip Flops: 62
Number used as Latches: 17
Number used as Latch-thrus: 0
Number used as AND/OR logics: 0
Number of Slice LUTs: 157 out of 9,112 1%
Number used as logic: 157 out of 9,112 1%
Number using O6 output only: 141
Number using O5 output only: 0
Number using O5 and O6: 16
Number used as ROM: 0
Number used as Memory: 0 out of 2,176 0%

Slice Logic Distribution:
Number of occupied Slices: 65 out of 2,278 2%
Number of MUXCYs used: 0 out of 4,556 0%
Number of LUT Flip Flop pairs used: 171
Number with an unused Flip Flop: 93 out of 171 54%
Number with an unused LUT: 14 out of 171 8%
Number of fully used LUT-FF pairs: 64 out of 171 37%
Number of unique control sets: 9
Number of slice register sites lost
to control set restrictions: 33 out of 18,224 1%

A LUT Flip Flop pair for this architecture represents one LUT paired with one Flip Flop within a slice. A control set is a unique combination of clock, reset, set, and enable signals for a registered element.
The Slice Logic Distribution report is not meaningful if the design is over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
Number of bonded IOBs: 25 out of 232 10%

IOB Latches: 3

Specific Feature Utilization:
Number of RAMB16BWERs: 0 out of 32 0%
Number of RAMB8BWERs: 0 out of 64 0%
Number of BUFIO2/BUFIO2_2CLKs: 0 out of 32 0%
Number of BUFIO2FB/BUFIO2FB_2CLKs: 0 out of 32 0%
Number of BUFG/BUFGMUXs: 1 out of 16 6%
Number used as BUFGs: 1
Number used as BUFGMUX: 0
Number of DCM/DCM_CLKGENs: 0 out of 4 0%
Number of ILOGIC2/ISERDES2s: 0 out of 248 0%
Number of IODELAY2/IODRP2/IODRP2_MCBs: 0 out of 248 0%
Number of OLOGIC2/OSERDES2s: 3 out of 248 1%
Number used as OLOGIC2s: 3
Number used as OSERDES2s: 0
Number of BSCANs: 0 out of 4 0%
Number of BUFHs: 0 out of 128 0%
Number of BUFPLLs: 0 out of 8 0%
Number of BUFPLL_MCBs: 0 out of 4 0%
Number of DSP48A1s: 0 out of 32 0%
Number of ICAPs: 0 out of 1 0%
Number of MCBs: 0 out of 2 0%
Number of PCILOGICSEs: 0 out of 2 0%
Number of PLL_ADVs: 0 out of 2 0%
Number of PMVs: 0 out of 1 0%
Number of STARTUPs: 0 out of 1 0%
Number of SUSPEND_SYNCs: 0 out of 1 0%

Average Fanout of Non-Clock Nets: 4.63

Peak Memory Usage: 4520 MB
Total REAL time to MAP completion: 23 secs
Total CPU time to MAP completion: 6 secs

Table of Contents

Section 13 - Utilization by Hierarchy

Section 1 - Errors

Section 2 - Warnings

WARNING:PhysDesignRules:372 - Gated clock. Clock net
  c2/current_state[3]_current_state[3]_AND_17_o is sourced by a combinatorial
  pin. This is not good design practice. Use the CE pin to control the loading
  of data into the flip-flop.
WARNING:PhysDesignRules:372 - Gated clock. Clock net
  c3/current_state[3]_GND_18_o_equal_10_o is sourced by a combinatorial pin.
  This is not good design practice. Use the CE pin to control the loading of
  data into the flip-flop.
WARNING:PhysDesignRules:372 - Gated clock. Clock net c3/invalid_G is sourced by
  a combinatorial pin. This is not good design practice. Use the CE pin to
  control the loading of data into the flip-flop.

Section 3 - Informational

INFO:MapLib:562 - No environment variables are currently set.
INFO:LIT:244 - All of the single ended outputs in this design are using slew
  rate limited output drivers. The delay on speed critical single ended outputs
  can be dramatically reduced by designating them as fast outputs.
INFO:Pack:1716 - Initializing temperature to 85.000 Celsius. (default - Range:
  0.000 to 85.000 Celsius)
INFO:Pack:1720 - Initializing voltage to 1.140 Volts. (default - Range: 1.140 to
  1.260 Volts)
INFO:Map:215 - The Interim Design Summary has been generated in the MAP Report
  (.mrp).
INFO:Pack:1650 - Map created a placed design.

Section 4 - Removed Logic Summary
----
  1 block(s) optimized away

Section 5 - Removed Logic

Optimized Block(s):
TYPE		BLOCK
VCC		XST_VCC

Section 6 - IOB Properties

+--
-+

IOB Name	Type	Direction	IO Standard	Diff	Drive	Slew	Reg (s)	Resistor	IOB
				Term	Strength	Rate			Delay
CARD_IN	IOB	INPUT	LVCMOS25						
CLK	IOB	INPUT	LVCMOS25						
COST<0>	IOB	OUTPUT	LVCMOS25		12	SLOW			
COST<1>	IOB	OUTPUT	LVCMOS25		12	SLOW			
COST<2>	IOB	OUTPUT	LVCMOS25		12	SLOW			
DOOR_OPEN	IOB	INPUT	LVCMOS25						
FAILED_TRAN	IOB	OUTPUT	LVCMOS25		12	SLOW			
INVALID_SEL	IOB	OUTPUT	LVCMOS25		12	SLOW			
ITEM_CODE<0>	IOB	INPUT	LVCMOS25						
ITEM_CODE<1>	IOB	INPUT	LVCMOS25						
ITEM_CODE<2>	IOB	INPUT	LVCMOS25						
ITEM_CODE<3>	IOB	INPUT	LVCMOS25						
KEY_PRESS	IOB	INPUT	LVCMOS25						
RELOAD	IOB	INPUT	LVCMOS25						
RESET	IOB	INPUT	LVCMOS25						
VALID_TRAN	IOB	INPUT	LVCMOS25						
VEND	IOB	OUTPUT	LVCMOS25		12	SLOW			
slotOutput<0>	IOB	OUTPUT	LVCMOS25		12	SLOW			
slotOutput<1>	IOB	OUTPUT	LVCMOS25		12	SLOW			
slotOutput<2>	IOB	OUTPUT	LVCMOS25		12	SLOW			
slotOutput<3>	IOB	OUTPUT	LVCMOS25		12	SLOW			

slotOutputsm<0>	IOB	OUTPUT	LVCMOS25		12	SLOW
slotOutputsm<1>	IOB	OUTPUT	LVCMOS25		12	SLOW
slotOutputsm<2>	IOB	OUTPUT	LVCMOS25		12	SLOW
slotOutputsm<3>	IOB	OUTPUT	LVCMOS25		12	SLOW
+----------
-+

Section 7 - RPMs

Section 8 - Guide Report

Guide not run on this design.

Section 9 - Area Group and Partition Summary

Partition Implementation Status

  No Partitions were found in this design.

Area Group Information

  No area groups were found in this design.

Section 10 - Timing Report

A logic-level (pre-route) timing report can be generated by using Xilinx static timing analysis tools, Timing Analyzer (GUI) or TRCE (command line), with the mapped NCD and PCF files. Please note that this timing report will be generated using estimated delay information. For accurate numbers, please generate a timing report with the post Place and Route NCD file.

For more information about the Timing Analyzer, consult the Xilinx Timing Analyzer Reference Manual; for more information about TRCE, consult the Xilinx Command Line Tools User Guide "TRACE" chapter.

Section 11 - Configuration String Details

Use the "-detail" map option to print out Configuration Strings

Section 12 - Control Set Information

Use the "-detail" map option to print out Control Set Information.

Section 13 - Utilization by Hierarchy

Use the "-detail" map option to print out the Utilization by Hierarchy section.