31	27	26	25	24	2	20	range 1915	range141	2range117	range60	
	funct7				rs2		rs1	funct3	rd	opcode	R-type
	iı	nm[11:0]			rs1	funct3	rd	opcode	I-type
	imm[11:5	[6]			rs2		rs1	funct3	imm[4:0]	opcode	S-type
i	mm[12 10]	:5]			rs2		rs1	funct3	imm[4:1 11]	opcode	SB-type
imm[31:12]					m[31:12	2]			rd	opcode	U-type
imm[20 10:1 11 19:12]									rd	opcode	UJ-type

RV32I Base Instruction Set

	rd	0110111				
		imm[31:12]			$^{\mathrm{rd}}$	0010111
	imn	n[20 10:1 11 19	0:12]		$^{\mathrm{rd}}$	1101111
imm[11:0]		rs1	000	rd	1100111
imm[12 10:5]		rs2	rs1	000	imm[4:1 11]	1100011
imm[12 10:5]		rs2	rs1	001	imm[4:1 11]	1100011
imm[12 10:5]		rs2	rs1	100	imm[4:1 11]	1100011
imm[12 10:5]		rs2	rs1	101	imm[4:1 11]	1100011
imm[12 10:5]		rs2	rs1	110	imm[4:1 11]	1100011
imm[12 10:5]		rs2	rs1	111	imm[4:1 11]	1100011
imm	11:0		rs1	000	rd	0000011
imm	11:0		rs1	001	rd	0000011
imm	11:0		rs1	010	rd	0000011
imm	11:0		rs1	100	rd	0000011
imm	11:0		rs1	101	rd	0000011
imm[11:5]		rs2	rs1	000	imm[4:0]	0100011
imm[11:5]		rs2	rs1	001	imm[4:0]	0100011
imm[11:5]		rs2	rs1	010	imm[4:0]	0100011
imm	11:0		rs1	000	rd	0010011
imm	11:0		rs1	010	rd	0010011
imm	11:0		rs1	011	rd	0010011
imm	11:0		rs1	100	rd	0010011
imm	11:0]	rs1	110	rd	0010011
imm			rs1	111	rd	0010011
0000000	T	shamt	rs1	001	rd	0010011
0000000		shamt	rs1	101	rd	0010011
0100000		shamt	rs1	101	rd	0010011
0000000		rs2	rs1	000	rd	0110011
0100000		rs2	rs1	000	rd	0110011
0000000		rs2	rs1	001	rd	0110011
0000000		rs2	rs1	010	rd	0110011
0000000		rs2	rs1	011	rd	0110011
0000000		rs2	rs1	100	rd	0110011
0000000		rs2	rs1	101	rd	0110011
0100000		rs2	rs1	101	rd	0110011
0000000		rs2	rs1	110	rd	0110011
0000000		rs2	rs1	111	rd	0110011
0000	pred	l succ	00000	000	00000	0001111
	0000		00000	001	00000	0001111
	00000000000			000	00000	1110011
000000	00000000001				00000	1110011
110000	0000	000	00000	010	$_{ m rd}$	1110011
110010			1 00000	010	$^{\mathrm{rd}}$	1110011
110000	0000	01	00000	010	rd	1110011
110010			00000	010	$_{ m rd}$	1110011
110000	0000	10	00000	010	$_{ m rd}$	1110011
110010	0000	10	00000	010	$^{\mathrm{rd}}$	1110011
			•	•		

AUIPC rd,imm JAL rd,imm JALR rd,rs1,imm BEQ rs1,rs2,imm BNE rs1,rs2,imm BLT rs1,rs2,imm BGE rs1,rs2,imm BLTU rs1,rs2,imn BGEU rs1,rs2,imi LB rd,rs1,imm LH rd,rs1,imm LW rd,rs1,imm LBU rd,rs1,imm LHU rd,rs1,imm SB rs1,rs2,imm SH rs1,rs2,imm SW rs1,rs2,imm ADDI rd,rs1,imm SLTI rd,rs1,imm SLTIU rd,rs1,imm XORI rd,rs1,imm ORI rd,rs1,imm ANDI rd,rs1,imm SLLI rd,rs1,shamt SRLI rd,rs1,sham SRAI rd,rs1,sham ADD rd,rs1,rs2 SUB rd,rs1,rs2 SLL rd,rs1,rs2 SLT rd,rs1,rs2 SLTU rd,rs1,rs2XOR rd,rs1,rs2 SRL rd,rs1,rs2SRA rd,rs1,rs2 OR rd,rs1,rs2 AND rd,rs1,rs2 FENCE FENCE.I SCALL SBREAK RDCYCLE rd RDCYCLEH rd RDTIME rd RDTIMEH rd RDINSTRET rd RDINSTRETH re

LUI rd,imm

31	27	26	25	24	20	range 1915	range141	2range117	range60	
	funct7	7			rs2	rs1	funct3	$^{\mathrm{rd}}$	opcode	R-type
imm[11:0			11:0]			rs1	funct3	$^{\mathrm{rd}}$	opcode	I-type
	imm[11:5]			rs2	rs1	funct3	imm[4:0]	opcode	S-type	
					Instruc	tion Set (in				1
		imm[rs1	110	rd	0000011	LWU rd,rs1,imm
		imm[11:0]			rs1	011	rd	0000011	LD rd,rs1,imm
	imm[11	:5]			rs2	rs1	011	imm[4:0]	0100011	SD rs1,rs2,imm
	000000			shar	nt	rs1	001	rd	0010011	SLLI rd,rs1,shan
	000000			shai	nt	rs1	101	$^{\mathrm{rd}}$	0010011	SRLI rd,rs1,shan
	010000			shai	nt	rs1	101	$^{\mathrm{rd}}$	0010011	SRAI rd,rs1,shar

000

001

101

101

000

000

001

101

101

rd

rd

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rd

rd

rd

 rd

 rd

rd

0011011

0011011

0011011

0011011

0111011

0111011

0111011

0111011

0111011

ADDIW rd,rs1,i

SLLIW rd,rs1,sh

SRLIW rd,rs1,sh

SRAIW rd,rs1,sl

ADDW rd,rs1,rs

SUBW rd,rs1,rs2

SLLW rd,rs1,rs2

SRLW rd,rs1,rs2

SRAW rd,rs1,rs2

MUL rd,rs1,rs2 MULH rd,rs1,rs2 MULHSU rd,rs1 MULHU rd,rs1,r DIV rd,rs1,rs2 DIVU rd,rs1,rs2 REM rd,rs1,rs2REMU rd,rs1,rs2

MULW rd,rs1,rs DIVW rd,rs1,rs2 DIVUW rd,rs1,r REMW rd,rs1,rs REMUW rd,rs1,

LR.W rd,rs1SC.W rd,rs1,rs2AMOSWAP.W r AMOADD.W rd AMOXOR.W rd AMOAND.W rd AMOOR.W rd,r AMOMIN.W rd AMOMAX.W ro AMOMINU.W r AMOMAXU.W

rs1DM99M C+

rs1

rs1

rs1

rs1

rs1

rs1

rs1

rs1

imm[11:0]

shamt

shamt

shamt

rs2

rs2

rs2

rs2

rs2

0000000

0000000

0100000

0000000

0100000

0000000

0000000

0100000

RV32M Standard Extension											
0000001	rs2	rs1	000	rd	0110011						
0000001	rs2	rs1	001	rd	0110011						
0000001	rs2	rs1	010	rd	0110011						
0000001	rs2	rs1	011	rd	0110011						
0000001	rs2	rs1	100	rd	0110011						
0000001	rs2	rs1	101	rd	0110011						
0000001	rs2	rs1	110	rd	0110011						
0000001	rs2	rs1	111	$^{\mathrm{rd}}$	0110011						

RV64M Standard Extension (in addition to RV32M)

0000001	rs2	rs1	000	rd	0111011
0000001	rs2	rs1	100	rd	0111011
0000001	rs2	rs1	101	rd	0111011
0000001	rs2	rs1	110	$^{\mathrm{rd}}$	0111011
0000001	rs2	rs1	111	rd	0111011

RV32A Standard Extension

00010	aq	rl	00000	rs1	010	$^{\mathrm{rd}}$	0101111
00011	aq	rl	rs2	rs1	010	$^{\mathrm{rd}}$	0101111
00001	aq	rl	rs2	rs1	010	$^{\mathrm{rd}}$	0101111
00000	aq	rl	rs2	rs1	010	rd	0101111
00100	aq	rl	rs2	rs1	010	rd	0101111
01100	aq	rl	rs2	rs1	010	rd	0101111
01000	aq	rl	rs2	rs1	010	rd	0101111
10000	aq	rl	rs2	rs1	010	rd	0101111
10100	aq	rl	rs2	rs1	010	$^{\mathrm{rd}}$	0101111
11000	aq	rl	rs2	rs1	010	$^{\mathrm{rd}}$	0101111
11100	aq	rl	rs2	rs1	010	rd	0101111

2

31	27	26	25	24		20	range 1915	range141	2range117	range60	
	funct7	,			rs2		rs1	funct3	$^{\mathrm{rd}}$	opcode	R-type
rs	3	fun	ct2		rs2		rs1	funct3	$^{\mathrm{rd}}$	opcode	R4-type
imm[11:0]		11:0]				rs1	funct3	rd	opcode	I-type	
imm[11:5]				rs2		rs1	funct3	imm[4:0]	opcode	S-type	

RV64A Standard Extension (in addition to RV32A)

	πv	04A	Standard Ex	tension (m a	addition	to Rv32A)	
00010	aq	rl	00000	rs1	011	rd	0101111
00011	aq	rl	rs2	rs1	011	rd	0101111
00001	aq	rl	rs2	rs1	011	rd	0101111
00000	aq	rl	rs2	rs1	011	rd	0101111
00100	aq	rl	rs2	rs1	011	rd	0101111
01100	aq	rl	rs2	rs1	011	rd	0101111
01000	aq	rl	rs2	rs1	011	rd	0101111
10000	aq	rl	rs2	rs1	011	rd	0101111
10100	aq	rl	rs2	rs1	011	rd	0101111
11000	aq	rl	rs2	rs1	011	rd	0101111
11100	aq	rl	rs2	rs1	011	rd	0101111

LR.D rd,rs1
SC.D rd,rs1,rs2
AMOSWAP.D rd
AMOADD.D rd,
AMOXOR.D rd,
AMOAND.D rd,
AMOOR.D rd,rs
AMOMIN.D rd,
AMOMIN.D rd,
AMOMAX.D rd
AMOMINU.D rd
AMOMAXU.D rd

RV32F Standard Extension

$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		RV32F Standard Extension										
rs3		L J		rs1								
TS3	imm[11	:5]	rs2	rs1	010	imm[4:0]	0100111					
rs3 00 rs2 rs1 rm rd 1001011 rs3 00 rs2 rs1 rm rd 1001111 0000000 rs2 rs1 rm rd 1010011 0000100 rs2 rs1 rm rd 1010011 0001100 rs2 rs1 rm rd 1010011 0001100 rs2 rs1 rm rd 1010011 0010100 rs2 rs1 rm rd 1010011 0010000 rs2 rs1 000 rd 1010011 0010000 rs2 rs1 000 rd 1010011 0010000 rs2 rs1 000 rd 1010011 0010100 rs2 rs1 000 rd 1010011 0010100 rs2 rs1 000 rd 1010011 1100000 rs2 rs1 000 rd 1010011 1100000 <	rs3	00	rs2	rs1	rm	rd	1000011					
FS3	rs3	00	rs2	rs1	rm	rd						
0000000	rs3	00	rs2	rs1	rm	rd	1001011					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	rs3			rs1	rm	rd	1001111					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	000000	00	rs2	rs1	rm	rd	1010011					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	000010	00	rs2	rs1	rm	rd	1010011					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	000100	00	rs2	rs1	rm	rd	1010011					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	000110	00	rs2	rs1	rm	rd	1010011					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	010110	00	00000	rs1	rm	rd	1010011					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	001000	00	rs2	rs1	000	rd	1010011					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	001000	00	rs2	rs1		rd	1010011					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	001000	00	rs2	rs1	010	rd	1010011					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	001010	00	rs2	rs1	000	rd	1010011					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	001010	00	rs2	rs1	001	rd	1010011					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	110000	00		rs1	rm	rd	1010011					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	110000	00	00001	rs1	rm	rd	1010011					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	111000	00	00000	rs1	000	rd	1010011					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			rs2	rs1								
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	101000	00	rs2	rs1	001	rd	1010011					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	101000	00		rs1	000	rd	1010011					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	111000	00	00000	rs1	001	rd	1010011					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	110100	00		rs1	rm							
000000000011 00000 010 rd 1110011 000000000010 00000 010 rd 1110011 000000000001 00000 010 rd 1110011 000000000011 rs1 001 rd 1110011 000000000010 rs1 001 rd 1110011 000000000001 3 rs1 001 rd 1110011 000000000010 00000 101 rd 1110011	110100	00	00001	rs1	rm	rd	1010011					
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$				rs1								
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$						rd						
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	00	00000000	10	00000	010	rd	1110011					
000000000010 rs1 001 rd 1110011 000000000001 3 rs1 001 rd 1110011 000000000010 00000 101 rd 1110011				00000								
000000000001 3 rs1 001 rd 1110011 000000000010 00000 101 rd 1110011	00	00000000	11	rs1								
000000000010 00000 101 rd 1110011												
			-									
000000000001 00000 101 rd 1110011												
	00	00000000	01	00000	101	rd	1110011					

FLW rd,rs1,immFSW rs1,rs2,imr FMADD.S rd,rs FMSUB.S rd,rs1FNMSUB.S rd,r FNMADD.S rd,1 FADD.S rd,rs1,r FSUB.S rd,rs1,rs FMUL.S rd,rs1,r FDIV.S rd,rs1,rs FSQRT.S rd,rs1 FSGNJ.S rd,rs1, FSGNJN.S rd,rs FSGNJX.S rd,rs FMIN.S rd,rs1,rs FMAX.S rd,rs1, FCVT.W.S rd,rs FCVT.WU.S rd, FMV.X.S rd,rs1 FEQ.S rd,rs1,rs2 FLT.S rd,rs1,rs2 FLE.S rd,rs1,rs2 FCLASS.S rd,rs FCVT.S.W rd,rs FCVT.S.WU rd, FMV.S.X rd,rs1 FRCSR rd FRRM rdFRFLAGS rd FSCSR rd,rs1 FSRM rd,rs1 FSFLAGS rd,rs1 FSRMI rd,imm ☐ FSFLAGSI rd,in

31	27	$26 \ 25$	24	20	range 1915	range141	2range117	range60	
	funct7	,	rs2		rs1	funct3	rd	opcode	R-type
	rs3	funct2	rs2		rs1	funct3	rd	opcode	R4-type
		imm[11:0]			rs1	funct3	rd	opcode	I-type
imm[11:5]			rs2		rs1	funct3	imm[4:0]	opcode	S-type

RV64F Standard Extension (in addition to RV32F)

1100000	00010	rs1	rm	$^{\mathrm{rd}}$	1010011	FCVT.L.S rd,rs1
1100000	00011	rs1	rm	$^{\mathrm{rd}}$	1010011	FCVT.LU.S rd,rs
1101000	00010	rs1	rm	$^{\mathrm{rd}}$	1010011	FCVT.S.L rd,rs1
1101000	00011	rs1	$_{ m rm}$	rd	1010011	FCVT.S.LU rd,rs

RV32D Standard Extension

		100 5210	Standard Ex	CCHSIOH				
	imm[11:0]		rs1	011	$^{\mathrm{rd}}$	0000111		
imm[11:	5]	rs2	rs1	011	imm[4:0]	0100111		
rs3	01	rs2	rs1	rm	$^{\mathrm{rd}}$	1000011		
rs3	01	rs2	rs1	rm	$^{\mathrm{rd}}$	1000111		
rs3	01	rs2	rs1	rm	$^{\mathrm{rd}}$	1001011		
rs3	rs3 01		rs1	rm	$^{\mathrm{rd}}$	1001111		
000000	1	rs2	rs1	rm	$^{\mathrm{rd}}$	1010011		
000010	0000101		rs1	rm	$^{\mathrm{rd}}$	1010011		
000100	1	rs2	rs1	rm	$^{\mathrm{rd}}$	1010011		
000110	1	rs2	rs1	rm	$^{\mathrm{rd}}$	1010011		
010110	1	00000	rs1	rm	$^{\mathrm{rd}}$	1010011		
001000	10001 rs2		rs1	000	$^{\mathrm{rd}}$	1010011		
001000	1	rs2	rs1	001	$^{\mathrm{rd}}$	1010011		
001000	1	rs2	rs1	010	$^{\mathrm{rd}}$	1010011		
001010	1	rs2	rs1	000	$^{\mathrm{rd}}$	1010011		
001010	1	rs2	rs1	001	$^{\mathrm{rd}}$	1010011		
010000	0	00001	rs1	rm	$^{\mathrm{rd}}$	1010011		
010000	1	00000	rs1	rm	$^{\mathrm{rd}}$	1010011		
101000	1	rs2	rs1	010	$^{\mathrm{rd}}$	1010011		
101000	1	rs2	rs1	001	$^{\mathrm{rd}}$	1010011		
101000	1	rs2	rs1	000	$^{\mathrm{rd}}$	1010011		
111000	1	00000	rs1	001	$^{\mathrm{rd}}$	1010011		
110000	1	00000	rs1	rm	$^{\mathrm{rd}}$	1010011		
110000	1100001		rs1	rm	$^{\mathrm{rd}}$	1010011		
110100	1101001		01 00000		rs1	rm	$^{\mathrm{rd}}$	1010011
110100	1	00001	rs1	rm	rd	1010011		

RV64D Standard Extension (in addition to RV32D)

1100001	00010	rs1	$^{ m rm}$	rd	1010011
1100001	00011	rs1	rm	rd	1010011
1110001	00000	rs1	000	rd	1010011
1101001	00010	rs1	rm	rd	1010011
1101001	00011	rs1	$_{ m rm}$	rd	1010011
1111001	00000	rs1	000	rd	1010011

FCVT.L.D rd,rs1
FCVT.LU.D rd,r
FMV.X.D rd,rs1
FCVT.D.L rd,rs1
FCVT.D.LU rd,r
FMV.D.X rd,rs1

FLD rd,rs1,imm FSD rs1,rs2,imm FMADD.D rd,rs FMSUB.D rd,rs1 FNMSUB.D rd,rs FNMADD.D rd,1 FADD.D rd,rs1,r FSUB.D rd,rs1,rs FMUL.D rd,rs1,r FDIV.D rd,rs1,rs $FSQRT.D\ rd,rs1$ FSGNJ.D rd,rs1, FSGNJN.D rd,rs FSGNJX.D rd,rs FMIN.D rd,rs1,rs FMAX.D rd,rs1,1 FCVT.S.D rd,rs1 FCVT.D.S rd,rs1 FEQ.D rd,rs1,rs2 $FLT.D\ rd,rs1,rs2$ FLE.D rd,rs1,rs2 FCLASS.D rd,rs FCVT.W.D rd,rs FCVT.WU.D rd, FCVT.D.W rd,rs FCVT.D.WU rd,

Table 1: Instruction listing for RISC-V