UM11040

Software user manual for SJA1105P, SJA1105Q, SJA1105R, SJA1105S

Rev. 2 — 5 February 2020 User manual

Document information

Information	Content
Keywords	SJA1105P, SJA1105Q, SJA1105R, SJA1105S, Ethernet, switch, software registers
Abstract	This user manual describes the configuration, register structure and mapping of the SJA1105P, SJA1105Q, SJA1105R, SJA1105S 5-port automotive Ethernet switch family.

Revision history

Rev	Date	Description
2	20200205	text clarification in Section 3.1, Section 4.2, Table 19 (bit VLAN_BC), Table 32 (bits 63:32), Section 6, Section 6.1.3.11, Figure 14, Table 120 (addr. 100A80h deleted); added references to accompanying documents; PTPPINDUR bit description clarified (Table 88), PLL_x_C R/W properties corrected (Table 116); added attachment for SPI calculations; typos corrected
1.0	20171124	first issue

1 Introduction

1.1 Scope of this document

This software user manual describes the configuration and operation of the SJA1105P/Q/R/S 5-port automotive Ethernet switch. Topics covered include the static configuration interface and format, the register structure, and mapping of the IP blocks. This document should be read alongside with the SJA1105P/Q/R/S data sheet (Ref. 1) and applications hints (Ref. 2), available from NXP Semiconductors.

1.2 Additional documentation

This document should be read alongside with the SJA1105P/Q/R/S data sheet (Ref. 1) and applications hints (Ref. 2), available from NXP Semiconductors. The data sheet focuses on typical hardware topics such as pinning, electrical behavior, signal timing, wave forms, current consumption, etc. Typical applications and specific use cases are discussed in the application hints document, which also includes advice on avoiding pitfalls.

2 Functional Overview

The building blocks used to make up the four variants of the SJA1105P/Q/R/S are shown in Fig 1. The base addresses of the core, CGU, RGU and ACU are given in Table 2. The dataflow followed by a single received frame as it passes through the switch is described in Section 2.1 to Section 2.3.

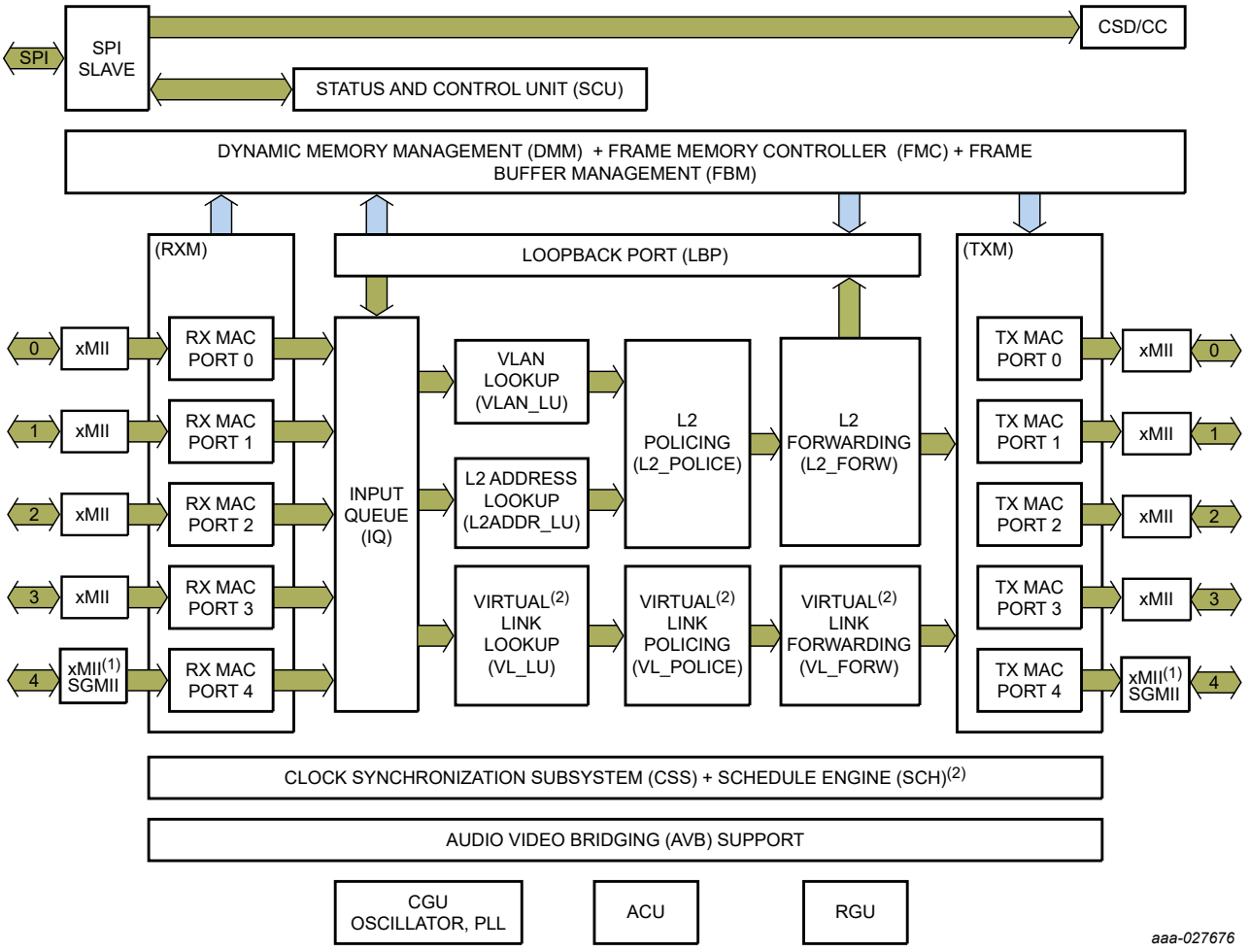
Some sections of this user manual are only applicable to specific variants.

Table 1. SJA1105P/Q/R/S variants

Device	Switch core device ID	PART_NR	SGMII interface	Pin-compatible with SJA1105EL and SJA1105TEL	TT-Ethernet compatible
SJA1105PEL	AF00030Eh	9A84h	no	yes	no
SJA1105QEL	AE00030Eh	9A85h	no	yes	yes
SJA1105REL	AF00030Eh	9A86h	port 4	no	no
SJA1105SEL	AE00030Eh	9A87h	port 4	no	yes

Table 2. SJA1105P/Q/R/S Memory map

Name	SPI base address	Description
ETH_DYN	00000000h	switch core, dynamic configuration area
ETH_STATIC	00020000h	switch core, static configuration area
CGU	00100000h	clock generation unit to control oscillator, PLLs and clocking
RGU	00100400h	reset generation unit
ACU	00100800h	auxiliary configuration unit
SGMII (SJA1105R/S only)	00180000h	SGMII subsystem



1. SGMII port in SJA1105R/S.
2. SJA1105Q/S only.

Figure 1. Block diagram of the SJA1105P/Q/R/S

2.1 Ingress Stage

A frame is received from a neighboring PHY or MAC on one of the available ports. The xMII block passes received data to the Receive MAC (RX MAC) connected to the reception port. The RX MAC performs low-level checks on the frame data and reports any CRC or MII errors detected to the status and control unit. The frame is discarded immediately if a low-level error is detected. A frame that passes all low-level checks is stored in frame memory in 128 byte segments. The RX MAC captures an ingress timestamp, extracts meta information from the frame, and forwards it to the Input Queue (IQ). If a VLAN tag was not embedded in the received frame, the RX MAC block assigns a configured Port VLAN ID and a configured Port VLAN Priority to the frame. The IQ module stores the frame meta information in a deterministic order and passes it to the forwarding stage for further processing. If multiple frames are received at the same time on different ports, the processing order is determined by the port numbers; a frame received on a port with a lower ID is processed before a frame received on a port with a higher ID. Note that this only influences the frame order on the egress stage if multiple concurrently received frames are forwarded to the same destination port.

2.2 Forwarding Stage

Valid MAC-level frames are passed from the ingress stage to the forwarding stage, which applies several higher-layer checks on the frame and extracts the forwarding information.

The VLAN Lookup (VLAN_LU) block reads the VLAN information configured for the VLAN ID associated with the frame. If a VLAN tag is embedded in the frame, the block checks if the reception port is configured to be a member of this VLAN. If it is not, the frame is dropped and reported to the status and control unit. It also checks if the VLAN associated with the frame is configured for mirroring or retagging and determines which egress port it should be transferred to.

If a QinQ tag is embedded in the Ethernet frame, only the outer tag (S-tag) is used for further lookups.

The Address Lookup (L2ADDR_LU) block extracts the address information in the form of the source MAC address and the VLAN ID. Both are stored for future forwarding decisions. This block also looks up the destination MAC address and combines it with the VLAN ID to determine where to forward the frame. The VLAN ID is ignored during learning and lookup if shared address learning is activated.

The Policing (L2_POLICE) block meters the incoming frame rate. The switch can be configured to drop packets if the maximum frame rate is exceeded. The Forwarding (L2_FORW) block uses the information obtained from other blocks to determine the set of ports to forward the frame to. The switch can be configured to limit the set of egress ports accessible to frames received on a specific ingress port. For example, it is possible to force any frame arriving on a particular ingress port to be forwarded to a specific egress port regardless of the forwarding information embedded in the frame. This block also determines the VLAN priority to be embedded in frames forwarded by the switch as well as the egress priority queue in which a frame is stored on a per priority and per port basis. It also determines if the mirroring port shall be included in the set of ports to which the frame is forwarded, based on the information configured for port-based and VLAN-based ingress and egress mirroring. The L2_FORW block also reserves the required memory space in the partition assigned to the frame by the policing module. The Loopback Port (LBP) replicates frames that are configured to be retagged based on the associated VLAN configuration. A different VLAN ID is embedded in the replicated frame, but association with the source port that the frame originally arrived on remains. The resulting frame is processed according to the forwarding rules for this MAC address and VLAN configuration.

2.3 Egress Stage

The egress stage recomposes the frame from the data stored in frame memory and the information gathered by the forwarding stage. It also performs the one-step transparent clock update for IEEE 1588 event frames which have the two-step bit deasserted in the frame header (twoStepFlag, see IEEE 1588-2008). The Transmit MAC (TX MAC) assigns the frame to the priority queue determined by the forwarding stage. It monitors the number of frames stored in the priority queue. If the maximum number allowed has been exceeded, the frame is dropped and an error condition is signaled to the status and control unit. The TX MAC also performs priority selection based on the strict-priority algorithm and considers whether the credit-based shaper assigned to the priority queue is in the transmission-allowed state.

2.4 Configuration

The device is configured in multiple steps. It will not be functional, and all xMII (except SGMII) ports will be tri-stated (except SGMII) to avoid electrical interfacing problems, until the static configuration is loaded.

The Clock Generation Unit (CGU) and the SGMII (SJA1105R/S only) are usually configured first. A static configuration is then uploaded. This contains port configuration information, VLAN settings and more. Alternatively, the CGU, ACU and SGMII can be configured as part of the static configuration upload. After these steps have been completed, the switch is operational and able to forward frames. If the configuration needs to be changed during runtime, settings can be altered through dynamic reconfiguration.

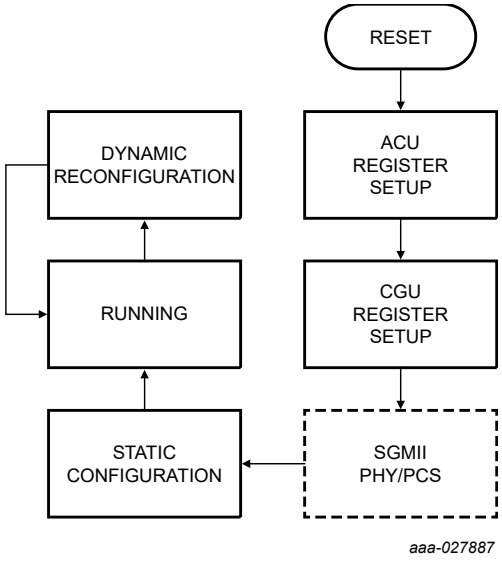


Figure 2. Configuration Flow

3 SPI Interface

All memory, control and status registers can be accessed via the Serial Peripheral Interface (SPI). The device operates as a slave device in transfer Mode 1 with CPOL = 0 and CPHA = 1 (as defined in the SPI Block guide from Motorola). Both master and slave must operate in the same mode. The SJA1105P/Q/R/S expects a frame format in which the access type, address and data are encoded in a single SPI transaction. The format must conform to the SPI framing described in the datasheet. The device uses a double word (32-bit) addressing scheme.

3.1 Write Access

A write access consists of a 32-bit control phase followed by a (virtually) unlimited number of 32-bit data words. The 21-bit address is encoded in control bits[24:4]. The access type is encoded in the MSB, control bit[31]. Both control and data phases are transmitted from MSB to LSB. Bit[31] is set to 1 to indicate a write operation. A data phase of at least 32 bits is transmitted after the control phase. Both control and data phases are mirrored to SDO during a write operation. Unused control bits must be set to logic 0.

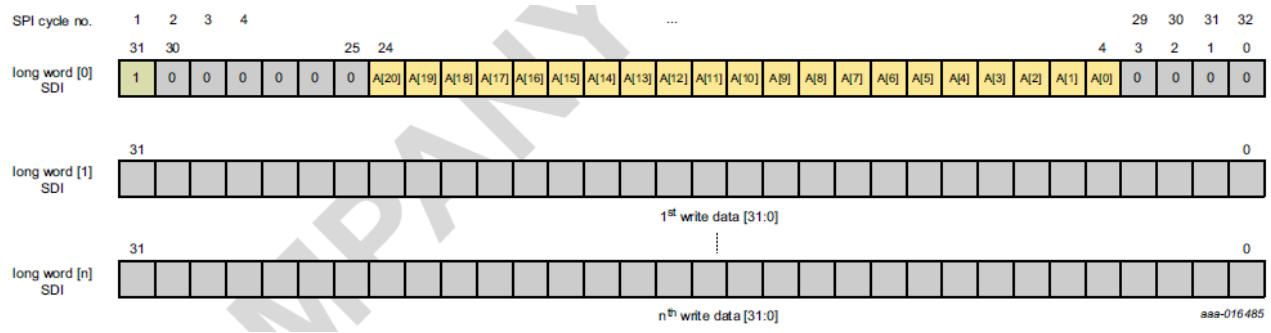


Figure 3. SPI write access to the switch on SDI

Figure 4. SPI write access to the switch on SDO

3.2 Read Access

A read access is similar to a write access. The access bit (bit[31]) is 0 to indicate a read operation. Bits[30:25] contain the number of 32-bit double words to be read from the device. The device shifts out the corresponding data in the data phase. As with a write access, the address phase is mirrored to SDO. Unused control bits must be logic 0.

Remark: For accesses to some registers, SPI timing is stricter than 25 MHz.

When CGU registers are read, a 64 ns delay must be inserted between the control and data phases to allow the device to retrieve the data. Alternatively, the access can be performed at a frequency below 17.8 MHz. In addition, a read-after-write time of >130 ns between an SPI write and read to the same register must be guaranteed.

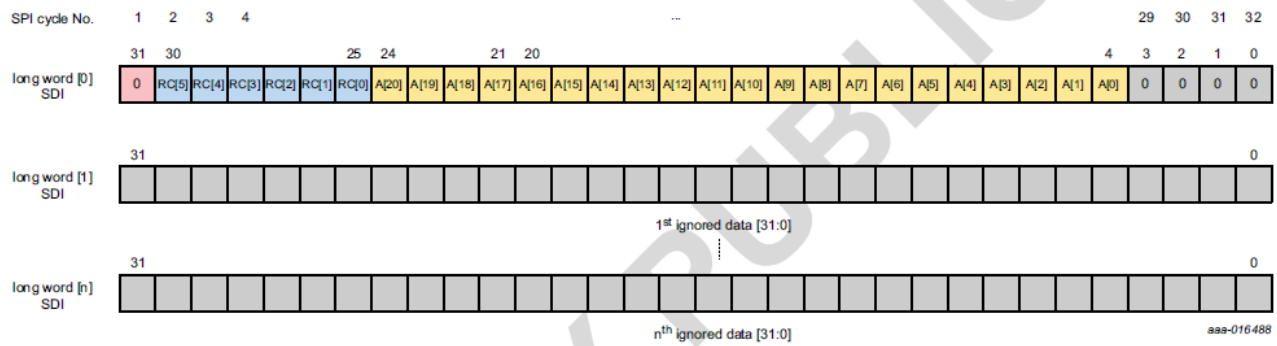


Figure 5. SPI read access to the switch on SDO

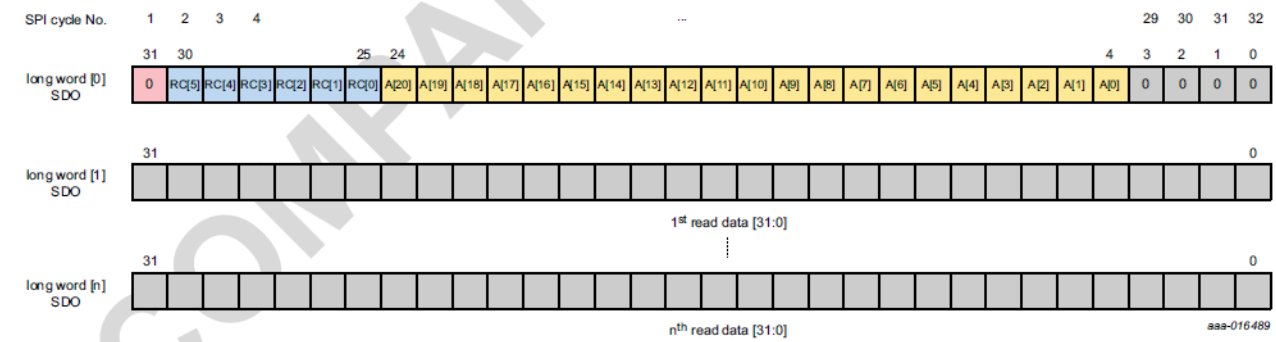


Figure 6. SPI read access to the switch on SDO

4 Static Control Interface

Two distinct interfaces are used to configure the switch core. After the device is powered up or reset, it expects to receive an input stream containing initial setup information over the static configuration interface. The initial configuration data sets the port modes, sets up VLANs, and defines other forwarding and quality-of-service rules. Once the device is operational, it can be reconfigured at runtime over the programming interface (see Section 6). This section explains the loader format, the individual configuration blocks (tables), and associated fields. A host microcontroller must upload a valid configuration stream every time the device is reset or power-cycled. The CONFIGS flag in the Initial device configuration flag register (Table 35) is set once the device has been configured successfully.

4.1 Generic Loader Format

Figure 7 shows the generic loader format. Each line represents a 32-bit double word. The format starts with a 32-bit switch core device ID (see Table 1). Care must be taken, as the ID differs between product variants.

The device ID is followed by a sequence of configuration blocks. The block order is arbitrary. The data format and coding of each block is described in Section 5. Each block starts with an 8-bit BlockID (left aligned in a double word) followed by the BlockLength in double words. This block header is protected with a CRC-32 checksum. The block header is followed by an arbitrary number of 32-bit words, as indicated by BlockLength.

The data double words are also protected with a CRC-32 checksum. The last block in the loader format is used as a delimiter. The length must be set to zero and the last CRC is computed over the entire loader data, including the Device ID. Unused data can be set to any arbitrary value. However, it must be reflected in the CRCs.

Checksums are calculated as CRC-32 Ethernet checksums with the lower bytes of each doubleword included first in the CRC calculation. See IEEE 802.3-2015, clause 3 for details.

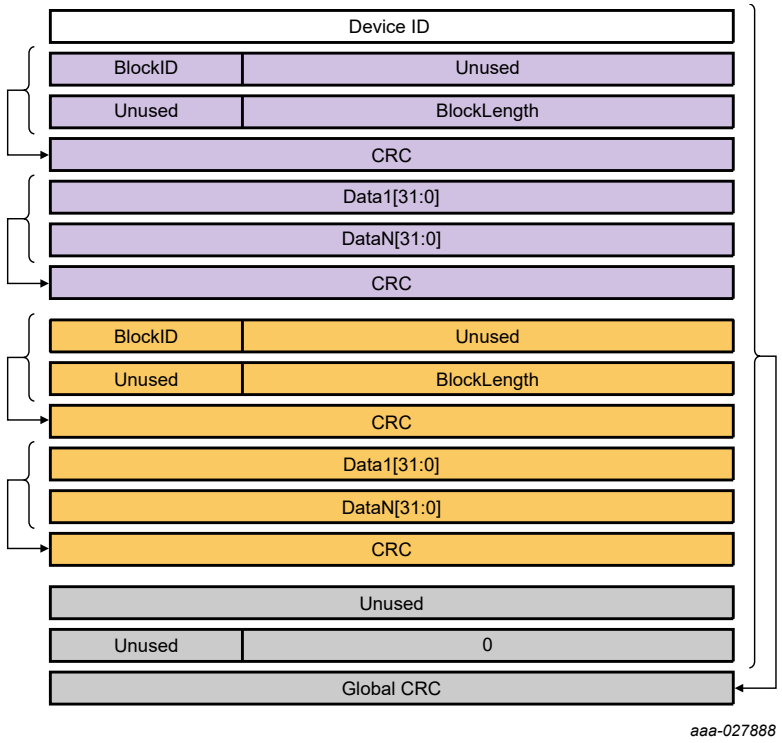


Figure 7. Generic Loader Format

4.1.1 Configuration Block Format

As discussed in the previous section, configuration data is structured into distinct configuration blocks as shown in Figure 7. Each block is composed of an integer number of 32-bit double words and carries data organized as a table with one or more entries (see Figure 8).

The layout (bit fields) of an entry is table-specific and is described in Section 5. The layout of some table entries can vary, depending on the context (e.g. the L2 Lookup Table differentiates between dynamically learned and static L2 entries.).

Note that entries are stored from lower word addresses to higher addresses in the loader format. That means the first 32 bits in a block correspond to the lower 32 bits of the respective entry.

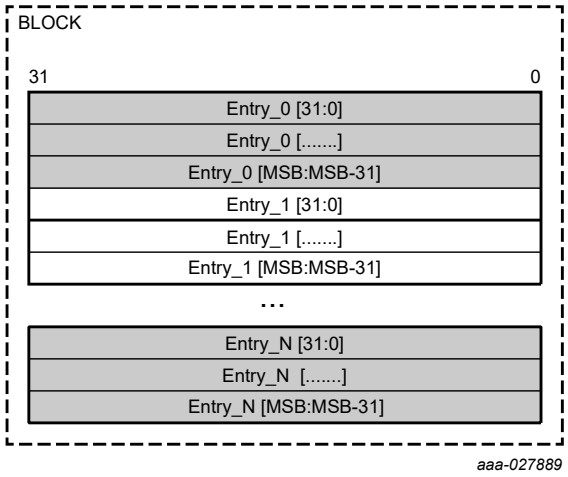


Figure 8. Block structure with multiple entries forming table.

4.2 Loading Configuration Data

Configuration information for the switch core must be loaded at start-up, using the generic loader format as described in Section 4.1. The configuration area starts at address 20000h. The entire configuration area is write-only. A read access to any address in this area returns arbitrary data. However, some parts of the configuration data can be read via the dynamic control interface (see Section 6).

The configuration can be downloaded in one SPI write transaction for minimal protocol overhead and configuration time. However, it may also be split into multiple transactions if there are other limiting factors, e.g. SPI controller constraints.

The first SPI write transaction must write to configuration base address 20000h. Subsequent transactions can use any destination address in the range 20001h to 2FFFFh. Note that the download mechanism in the switch automatically advances the download address based on the size of previously downloaded blocks

If the device does not accept a configuration (CONFIGS flag remains de-asserted), loading can be reinitiated by restarting the configuration process. The SJA1105P/Q/R/S always recognizes a write operation to address 20000h. The device enters configuration mode if the first doubleword is the device ID.

Once the device is successfully configured (CONFIGS flag is asserted), the configuration cannot be changed via this interface until the device is reset. However dynamic changes can be made through the dynamic interface.

A spreadsheet is attached to this document that can be used to calculate the length of the configuration data stream and the download time at a given SPI data rate.

5 Configuration Tables

This section describes the contents of the configuration tables. Each of the table is associated with a block in the generic loader format. Some of the tables must be loaded, others are optional, and some are only accessible over the runtime interface.

Some of the tables control the Time-Triggered Ethernet functionality of the device. These tables are only available in the SJA1105Q/S variants.

Table 3. Configuration tables used for static configuration

The tables in italics are (e.g. Schedule table) are not available in all variants

Table name	Block ID	Loading mandatory?	Variants
Schedule table	*00h*	*No*	*SJA1105Q/S*
Schedule Entry Points Table	*01h*	*yes, if Schedule table is loaded*	*SJA1105Q/S*
VL Lookup Table	*02h*	*no*	*SJA1105Q/S*
VL Policing table	*03h*	*yes, if VL Lookup table is loaded*	*SJA1105Q/S*
VL Forwarding Table	*04h*	*yes, if VL Lookup table is loaded*	*SJA1105Q/S*
L2 Address Lookup table	05h	no	all
L2 Policing table	06h	yes, at least one entry	all
VLAN Lookup table	07h	no, by default VLAN 0 is enabled	all
L2 Forwarding table	08h	yes	all
MAC Configuration table	09h	yes	all
Schedule Parameters table	*0Ah*	*yes, if Schedule table is loaded*	*SJA1105Q/S*
Schedule Entry Points Parameters table	*0Bh*	*yes, if Schedule table is loaded*	*SJA1105Q/S*
VL Forwarding Parameters table	*0Ch*	*yes, if VL Forwarding table is loaded*	*SJA1105Q/S*
L2 Lookup Parameters table	0Dh	no	all
L2 Forwarding Parameters table	0Eh	yes	all
Clock Synchronization Parameters table	*0Fh*	*no*	*SJA1105Q/S*
AVB Parameters table	10h	no	all
General Parameters table	11h	yes	all
Retagging table	12h	no	all
Credit-Based Shaping table	13h	no	all
xMII Mode Parameters table	4Eh	yes	all
CGU Config Parameters	80h	no	all
RGU Config Parameters	81h	no	all
ACU Config Parameters	82h	no	all
SGMII Config Parameters	*C8h*	*no*	*SJA1105R/S*

Note that this table only lists tables that can be loaded through the static configuration interface. Other tables can only be programmed at runtime.

Table 4. Configuration tables only programmable during runtime

Table name	Comment
L2 Address Lookup table	for dynamically learned L2 entries (when LOCKEDS=0)
Management L2 Address Lookup table	for management frames sent by the host controller

5.1 Time-Triggered Ethernet (SAE AS6802) Configuration Tables

SJA1105Q and SJA1105S only

The following sections list the configuration tables that control settings specific to Time-Triggered Ethernet.

5.1.1 Schedule table

Table 5 shows the layout of entries in the Schedule table. A schedule can host up to 8 periods of arbitrary length. These periods are referred to as subschedules. The user may use any number of subschedules but if a schedule is enabled, subschedule zero must be activated. The number of subschedules defined, as well as whether the schedule is enabled, is determined by the settings in the Schedule Entry Points table (as discussed in Section 5.1.2). If the schedule is disabled, writing to this configuration block has no effect (and can be omitted). Entries for a particular subschedule must be provided in back-to-back write access cycles and must be ordered according to their appearance on the timeline. The order in which the subschedules are provided is arbitrary (but it determines the contents of the Schedule Entry Points table , Table 6). Entries of subschedules with lower indices must be provided prior to entries of subschedules with higher indices. The entries are referenced by the ADDRESS field in the Schedule Entry Points table as well as by the SUBSCHEIND fields of the Schedule Parameters table (Table 13) where the reference equals the ordinal number used to load the respective entry decremented by one (so the first entry of the Schedule table is referenced as 0). The table contains up to 1024 entries. This table is compulsory if entries are provided for the Schedule Entry Points table.

Table 5. Schedule Table (block 00h)

Bit	Symbol	Description
63:54	WINSTINDEX	Defines the index in the VL Forwarding table referred to by the WINST flag of the trigger. It is only used when WINST is set.
53	WINEND	When set, indicates that the reception window of the entry in the VL Forwarding table indexed by VLINDEX ends here.
52	WINST	When set, indicates that the reception window of the entry in the VL Forwarding table as indexed by WINSTINDEX starts here.
51:47	DESTPORTS	Defines the ports (1 bit per port) that the respective trigger event applies to. Bits at lower bit positions are assigned to ports with lower port numbers.
46	SETVALID	This flag is used to mark the first trigger to apply on a sampled non-time-triggered input. it allows the delivery order of a sampled non-time-triggered input to be fixed offline. If such a delivery order is not needed, the flag is set for all triggers having the same VLINDEX value. For time-triggered input, the flag is usually set for all entries (since receive and transmit triggers are in phase anyway). The TXEN flag of an entry must be set for this flag to have an effect.
45	TXEN	If this flag is set, the current entry triggers the dispatch of an output VL as indexed by the VLINDEX of the entry.

Bit	Symbol	Description
44:36	RESMEDIA	Contains an 'enable' flag at the highest bit position and one flag per priority at the output port, where the flag at the lowest bit position is assigned to priority 0. If the 'enable' flag is set: the switch stops process priority queues whose respective flags are set in the lower bit positions of this field for all Ethernet ports that have their respective flag set in DESTPORTS the switch enables processing of priority queues whose respective flags are cleared in the lower bit positions of this field for all Ethernet ports that have their respective flag set in DESTPORTS The reservation state of ports not having their respective flag set in DESTPORTS does not change. Media reservation is processed individually for each subschedule and a priority queue at a specific port remains suspended as long as at least one subschedule has a reservation pending for this priority at this port. Transmission of locally sourced protocol control frames cannot be blocked by media reservation. At times that the schedule is stopped (not synchronized), all media reservation is removed until a trigger event that enables media reservation occurs after integration.
35:26	VLINDEX	Defines the VL Forwarding table index (as discussed in Table 11) referenced by the trigger. The contents of the field are arbitrary when the TXEN flag of the entry is not set. If the TXEN flag of the entry is set, the value in the VLINDEX field must be less than the number of entries defined for the VL Forwarding table.
25:8	DELTA	This parameter defines by how much the current trigger event precedes the next trigger event of the same subschedule in multiples of 200 ns. The user must ensure that no two entries in this, or another, subschedule ever fire at the same time. To avoid the former, a value of zero is not allowed for this field. Schedule analysis is needed to prevent the latter (this analysis must take the contents of the Schedule Entry Points table into account).
7:0	Not used	

5.1.2 Schedule Entry Points table

SJA1105Q and SJA1105S only

The Schedule Entry Points table establishes the link between the synchronization algorithm and the schedule. The schedule will not be active if the user fails to load this table (even if the Schedule table is loaded). Each entry point into the schedule consists of eight entries in the Schedule Entry Points table. The entries included in an entry point must be sorted in ascending order (i.e. smaller values must be loaded before larger values) according to their respective DELTA values. Undefined entries (if the subschedules are not all used) must be provided after the valid entries. The entry point must contain exactly one valid entry for each active subschedule (the table thus provides space for up to 2048 entries). No two entries of an entry point can contain identical DELTA values and zero is not allowed.

Table 6. Schedule Entry Points table (block 01h)

Bit	Symbol	Description
31:29	SUBSCHINDX	This field defines the subschedule the respective entry point refers to. The value provided here must identify an active subschedule as defined by the SUBSCHEIND field of the Schedule Parameters configuration block. Any two entries of an entry point assigned to an active subschedule must contain different values for this field. An arbitrary value may be provided for inactive subschedules.

Bit	Symbol	Description
28:11	DELTA	This field defines the delay before this entry fires in multiples of 200 ns. Any two entries of an entry point assigned to an active subschedule must contain different values for this field. A value of zero is not allowed. An arbitrary value may be provided for inactive subschedules.
10:1	ADDRESS	This field provides the index in the Schedule table holding the event to fire at the respective time. This index must be within the range assigned to the subschedule as identified by the SUBSCHINDX field of this entry and defined by the respective SUBSCHEIND field of the Schedule Parameters configuration block. An arbitrary value may be provided for inactive subschedules.
0	not used	

5.1.3 VL Lookup table

SJA1105Q and SJA1105S only

Table 7 and Table 8 show the layout of an entry in the VL Lookup table. The table establishes the link between the stream identifier and the entry in the VL Policing table. The layout depends on the setting of the VLLUPFORMAT flag in the General Parameters configuration block. If the user does not load this table, all critical input traffic is dropped. The table has 1024 entries.

If VLLUPFORMAT is set to 0, the entries in the VL Lookup table must be sorted in ascending order (i.e. the smallest value must be loaded first) according to the following sort order: MACADDR, VLANID, PORT, VLANPRIOR. If VLLUPFORMAT is set to 1, the entries in the VL Lookup table must be sorted in ascending order according to the following sort order: VLID, PORT.

Table 7. VL Lookup table when VLLUPFORMAT = 0 (block 02h)

Bit	Symbol	Description
95:91	DESTPORTS	This field contains the set of destination ports to which a frame matching this entry is forwarded if ISCRITICAL is cleared.
90	ISCRITICAL	When this field is set, the configured entry is treated as rate-constrained or time-triggered; if this field is cleared, the configured entry is a static configuration of a best-effort flow and is treated as best-effort.
89:42	MACADDR	This field contains the destination MAC address to be associated with the respective table index.
41:30	VLANID	This field contains the VLAN ID to be associated with the respective table index position.
29:27	PORT	This field contains the number of the input port the respective stream (as identified by MACADDR, VLANID and VLANPRIOR) is allowed to access. A stream may be allowed on any number of ports. If allowed on more than one port, it will have dedicated entries within the VL Policing table configuration block for each eligible source port.
26:24	VLANPRIOR	This field contains the VLAN Priority to be associated with the respective table index position.
23:0	not used	

Table 8. VL Lookup table when VLLUPFORMAT = 1 (block 02h)

Bit	Symbol	Description
95:91	EGRMIRR	All traffic matching the stream identified by the VLID and PORT fields of the entry, and routed to any of the ports having its flag asserted in this field, is routed to the mirror port (as defined by the MIRR_PORT field of the General Parameters configuration block).
90	INGRMIRR	If this flag is set, all traffic matching the stream identified by the VLID and PORT fields of the entry is routed to the mirror port as defined by the MIRR_PORT field of the General Parameters configuration block.
89:58	not used	
57:42	VLID	This field contains the VL ID to be associated with the respective table index position.
41:30	not used	
29:27	PORT	This field contains the number of the port the respective VL ID is allowed to access. A VL ID may be allowed on any number of ports. If allowed on more than one port, it will have dedicated entries in the VL Policing table configuration block for each source port.
26:0	not used	

5.1.4 VL Policing table

SJA1105Q and SJA1105S only

Table 9 and Table 10 show the layout of an entry in the VL Policing table. These entries provide timing and sizing rules for critical traffic. The rules to be applied depend on the traffic type. The table entries have different layouts depending on whether they are used to police time-triggered traffic or rate-constrained traffic. The table contains 1024 entries.

Table 9. VL Policing table – time-triggered VLs TTRC = 1 (block 03h)

Bit	Symbol	Description
63	TTRC	A value of 1 at this bit position indicates that the entry defines a time-triggered VL.
62:52	MAXLEN	This field defines the maximum length of frames of this entry in bytes, including all Ethernet overhead (6-byte destination MAC address, 6-byte source MAC address, 2-bytes EtherType field, 4-byte frame checksum). The maximum allowed value for this field is 2043.
51:42	SHARINDX	Contains the index in the VL Forwarding table to be used with this entry. This index is usually the index of the entry itself. All entries for time-triggered VLs having identical values set for this field share memory space. They can be used to implement a pick-first-valid redundancy mechanism on time-triggered VLs on input. The dispatch policy is determined by the entry in the VL Forwarding table indexed by this field.
41:0	not used	

Table 10. VL Policing table – rate-constraint VLs TTRC = 0 (block 03h)

Bit	Symbol	Description
63	TTRC	A value of 0 at this bit position indicates that the entry defines a rate-constrained VL.
62:52	MAXLEN	This field defines the maximum length of frames of this entry in bytes, including all Ethernet overhead (6-byte destination MAC address, 6-byte source MAC address, 2-bytes EtherType field, 4-byte frame checksum). The maximum allowed value for this field is 2043.

Bit	Symbol	Description
51:42	SHARINDX	Contains the index in this table that points to the BAG and JITTER fields to be used for this entry. This index is usually the index of the entry itself. For shared BAGs, all entries in this table that share the BAG must contain the same value for this field and this value must be the index of one of the entries sharing the BAG. The values of the BAG and JITTER fields of entries that are not pointed to by any entry are not used. Unlike time-triggered VLs, the contents of this field are not used to access the VL Forwarding table. Rather, the index received from searching the VL Lookup table is used to access the VL Forwarding table for VLs being policed in rate-constrained fashion.
41:28	BAG	The bandwidth allocation gap (BAG) value to be used for this entry in multiples of 100 µs. A value of zero disables the bag check. In the latter case, JITTER must also be set to zero.
27:18	JITTER	The bandwidth allocation gap (BAG) jitter value to be used for this entry in multiples of 10 µs. The value provided for this field must not be larger (in seconds) than the value provided for the BAG field. For example, if the value of BAG was 5, the maximum allowed value for JITTER would be 50. This is deemed sufficient to police traffic received from an end system which, according to the ARINC 664 p7 specification, exhibits a maximum jitter of 500 µs at a minimum BAG value of 1 ms. Should jitter accumulate in a multi-hop network to exceed the BAG value, policing must be disabled (by setting BAG to zero), starting at the first switch where jitter exceeds the BAG.
17:0	not used	

5.1.5 VL Forwarding table

SJA1105Q and SJA1105S only

Table 11 shows the layout of an entry in the VL Forwarding table. This table provides forwarding definitions for critical traffic. The table has 1024 entries.

Table 11. VL Forwarding table (block 04h)

Bit	Symbol	Description
31	TYPE	A value of 1 at this bit position indicates that the entry defines a time-triggered VL (i.e., frames of the VL are dispatched to destination ports in response to triggers from the schedule). A value of 0 at this bit position indicates that the entry defines a rate-constrained VL (i.e., frames of the VL are immediately dispatched to destination ports).
30:28	PRIORITY	Priority at the output port for frames matching this entry, where larger values indicate higher priority
27:25	PARTITION	VL memory partition that frames matching this entry draw from.
24:20	DESTPORTS	Defines the ports that frames matching this entry are routed to (1 bit per port). Bits at lower bit positions are assigned to ports with lower port numbers. In the case of rate-constrained VLs, these flags define the ports the frame is dispatched to when all policing checks have been passed. In the case of time-triggered VLs, this field should be set to bit-wise OR of all the DESTPORTS fields of the entries within the Schedule table with VLINDEX pointing to this entry in the VL Forwarding table and have TXEN asserted.
19:0	not used	

5.1.6 VL Forwarding Parameters

SJA1105Q and SJA1105S only

Table 12 shows the layout of an entry in the VL Forwarding configuration block.

Table 12. VL Forwarding Parameters table (block 0Ch)

Bit	Symbol	Description
95:86	PARTSPC(7)	These fields define the maximum amount of frame memory that can be used by a VL memory partition. A VL memory partition is a set of VLs that use shared memory to store their frames. When a frame is received and passes all policing checks, it draws from the VL memory partition as identified by the PARTITION field of the respective entry in the VL Routing table. Once the frame has been transmitted to all ports, the memory used to store the frame is credited to the respective VL memory partition. This parameter specifies the number of 128-byte memory blocks contained in the memory partition. A frame will require as many blocks as needed to ensure the sum of the bytes allocated is greater than or equal to the number of bytes contained in the frame, including Ethernet header and checksum but excluding a VLAN tag (if any). A block cannot be shared between frames. **Note:** The total number of assigned blocks (8 partitions for L2 traffic PLUS 8 partitions for VL traffic) must never exceed 910 if retagging is used or 929 if retagging is not used (see also Table 25)
…	…	
25:16	PARTSPC(0)	
15	DEBUGEN	Mirroring and re-tagging will be available for critical traffic only if this flag is set.
14:0	Not used	

5.1.7 Schedule Parameters

SJA1105Q and SJA1105S only

Table 13 shows the layout of an entry in the Schedule Parameters configuration block. This configuration block is compulsory if the user provides values for the Schedule Entry Points table (Table 4).

Table 13. Schedule Parameters table (block 0Ah)

Bit	Symbol	Description
95:86	SUBSCHEIND(7)	These fields define the last entry of the respective subschedule in the Schedule table. If the schedule is used at all, subschedule zero will always be active. For all other subschedules, the field must be set to the value of the active subschedule with the largest index that has an index smaller than the respective inactive subschedule. For example, if subschedules 0 and 3 are used while all other subschedules are unused, and subschedule 0 contains 5 schedule entries while subschedule 3 contains 8, then SUBSCHEIND(0), SUBSCHEIND(1) and SUBSCHEIND(2) would be set to 4 while all other entries would be set to 12. The array must contain a valid entry for each active subschedule.
…	…	
25:16	SUBSCHEIND(0)	
15:0	not used	

5.1.8 Schedule Entry Points Parameters

SJA1105Q and SJA1105S only

Table 14 shows the layout of an entry in the Schedule Entry Points Parameters configuration block. This configuration block is compulsory if the user provides values for the Schedule Entry Points table (Table 6).

Table 14. Schedule Entry Points Parameters table (block 0Bh)

Bit	Symbol	Description
31:30	CLKSRC	This field defines the clock source driving the schedule: **00** deactivates schedule execution **01** configures the switch to run in standalone mode, i.e., immediately integrating into the schedule without applying any clock correction **10** selects SAE AS6802 as clock source **11** selects the internal PTP clock which is under the control of the host as clock source.
29:27	ACTSUBSCH	This field defines the number of active subschedules minus one. Subschedule zero must always be defined if the Schedule Entry Points table is loaded.
26:0	Not used	

5.1.9 Clock Synchronization Parameters

SJA1105Q and SJA1105S only

Table 15 shows the layout of an entry in the Clock Synchronization Parameters configuration block.

Table 15. Clock Synchronization Parameters table (block 0Fh)

Bit	Symbol	Description
479:432	ETSSRCPCF	This field provides the Ethernet MAC address used as the source address for protocol control frames generated by the switch when the SWMASTER flag is set.
431:428	WAITTHSYNC	If an out-of-schedule input protocol control frame has this number, or more, membership flags set, the synchronization engine resets its time base to the frame.
427:408	WFINTMOUT	This parameter defines the maximum length of time the synchronization engine remains in WAIT_FOR_IN state, in multiples of 8 ns.
407:404	UNSYTOTSYTH	The value provided for this field defines the minimum number of in-schedule clock masters needed to convince the synchronization engine to switch from UNSYNC state to TENTATIVE SYNC state.
403:400	UNSYTOSYTH	This parameter defines the minimum number of flags that must be set in the membership field of an input integration frame to cause the synchronization algorithm to switch from UNSYNC state to SYNC state.
399:396	TSYTOSYTH	This value defines the minimum number of in-schedule clock masters needed to switch the synchronization engine from TENTATIVE SYNC state to SYNC state.
395:392	TSYTH	This parameter defines the minimum number of in-schedule clock masters needed to keep the synchronization engine in TENTATIVE SYNC state.
391:388	TSYTOUSYTH	This field defines the minimum number of out-of-schedule clock masters needed to convince the synchronization engine to switch from TENTATIVE SYNC state UNSYNC state.
387:384	SYTH	The value provided for this field defines the minimum number of in-schedule clock masters needed to keep the synchronization engine in SYNC state.

Bit	Symbol	Description
383:380	SYTOUSYTH	This parameter defines the minimum number of out-of-schedule clock masters needed to convince the synchronization engine to switch from SYNC state to INTEGRATE state or UNSYNC state, respectively.
379:378	SYPRIORITY	Used to check the sync priority of input protocol control frames and to set the sync priority field of output protocol control frames.
377:374	SYDOMAIN	Used to check the sync domain of input protocol control frames and to set the sync domain field of output protocol control frames.
373:370	STTH	This parameter defines the minimum number of in-schedule clock masters needed to keep the synchronization engine in STABLE state; if the number of in-schedule clock masters remains below this value for as many cycles as defined by the NUMUNSTBCY parameter, the synchronization engine switches to INTEGRATE state.
369:366	STTOINTTH	This field defines the minimum number of out-of-schedule clock masters needed to convince the synchronization engine to switch from STABLE state to INTEGRATE state.
365:355	PCFSZE	This parameter determines the size, in bytes, of a PCF both on input as on output, including: 6-byte destination MAC address, 6-byte source MAC address, 2-byte EtherType field, and 4-byte frame checksum. This parameter is used to assemble output PCFs by appending as many trailing zeroes as needed to achieve the configured frame size. On input, the length of a PCF is expected to match the value of this parameter. If not, the frame is dropped. The clock synchronization block executes this check. To have a length limitation active for PCFs that pass through the switch, the MAXLEN field of the respective VL Policing table entries must be used. The minimum required value for this field is 64, the maximum allowed value is 2043.
354:351	PCFPRIORITY	This parameter determines the priority of a PCF sourced by a switch configured as compression master. It does not affect PCFs that are routed by the switch (even if the switch is configured as a compression master). The value of this parameter must be larger than the PRIORITY field of entries of the VL Forwarding Table or the VLANPMAP values of the L2 Forwarding configuration block (or their respective dynamically changed values) for a PCF to win the priority selection.
350:336	OBVWINSZ	This parameter defines the value of the observation window used by the compression master to collect and compress input protocol control frames. It is specified in multiples of 8 ns.
335:329	NUMUNSTBCY	This value defines the number of cycles of low clique support (i.e. the number of in-schedule clock masters that remain below the value of the STTH parameter) that can pass before the synchronization engine switches to INTEGRATE state. If it is zero, the synchronization engine will transit to INTEGRATE state at the end of the first acceptance window while in STABLE state (if support is not provided for the clique).
328:322	NUMSTBCY	This value defines the number of cycles of clique support (i.e. the number of in-schedule clock masters meets the value of the SYTH parameter) needed to cause the synchronization engine to transit from SYNC state to STABLE state. If it is zero, the synchronization engine will transit to STABLE state at the end of the first acceptance window while in SYNC state (if there is support for the clique). The parameter is only used when the SYTOSTBEN flag is set.
321:295	MAXTRANSPCLK	Determines the age at which a frame is processed by the compression master or the sync engine. It is provided in multiples of 8 ns and must account for the maximum PCF latency from synchronization masters or compression masters to this switch.
294:287	MAXINTEGCY	Determines the maximum value of the integration cycle that the synchronization engine will accept in input PCFs. If the IPCFRAMESY flag is set, this field determines the maximum value of output PCFs generated by the switch.

Bit	Symbol	Description
286:257	LISTENTMOUT	This parameter defines the maximum number of clock cycles that the synchronization engine remains in INTEGRATE state before switching to UNSYNC state when the SWMASTER flag is set. It is specified in multiples of 8 ns.
256:230	INTCYDUR	This field defines the duration of an integration cycle in multiples of 8 ns. The actual duration of the cycle will be by one greater than the value given in this field.
229: 226	INTTOTENTTH	This value defines the minimum number of clock masters supporting an integration frame needed to perform a transition from INTEGRATE state to WAIT 4 CYCLE START state.
225:222	INTTOSYNCTH	This value defines the minimum number of clock masters needed to convince the synchronization engine to switch from INTEGRATE state to SYNC state.
221:206	VLIDOUT[4]	This field defines the VL IDs to be used for protocol control frames generated by the switch when the SWMASTER flag is set. This value is always used for the VL ID field of Coldstart frames. If the VLIDSELECT flag is cleared, the ID of coldstart acknowledgement frames will be one greater than this value; if the VLIDSELECT flag is set, this value will be the VL ID. If the VLIDSELECT flag is cleared, integration frames will have an ID that is two greater than this value; if the VLIDSELECT flag is set, this value will be the VL ID. The value of the field must be less than 65534 if the VLIDSELECT flag is cleared.
	…	
157:142	VLIDOUT[0]	
141:126	VLIDINMIN	This field defines the minimum VL ID used for input protocol control frames. All critical traffic input frames with a VL ID greater than or equal to this value and less than or equal to the value of VLIDINMAX are processed by the clock synchronization block of the IP. The value of the field must be smaller than the value of the VLIDINMAX field.
125:110	VLIDINMAX	This field defines the maximum VL ID that is used for input protocol control frames. All critical traffic input frames with a VL ID less than or equal to this value and greater than or equal to the value of VLIDINMIN are processed by the clock synchronization block of the IP. The value of the field must be larger than the value of the VLIDINMIN field. If the SWMASTER flag is set, the value of this parameter must be less than VLIDINMIN plus 24. Otherwise it must be less than VLIDINMIN plus three.
109:90	CAENTMOUT	This parameter defines how long the synchronization engine remains in CA ENABLED state following the reception of a coldstart or coldstart acknowledge protocol control frame in UNSYNC state. It is specified in multiples of 8 ns.
89:75	ACCDEVWIN	This parameter is specified in multiples of 8 ns and determines the maximum deviation of an integration protocol control frame from the expected arrival time to be still considered in schedule.
74	VLIDSELECT	This parameter determines if all protocol control frames use the same VL ID (when set) or dedicated VL IDs for each type (when cleared).
73	TENTSYRELEN	Determines if the switch relays time-triggered traffic while the clock synchronization engine is in TENTATIVE SYNC state.
72	ASYTENSYEN	If this flag is set, the asynchronous clique detection mechanisms are enabled in TENTATIVE SYNC state.
71	SYTOSTBEN	This parameter enables the transition of the clock synchronization algorithm from SYNC state to STABLE state if enough rounds (as specified by NUMSTBCY) have been passed in SYNC state.
70	SYRELEN	Determines if the switch relays time-triggered traffic at times the clock synchronization engine resides in SYNC state.
69	SYSYEN	If this flag is set, the synchronous clique detection mechanisms are enabled in SYNC state.
68	SYASYEN	If this flag is set, the asynchronous clique detection mechanisms are enabled in SYNC state

Bit	Symbol	Description
67	IPCFRAMESY	When this flag is set, the switch periodically transmits integration protocol control frames with a period defined by the INTCYDUR field. When set, it requires flags VLIDSELECT, SYTOSTBEN, ACCDEVWIN, VLIDOUT, MAXINTEGCY, SYDOMAIN, SYPRIORITY and ETSSRCPCF and either OUTPRTSLAVE or OUTPRTMASTER to be configured. The remaining Clock Synchronization Parameters are not used if this flag is set.
66	STABASYEN	If this flag is set, the asynchronous clique detection mechanisms are enabled in STABLE state.
65	SWMASTER	If this flag is set, the switch acts as a compression master for the clock synchronization algorithm.
64	FULLCBG	If this flag is set, a switch with SWMASTER set exhibits guardian functionality on input protocol control frames. It is intended to be cleared in high-integrity environments (i.e. where sync master end systems are set up as high-integrity components).
63:61	SRCPORT(7)	These fields establish a mapping of protocol control frame membership flags to switch source ports. They are used to prevent source port spoofing. In case of multi-hop networks, a single port may host several membership flags (at the compression master). If specific membership flags are not used, their respective entries would be set to values greater than 4. If the SWMASTER flag is cleared, SRCPORT(0) must be set to the index of the port connected to the compression master and all other ports to a value greater than 4.
…	…	
42:40	SRCPORT(0)	
39:35	OUTPRTSLAVE	This vector contains a flag for each port defining if integration protocol control frames sourced at the switch are output to the respective Ethernet port. It has an effect only when the SWMASTER flag or the IPCFRAMESY flag is set. Any protocol control frames not sourced at the switch are routed through the switch like non-protocol control frames. Policing and forwarding tables must be set up for the respective VLs.
34:30	OUTPRTMASTER	This vector contains a flag for each port defining if protocol control frames sourced at the switch are output to the respective Ethernet port. In contrast to a port having its flag set in OUTPRTSLAVE, ports having their flag set in this field output coldstart protocol control frames as well as coldstart acknowledge protocol control frames, in addition to integration protocol control frames. It has an effect only when the SWMASTER flag or the IPCFRAMESY flag is set. Any protocol control frame not sourced at the switch will be routed through the switch in the same way as non-protocol control frames. Policing and forwarding tables must be set up for the respective VLs.
29:0	not used	

5.2 General Configuration Tables

All Variants

The following section lists the configuration tables that control the IEEE 802.3 traffic forwarding rules and other switch-related configuration options. Note that some settings in the table control Time-Triggered Ethernet (SAE AS6802) functionality. These are highlighted separately.

5.2.1 L2 Address Lookup table

The L2 Address Lookup table controls TCAM address lookup and frame forwarding.

Table 16 and Table 17 show the possible layouts of an entry in the L2 Address Lookup table. Parts of the table can be statically configured prior to dynamic address learning. Unlike other configuration blocks, loading of this block must not start before the L2BUSYS flag in the status area has been set (see Table 37). Loaded entries in this table share memory with entries dynamically learned during operation. However, loaded

entries never time-out and cannot be replaced by learned entries. Physically, the memory used to store the lookup table is a 1024-entry TCAM array. This allows 1024 non-conflicting forwarding rules to be stored.

The L2 Address Lookup table is used to store unicast as well as multicast forwarding rules. Fig 12 illustrates L2 Address Lookup operation.

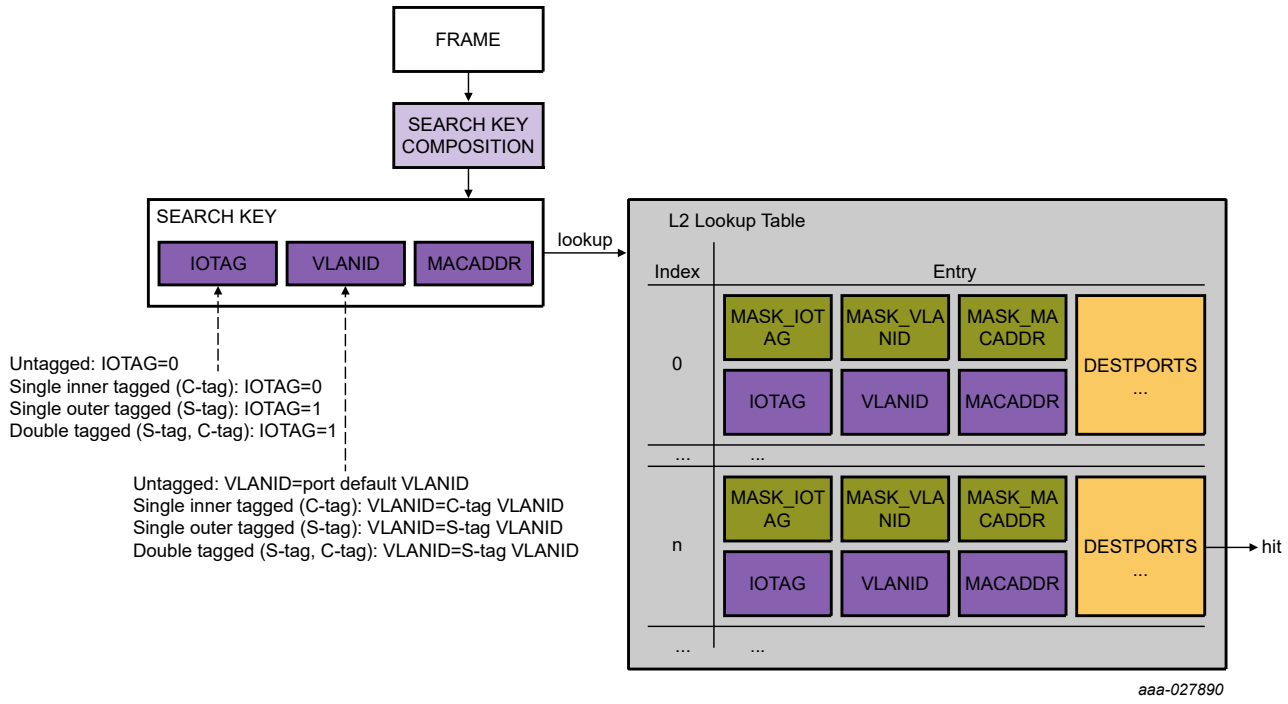


Figure 9. L2 Address Lookup

The L2 Address Lookup logic operates on a single (VLANID, MAC) pair. In the case of a double tagged frame (S-Tag, C-Tag), the outer VLANID (S-Tag) is always used for searches in the TCAM. In the case of a single outer tagged (S-tag) or single inner tagged (C-tag) frame, there is only one VLANID.

The flag IOTAG is used to indicate if the VLANID belongs to an inner (C-tag) or outer (S-tag) tag. If the frame is a double tagged frame (S-Tag, C-tag) or a single outer tagged frame (S-Tag), IOTAG will be set to 1. For frames that are untagged or have a single inner tag (C-tag), IOTAG will be set to 0.

For each frame, the TCAM is searched with the following key: IOTAG & VLANID & MACADDR.

Table 16 shows the layout for entries configured over the static configuration interface. Each entry programs a static address lookup (LOCKEDS = 1). Dedicated layouts are used for dynamically learned entries and MGMT entries. These layouts are only used for dynamic configuration and cannot be used for static configuration. The runtime interface can be used to read, write and modify all possible entry types: static entries, dynamically learned entries (LOCKEDS = 0) and MGMT entries[1].

Note that the TCAM is queried twice, first with the source address MAC for ENFPORT and learning check, then with the destination address MAC for forwarding decisions. For shared learning, the TCAM is always searched with VLANID = 0.

1 See section 5.2.1.1 for the definition of MGMT entries.

Table 16. L2 Address Lookup table (LOCKEDS = 1) (block 05h)

Bit	Symbol	Description
159	TSREG	see TAKETS
158:147	MIRRVLAN	see RETAG
146	TAKETS	This flag controls TCAM-based trapping (automatic forwarding to the HOST port) and timestamping behavior. If a destination MAC address received on the Host Port produces a match in the TCAM memory, and both TAKETS and LOCKEDS flags are asserted, then an egress timestamp is captured for each frame transmitted to a destination port as defined by DESTPORTS. The egress timestamp is stored in one of the two per-port egress timestamp registers (i.e. *PTPEGR_TS = 2*PORT+TSREG*, where PORT is the destination port for which a timestamp is captured). If a received frame produces a match in the TCAM memory, this flag and LOCKEDS are both found asserted, and the frame is received on any port other than Host Port or Cascaded Port, the respective frame is forwarded to the Host Port followed by the Meta-data follow-up frame that contains the ingress timestamp of the received frame.
145	MIRR	If the destination **or** source MAC address of a received frame produces a match in the TCAM and this flag is found asserted in any (or both) of the matched TCAM entries, the frame is mirrored to MIRR_PORT (if MIRR_PORT is a valid port). If the flag is found asserted for a *source* MAC address match, then the mirrored frame is handled according to the ingress mirroring rules (it is tagged with the INGMIRRVID associated with the port on which the frame is received). If the flag is found asserted for a *destination* MAC address match, then the mirrored frame is handled according to the egress mirroring rules (it is tagged with the EGRMIRRVID from the General Parameters table). If the flag is found asserted for both the destination and source MAC addresses, then the flag MIRRCIE resolves if the frame is handled as an ingress or egress mirrored frame.
144	RETAG	If a destination **or** source MAC address of a received frame produces a match in the TCAM and this flag is found asserted in any of the matched TCAM entries, then the frame is retagged using the MIRRVLAN as the new VLAN ID. Retagging means creating copies of tagged Ethernet frames, which will receive new VLAN IDs and are then routed as if they were received on the original source port. If the flag is found asserted for both the destination and source MAC addresses, then the flag from the source MAC address match has precedence and the frame is retagged using the MIRRVLAN VLAN ID from the TCAM entry associated with the source MAC address. If the original frame is dropped and only the retagged frame is to be forwarded, DESTPORTS should be set to zero. If DESTPORTS is not set to zero, two frames will be transmitted: the original frame and the retagged frame
143	MASK_IOTAG	The mask used by TCAM memory for search operations. Bits that are zero indicate don't-care. Bits that are one are evaluated during search operation.
142:131	MASK_VLANID	see MASK_IOTAG
130:83	MASK_MACADDR	see MASK_IOTAG
82	IOTAG	If this bit is deasserted, this entry will match a VLANID originating from an inner tag (C-tag). If this bit is asserted, this entry will match with a VLAN originaing from an outer tag (S-tag). *Note that TCAM matching depends on whether or not this bit is masked by the don't-care bits of the MASK.*
81:70	VLANID	The VLAN ID this entry is to be used for. VLANID is only included in the lookup process if SHARED_LEARN is cleared, otherwise this parameter is ignored.
69:22	MACADDR	The MAC address this entry is to be used for; can be a unicast or multicast address.

Bit	Symbol	Description
21:17	DESTPORTS	Defines the ports (one bit per port) to which frames carrying MACADDR as destination MAC address will be forwarded. Bits at lower bit positions are assigned to ports with lower port numbers. E.g. a frame whose IOTAG, VLANID and destination address match will be forwarded to the ports indicated by DESTPORTS
16	ENFPORT	If this flag is found set, MACADDR will be enforced as source MAC address on ports having their flag set in DESTPORTS; i.e., if a L2 frame carrying MACADDR as its source MAC address is received on a port other than those set in MACADDR, it will be dropped.
15:6	INDEX	Contains the address in physical memory where this entry is to be stored. *Note that a lower index has precedence over a higher index if multiple rules match.*
5:0	Not used	

Table 17. L2 Address Lookup table (LOCKEDS = 0) (only used for dynamically learned entries)

Bit	Symbol	Description
159	TOUCHED	Internal flag for aging.
158:144	AGE	Stores the aging counter of the associated entry. When aging is performed and the counter is equal to a configured maximum age value (see MAXAGE, L2 Address Lookup Parameters), the entry is invalidated and marked as available for dynamic learning.
143	MASK_IOTAG	*See Table 16*
142:131	MASK_VLANID	
130:83	MASK_MACADDR	
82	IOTAG	
81:70	VLANID	
69:22	MACADDR	
21:17	DESTPORTS	
16	ENFPORT	
15:6	INDEX	
5:0	Not used	

5.2.1.1 Management L2 Address Lookup table

This section provides the layout of an entry of the Management L2 Lookup Table. This table controls how management frames are forwarded.

Management (MGMT) frames are special frames that are identified by the MAC address filter (MAC_FLT, see General Parameters, Section 5.2.11). In typical applications, these frames have multicast addresses in the 01-80-C2 range.

If such a frame is identified by the switch (MAC_FLT match), it is forwarded to the HOST_PORT for processing. The processor can also send a MGMT frame. To do so, the switch needs to know the destination (DESTPORTS) of the frame through a MGMT route. A MGMT route is set up by creating an entry in the Management L2 Address Lookup table. If the processor sends a MGMT frame to the HOST_PORT without a

MGMT route being set up, the frame is dropped. A MGMT entry is valid for a single frame only and is automatically invalidated after it is used.

The Management L2 Lookup table is a four entry table located next to the L2 Lookup table. This table is only accessed through the dynamic control interface where the host may insert management forwarding information.

This table is in addition to, and its entries have a similar layout to, the L2 Lookup Table.

Table 18. Management L2 Address Lookup table (no block ID – only runtime accessible)

Bit	Symbol	Description
95:72	Not used	
71	TSREG	Defines the offset to be used for any port set in DESTPORTS to store the IEEE 1588 timestamp in the IEEE 1588 egress timestamp register. The egress timestamp will be put into the following timestamp register *PTPEGR_TS = 2*PORT+TSREG*
70	TAKETS	If set, egress timestamps are captured. See TSREG
69:22	MACADDR	Defines which destination MAC address this management address is used for.
21:17	DESTPORTS	Defines the ports (one bit per port) to which the management frame is forwarded
16	MGMTVALID	This flag must be asserted when a management entry is programmed by the host. An entry will be valid only for a single received frame for which the destination MAC address matches. After that the management entry will be invalidated and MGMTVALID is deasserted. An invalid entry will be ignored. In case no management entry is available, a frame matching the link-layer filtering (MAC_FLT) will be dropped.
15:6	INDEX	Defines the index which is used in the management table. This value must be between 0 and 3. Upper bits must be zero.
5:0	Not used	

5.2.2 VLAN Lookup table

Table 19 shows the layout of an entry in the VLAN Lookup Table. The table is used to statically configure VLAN information. A table entry defines the ports that are members of a specific VLAN. It also defines the broadcast domain, together with the set of ports on which a VLAN tag must be inserted or removed on egress. The table supports 4096 entries.

The switch supports double tagging but only a single VLANID is used for the VLAN lookup. In the case of a double tagged (S-tag, C-tag) frame, the VLANID associated with the outer tag (S-tag) is used for the VLAN Lookup. For single C-tag or single S-tag frames, the VLANID of the respective tag is used. This behavior cannot be configured.

Table 19. VLAN Lookup Table (block 07h)

Bit	Symbol	Description
63:59	VING_MIRR	This vector controls VLAN ingress mirroring. All traffic that matches this VLAN entry (see VLANID) and that is received on any of the ports whose flag is asserted in this field is forwarded to the mirror port, as defined by the MIRR_PORT field of the General Parameters configuration block.

Bit	Symbol	Description
58:54	VEGR_MIRR	This vector controls VLAN egress mirroring. All tagged traffic that matches this VLAN entry (see VLANID) and is forwarded to any of the ports whose flag is asserted in this field is forwarded to the mirror port, as defined by the MIRR_PORT field of the General Parameters configuration block.
53:49	VMEMB_PORT	Defines the set of ports on which a frame tagged with the respective VLAN ID may be received. All bits must be set in order to deactivate VLAN-based ingress port admission.
48:44	VLAN_BC	This field restricts the broadcast domain of a VLAN. A cleared bit inhibits egress of traffic (unicast, multicast or broadcast) on the associated port. All bits must be asserted to enable unrestricted reachability on all ports for this VLAN. When all bits are cleared, all frames for this VLAN are dropped.
43:39	TAG_PORT	Defines if a frame associated with the respective VLAN ID is transmitted untagged (without an IEEE 802.1Q VLAN tag field) or transmitted with a tag (the flag of these ports would be set in TAG_PORT). As each untagged frame gets tagged on ingress with the port VLAN ID, all bits must be cleared in order to transmit untagged frames at the output. If TAG_PORT is deasserted and a double tagged frame is received, it will be sent with the inner tag (C-tag) only.
38:27	VLANID	The VLAN ID associated with this entry. The VLANID used for the lookup is extracted from the outermost tag (S-tag for double tagged frames and C-tag for single tagged frames).
26:0	Not used	

It is not mandatory to load a VLAN Lookup table. A default entry is automatically generated for VLANID 0 with the following settings: VING_MIRR = 0, VEGR_MIRR = 0, VMEMB_PORT = 11111b, VLAN_BC = 11111b, TAG_PORT = 0, VLANID = 0. If the static configuration stream has an entry for VLANID = 0, the default values are overwritten.

5.2.3 L2 Policing table

Table 20 shows the layout of an entry in the L2 Policing table. This table defines traffic policing rules individually for each port. It also defines the priority value for each port. The switch can monitor the bandwidth and the maximum frame sizes per port and per priority level (PCP value).

The table has 45 entries. Ethernet frames for which the user has not provided an entry are automatically mapped to entry 0. If this entry is not loaded, all L2 traffic will be dropped.

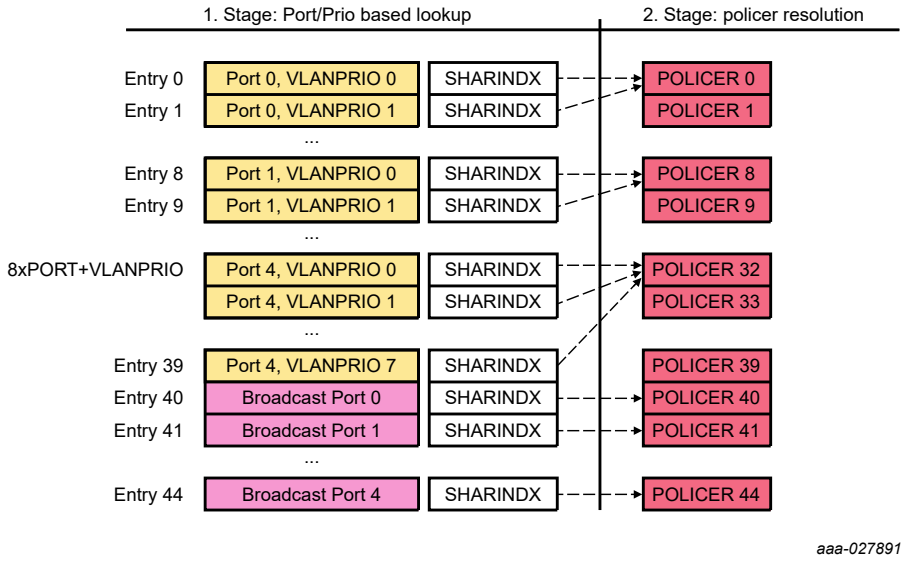
The entry to which an incoming frame maps is determined in the following way: if the incoming frame is classified as broadcast, the matching entry is 40 + PORT (where PORT is the physical port number between 0 and 4 on which the frame was received); if the frame is not classified as broadcast, the matching entry is 8 × PORT + VLANPRIO where VLANPRIO is the VLAN priority value associated with the frame.

The switch allows traffic from different ports or priorities to share common policing blocks. Resolving the actual policing block is a two stage process. First, the device determines the entry as discussed above (i.e. 8 × PORT + VLANPRIO or 40 + PORT). The SHARINDX field of this entry is then used to determine the policing block. This SHARINDX field can point to any of the 45 available policing blocks.

The algorithm used for bandwidth budgeting works as follows. Each policing block contains the parameters SMAX and RATE. Initially, the bandwidth credit of an entry

gets set to SMAX. When a valid Ethernet frame is received, the value of the bandwidth credit is decreased by the number of bytes in the frame (including Ethernet header and checksum). Every 8 µs the credit level is incremented by the value of RATE bytes divided by 64, to a maximum of SMAX bytes. This results in a datarate of (RATE × 8 bit / 64) / (8 µs). Analogously, RATE is set to a value of datarate (in unit bit/s) divided by 15625.

An associated frame gets dropped if the resulting value of the bandwidth credit is less than or equal to zero. This makes it possible to control the traffic rate individually for each port. In addition to the rate, each entry specifies the maximum length of frames associated with this entry and the memory partition that gets credited for this frame. This makes it possible to partition the maximum amount of frame memory available for different traffic classes.



1. Example only: All priority levels per port map to a single policer. Each port has a unique broadcast policer

Figure 10. Port / priority to policer resolution

Table 20. L2 Policing table (block 06h)

Bit	Symbol	Description
63:58	SHARINDX	This field contains the index pointing to the policing entry associated with this frame. It is a pointer to the L2 Policing table itself and can be used to merge several traffic classifications in one combined policing entry. As an example, if all incoming L2 traffic from port 0 is to be policed by policing block 0, the value of SHARINDX for entries 0 through 7 and entry 40 (broadcast) must be set to 0.
57:42	SMAX	This field contains the maximum burst size in bytes for received frames. Its value is used to initialize the bandwidth budget for this entry on start-up. This field defines the maximum bandwidth budget when no traffic associated with this entry has been received for a long time.
41:26	RATE	Admitted bandwidth in multiples of 15.625 kbps. This field contains the rate at which the bandwidth budget of traffic associated with this entry is credited when the port does not receive any traffic. The budget is credited RATE bytes divided by 64 every 8 µs with a maximum value of SMAX. A port allowed to source traffic at 1 Gbit/s would thus have a value of 64000 set for this field.

Bit	Symbol	Description
25:15	MAXLEN	This field defines the maximum length of frames of this entry in bytes including all Ethernet overhead (6-byte destination MAC address, 6-byte source MAC address, 2-bytes EtherType field, 4-byte frame checksum). The maximum allowed value for this field is 2043. For an untagged Ethernet frame with a payload size of 1500, MAXLEN must be set to 1518. For a single tagged Ethernet frame with a payload size of 1500, MAXLEN must be set to 1522. For a double tagged Ethernet frame with a payload size of 1500, MAXLEN must be set to 1526.
14:12	PARTITION	Memory partition that Ethernet frames matching this entry will draw from.
11:0	not used	

5.2.4 L2 Forwarding table

This table defines the mapping of ingress VLAN priority values to egress VLAN priority values as well as the mapping of egress VLAN priority values to priority queues physically available on the transmission ports. In addition, this table is used to define forwarding limitations for each ingress port.

The table contains 13 entries. Table 21 shows the layout of an entry in the L2 Forwarding table.

The first five entries in the table are used for a per-port based remapping of the ingress priority values to egress priority values. In the example, frames arriveing on port 0 with a priority of 4 are re-mapped to a priority value of 7. This means that the remapped priority will be used as the PCP (Priority Code Point) value on all egress ports forwarding the frame with a VLAN tag included (obtained by the TAG_PORT parameter in the VLAN configuration, see Table 19).

The last eight entries in the table are used for a per-egress priority-based mapping of logical priority values to physical priority queues of the different ports. There is one entry to control the mapping per priority level. In the example the mapping of priority level 7 on port 3 is mapped to queue 5.

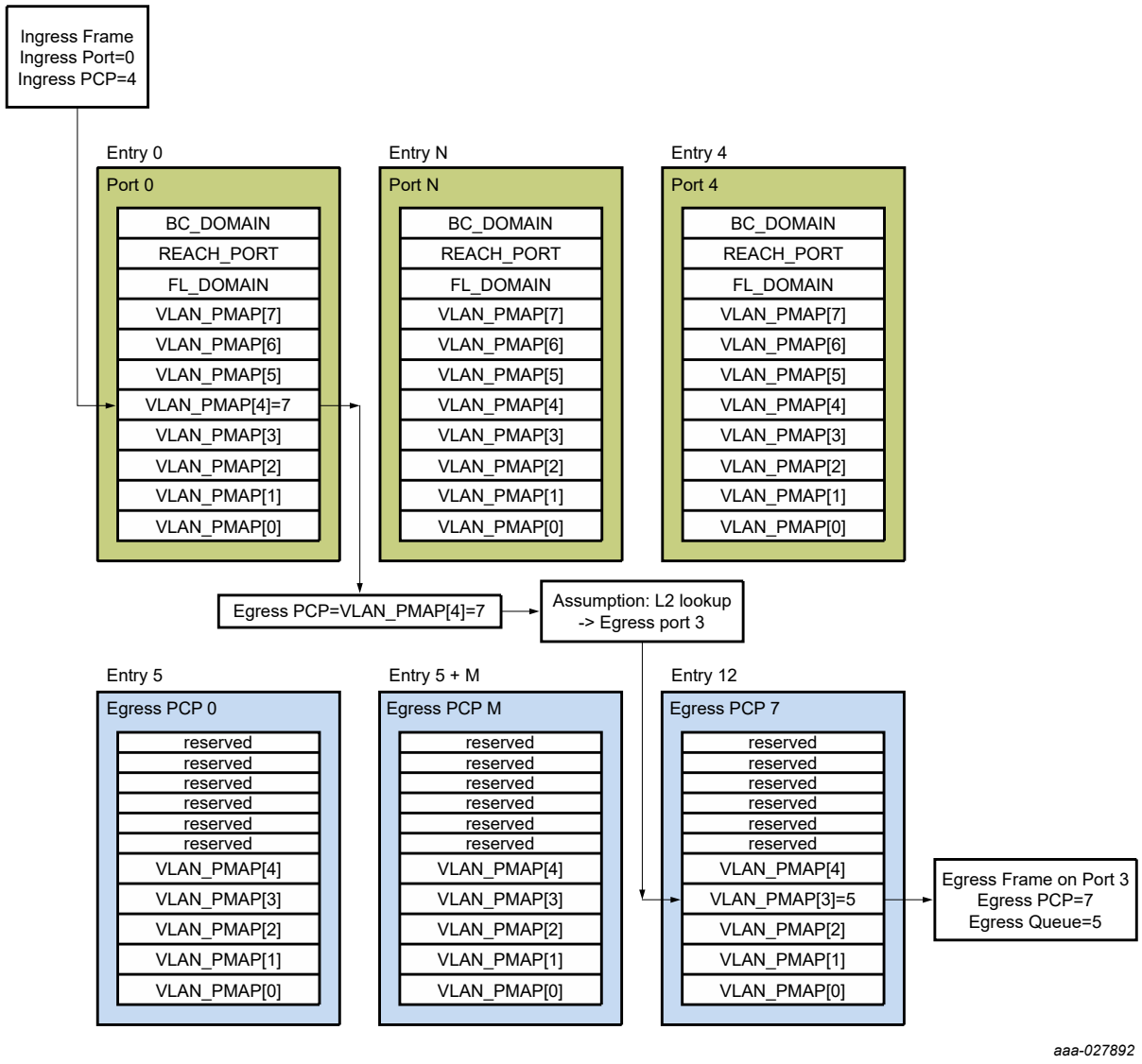


Figure 11. Ingress to Egress PCP resolution and queue selection

Table 21. L2 Forwarding table (block 08h)

Bit	Symbol	Description
63:59	BC_DOMAIN	Only valid for the first five entries in the table. Defines the broadcast domain of the port associated with the entry. Each port is assigned a bit in this field with the LSB mapping to port 0. Broadcast Ethernet frames received from the respective port are forwarded to the ports whose flags are set in this vector. The flag of the port associated with the entry itself must be cleared (to prevent loops).
58:54	REACH_PORT	Only valid for the first five entries in the table. Defines which ports can be reached by traffic received on the port associated with the entry. Each port is assigned a bit in this field with the LSB mapping to port 0. If a frame is received on the port associated with the entry and its destination MAC address is known (i.e. is contained in the L2 Address Lookup table), the frame is forwarded to the destination port only if the flag of the destination port is set in this field.

Bit	Symbol	Description
53:49	FL_DOMAIN	Only valid for the first five entries in the table. Defines the destination ports of unknown traffic at the port associated with this entry. Each port is assigned a bit in this field with the LSB mapping to port 0. If an Ethernet frame (that is not a broadcast frame) is received on the port associated with the entry and its destination MAC address is not known (i.e. is not contained in the L2 Address Lookup table), the frame is forwarded to those ports that have their respective flag set in this field. The flag of the port associated with the entry itself must be cleared (to avoid loops).
48:46	VLAN_PMAP[7]	For the first five entries in the table, this value defines the ingress VLAN priority remapping. The source port associated with the incoming frame is used as an index into the table, allowing ingress VLAN priority to egress VLAN priority mapping for each port. The result of the mapping is embedded in the transmitted frame on all ports included in the tagged set of the VLAN associated with the frame. For indices 5 to 12, this field contains the mapping of egress VLAN priority (determined by the first 5 entries in the table) to physical priority queues. In this case, the destination port is used as index into VLAN_PMAP.
…		
27:25	VLAN_PMAP[0]	
24:0	not used	

5.2.5 MAC Configuration table

Table 22 provides the layout of an entry in the MAC Configuration Table. The table is used to configure individual ports on the switch. The table has five entries. Configuration information for ports that are not used must be provided with EGRESS and INGRESS disabled.

Fig 15 shows an example of how to set queue depth per port. Each egress port can accommodate up to 512 frames in up to 8 queues. The 512 queue slots can be assigned arbitrarily to queues using the MAC Configuration table. The configuration of the queue sizes is performed by assigning each queue a consecutive range of unique slots from the common pool. This is done by marking the bottom (Base) and top (Top) area to be assigned to the queue. All 512 slots can be freely assigned. The following example shows a case in which all queues get an even distribution of 10 frames per queue, leaving some slots unassigned.

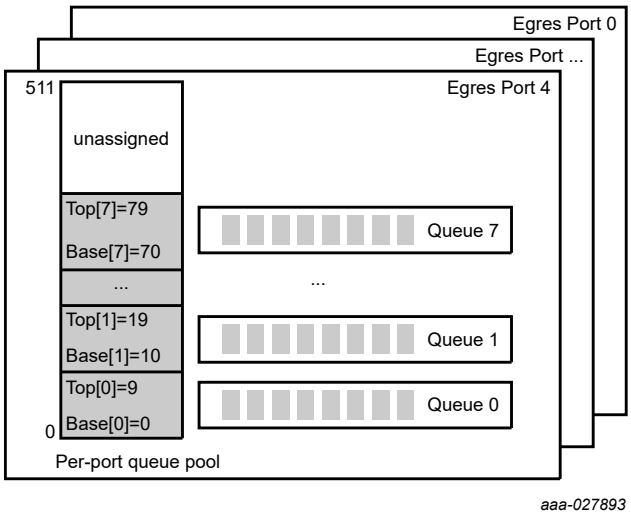


Figure 12. Example of setting the egress queue sizes

Table 22. MAC Configuration Table (block 09h)

Bit	Symbol	Description	
255:247	TOP[7]	The fields TOP, BASE and ENABLED are used to define the maximum number of frames of the respective priority that may be waiting in the output queue of the associated Ethernet port. If the respective priority is enabled at the port as indicated by ENABLED being set, then the value of TOP must be at least as large as the value configured for BASE for the priority at the relevant port. The maximum number of frames of the respective priority at the port is then TOP minus BASE plus one. Note: No two enabled queues at the same port may have overlapping intervals set for the TOP and BASE parameters. If ENABLED is not set for a priority, the values configured for the TOP and BASE parameters are ignored. The maximum total value allowed for these parameters is 511.	
246:238	BASE[7]		
237	ENABLED[7]		
…	…		
122:114	TOP[0]		
113:105	BASE[0]		
104	ENABLED[0]		
103:99	IFG	This parameter allows the standard Ethernet IFG of 12 bytes to be extended for output traffic on this port.	
98:97	SPEED		Port speed:
		11	Fixed 10 Mbps
		10	Fixed 100 Mbps
		01	Fixed 1 Gbps
		00	Speed set by host through runtime interface
96:81	TP_DELIN	Used to set a correction for updating the transparent clock of IEEE 1588v2 one-step event messages and Time-Triggered Ethernet (SAE AS6802) PCFs at the input port in multiples of 8 ns. This value can be changed during runtime if SPEED = 00.	
80:65	TP_DELOUT	Used to set a correction for updating the transparent clock of IEEE 1588v2 one-step event messages and Time-Triggered Ethernet (SAE AS6802) PCFs at the output port in multiples of 8 ns. This value can be changed during runtime if SPEED = 00.	
64:57	MAXAGE	*Note: SJA1105Q and SJA1105S only* Defines the maximum allowed age of critical traffic frames on the output in multiples of 4000 µs. The clock used to measure the age has a resolution of the same granularity. The minimum reasonable setting for this parameter is thus one (otherwise frames may get dropped depending on whether the clock wraps between reception and transmission). A value of 255 turns off the age check. This parameter should be set to zero in the SJA1105P and SJA1105R.	
56:54	VLANPRIO	Defines the IEEE 802.1Q priority value used to prioritize an untagged frame on this port. The value is in the range 0 to 7. This value is used as an index to VLAN_PMAP[7:0] in Table 21 to resolve the ingress priority to egress priority and ultimately physical priority queue mapping. This value is also used to calculate the index for the rate-policing entry to which untagged frames are assigned to (see L2 Policing Table).	
53:42	VLANID	Defines the VLAN ID used to tag untagged incoming frames on this port. Values can be chosen arbitrarily in the range 0 to 4095. The port default VLANID must be made known to the VLAN lookup table; port must be a member port (VMEMB_PORT).	
41	ING_MIRR	If this flag is set, all traffic received on this port is forwarded to the mirror port as defined by the MIRR_PORT field of the General Parameters configuration block.	
40	EGR_MIRR	If this flag is set, all traffic forwarded to this port is forwarded to the mirror port as defined by the MIRR_PORT field of the General Parameters configuration block. Note that this does not apply to locally generated PCFs, Time-Triggered Ethernet (SAE AS6802) (SJA1105Q and SJA1105S only).	

Bit	Symbol	Description
39	DRPNONA664	*SJA1105Q and SJA1105S only* If this flag is set, frames carrying an EtherType other than 800h are dropped on input at this port. This includes VLAN-tagged frames. Only non-VLAN IP frames are accepted at the port. Tha parameter should be set to zero in the SJA1105P and SJA1105R
38	DRPDTAG	Drop double tagged frames. When this flag is set, double-tagged ingress traffic is dropped at the respective port (i.e. traffic that has TPID1 as the outer tag followed by TPID2 as the inner tag). Flag affects L2 traffic only.
37	DRPSOTAG	If the frame carries a single outer tag (S-tag), drop it
36	DRPSITAG	If the frame carries a single inner tag (C-tag), drop it
35	DRPUNTAG	If this flag is set, untagged ingress traffic is dropped at the respective port.
34	RETAG	When set, this flag enables retagging (using VLANID configured for the respective port but maintaining the priority value) of priority-tagged input (VLAN ID 0) on the respective port. For double tagged frames, only the outer tag (S-tag) is retagged. This flag has no effect on untagged frames or frames with a VLANID other than 0. Untagged frames are always implicitly tagged with the port default vlan (VLANID). Note that contrary to the retagging feature as provided by the Retagging Table (see Section 5.2.6), the frame is not cloned. Only the VLANID is substituted.
33	DYN_LEARN	This flag enables address learning at the respective port when set. Note that learning is independent of whether input traffic is enabled.
32	EGRESS	This flag enables output on the respective port when set. If this flag is deasserted, frames will not be dispatched to the egress port and normal L2 forwarding to this port stops. Management traffic (including META frames) sent by the host controller over the L2 Lookup Table TAKETS mechanism, or through the L2 Management Table mechanism, is sent regardless of the state of this flag. For Time-Triggered Ethernet enabled devices (SJA1105Q and SJA1105S), critical frames and locally generated PCF frames will be transmitted, regardless of this setting.
31	INGRESS	This flag enables input on the respective port when set. Management traffic flows to the port regardless of the state of the INGRESS flag.
30	MIRRCIE	Controls Ingress/Egress conflict behavior. A mirroring conflict exists if a single frame is simultaneously subject to ingress and egress mirroring. In this case the switch decides if the mirror frame sent to the MIRR_PORT is handled as an ingress or as an egress mirror frame based on this flag. If the MIRRCIE flag associated with the port on which the frame was received is set, the switch will handle the mirror frame sent to the MIRR_PORT as an ingress mirror frame and if this flag is cleared, the mirror frame is handled as an egress mirror frame. If a frame is handled as a mirror ingress frame, it is sent on the mirror port with an outer tag of INGMIRRVID (see description of INGMIRRVID field from MAC Configuration Table). If a frame is handled as a mirror egress frame, it is sent on the mirror port with an outer tag according to EGRMIRRVID (see description of the EGRMIRRVID field from the General Parameters configuration block).

Bit	Symbol	Description
29	MIRRCETAG	This flag resolves a conflict in settings for egress tagging behavior when a mirrored frame subject to being tagged is sent to untagged ports. An egress mirroring conflict exists if a single frame is subject to egress mirroring at tagged and untagged ports at the same time. The switch decides if the mirror frame is sent to the MIRR_PORT tagged or untagged based on this flag. The switch sends the mirror frame to the MIRR_PORT tagged when the MIRRCETAG flag is set, and untagged when it is cleared.
28:17	INGMIRRVID	VLAN tag added to ingress mirrored frames. And ingress mirrored frame is tagged with and additional outer tag if this field is non-zero. It is not applicable when mirroring double tagged frames. If a frame is subject to ingress mirroring, the PCP and DEI values of the mirrored frame will correspond to INGMIRRPCP and INGMIRRDEI, respectively.
16:14	INGMIRRPCP	see INGMIRRVID
13	INGMIRRDEI	see INGMIRRVID
12:0	Not used	

5.2.6 Retagging table

Table 23 shows the layout of an entry in the Retagging table. This table is used to create copies of tagged Ethernet frames that will receive new VLAN IDs and will then be forwarded as if they were received on the original source port. The table has 32 entries and is optional. One of the applications of this table is to replicate and retag frames for debugging and monitoring purposes. Consider a deeply embedded network composed of multiple switch devices and different VLAN configurations. To access the traffic from a debugging port, all frames tagged for debug monitoring must be forwarded to this port. In order to do this, the device is re-reconfigured during runtime to create a copy of every frame selected for monitoring/mirroring and route it to a VLAN that is configured to carry monitoring/debugging traffic. The forwarding rules for this VLAN then make sure that the retagged traffic finds its way through the network to be accessed by the monitoring device.

Table 23. Retagging Table (block 12h)

Bit	Symbol	Description
63:59	EGR_PORT	If a frame with VLAN ID VLAN_ING is forwarded to any port whose flag is set in this field, a copy with VLAN ID VLAN_EGR is generated. Only one copy is generated, even if the frame is forwarded to multiple ports having their respective flags set in this field or if the frame is received on any of the ports having their respective flags set in ING_PORT. The LSB of this field is assigned to port 0.
58:54	ING_PORT	If a frame with VLAN ID VLAN_ING is received on any port whose flag is set in this field, a copy with VLAN ID VLAN_EGR is generated. Only one copy is generated, even if the frame is forwarded to any of the ports having their respective flags set in EGR_PORT as well. The LSB of this field is assigned to port 0.
53:42	VLAN_ING	The VLAN ID of the ingress frame.
41:30	VLAN_EGR	This VLAN ID replaces the VLAN ID of the original frame at egress. The priority code point of the VLAN tag is not changed.
29	DO_NOT_LEARN	If this flag is asserted, address learning is disabled for all frames carrying a VLAN ID that matches VLAN_EGR of the entry. This applies to frames being received on any of the Ethernet ports. Source addresses of frames generated by the retagging function are never learned anyway.

Bit	Symbol	Description
28	USE_DEST_PORTS	If this flag is asserted, DESTPORTS of the entry is used to route all frames carrying a VLAN ID that matches VLAN_EGR of the entry. This applies to both frames generated by the retagging function and to frames being received on any of the Ethernet ports. The configured route will bypass all other forwarding decisions. A frame may still be dropped at the egress port (if the respective transmit priority queue is filled to capacity) or by rate limitation and memory partition constraints. If several entries produce a match, the DESTPORTS field of the one with the smallest index is used.
27:23	DESTPORTS	This field provides a dedicated route for all frames carrying a VLAN ID that matches VLAN_EGR of the entry. This applies to both frames generated by the retagging function and to frames being received on any of the Ethernet ports. The configured route will bypass all other forwarding decisions. A frame may still be dropped at the egress port (if the respective transmit priority queue is filled to capacity) or by rate limitation and memory partition constraints.
22:0	Not used	

5.2.7 L2 Lookup Parameters table

Table 24 shows the layout of the L2 Lookup Parameters block. Parameters that control the address learning process are loaded into this block. It specifies how long dynamically learned entries are valid. It also defines the maximum number of entries in the address lookup table that are available for the dynamic address learning process (in order to reserve space for entries used by higher layer protocols like MMRP, SRP or IGMP). It specifies if the MAC addresses learned are shared among all VLANs or are distinct for every VLAN.

Table 24. L2 Lookup Parameters table (block 0Dh)

Bit	Symbol	Description
127:123	DRPBC	A received broadcast L2 frame, received on a port having this flag set, is dropped. This condition overrules the host trapping mechanism and does not apply to TT traffic.
122:118	DRPMC	A received multicast L2 frame, received on a port having this flag set, is dropped. This condition overrules the host trapping mechanism and does not apply to TT traffic.
117:113	DRPUNI	A received unicast L2 frame, received on a port having this flag set, is dropped. This condition overrules the host trapping mechanism and does not apply to TT traffic.
112:102	MAXADDRP[4]	Specifys the maximum number of MAC address dynamically learned from the respective port. It is used to limit the number of learned MAC addresses per port.
..	..	
68:58	MAXADDRP[0]	
57:43	MAXAGE	This parameter defines the timeout for dynamically learned routes in multiples of 10 ms. An entry will age out (and can be reclaimed) some time in the interval [MAXAGE x 10ms, (MAXAGE+1) x 10 ms] after it has been learned. The timer will be started every time a new entry is learned. The timer will be re-started when an existing entry is confirmed by means of reception of another frame with identical source MAC address. Static entries (LOCKEDS = 1) of the L2 Address Lookup table will not be affected by the aging mechanism. If the parameter is set to zero, aging will be de-activated and learned addresses will not be forgotten until reset or when changed by the host.

Bit	Symbol	Description
42:33	START_DYNSPC	Specify the border in the L2 Lookup Table memory between static and dynamic learned MAC addresses. Its purpose is to reserve some space in the L2 Address Lookup table for static MAC addresses. A static MAC address is an address written by the host in the L2 Lookup Table with LOCKEDS flag set. A dynamic address is an address learned dynamically by the switch's learning process. If static entries are pre-programmed (LOCKEDS = 1), the user must partition the available L2 space. START_DYNSPC must point to the first available index which can be claimed by dynamic learning.
32:28	DRPNOLEARN	If a frame is received on a port having this flag asserted and its source MAC address cannot be learned (e.g. because the maximum number of allowed addresses is exceeded), the frame is dropped. Frames that are not learnt because DYN_LEARN (MAC Configuration Table) is deasserted are not dropped if this flag is set.
27	SHARED_LEARN	A value of 0 specifies that the VLAN ID is included in L2 learning. If this field is asserted, a learned L2 entry will have the VLAN bits set to 'don't care'.
26	NO_ENF_HOSTPRT	This parameter, when asserted, turns off port enforcement for management traffic received at the host port. All traffic producing a match with the MAC_FLT[i] and MAC_FLTRES[i] parameters of the General Parameters configuration table is considered management traffic. The HOST_PORT parameter in the General Parameters configuration block identifies the host port. This flag is ignored if HOST_PORT does not contain a valid port number. Port enforcement is enabled for a MAC address by setting the ENFPORT flag of the respective entry in the L2 Address Lookup table. The NO_ENF_HOSTPRT flag overrules the ENFPORT flag for management traffic received at the host port.
25	NO_MGMT_LEARN	This parameter, when asserted, will turn off address learning for management traffic received at the host port. Address learning includes learning a new address as well as updating a previously learned address (i.e. resetting its age and set receive port value). All traffic producing a match with the MAC_FLT[i] and MAC_FLTRES[i] parameters of the General Parameters configuration block is considered management traffic. The host port is identified by the HOST_PORT parameter of the General Parameters configuration block. If HOST_PORT does not contain a valid port number, this flag will not be used.
24	USE_STATIC	If this flag is set, the dynamic learning process is allowed to use free static entries from the static space (see START_DYNSPC field description).
23	OWR_DYN	If the dynamic address learning space from the L2 Lookup Table is full (i.e. all entries contain dynamic information), and a new dynamic entry needs to be added by the address learning mechanism, this flag allows a dynamic learned entry to be overwritten. If this flag is de-asserted, new addresses eligible for Address Learning are no longer learned. If this flag is set and the available L2 space is depleted, the switch uses a round-robin policy to find the eviction candidate. The switch will start overwriting old dynamic entries (but never static entries) incrementally starting from START_DYNSPC.
22	LEARN_ONCE	If this flag is set, once a MAC address is learnt, it will not be possible to learn the same address on a different port until the entry in the L2 Lookup Table ages out. When this situation occurs, the respective frame is dropped. **Note**: If set, all L2 entries will be implicitly port enforced, regardless of the ENFPORT settings.
21:0	Not used	

5.2.8 L2 Forwarding Parameters

Table 25 shows the layout of the L2 Forwarding Parameters block. This block defines the memory space available for traffic mapped to any of the L2 available memory partitions, as configured in the L2 Policing table. This block also allows to limit the dynamic reconfiguration of priority queue mapping in order to ensure that low-priority traffic is not assigned to high-priority queues.

Table 25. L2 Forwarding Parameters table (block 0Eh)

Bit	Symbol	Description
95:93	MAX_DYNP	This field defines the maximum VLAN_PMAP[7:0] values (L2 Forwarding table) that will be accepted for dynamic updates. Note that this parameter only applies to dynamic updates. Larger values are accepted during configuration load entries. This parameter also only affects the mapping of egress priority values to physical priority queues (the latter 8 entries in the L2 Forwarding table); the mapping of ingress priority values to egress priority values is not restricted.
92:83	PART_SPC[7]	These fields define the maximum amount of frame memory that an L2 memory partition can use. A memory partition is used by a set of ports that store their frames in shared memory. When a frame is received and passes all policing checks, it draws from the memory partition as identified by the PARTITION field of the respective entry in the L2 Policing table. Once the frame has completed transmission to all ports, the memory needed to store the frame is credited to the respective memory partition. The parameter specifies the number of 128-byte memory blocks contained in the memory partition. A frame requires as many blocks as needed to ensure that the sum of the bytes in the block is greater than or equal to the number of bytes contained in the frame, including Ethernet header and checksum but excluding any VLAN tag. A block cannot be shared between frames. **Note:** The total number of assigned blocks (8 partitions for L2 traffic PLUS 8 partitions for VL traffic) must never exceed 910 if retagging is used or 929 if retagging is not used. Also see VL Forwarding Parameters.
…	…	
22:13	PART_SPC[0]	
12:0	Not used	

5.2.9 AVB Parameters

Table 26 shows the layout of the AVB Parameters block. The AVB Parameters table specifies the source and destination MAC addresses of the meta frame created by the switch for frames trapped by filtering rules for which an ingress timestamp is captured. The source port information and the SWITCHID can be used to distinguish the meta frames from different switches when multiple switches are used in a cascaded architecture. If INCL_SRCPT is set, the switch embeds the SWITCHID and the source port in bytes one and two of the destination MAC address of the original frame.
The payload format of the meta frame is depicted in Fig 16. The meta frame is sent immediately after the trapped frame that triggered the action.

Also, the timestamp synchronization across multiple cascaded switches is controlled. For this, all cascaded switches must have their PTP_CLK inout pins connected to each other.

Table 26. AVB Parameters table (block 10h)

Bit	Symbol	Description
127	L2CBS	If de-asserted, the CBS blocks use L1 (preamble, SFD, IFG, length) or L2 (length) data rate when shaping the output traffic. **Note:** It is recommended to have this flag deasserted for 802.1Qav compliance.

Bit	Symbol	Description
126	CAS_MASTER	If the device is used in a cascaded setup, the internal free running timestamp counters can be synchronized using the PTP_CLK pin. If CAS_MASTER is asserted, the device will operate as a cascade sync master and configures PTP_CLK as an output, otherwise the device is a cascade slave with PTP_CLK configured as an input. On a write to the CASSYNC flag, the cascaded master will toggle PTP_CLK and take a timestamp of its free running (or rate corrected) counter. The timestamp is stored in PTPSYNCTS. The cascaded slave senses a state transition on the PTP_CLK input and also take a timestamp which is stored in the PTPSYNCTS register. If CORRCLK4TS is false, the free running clock is used; if CORRCLK4TS is true, the rate corrected clock is used for generating the timestamp.
125:78	DESTMETA	This field defines the destination MAC address used for meta frames
77:30	SRCMETA	This field defines the source MAC address used for meta frames
29:0	Not used	

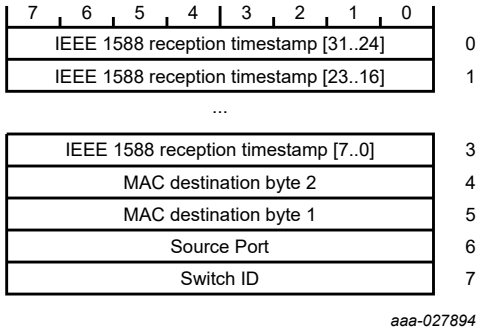


Figure 13. Structure of the meta-data follow-up frame

5.2.10 Credit-Based Shaping Table

Table 27 shows the layout of the Credit-Based Shaping (CBS) Table. The device has 16 credit-based shaping blocks which can be assigned to any queue. This table can have up to 16 entries. Not all of the 16 table entries must be provided during configuration. Unused entries will deactivate the corresponding CBS shaper.

Table 27. Credit-based shaping table (block 13h)

Bit	Symbol	Description
159:157	CBS_PORT	Specifies the port to which the credit-based shaping block is applied to.
156:154	CBS_PRIO	Specifies the priority queue to which the credit-based shaping block is applied.
153:122	CREDIT_LO	Specifies the value at which the credit counter negatively saturates upon transmission of a frame. This can be used to reduce the gap between multiple bursted high priority frames from the same queue, if shaping is enabled on this queue. The parameter defines the uppermost 32 bits of the credit counter, the lower 16 bits are set to zero. Note: IEEE 802.3Qav does not specify this as an input parameter. For nominal IEEE 802.3Qav operation, set this value to 3FFFFFFFh.

Bit	Symbol	Description
121:90	CREDIT_HI	Specifies the value at which the credit counter positively saturates during idle periods. This can be used to limit the burst length of frames from a queue to which a shaper is applied. The parameter defines the uppermost 32 bits of the credit counter, the lower 16 bits are set to zero. Note: IEEE 802.3Qav does not specify this as an input parameter. For nominal IEEE 802.3Qav operation, set this value to 3FFFFFFFh.
89:58	SEND_SLOPE	Specifies the rate (in unit of byte/s) at which the credit counter is decreased. The credit counter value is decreased whenever the currently transmitted frame is sourced from the priority queue to which the shaper is applied to. For CBS in L1 operation (L2CBS deasserted): SEND_SLOPE = (PORT_SPEED[bit/s] - DATARATE[bit/s]) / 8
57:26	IDLE_SLOPE	Specifies the rate (in unit of byte/s) at which the credit counter is increased. The counter value is increased whenever it is negative or the priority queue to which the shaper is applied holds a frame ready for transmission but the media is occupied by a frame sourced from a different queue. For CBS in L1 operation (L2CBS deasserted): IDLE_SLOPE = DATARATE[bit/s] / 8
25:0	Not used	

5.2.11 General Parameters

Table 28 shows the layout of the General Parameters table. This table contains general parameters used to configure basic switch properties.

Table 28. General Parameters table (block 11h)

Bit	Symbol	Description
351	VLLUPFORMAT	*Note: SJA1105Q and SJA1105S only* This field specifies the addressing scheme to be used to identify time-triggered and rate-constrained traffic. If this parameter is set to 1, time-triggered and rate-constrained traffic is identified by (1) the upper 32 bits of the frame destination MAC address filtered by VIMASK is equal to VIMARKER and (2) the lower 16 bits configured together with the source port in the VL lookup table. If the parameter is set to 0, the frame is considered as rate-constrained or time-triggered if the combination of destination MAC address, VLAN ID, VLAN priority and source port is configured in the VL lookup table.
350	MIRR_PTACU	If this flag is set, the host can dynamically change the value of MIRR_PORT. If the flag is not set, changes of MIRR_PORT are prohibited.
349:347	SWITCHID	This field contains the configured switch ID used to identify the source of trapped frames forwarded to the host CPU in case the switch is composed from multiple cascaded devices.
346:344	HOSTPRIO	This field contains the priority value identifying the priority queue on HOST_PORT when a trapped frame is forwarded to the port connected to the host processor.
343:296	MAC_FLTRES[1]	This field contains a bit mask identifying a bridge level or MAC level management frame to be forwarded to HOST_PORT. A received L2 frame produces a match if DEST_MAC and MAC_FLT[i] = MAC_FLTRES[i] holds. For example, to forward all groupcast traffic for the reserved OUI 01-80-C2-... to the host port, this field must be set to 01-80-C2-00-00-00.
295:248	MAC_FLTRES[0]	

Bit	Symbol	Description
247:200	MAC_FLT[1]	This field contains a bit mask identifying a bridge level or MAC level management frame to be forwarded to HOST_PORT. A received L2 frame produces a match if DEST_MAC and MAC_FLT[i] = MAC_FLTRES[i] holds. For example, to forward all groupcast traffic for the reserved OUI 01-80-C2-... to the host port, this field must be set to FF-FF-FF-00-00-00. If the INCL_SRCPT[i] flag is set, MAC_FLT[i] must have set bytes 1 and 2 to zero (i.e.must be set to xx-xx-xx-00-00-xx, where an 'x' denotes an arbitrary user-defined value).
199:152	MAC_FLT[0]	
151	INCL_SRCPT[1]	If this field is set: for any frame where the destination MAC address matches the filter MAC_FLT[i] / MAC_FLTRES[i], the switch embeds the source port ID in byte 2 and the SWITCHID in byte 1 of the MAC address, where byte 0 is the least significant byte. If the flag is set, bytes 1 and 2 of MAC_FLT[i] must be set to zero (i.e. must be set to xx-xx-xx-00-00-xx, where an 'x' denotes an arbitrary user-defined value).
150	INCL_SRCPT[0]	
149	SEND_META[1]	If this field is set, the switch generates a meta frame containing the timestamp, source port ID and configured SWITCHID for any frame where the destination MAC address matches MAC_FLT[i] / MAC_FLTRES[i]. The meta frame gets sent immediately after the filtered frame that produced the match.
148	SEND_META[0]	
147:145	CASC_PORT	If this field contains a valid port number, MGMT traffic (see MAC_FLT) received on this port is automatically forwarded to HOST_PORT without including the source port and SWITCHID information in the destination MAC address. Cascading is disabled by setting an invalid port number for CASC_PORT (i.e. a value greater than 4).
144:142	HOST_PORT	Management traffic (see MAC_FLT) is forwarded to this port. Note: if HOST_PORT is not configured (HOST_PORT greater than 4), MGMT traffic is dropped.
141:139	MIRR_PORT	Traffic to be mirrored flows to this port if this field contains a valid port number. Traffic to be mirrored is identified by the EGR_MIRR and ING_MIRR flags of the entry in the MAC Configuration table for this port and by the VEGR_MIRR and VING_MIRR vectors of a VLANs entry in the VLAN Lookup table. Note that mirroring will be faithful only if the switch operates lossless. The decision to mirror a frame is taken when the frame is dispatched to the destination port. The frame will still be mirrored if the destination port does not accept it, e.g. because the respective priority queue is full. On the other hand, the mirror port may refuse to mirror frames, e.g. because the respective priority queues are full. A frame is dispatched to a port at most once; so if the port configured as mirror port by this field is also the intended forwarding destination for the frame, it is only dispatched once. Also, if several destination ports need to mirror a frame, the frame will still be dispatched only once to the mirror port. In the case of time-triggered frames, the frame will be dispatched to the mirror port with its regular trigger in case the mirror port is on the route of the frame anyway (in case of loss of sync the frame may not get mirrored). If the mirror port is not on the route of a time-triggered frame, the frame will be dispatched to the mirror port with the first trigger that has the SETVALID flag asserted if ingress mirroring is enabled. If the mirror port is not on the route of a time-triggered frame and ingress mirroring is not selected for the frame, the frame will be dispatched to the mirror port with the first trigger that dispatches the frame to any port for which egress mirroring is selected.
138:107	VIMARKER	*SJA1105Q and SJA1105S only* Provides the upper 32 bits of the Ethernet destination MAC address of frames considered to be critical traffic. More significant bytes of the MAC address are placed at lower bit positions in VIMARKER). The value of this parameter will be used for PCFs generated by the switch if it is configured as a compression master (without previously applying VIMASK).

Bit	Symbol	Description
106:75	VIMASK	*SJA1105Q and SJA1105S only* Provides a bit-mask used for telling critical traffic from non-critical traffic. For the check, a bit-wise AND operation is performed both on VIMARKER and on the upper 32 bits of the Ethernet destination MAC address of the frame in question before the comparison. The parameter has the same byte order as VIMARKER so lower byte positions of VIMASK are used to mask the more significant bytes of the MAC address. When applying VIMASK to VIMARKER, bits at identical positions are logically ANDed.
74:59	TPID	This field contains the Ethernet Type Identifier used to identify outer tagged (S-tag) VLAN traffic. Typically set to 88A8h
58	IGNORE2STF	When set, this flag specifies that the ‘twoStepFlag’ of the ‘flagField’ of an IEEE 1588v event message shall be ignored. In this case, the ‘correctionField’ of an IEEE 1588v2 event message will always get updated with the residence time, even if the ‘twoStepFlag’ is asserted.
57:42	TPID2	This field contains the Ethernet Type Identifier used to identify inner tagged (C-tag) VLAN traffic. Typically set to 8100h
41	QUEUE_TS	If a trapped frame is forwarded towards the HOST_PORT and this flag is set, a timestamp is taken when the frame is added to the HOST_PORT output queue (HOSTPRIO priority). This timestamp is inserted in the follow up meta frame immediately after the ingress timestamp field (so the follow meta frame size is increased with 4 bytes when this flag is set). Note that this timestamp is *not* the egress timestamp and must never be used for PTP residence time calculations. This timestamp is intended for debugging only.
40:29	EGRMIRRVID	VLAN tag added to egress mirrored frames. If this field is non-zero, then an egress mirrored frame will be tagged with an additional outer tag. Not applicable when mirroring double-tagged frames. If the additional tag is used, PCP and DEI values of the mirrored frame will correspond to EGRMIRRPCP and EGRMIRRDEI, respectively.
28:26	EGRMIRRPCP	See EGRMIRRVID
25	EGRMIRRDEI	See EGRMIRRVID
24:22	REPLAY_PORT	*SJA1105Q and SJA1105S only* When a critical frame is received on the REPLAY_PORT port and REPLAY_PORT corresponds to a valid port (< 5), the IVL Lookup Process will ignore the received port in the VL Lookup Table. It is the responsibility of the host to configure the VL Lookup Table with at least one entry per VL ID (the VL lookup from REPLAY_PORT will not work if the host configures more than one entry in the VL lookup table for the same VL ID but for different receive ports).
21:0	Not used	

5.2.12 xMII Mode Parameters

Table 29 shows the layout of the xMII Mode Parameters block. This block is used to set the xMII mode of operation. When PHY mode is selected, the port on this switch interface behaves as a PHY and the partner should behave as a MAC. When MAC mode is selected, the switch interface port behaves as a MAC and the partner should be a PHY. In order to set up the clocking scheme, the CGU must also be configured.

Table 29. xMII Mode Parameters Table (block 4Eh)

Bit	Symbol	Description	
31	PHY_MAC[4]	This parameter is used to select the interface mode for port 4.	
		1	PHY mode

Bit	Symbol	Description	
		0	MAC mode Note: For SGMII, MAC must be selected
30:29	xMII_MODE[4]	This parameter is used to set the xMII mode for port 4.	
		00	MII
		01	RMII
		10	RGMII
		11	SGMII (SJA1105R/S only) port deactivated (pins tristate) for SJA1105P/Q Note: see SGMII registers (DIGITAL_CONTROL_1, TX_DISABLE) on how to disable SGMII.
…		port 1 to port 3: see port 0	
19	PHY_MAC[0]	This parameter is used to select the interface mode for port 0.	
		1	PHY mode
		0	MAC mode
18:17	xMII_MODE[0]	This parameter is used to set the xMII mode for port 0.	
		00	MII
		01	RMII
		10	RGMII
		11	port deactivated (pins tristate)
16:0	not used		

5.3 RGU Table

Table 30 configures the RGU subsystem.

Table 30. RGU table (block 81h)

Bit	Symbol	Description
31:0	UNIT_DISABLE	see RGU's UNIT_DISABLE register

5.4 CGU Table

Table 31 configures the clock generation subsystem. When this table is provided, the data is written to registers in the order of the table, from lowest to highest address. A detailed description of these registers can be found in Section 6.3:

Table 31. CGU table (block 80h)

Bit	Symbol	Description
1407:1376	RFRQ	see RFRQ register
1375:1344	PLL_0_C	see PLL_x_C register
1343:1312	PLL_1_C	
1311:1280	IDIV_0_C	see IDIV_x_C register
1279:1248	IDIV_1_C	

Bit	Symbol	Description
1247:1216	IDIV_2_C	
1215:1184	IDIV_3_C	
1183:1152	IDIV_4_C	
1151:1120	BASE_SAFE_CLK_C	see BASE_SAFE_CLK_C register
1119:1088	BASE_SWITCH_CLK_C	see BASE_SWITCH_CLK_C register
1087:1056	BASE_PERPH_CLK_C	see BASE_PERPH_CLK_C register
1055:1024	**MII0**_MII_TX_CLK_C	see MII0_MII_TX_CLK_C register (Port 0)
1023:992	**MII0**_MII_RX_CLK_C	see MII0_MII_RX_CLK_C register (Port 0)
991:960	**MII0**_RMII_REF_CLK_C	see MII0_RMII_REF_CLK_C register (Port 0)
959:928	**MII0**_RGMII_TX_CLK_C	see MII0_RGMII_TX_CLK_C register (Port 0)
927:896	**MII0**_EXT_TX_CLK_C	see MII0_EXT_TX_CLK_C register (Port 0)
895:864	**MII0**_EXT_RX_CLK_C	see MII0_EXT_RX_CLK_C register (Port 0)
…	…	…
287:256	**MII4**_MII_TX_CLK_C	see MII4_MII_TX_CLK_C register (Port 4)
255:224	**MII4**_MII_RX_CLK_C	see MII4_MII_RX_CLK_C register (Port 4)
223:192	**MII4**_RMII_REF_CLK_C	see MII4_RMII_REF_CLK_C register (Port 4)
191:160	**MII4**_RGMII_TX_CLK_C	see MII4_RGMII_TX_CLK_C register (Port 4)
159:128	**MII4**_EXT_TX_CLK _C	see MII4_EXT_TX_CLK_C register (Port 4)
127:96	**MII4**_EXT_RX_CLK _C	see MII4_EXT_RX_CLK_C register (Port 4)
95:0	reserved	-

5.5 ACU Table

Table 32 configures the auxiliary configuration unit subsystem. When this table is provided, the data is written to the corresponding registers. A detailed description of these registers can be found in Section 6.4:

Table 32. ACU table (block 82h)

Bit	Symbol	Description
671:640	CFG_PAD_MII0_TX	see CFG_PAD_MII0_TX register
639:608	CFG_PAD_MII0_RX	see CFG_PAD_MII0_RX register
607:576	CFG_PAD_MII1_TX	see CFG_PAD_MII1_TX register
575:544	CFG_PAD_MII1_RX	see CFG_PAD_MII1_RX register
543:512	CFG_PAD_MII2_TX	see CFG_PAD_MII2_TX register
511:480	CFG_PAD_MII2_RX	see CFG_PAD_MII2_RX register
479:448	CFG_PAD_MII3_TX	see CFG_PAD_MII3_TX register
447:416	CFG_PAD_MII3_RX	see CFG_PAD_MII3_RX register
415:384	CFG_PAD_MII4_TX	see CFG_PAD_MII4_TX register
383:352	CFG_PAD_MII4_RX	see CFG_PAD_MII4_RX register

Bit	Symbol	Description
351:320	CFG_PAD_MII0_ID	see CFG_PAD_MII0_ID register
319:288	CFG_PAD_MII1_ID	see CFG_PAD_MII1_ID register
287:256	CFG_PAD_MII2_ID	see CFG_PAD_MII2_ID register
255:224	CFG_PAD_MII3_ID	see CFG_PAD_MII3_ID register
223:192	CFG_PAD_MII4_ID	see CFG_PAD_MII4_ID register
191:160	CFG_PAD_MISC	see CFG_PAD_MISC
159:128	CFG_PAD_SPI	see CFG_PAD_SPI
127:96	CFG_PAD_JTAG	see CFG_PAD_JTAG
95:64	TS_CONFIG	see TS_CONFIG
63:32	reserved	initialize with 00000000h
31:0	UNIT_DISABLE	see ACU's UNIT_DISABLE

5.6 SGMII Table

SJA1105R and SJA1105S only

Table 33 configures the SGMII interface. When this table is loaded, the data is written to the corresponding registers. The registers in the SGMII interface are 16 bits wide, but the corresponding bit space in the config stream is 32 bits wide – therefore the upper 16 bits should be set to 0000b. Some parts of the config table are reserved. Use the initialization value provided. A detailed description of the other registers can be found in Section 6.5:

Table 33. SGMII table (block C8h)

Bit	Symbol	Description
1151:1120	DIGITAL_ERROR_CNT	see DIGITAL_ERROR_CNT register
1119:1088	DIGITAL_CONTROL_2	see DIGITAL_CONTROL_2 register
1087:1056	reserved	initialize with 0000.0000h
1055:1024	reserved	initialize with 0000.0000h
1023:992	reserved	initialize with 0000.0000h
991:960	reserved	initialize with 0000.0100h
959:928	reserved	initialize with 0000.023Fh
927:896	reserved	initialize with 0000.000Ah
895:864	reserved	initialize with 0000.1C22h
863:832	reserved	initialize with 0000.0001h
831:800	reserved	initialize with 0000.0003h
799:768	reserved	initialize with 0000.0000h
767:736	reserved	initialize with 0000.0001h
735:704	reserved	initialize with 0000.0005h
703:672	reserved	initialize with 0000.0101h
671:640	reserved	initialize with 0000.0000h
639:608	reserved	initialize with 0000.0001h

Bit	Symbol	Description
607:576	reserved	initialize with 0000.0000h
575:544	reserved	initialize with 0000.000Ah
543:512	reserved	initialize with 0000.0000h
511:480	reserved	initialize with 0000.0000h
479:448	reserved	initialize with 0000.0000h
447:416	reserved	initialize with 0000.0000h
415:384	reserved	initialize with 0000.899Ch
383:352	DEBUG_CONTROL	see DEBUG_CONTROL register
351:320	TEST_CONTROL	see TEST_CONTROL register
319:288	reserved	initialize with 0000.000Ah
287:256	AUTONEG_CONTROL	see AUTONEG_CONTROL register
255:224	DIGITAL_CONTROL_1	see DIGITAL_CONTROL_1 register
223:192	AUTONEG_ADV	see AUTONEG_ADV register
191:160	BASIC_CONTROL	see BASIC_CONTROL register
159:128	reserved	initialize with 0000.0004h
127:96	reserved	initialize with 0000.0000h
95:64	reserved	initialize with 0000.0000h
63:32	reserved	initialize with 0000.0000h
31:0	reserved	initialize with 0000.0000h

6 Dynamic Control Interface

This section describes the runtime interface to the device. The host communicates with the device via the SPI interface. All register addresses are relative to base address 00000000h unless specified otherwise.

Register acess is handled in the following way: writing to an R-only register or R-only bit has no effect and reading from a W-only register or R-only bit returns 0.

6.1 Ethernet Switch Core (ETH)

The ETH runtime interface consists of a status area with R-only registers and a control area.

6.1.1 Status Area

The status area is divided into five sections: general status information, clock synchronization, memory partitioning, Ethernet port status information and virtual link status information. Reserved bits return 0 when read.

6.1.1.1 General Status Information

Configuration data loaded via the configuration interface must start with the device ID.

Table 34. Device ID register (address 00h)

Bit	Symbol	Access	Value	Description
31:0	DEVICEID	R	See Table 1	Ethernet switch core device identification code[1]

[1] Note that this identifies the Ethernet switch core. See also the JTAG device id given in Table 1.

6.1.1.2 Configuration Status Information

Table 35. Initial device configuration flag register (address 01h)

Bit	Symbol	Access	Value	Description
31	CONFIGS	R		device configuration status; this flag should be checked after loading the static configuration; if set, the configuration is locked and cannot be overridden without resetting the device.
			0	configuration is invalid
			1	configuration is valid
30	CRCCHKL	R		local CRC check for the most recently loaded static configuration block; if used, this flag should be checked after each block is loaded. *cleared on reset/power-on and when the reconfiguration is restarted (e.g. if it was not successful).*
			0	check OK
			1	check failed
29	IDS	R		device identifier flag; if found set, device ID in the loaded configuration did not match the physical device. *cleared on reset/power-on and when the reconfiguration is restarted (e.g. if it was not successful).*
			0	matching device identifier found
			1	matching device identifier not found
28	CRCCHKG	R		global CRC check. If found set, the global CRC of the static configuration was incorrect. *cleared on reset/power-on and when the reconfiguration is restarted (e.g. if it was not successful).*
			0	check OK
			1	check failed
27:4	reserved	R	all 0s	
3:0	NSLOT	R	xxx	free running 0 to 9 counter. Wraps at value 9.

6.1.1.3 VL Route and Partition Status Information

SJA1105Q and SJA1105S only

VLROUTES is set when a critical frame is dropped because the configured route does not contain a port index. This information could be used, for example, to drop PCF traffic processed by a switch configured as a compression master for which the user wants to avoid receiving VLNOTFOUND errors on the respective input ports.

VLPARTS is set when a critical frame is dropped because the associated memory partition did not have enough space to store it. When this flag is set, the corresponding flag in the memory partition section is also set.

SJA1105Q and SJA1105S only

Table 36. VL route/partition status register (address 02h)

Cleared on reset/power-on and on read

Bit	Symbol	Access	Value	Description
31:16	VLIND	R	xxxxh	index in VL Forwarding Table that caused the VLROUTES or VLPARTS flag to be set
15:8	VLPARIND	R	xxxxh	ndex of partition that caused the VLPARTS flag to be set
7:2	reserved	R	All 0s	
1	VLROUTES	R		configured route status
			0	route ok; no dropped frames
			1	critical traffic frame dropped because route configuration does not contain any valid port
0	VLPARTS	R		partition overflow error status:
			0	memory partition ok; no dropped frames
			1	critical traffic frame dropped due to memory partition overflow

6.1.1.4 General Status Registers

L2BUSYFDS is set if a frame received at PORTENF was dropped because it was received while the L2 Address Lookup table was being initialized. If the host respects the rule not to load the L2 Address Lookup table before the L2BUSYS flag is cleared, this condition will only occur in a setup that does not load the L2 Address Lookup table. To avoid setting this flag, wait for the L2BUSYS flag to be cleared before writing the last configuration word.

L2BUSYS = 1 indicates that the L2 Address Lookup table is being initialized. This flag will be set after a configuration reset condition: the device has not yet received a valid configuration but has received the first word of the configuration stream. The flag is cleared once initialization is complete and will remain cleared until a new power cycle or reset occurs. The L2 Address Lookup table cannot be loaded before this flag has been cleared.

Table 37. General Status Register 1 (address 03h)

Cleared on reset/power-on and on a read access by the host.

Bit	Symbol	Access	Value	Description
31:16	MACADDRL	R	xxxxh	lower (15 to 0) 16 bits of the source MAC address that triggered ENFFDS
15:8	PORTENF	R	xxh	number to the port that triggered ENFFDS
7:5	reserved	R	all 0s	
4	FWDS	R		forwarding frame drop status:
			0	no dropped frames
			1	frame dropped because input port was not set to ‘forwarding’ when frame received
3	MACFDS	R		standard group MAC address frame drop status:
			0	no dropped frames

Bit	Symbol	Access	Value	Description
			1	frame dropped because it contained a filtered MAC address when the switch is not configured to forward such traffic
2	ENFFDS	R		enforced frame drop status:
			0	no dropped frames
			1	frame received at PORTENF dropped because it carried a source MAC address declared to be enforced on a different port in the L2 Address Lookup table
1	L2BUSYFDS	R		L2 Address Lookup table busy/frame drop status:
			0	not busy; no dropped frames
			1	frame received at PORTENF dropped because it was received while L2 Address Lookup table was being initialized
0	L2BUSYS	R		L2 Address Lookup table status:
			0	L2 Address Lookup table initialization complete
			1	L2 Address Lookup table is being initialized

Table 38. General Status Register 2 (address 04h)

Bit	Symbol	Access	Value	Description
31:0	MACADDRU	R	xxxxh	upper (47 to 16) 32 bits of the source MAC address that triggered ENFFDS

Table 39. General Status Register 3 (address 05h)

Bit	Symbol	Access	Value	Description
31:16	MACADDHCL	R	xxxxh	lower (15 to 0) 16 bits of the source MAC address that triggered HASHCONFS
15:4	VLANIDHC	R	xxxh	VLAN ID that triggered HASHCONFS
3:1	reserved	R	00	
0	CONFLICT	R		learning conflict status
			0	no conflict encountered
			1	unresolved learning in L2 Address Lookup table; means that all available TCAM slots for dynamic address learning are already occupied

Table 40. General Status Register 4 (address 06h)

Bit	Symbol	Access	Value	Description
31:16	MACADDHCU	R	xxxxh	upper (47 to 16) 32 bits of the source MAC address that triggered HASHCONFS

WPVLANID contains the VLAN ID that triggered WRONGPORTS or VNOTFOUNDS, if one of these flags is set. The VLAN ID either comes directly from a tagged frame, or it is the default VLAN ID of the port in case of an untagged frame. The default VLAN ID is defined the MAC Configuration table (see Table 22).

VLANBUSYS = 1 indicates that the VLAN Lookup table is being initialized. This flag will be set after a configuration reset condition: the device has not yet received a valid configuration but has received the first word of the configuration stream. The flag is cleared once initialization is complete and will remain cleared until a new power cycle or reset occurs. The VLAN Lookup table cannot be loaded before this flag has been cleared.

Table 41. General Status Register 5 (address 07h)

Flags cleared at power-on/reset and on a read access by the host.

Bit	Symbol	Access	Value	Description
31:16	WPVLANID	R	xxxxh	VLAN ID that triggered WRONGPORTS or VNOTFOUNDS; contains valid data when one of these flags is set.
15:8	PORT	R	xxh	input port number that triggered WRONGPORTS or VNOTFOUNDS; contains valid data when one of these flags is set.
7:5	reserved	R	000	
4	VLANBUSYS	R		VLAN Lookup table status:
			0	VLAN Lookup table initialization complete
			1	VLAN Lookup table is being initialized
3	WRONGPORTS	R		port status for VLAN frame:
			0	no frame dropped
			1	frame received at PORT has been dropped because the port is not configured for the VLAN ID in the VLAN Lookup table
2	VNOTFOUNDS	R		unconfigured VLANID drop status:
			0	no frame dropped
			1	frame with VLAN ID in WPVLANID and received at port PORT has been dropped because this VLAN ID was not configured in in the VLAN Lookup table
1:0	reserved	R	00	

Table 42. General Status Register 6 (address 08h)

SJA1105Q and SJA1105S only

Flags cleared at power-on/reset and on a read access by the host.

Bit	Symbol	Access	Value	Description
31:16	VLID	R	xxxxh	VLID that did not produce a hit in the VL Lookup table; contains valid data when VLNOTFOUND is set
15:8	PORTVL	R	xxh	index of port at which VLID (that did not produce a hit in the VL Lookup table) was received

Bit	Symbol	Access	Value	Description
7:1	reserved	R	00h	
0	VLNOTFOUND	R		port/VLAN ID status:
			0	no frame dropped
			1	PORTVL and VLID contain a tuple that did not generate a hit in the VL Lookup table

EMPTYS = 1 (see Table 43) indicates that dynamic memory management experienced an 'out of memory' condition between the most recent read access to this field and the current one. This means that the configuration of memory partition sizes does not comply with the configuration rules. The switch will not behave as expected when this error occurs.

Table 43. General Status Register 7 (address 09h)

Flags cleared at power-on/reset and on a read access by the host.

Bit	Symbol	Access	Value	Description
31	EMPTYS	R		dynamic memory status
			0	memory ok
			1	'out of memory' condition registered in dynamic memory management
30:0	HANDLES	R	Xxxxxxxxh	the number of frame handles available to dynamic memory management; the number of frames currently allocated in the device is 1024-HANDLES; will be set to 1024 after a power-on or a reset, but the receive ports will immediately start to draw buffers (one buffer per port). This data is provided for testing and debugging. Note that HANDLES are not the 128-byte buffers used to store frame data.

Table 44. General Status Register 8 (address 0Ah)

Flags cleared at power-on/reset and on a read access by the host.

Bit	Symbol	Access	Value	Description
31	reserved	R	0	
30:0	HLWMARK	R	xxxxxxxxh	low watermark of the number of frame handles since the last read; see HANDLES in Table 43

Table 45. General Status Register 9 (address 0Bh)

Flags cleared at power-on/reset and on a read access by the host.

Bit	Symbol	Access	Value	Description
31:16	reserved	R	0	
15:8	PORT	R	xxh	port number where frame dropped if FWDS or PARTS is set
7:2	reserved	R	0	
1	FWDS	R		port forwarding drop status

Bit	Symbol	Access	Value	Description
			0	no dropped frames
			1	port identified by PORT sourced a L2 frame that was dropped because the configured forwarding direction did not contain any ports
0	PARTS	R		port/VLAN ID status:
			0	no dropped frames
			1	L2 frame received at PORT dropped because the respective memory partition did not have enough space to hold the frame

Table 46. General Status Register 10 (address 0Ch)

Flags cleared at power-on/reset and on a read access by the host.

Bit	Symbol	Access	Value	Description
31:23	reserved	R		
22:0	RAMPARERRL	R	xxxxh	If one of these flags is found set, a parity error has been detected in a memory block. Each memory block is assigned a dedicated flag in this vector. If any of these flags are found set during operation, the host must reset the switch. The switch will stop forwarding frames if a memory parity error is detected. That means When a parity error occurs in the frame memory, the current frame is transmitted with TX_ER asserted. When a parity error occurs in any other memory all the frames are transmitted with TX_ER asserted, until reset is applied.

Table 47. General Status Register 11 (address 0Dh)

Flags cleared at power-on/reset and on a read access by the host.

Bit	Symbol	Access	Value	Description
31:5	reserved	R		
4:0	RAMPARERRU	R	xxxxh	See RAMPARERRL

6.1.1.5 PTP Egress Timestamping

The device has two egress timestamp registers per port. These timestamp registers are allocated to the port as follows:

n = 2 x PORT + TSREG

Here PORT is the port number (0 to 4) and TSREG is either 0 or 1 depending what timestamp register is selected in the L2 Forwarding Table (TCAM) or the Management Entry. The timestamp registers are available in all variants of the device.

The address of the PTPEGR_TSn register is *C0h+ (n x 2) + 1.*

The address of the UPDATE_n register is *C0h+ (n x 2).*

Table 48. Egress Timestamp Register 0 to 9 (address C1h, C3h, C5h, C7h, C9h, CBh, CDh, CFh, D1h, D3h)

Flags cleared at power-on/reset and on a read access by the host.

Bit	Symbol	Access	Value	Description
31:0	PTPEGR_TSn	R	xxxxxxh	PTP egress timestamp

Table 49. Timestamp Register 0 to 9 (address C0h, C2h, C4h, C6h, C8h, CAh, CCh, CEh, D0h, D2h)

Flags cleared at power-on/reset and on a read access by the host.

Bit	Symbol	Access	Value	Description
31:1	reserved	R	00h	
0	UPDATE_n	R	X	Set if the timestamp PTPEGR_TSn was captured

6.1.1.6 Time-Triggered Ethernet (SAE AS6802) Clock Synchronization

SJA1105Q and SJA1105S only

Table 50. Synchronization engine status register 0 (address 5Ah)

Bit	Symbol	Access	Value	Description
31:0	SYNCSTATE	R		state of synchronization engine
			0	INIT
			1	INTEGRATE
			2	UNSYNC
			3	WAIT_4_CYCLE_START
			4	CA_ENABLED
			5	WAIT_FOR_IN
			6	TENTATIVE_SYNC
			7	SYNC
			8	STABLE

Table 51. Synchronization engine status register 1 (address 5Bh)

Bit	Symbol	Access	Value	Description
31:0	INTEGCY	R	xxxxxxh	This field contains the local_integration_cycle state variable of the clock synchronization algorithm

Table 52. Synchronization engine status register 2 (address 5Ch)

Bit	Symbol	Access	Value	Description
31:0	ACTCORR	R	xxxxxxh	This field displays the correction value most recently applied by the clock synchronization algorithm as a 32-bit two's complement number. It displays zero if no term has ever been applied. A negative value indicates that the local clock is running too fast with respect to the cluster clock.

Table 53. Synchronization engine status register 3 (address 5Dh)

Bit	Symbol	Access	Value	Description
31:0	MAXCORR	R	xxxxxxh	This field displays the largest correction value ever applied by the clock synchronization algorithm as 32 bits two's complement. It displays zero if no term has ever been applied. A negative value indicates that the local clock is running too fast with respect to the cluster clock.

Table 54. Synchronization engine status register 4 (address 5Eh)

Bit	Symbol	Access	Value	Description
31:0	MINCORR	R	xxxxxxh	This field displays the smallest correction value ever applied by the clock synchronization algorithm as 32 bits two's complement. A negative value indicates that the local clock is running too fast with respect to the cluster clock.

Table 55. Synchronization engine status register 5 (address 5Fh)

Bit	Symbol	Access	Value	Description
31:16	reserved			
15:0	SYNCLOSS	R	xxxxxxh	This field displays the number of transitions of the clock synchronization state machine from SYNC/STABLE state to a state other than SYNC/STABLE state as a 16-bit integer value. The counter stops counting when it reaches its maximum value.

Table 56. Synchronization engine status register 6 (address 60h)

Bit	Symbol	Access	Value	Description
31:8	reserved			
7:0	LOCMEM	R	xxxxxxh	This field displays the local_membership_comp state variable of the clock synchronization algorithm.

Table 57. Synchronization engine status register 7 (address 61h)

Bit	Symbol	Access	Value	Description
31:8	reserved			
7:0	MINMEMVAR	R	xxxxxxh	This field displays the membership vector with the smallest number of flags set of all in-schedule integration frames ever processed by the synchronization state machine. The field maintains its value when synchronization is lost; it is never reset. The field does not reflect PCF frames dropped by low-level filtering or because failing on the BAG check. Field will contain all 1s after power-on or reset.

Table 58. Synchronization engine status register 8 (address 62h)

Bit	Symbol	Access	Value	Description
31:8	reserved			

Bit	Symbol	Access	Value	Description
7:0	MAXMEMVAR	R	xxxxxxh	This field displays the membership vector with the largest number of flags set of all in-schedule integration frames ever processed by the synchronization state machine. The field maintains its value when synchronization is lost; it is never reset. The field does not reflect PCF frames dropped by low-level filtering or because failing on the BAG check. Field will contain all 0s after power-on or reset.

Table 59. Synchronization engine status register 9 (address 63h)

Bit	Symbol	Access	Value	Description
31:24	reserved			
23:16:	LOCASYNMEM1	R	xxh	This field displays the local_async_membership_comp vector state variable of the clock synchronization algorithm with index one.
15:0	reserved			
7:0	LOCASYNMEM0	R	xxh	This field displays the local_async_membership_comp vector state variable of the clock synchronization algorithm with index zero

Table 60. Synchronization engine status register 10 (address 64h)

Bit	Symbol	Access	Value	Description
31:8	reserved			
7:0	MINASYNMEM	R	xxxxxxh	This field displays the bit vector of the async membership count variable of the clock synchronization algorithm with the smallest number of flags set or all-ones if no evaluation has yet taken place. The field maintains its value even if synchronization is lost. It is never reset. After power-on or reset, it contains all-ones.

Table 61. Synchronization engine status register 11 (address 65h)

Bit	Symbol	Access	Value	Description
31:8	reserved			
7:0	MAXASYNMEM	R	xxxxxxh	This field displays the membership vector with the largest number of flags set of all in-schedule integration frames ever processed by the synchronization state machine. The field maintains its value when synchronization is lost; it is never reset. The field does not reflect PCF frames dropped by low-level filtering or because failing on the BAG check. Field will contain all 0s after power-on or reset.

Table 62. Synchronization engine status register 12 (address 66h)

Bit	Symbol	Access	Value	Description
31:8	reserved			

Bit	Symbol	Access	Value	Description
7:0	CAMEM	R	xxxxxxh	This field displays the membership vector contained in the coldstart frame or coldstart acknowledge frame that caused the most recent transition from UNSYNC state to CA_ENABLED state, or all-zeroes if no such transition has taken place. Note that this field retains all 0s for a switch that is not configured as a compression master.

Table 63. Synchronization engine status register 13 (address 67h)

Bit	Symbol	Access	Value	Description
31:8	reserved			
7:0	SYSNMEM	R	xxxxxxh	This field displays the membership vector contained in the integration frame that caused the most recent transition from UNSYNC state to SYNC state or TENTATIVE SYNC state or all-zeroes if no such transition has yet taken place. Note that this field retains all 0s if the switch never took part in starting the network (which is always the case for switches that are not configured as compression masters).

Table 64. Synchronization engine status register 14 to 22 (address 68h to 6Fh)

'n' is an index from 0 to 7

Bit	Symbol	Access	Value	Description
31:0	MOFFSETn	R	xxxxxxh	This field (in each of the eight registers) contains a timestamp taken whenever a frame of the respective synchronization master becomes permanent. The source of the timestamp is the local clock of the synchronization engine. The address assigned to a specific synchronization master equals its bit position within the membership vector. These fields always return zero on read for switches whose SWMASTER flag is not set.

Table 65. Synchronization engine status register 23 (address 70h)

Bit	Symbol	Access	Value	Description
31:30	reserved			
29:0	TIMER	R	xxxxxxh	This field displays the local timer state variable of the clock synchronization algorithm.

Table 66. Synchronization engine status register 24 (address 71h)

Bit	Symbol	Access	Value	Description
31:27	reserved			
26:0	CLOCK	R	xxxxxxh	This field displays the local clock state variable of the clock synchronization algorithm.

6.1.1.7 Memory Partitioning

Table 67. VL memory partition status registers (address range 80h to 87h)

SJA1105Q and SJA1105S only

'n' is an index from 0 to 7

Bit	Symbol	Access	Value	Description
31	PARTDRPVLn	R		VL memory partition status: Flag cleared at power-on/reset and on a read access by the host.
			0	no memory error
			1	If this flag is set, the respective VL memory partition suffered at least one out-of-memory error after the previous read access to this field.
30:0	PARTSPCVLn	R	xxxxxxh	Each of these fields contains the number of frames left for the respective VL memory partition at the time of the read access. After configuration (and before receiving the first frame drawing from a particular partition), each field will be set to the value specified by the respective PartitionSpace parameter of the VL Forwarding Parameters configuration block. A critical traffic frame will only be accepted if there is space left within the respective VL memory partition.

Table 68. VL memory partition error counters (address range 800h to 807h)

SJA1105Q and SJA1105S only

'n' is an index from 0 to 7

Bit	Symbol	Access	Value	Description
31:0	PARTDRPCNTVLn	R	xxxxxxh	Each of these fields contains the number of frames dropped due to lack of VL memory partition space since power-on or reset. The counter wraps.

Table 69. L2 memory partition status registers (address range 100h to 107h)

'n' is an index from 0 to 7

Bit	Symbol	Access	Value	Description
31	L2PARTSn	R		switch memory partition status for L2 Ethernet traffic
			0	no memory error
			1	If this flag is set, the respective memory partition suffered at least one out-of-memory error after the previous read access to this field.
30:0	L2PSPCn	R	xxxxxxxxh	Each of these fields contains the number of frames left for the respective L2 memory partition at the time of the read access. After configuration (and before receiving the first frame drawing from a particular partition) each field will be set to the value specified by the respective PART_SPC parameter of the L2 Forwarding Parameters configuration block. A frame will only be accepted if there is space left within the respective memory partition.

Table 70. L2 memory partition error counters (address range 1000h to 1007h)

Bit	Symbol	Access	Value	Description
31:0	PARTDROPn	R		Each of these fields contains the number of frames dropped due to lack of L2 memory partition space since power-on or reset. The counter wraps. *n* reflects the partition number and ranges from 0 to 7.

6.1.1.8 Ethernet port status

Ethernet port statistics and diagnostic information is presented in four categories. Ethernet MAC level statistics capture xMII interface errors. High level port status part 1 and part 2 present higher layer Ethernet statistics. These Ethernet statistics counters present counters defined in RFC2863.

6.1.1.8.1 MAC level port status

Table 71. Ethernet MAC-level port status base addresses

Port number	Base address
Ethernet port 4	208h
Ethernet port 3	206h
Ethernet port 2	204h
Ethernet port 1	202h
Ethernet port 0	200h

Table 72. Ethernet port status - MAC-level diagnostic counters (offset 0h)

Counters cleared at power-on/reset and on any read access by the host.

Bit	Symbol	Access	Value	Description
31:24	N_RUNT	R	xxh	This field counts the number of frames that do not have a SOF, alignment or MII error, but are shorter than 64 bytes. The counter does not wrap
23:16	N _SOFERR	R	xxh	This field counts the number of frames that started less than 16 clock cycles after the most recent frame that at least had a correct SOF pattern, with a byte other than 55h or D5h, have a byte other than D5h being the first byte that is different from 55h (if the frame starts with a preamble), that have the MII error input being asserted prior to or up to the SOF delimiter byte or that terminated before the SOF delimiter byte or immediately after the SOF delimiter byte. The field does not wrap.
15:8	N_ALIGNERR	R	xxh	This field counts the number of frames that started with a valid start sequence (preamble plus SOF delimiter byte) but whose length is not a multiple of 8 bits (at the given line speed). The field does not wrap.
7:0	N_MIIERR	R	xxh	This field counts the number of frames that started with a valid start sequence (preamble plus SOF delimiter byte) but terminated with the MII error input being asserted. The field does not wrap.

Table 73. Ethernet port status - MAC-level diagnostic flags (offset 1h)

Flags cleared at power-on/reset and on a read access by the host.

Bit	Symbol	Access	Value	Description
31:27	reserved	R		
27	TYPEERR	R		This flag is set if a protocol control frame was received on the respective port with a type value that is not defined.
26	SIZEERR	R		This flag is set if a protocol control frame was received on the respective port with a size other than was specified by the PCFSZE parameter in the Clock Synchronization Parameters block of the configuration file.
25	TCTIMEOUT	R		This flag is set if a protocol control frame was received on the respective port that had a transparent clock value that does not allow processing of the frame at its permanence point (i.e. the value contained in the transparent clock field does not have enough margin with respect to the value of the MAXTRANSPCLK parameter of the Clock Synchronization Parameters block of the configuration file).
24	PRIORERR	R		This flag is set if a protocol control frame was received on the respective port that had a priority value other than the one set in the SYPRIORITY parameter of the Clock Synchronization Parameters block of the configuration file.
23	NOMASTER	R		This flag is set if a coldstart protocol control frame or a coldstart acknowledgement protocol control frame has been received on the respective port although the switch is not configured as a compression master.
22	MEMOV	R		This flag is set if a protocol control frame was received on the respective port that had flags of the membership vector set that are not supported (only bit positions 0 to 7 are supported).
21	MEMERR	R		This flag is set if the switch is configured as compression master (the SWMASTER flag of the Clock Synchronization Parameters configuration block is set) and a protocol control frame was received on the respective port whose membership vector does not match the VL ID of the protocol control frame.
20	reserved	R		
19	INVTYP	R		This flag is set if a protocol control frame (as defined by the VL ID) was received on the respective port that had an EtherType value other than h'891D.
18	INTCYOV	R		This flag is set if a protocol control frame was received on the respective port that had an integration cycle value larger than MAXINTEGCY of the Clock Synchronization Parameters configuration block.
17	DOMERR	R		This flag is set if a protocol control frame was received on the respective port that had a domain value that does not match the value set for the SYDOMAIN parameter of the Clock Synchronization Parameters configuration block.

Bit	Symbol	Access	Value	Description
16	PCFBAGDROP	R		This flag is set if a protocol control frame was received on the respective port that was to become permanently more than MAXTRANSPCLK past the preceding protocol control frame of the same master. This check is performed at compression master switches only.
15:12	SPCPRIOR	R		see flag SPCERR
11:8	AGEPRIOR	R		see flag AGEDRP
7	reserved	R		
6	PORTDROP	R		This flag is set to indicate that a frame was dropped at the respective port because the port has not been enabled for traffic in the L2 Policing table
5	LENDROP	R		This flag is set to indicate that a frame was dropped at the respective port because the frame was longer than defined in the L2 Policing table.
4	BAGDROP	R		This flag is set to indicate that a frame was dropped at the respective port because there was no bandwidth left on the port as defined in the L2 Policing table.
3	POLIECERR	R		This flag is set to indicate that a critical traffic frame failed on either the VL-specific length check or on the timeliness check (BAG check, TT window check, or unreleased check for input RC frames that are routed as TT) at the respective port. The flag is reset on power-on/reset and whenever the host reads the status word containing the flag.
2	DRPNONA664ERR	R		This flag is set to indicate that a frame was dropped at the respective port because its EtherType field contained a value other than 800h while the DRPNONA664 flag of the MAC Configuration block was set
1	SPCERR	R		This flag is set to indicate that a frame was dropped at the respective port because the respective priority queue as defined by the BASE and TOP parameters (in the MAC configuration block) did not have any space left or is deactivated (as defined by the ENABLED array of flags within the MAC Configuration table). If the flag is set, SPCPRIOR will contain the index of the priority queue that hosted the dropped frame.
0	AGEDRP	R		This flag is set to indicate that a critical traffic frame was dropped at the respective port because it hit the maximum age as specified by the MAXAGE parameter of the port (in the MAC Configuration table). If the flag is set, AGEPRIOR will contain the index of the priority queue that hosted the dropped frame.

6.1.1.8.2 High level port status part 1

Table 74. Ethernet high level port status part 1 base addresses

Port number	Base address
Ethernet port 4	440h
Ethernet port 3	430h
Ethernet port 2	420h

Port number	Base address
Ethernet port 1	410h
Ethernet port 0	400h

Table 75. High level statistics part 1 registers

Counters cleared at power-on/reset.

Offset	Bit	Symbol	Access	Description
0h	31:0	N_TXBYTE	R	This field contains the lower 32 bits of the number of bytes (all data bytes of an Ethernet frame from the first byte of the Ethernet destination MAC address to the last byte of the checksum but not including preamble bytes nor SOF delimiters) transmitted to the respective port since power-on or reset. The counter wraps. When reading from this address, the upper bits of the counter are stored to a shadow register accessible on relative address 1h.
1h	31:0	N_TXBYTESH	R	This field contains the upper bits of the most recently read N_TXBYTE, N_TXFRM, N_RXBYTE or N_RXFRM counter, no matter what the port was. The intended use is to read the N_TXBYTE field and the N_TXBYTESH field of a specific port as an atomic action, i.e. without reading any of the N_TXBYTE, N_TXFRM, N_RXBYTE or N_RXFRM fields of the same port or of other ports in between. This ensures that a consistent counter value is received. The counter wraps.
2h	31:0	N_TXFRM	R	This field contains the lower 32 bits of the number of frames transmitted to the respective port since power-on or reset. The counter wraps. When reading from this address, the upper bits of the counter are stored to a shadow register accessible on relative address 3h.
3h	31:0	N_TXFRMSH	R	This field contains the upper bits of the most recently read N_TXBYTE, N_TXFRM, N_RXBYTE or N_RXFRM counter, no matter what the port was. The intended use is to read the N_TXFRM field and the N_TXFRMSH field of a specific port as an atomic action, i.e. without reading any of the N_TXBYTE, N_TXFRM, N_RXBYTE or N_RXFRM fields of the same port or of other ports in between. This ensures that a consistent counter value is received. The counter wraps.
4h	31:0	N_RXBYTE	R	This field contains the lower 32 bits of the number of bytes (all data bytes of an Ethernet frame from the first byte of the Ethernet destination MAC address to the last byte of the checksum but not including preamble bytes nor SOF delimiters) received on the respective port in MAC-level correct frames since power-on or reset. The counter wraps. When reading from this address, the upper bits of the counter are stored to a shadow register accessible on relative address 5h.

Offset	Bit	Symbol	Access	Description
5h	31:0	N_RXBYTESH	R	This field contains the upper bits of the most recently read N_TXBYTE, N_TXFRM, N_RXBYTE or N_RXFRM counter, no matter what the port was. The intended use is to read the N_RXBYTE field and the N_RXBYTESH field of a specific port as an atomic action, i.e. without reading any of the N_TXBYTE, N_TXFRM, N_RXBYTE or N_RXFRM fields of the same port or of other ports in between. This ensures that a consistent counter value is received. The counter wraps.
6h	31:0	N_RXFRM	R	This field contains the lower 32 bits of the number of MAC-level correct frames received on the respective port since power-on or reset. The counter wraps. When reading from this address, the upper bits of the counter are stored to a shadow register accessible on relative address seven.
7h	31:0	N_RXFRMSH	R	This field contains the upper bits of the most recently read N_TXBYTE, N_TXFRM, N_RXBYTE or N_RXFRM counter, no matter what the port was. The intended use is to read the N_RXFRM field and the RSFRAMESSH field of a specific port as an atomic action, i.e. without reading any of the N_TXBYTE, N_TXFRM, N_RXBYTE or N_RXFRM fields of the same port or of other ports in between. Only in this way can a consistent counter value be received. The counter wraps.
8h	31:0	N_POLERR	R	This field counts the number of frames that were dropped based on the L2 policing operation. • rate limit exceeded • length limit exceeded • source address spoofing (ENFPORT), • the policing table linked with the associated reception port/priority is not configured • a frame received from the host port produced a match with MAC_FLT/MAC_FLTRES but the host did not provide routing information for the respective destination MAC address • A received frame matches with MAC_FLT/MAC_FLTRES but HOST port is not configured. • A broadcast/multicast/unicast frame is dropped due to DRPBC/DRPMC/DRPUNI settings. • The flag LEARN_ONCE is set and a frame is received on another port that it was learnt on. The counter wraps.
9h	31:0	N_CTPOLERR	R	*SJA1105Q and SJA1105S only* This field counts the number of frames which were dropped based on the critical traffic policing operation, i.e., BAG mismatch, window missmatch, or per-VL size limit violation since power-on or reset. The counter wraps.
Ah	31:0	N_VLNOTFOUND	R	*SJA1105Q and SJA1105S only* This field counts the number of frames that were dropped because the Virtual Link ID has not been configured for this port since power-on or reset. The counter wraps.
Bh	31:0	N_CRCERR	R	This field counts the number of frames that had a receive-side CRC error on this port since power-on or reset. The counter wraps.

Offset	Bit	Symbol	Access	Description
Ch	31:0	N_SIZEERR	R	This field counts the number of frames received since power-on or reset with an invalid length (2 kB or more or the length contained in the Type/Length field of the frame did not match the actual length) as well as frames received while ingress traffic was disabled (INGRESS = 0) on this port. The counter wraps.
Dh	31:0	N_UNRELEASED	R	*SJA1105Q and SJA1105S only* This counter is incremented when a frame is received on the respective port that meets the conditions for increasing the Unreleased counter of any Virtual Link Status entry. This means that this counter is also incremented when the respective Virtual Link Status entry is not increased because it has already reached its maximum value (since the Unreleased counter of the respective Virtual Link Status entry does not wrap). The counter wraps.
Eh	31:0	N_VLANERR	R	This field counts the number of frames that were dropped since power-on or reset because the VLAN ID was either not found in the VLAN Lookup table, the respective port is not listed in the VMEMB_PORT vector of the configured VLANID, or a legal or illegal double-tagged frame was received while double-tagged traffic was not allowed (DRPDTAG = 1). The counter wraps.
Fh	31:0	N_N664ERR	R	This field counts the number of frames dropped since power-on or reset because they had an EtherType field other than 800h while the DRPNONA664 flag was set for the respective port in the MAC Configuration table (Table 22), they were not tagged while untagged traffic was not allowed (DRPUNTAG = 1; see Table 22), or they were not routed to any destination (because destination ports were down because flag EGRESS = 0, destination ports were not reachable for traffic sourced at the respective ingress port as per REACH_PORT of the respective ingress port, or destination ports were not members of the VLAN broadcast domain as per VLAN_BC of the respective VLAN). The counter wraps.

6.1.1.8.3 High level port status part 2

Table 76. Ethernet high level port status part 2 base addresses

Port number	Base address
Ethernet port 4	640h
Ethernet port 3	630h
Ethernet port 2	620h
Ethernet port 1	610h
Ethernet port 0	600h

Table 77. High level statistics part 2 registers

Flags and counters cleared at power-on/reset.

Offset	Bit	Symbol	Access	Description
Bh	24:16	QLEVEL_HWM_7	R	These fields represent the highest watermark for the queue occupancy level of a TX MAC output priority queue which indicates the maximum fill of the queue since the last read.
Bh	15:9	reserved	R	
Bh	8:0	QLEVEL_7	R	These fields represent the number of frames stored in each TXMAC output priority queue (they are per port and priority fields).
…	…	…		
4h	24:16	QLEVEL_HWM_0	R	see above
4h	15:9	reserved		
4h	8:0	QLEVEL_0	R	see above
3h	31:0	N_QFULL	R	This field counts the number of frames that were dropped on egress because the respective priority queue of the destination port (as defined per VLAN_PMAP of the L2 Forwarding table) or of a critical traffic frame (as defined per PRIORITY of the VL Forwarding table received at this port) did not have any space left since power-on or reset. The counter wraps.
2h	31:0	N_PART_DROP	R	This field counts the number of frames that were dropped on ingress because the respective memory partition of the port (as defined per PARTITION of the L2 Policing table) or of a critical traffic frame (as defined per PARTITION of the VL Forwarding table received at this port) had no space left after power-on or reset. The counter wraps.
1	31:0	N_EGR_DISABLED	R	This field counts the number of frames that were not routed to the port this counter is assigned to, since power on or reset, because the port was down (EGRESS = 0). The counter wraps.
0	31:0	N_NOT_REACH	R	This field counts the number of frames that produced a match in the L2 Lookup table since power-on or reset, but were not routed to the port this counter is assigned to because the port is not reachable for the respective ingress port as per REACH_PORT in the L2 Forwarding table. The counter wraps.

6.1.1.8.4 Statistics Counters

Table 78. Ethernet statistics counters base addresses

Port number	Base address
Ethernet port 4	1460h
Ethernet port 3	1448h
Ethernet port 2	1430h
Ethernet port 1	1418h
Ethernet port 0	1400h

Table 79. Ethernet statistics counter registers

Flags and counters cleared at power-on/reset.

Offset	Bit	Symbol	Access	Description
16h	31:0	N_DROPS_NOLEARN	R	The number of received frames that are dropped because their source MAC address cannot be learned and the switch is configured to drop this traffic on the received port
15h	31:0	N_DROPS_EMPTY_ ROUTE	R	The number of received frames that are dropped because their destination route is empty.
14h	31:0	N_DROPS_ILL_DTAG	R	The number of received frames that are dropped because they are classified as illegal double tagged traffic. A double tagged frame is classified as illegal double tagged traffic if it cannot be classified as double-tagged. This means that the frame carries 2 TPIDs but both are outer-tags or inner-tags or their order is reversed (inner-tag is followed by the outer-tag).
13h	31:0	N_DROPS_DTAG	R	Counts the received double tagged frames that are dropped because the switch is configured to drop this traffic on the received port.
12h	31:0	N_DROPS_SOTAG	R	Counts the received single outer tagged frames that are dropped because the switch is configured to drop this traffic on the received port.
11h	31:0	N_DROPS_SITAG	R	Counts the received single inner tagged frames that are dropped because the switch is configured to drop this traffic on the received port.
10h	31:0	N_DROPS_UTAG	R	The field counts the received untagged frames that are dropped because the switch is configured to drop this traffic on the received port.
Fh	31:0	N_TX_BYTES_1024_ 1518	R	Counts transmitted frames with length >= 1024 and <= 2047.
Eh	31:0	N_TX_BYTES_512_1023	R	Counts transmitted frames with length >= 512 and <= 1023.
Dh	31:0	N_TX_BYTES_256_511	R	Counts transmitted frames with length >= 256 and <= 511
Ch	31:0	N_TX_BYTES_128_255	R	Counts transmitted frames with length >= 128 and <= 255
Bh	31:0	N_TX_BYTES_65_127	R	Counts transmitted frames with length >= 64 and <= 127
Ah	31:0	N_TX_BYTES_64	R	Counts transmitted frames with length = 64
9h	31:0	N_TX_MCAST	R	The field counts transmitted multicast frames.
8h	31:0	N_TX_BCAST	R	The field counts transmitted broadcast frames.
7h	31:0	N_RX_BYTES_1024_ 1518	R	Counts received frames with length >= 1024 and <= 2047.
6h	31:0	N_RX_BYTES_512_1023	R	Counts received frames with length >= 512 and <= 1023.
5h	31:0	N_RX_BYTES_256_511	R	Counts received frames with length >= 256 and <= 511
4h	31:0	N_RX_BYTES_128_255	R	Counts received frames with length >= 128 and <= 255
3h	31:0	N_RX_BYTES_65_127	R	Counts received frames with length >= 64 and <= 127
2h	31:0	N_RX_BYTES_64	R	Counts received frames with length = 64
1h	31:0	N_RX_MCAST	R	The field counts received multicast frames.
0h	31:0	N_RX_BCAST	R	The field counts received broadcast frames.

6.1.1.9 Time-Triggered Ethernet (SAE AS6802)/TSN Virtual link status

SJA1105Q and SJA1105S only

Virtual link status is provided by two double words per VL that contain all status information for the respective VL. The status words at addresses 10000h and 10001h are assigned to the input VL with the lowest ID (as contained in the VL Lookup table). The status words at addresses 10002h and 10003h are assigned to the second lowest ID, and so on. All the counters are reset at power-on and whenever the host submits a request to clear the status words by asserting the CLEARVLS flag in the Control area (see Table 57). All of the counters wrap. Reading counters at an offset that are not defined in the VL Lookup table of the configuration data returns arbitrary values.

Table 80. Virtual link status register 0 (address 10000h)

Bit	Symbol	Access	Description
31:16	TIMINGERRn	R	This counter is incremented when a VL configured to be RC-policed on input fails on the BAG check, if a VL configured to be TT-policed on input fails on the window check (either because the window is closed, synchronization is not established, or flushing the TT buffers after loss of synchronization has not been completed yet), or if a VL configured to be TT-dispatched is received at a time synchronization is not established or flushing the TT buffers after loss of synchronization has not been completed yet. The counter is incremented by 1 at most for each frame (e.g. when receiving a frame of a VL that is configured to be RC-policed and TT-dispatched at a time synchronization is not established and if this frame also violates the BAG, the counter is incremented by 1).
15:0	UNRELEASEDn	R	This counter is incremented whenever a frame is received for a VL that is dispatched in time-triggered fashion at a time the most recently received frame has not yet been dispatched to all destination ports. In a correct setup, this can only be the case for a VL that is policed in RC mode but is dispatched in TT mode. For VLs being policed in TT fashion the receive window check is supposed to fail at times the VL has ports left in the dispatch schedule. The respective check is only performed for frames that passed all policing checks (BAG or window) as well as the memory partition check.

Table 81. Virtual link status register 1 (address 10001h)

Bit	Symbol	Access	Description
31:16	reserved	R	
15:0	LENGTHERRn	R	This counter is incremented whenever a frame of the VL is received that contains more bytes than specified by the MAXLENGTH parameter of the respective VL Policing table entry.

6.1.2 Control Area

The controls area manages some of the switch functionality during run time. Write access to an address not listed in this section is ignored.

6.1.2.1 General Control

Bits RPARINITL[22:0] and RPARINITU[4:0] are used to configure the RAM parity check. After power-on or reset, these bits will contain all 0s, resulting in even parity. These bits

are intended for self-testing: the host could load a configuration, apply stimulus, change the parity bit of a specific block and check if the respective RAMPARERR flag is set after applying enough stimulus to trigger a parity check. When read, these fields will return the value most recently written by the host or all 0s after power-on or reset.

Table 82. RAM parity check configuration register 0 (address 0Eh)

Bit	Symbol	Access	Description
31:23	reserved	R	
22:0	RPARINITL	R/W	This field is used to change the parity check. For each bit, 0 selects even parity and 1 selects odd parity. The parity is set to all zeros after reset.

Table 83. RAM parity check configuration register 1 (address 0Fh)

Bit	Symbol	Access	Description
31:5	reserved	R	
4:0	RPARINITU	R/W	This field is used to change the parity check. For each bit, 0 selects even parity and 1 selects odd parity. The parity is set to all zeros after reset.

Table 84. Ethernet port status control register 0 (address 10h)

Bit	Symbol	Access	Description
31:5	reserved	R	
4:0	CLEARPORT	W	This field is used to reset the MAC-level diagnostics counters and flags for each port. Setting a bit to 1 resets the relevant MAC-level port status information, as described in Section 5.2.5. High-level diagnostic counters belonging to a port cannot be reset. This field returns all 0s on read.

Table 85. VL status control register (address 11h)

SJA1105Q and SJA1105S only

Bit	Symbol	Access	Description
31:5	reserved	R	
4:0	CLEARVLS	W	Setting this bit to 1 triggers a reset of the status information for all VLs. It remains set during the reset process and is cleared once the operation is complete. Setting this bit again while a reset is in progress has no effect. The switch will not update any counters while the reset is in progress. All counters will show zero immediately after this flag is cleared.

Table 86. Ethernet port status control register 1 (address 12h)

Bit	Symbol	Access	Description
31:5	reserved	R	

Bit	Symbol	Access	Description
4:0	INHIBITTX	W	This vector represents the set of ports on which the transmission is inhibited. A port inhibits transmission if the respective bit is set to 1. Transmission to the respective port resumes when the bit is cleared. If inhibit is enabled, frame output is stopped, but frames are still dispatched to the queue and the queue processing continues. The frames will not be handed over to the xMII interface. In effect, resource utilization in the switch (e.g. frame memory occupied by frames being forwarded to an inhibited port) will not change in response to this flag. Changing the flag will have an effect once the port is in an IFG, a change cannot generate malformed packets. Note that in contrast to the EGRESS bit (MAC Configuration Table), the transmission of all frames will stop including management frames and Time-Triggered Ethernet PCFs.

Table 87. PTP control register 1 (address 18h)

Bit	Symbol	Access	Description
31	VALID	W	Setting this flag in combination with PTPSTRTSCH or PTPSTOPSCH dynamically changes the behaviour of the schedule running based on the PTP time and the external PTP_CLK pin.
30	PTPSTRTSCH	R/W	*SJA1105Q and SJA1105S only* Setting this flag in combination with VALID to true triggers the switch to integrate all active subschedules into the schedule at the first entry configured in the Schedule Entry Points table. This action is performed at a time when the PTP clock synchronized by the host exceeds the value of PTPSCHTM and only if the value of CLKSRC in the Schedule Entry Points Parameter table is set to 11 (PTP clock) and the schedule is not already running. On read, this flag is found true if CLKSRC is set to PTP and the schedule is running correctly running.
29	PTPSTOPSCH	R/W	*SJA1105Q and SJA1105S only* Setting this flag in combination with VALID to true triggers the switch to stop schedule execution immediately if CLKSRC (Table 13) is set to 11 (PTP clock). This flag has precedence over PTPSTRTSCH. On read, this flag will be found set if CLKSRC is set to PTP and the schedule is not running.
28	STARTPTPCP	W	Setting this flag in combination with VALID triggers the switch to begin toggling the external PTP_CLK pin at a rate of PTPPINDUR when the PTP clock synchronized by the host exceeds the value of PTPPINST.
27	STOPPTPCP	W	Setting this flag in combination with VALID triggers the switch to stop toggling the external PTP_CLK pin.
26	CASSYNC	R/W	This flag is used to determine the timestamp counter (or PTP clock) offset between a cascaded master (CAS_MASTER is asserted) and the cascade slave (CAS_MASTER is deasserted). See description of CAS_MASTER.
25:4	reserved		

Bit	Symbol	Access	Description
3	RESPTP	W	Asserting this flag in combination with VALID causes PTPCLK, PTPTSCLK and PTPCLKRATE to be reset to their power-on defaults: the clocks are set to 0 and the rate is set to 1. Note that this may corrupt ingress timestamps when it happens in a time frame between frame start at the source port and 2 µs past the frame end at the source port. This flag always returns 0 on read.
2	CORRCLK4TS	W	Asserting this flag in combination with VALID causes subsequent timestamps on ingress and egress management frames to be taken based on PTPCLK. If the flag is de-asserted, timestamps are taken based on PTPTSCLK. The latter is also the default after power-on or reset. Note that taking ingress timestamps is only safe when they are taken based on PTPTSCLK. Using PTPCLKVAL for timestamping may deliver corrupted ingress timestamps if (a) PTPCLKRATE is larger than 1.2 or (b) the user writes to PTPCLK. Also changing the value of this field may corrupt ingress timestamps that occur in a time frame between frame start at the source port at 2 µs past the frame end at the source port. This flag always returns 0 on read.
1	PTPCLKSUB	W	If a new value is written to the field PTPCLKVAL and this flag is set, the new written value is subtracted from the value of the rate corrected PTPCLKVAL. It is used to correct (subtract an offset) the rate corrected PTPCLKVAL.
0	PTPCLKADD	W	Asserting this flag in combination with VALID causes subsequent writes to PTPCLKVAL to be added to the clock rather than setting a new value. After power-on or reset the switch will be in set mode (i.e. writes to PTPCLKVAL will set a new value rather than adding an offset to the current value). This flag always returns 0 on read.

Table 88. PTP control registers 2 to 6 (address 13h-17h)

Address	Bit	Symbol	Access	Description
17h	31:0	PTPPINDUR	W	Thie field specifies the interval between two edges on the external clock on pin PTP_CLK (in multiples of PTP_CLK tick duration). PTP_CLK tick duration is 8 ns by default and can change depending on the setting of PTPCLKRATE. This field returns 0 on read.
16h	31:0	PTPPINSTU	W	This field specifies the upper 32 bits of PTPTSCLK at which the switch starts toggling the external PTP_CLK pin.
15h	31:0	PTPPINSTL	W	This field specifies the lower 32 bits of PTPTSCLK at which the switch starts toggling the external PTP_CLK pin.
14h	31:0	PTPSCHTMU	W	*SJA1105Q and SJA1105S only* Upper 32 bits of PTPSCHTM specifies the time on the synchronized PTP clock at which the switch integrates into the schedule if the parameter CLKSRC in the Schedule Entry Points Parameter table is set to select the PTP clock to drive the schedule.
13h	31:0	PTPSCHTML	W	*SJA1105Q and SJA1105S only* Lower 32 bits of PTPSCHTM. See above.

Table 89. PTP control registers 7 to 14 (address 19h-20h)

Address	Bit	Symbol	Access	Description
20h	31:0	PTPSYNCTSU	R	It is a shadow register (upper 32bits) used to obtain the PTP CLK offset between a switch cascaded master and the cascaded slaves (see CASSYNC description).
1Fh	31:0	PTPSYNCTSL	R	See above (lower 32 bits)
1Eh	31:0	PTPCLKCORP	W	*SJA1105Q and SJA1105S only* On write, this field defines the time between consecutive clock corrections applied to the schedule module in multiples of 8 ns (i.e. the first clock correction gets applied to the schedule execution module at time PTPSCHTM + PTPCLKCORP x 8 ns. The second clock correction is applied after a period of PTPCLKCORP x 8 ns). The field is ignored on read.
1Dh	31:0	PTPTSCLKU	R	Upper 32 bit of PTPTSCLK. This field is read only, write access is ignored. On read, this field contains the current value of the PTP timestamp clock that is used to timestamp MAC management frames on ingress and egress. Upon reading the least significant 32 bits (PTPTSCLKL), the most significant 32 bits (PTPTSCLKU) are latched to a shadow register to provide a consistent snapshot of this 64-bit value. The field represents the time elapsed since power-on or reset in multiples of 8 ns measured on the free running clock.
1Ch	31:0	PTPTSCLKL	R	Lower 32 bit of PTPTSCLK.
1Bh	31:0	PTPCLKRATE	W	This field determines the speed of PTPCLKVAL. It implements a fixed-point clock rate value with a single-bit integer part and a 31-bit fractional part allowing for sub-ppb rate corrections. PTPCLKVAL ticks at the rate of PTPTSCLK multiplied by this field. So any value having the integer part set to 0 (i.e. bit 31 set to 0) will cause PTPCLKVAL to be slower than PTPTSCLK. Any value having the integer part set to one will cause PTPCLKVAL to be at least as fast as PTPTSCLK E.g. a value of h'90000000 will cause PTPCLKVAL to tick 1.125 = (2^0 + 2^{-3}) faster than PTPTSCLK. The reset value is 80000000h.
1Ah	31:0	PTPCLKVALU	R/W	Upper 32 bits of PTPCLKVAL Depending on the value of PTPCLKADD, a write to this field will cause the internal PTP clock counter to be set to the value provided by the host (in case PTPCLKADD is de-asserted) or to add the value provided by the host to the current value of the internal PTP clock counter. A read access to this field returns the current value of the internal (rate-corrected) PTP clock counter. On reading the least significant 32 bits, the most significant 32 bits are latched to a shadow register to provide a consistent snapshot of this 64-bit value. This value represents the current PTP time in multiples of 8 ns.
19h	31:0	PTPCLKVALL	R/W	Lower 32 bits of PTPCLKVAL

6.1.3 Dynamic Reconfiguration

Dynamic reconfiguration of the switch refers to those features of the programming interface's control area that allow specific parameter values of the loaded configuration to be changed at run time. The following sections provide details of the dynamic reconfiguration of specific parts of the loaded configuration.

6.1.3.1 L2 Lookup Table

The register entries in this section are used to dynamically reconfigure the L2 Address Lookup table.

Table 90. L2 Address Lookup table reconfiguration register 0 (address 29h)

Bit	Symbol	Access	Description
31	VALID	R/W	By writing a value that has this flag set the host triggers a dynamic change of the contents of the L2 Lookup Table (if RDWRSET is set) or a read access (when RDWRSET is cleared). A write access of the host will only be accepted at times this flag is found cleared. The flag will remain set until the switch has completed the access and will be cleared automatically afterwards. The address of the access will be extracted from the INDEX field of ENTRY both for reads and writes.
30	RDWRSET	R/W	Determines if an access is a read access (if the flag is cleared) or a write access (if the flag is set). On read this flag will display the value most recently written by the host. A write request is accepted only when HOSTCMD is set to write host or invalid. A read request is accepted only when HOSTCMD is set to search host or read host.
29	ERRORS	R	Will be ignored on write. On read the flag has meaning at times when the VALID flag is found reset. If found set, the most recent access resulted in an error because it was issued prior to completing the configuration load procedure.
28	LOCKEDS	R/W	On write will specify the format of ENTRY (see description for ENTRY). On read the flag will be found cleared at times the VALID flag is found set. The flag will also be found cleared in response to a read having the MGMTROUTE flag set. In response to a read with the MGMTROUTE flag cleared, the flag be set if the most recent access operated on an entry that was either loaded by configuration or through dynamic reconfiguration (as opposed to automatically learned entries).
27	VALIDENT	R/W	In case of a write access with the MGMTROUTE flag cleared, this flag determines if the respective entry should be marked valid. Marking an entry as invalid (i.e., clearing VALIDENT) has the effect that the entry at the respective position will be available for address learning again. On read with the MGMTROUTE flag cleared the flag will be set if the most recent access operated on a valid entry (i.e. an entry that contains either a programmed route or a dynamically learned one). In case of a write access with the MGMTROUTE flag set, the flag will be ignored. It will always be found cleared for read accesses with the MGMTROUTE flag set.

Bit	Symbol	Access	Description
26	MGMTROUTE	R/W	On write the host will set this flag to indicate that the request is targeted for a management route entry. In this case the INDEX field of ENTRY needs to point to one of the 4 supported management route entries. Any management frames received from the port as indexed by the HOSTPORT field of the General Parameters will be checked for a match in the management route entries and be routed accordingly. If no matching entry is found, the respective management frame will be dropped. A management route entry will be valid only if it has the ENFPORT flag set and it will be valid only for a single frame. Upon a match, the ENFPORT flag of the respective entry will be cleared. This can be used by the host as an acknowledgement. If the host provides several management route entries with identical values for the MACADDR, the one at the lowest index will be used first. On read the flag will display the value most recently written by the host. To specify if a PTP egress timestamp shall be captured on each port upon transmission of the frame, the LSB of VLANID in the ENTRY field provided by the host must be set. Bit 1 of VLANID then specifies the register of this port in which the timestamp gets stored in (if the respective management frame is sent on port n, the timestamp can be received at address 192+n×2 if bit 1 of VLANID is set to 0 or at 192+n × 2+1 otherwise).
25:23	HOSTCMD	R/W	This field controls the TCAM command performed on the supplied ENTRY. Possible commands are: host search: **b001** host read: **b010** host write: **b011** host invalidate entry: **b1--** On read the field will display the value most recently written by the host.

Table 91. L2 Address Lookup table reconfiguration register 1 to 3 (address 24h-28h)

Address	Bit	Symbol	Access	Description
28h	31:0	ENTRY[153:122]	R/W	On write this field contains the new value for the entry in the L2 Address Lookup table to be updated if VALIDENT is set. If VALIDENT is not set on write, this field is ignored. The format to be used matches that specified in Section 5.2.1. On read this field displays the value most recently written by the host if this most recent access had the RDWRSET set. If the most recent host access requested a read (RDWRSET not set), the field displays the table entry data once the access completes (as indicated by the VALID flag being cleared). The layout of the bits in ENTRY is, depending on the use of the entry, one of the following: L2 Address Lookup table (LOCKEDS=1) L2 Address Lookup table (LOCKEDS=0) Management L2 Address Lookup table When an entry in the Table is updated, a key is calculated as bitwise-AND between MASK from and the concatenated values of the IOTAG, VLANID and MACADDR fields. Only the value of this key is memorized in the L2 Address Lookup table. Any attempt to read the values of IOTAG, VLANID and MACADDR will return the value of this key. See the description of the L2 Address Lookup table.
27h	31:0	ENTRY[121:90]	R/W	
26h	31:0	ENTRY[89:58]	R/W	
25h	31:0	ENTRY[57:26]	R/W	
24h	31:6	ENTRY[25:0]	R/W	

Address	Bit	Symbol	Access	Description
24h	5:0	Reserved	R	

6.1.3.2 L2 Forwarding Table

This interface is used for the dynamical reconfiguration of the VLAN priority mapping and the port reachability restrictions as specified in the L2 Forwarding Table.

Table 92. L2 Forwarding table reconfiguration register 0 (address 2Ch)

Bit	Symbol	Access	Description
31	VALID	R/W	By writing a value that has this flag set the host triggers a dynamic change of the entry with INDEX. If this flag is found set on read, the switch is still busy processing the most recent update request (which may need up to 10 clock cycles to complete)
30	ERRORS	R	Will be ignored on write. On read, it has meaning if VALID is found reset and the flag value reflects if a dynamic reconfiguration attempt was successful. Such an attempt may fail if at least one value in VLAN_ PMAP exceeds the value configured for MAX_DYNP in case the purpose of the dynamic reconfiguration attempt is to change the egress VLAN priority to priority queue mapping and thus, the value of INDEX is greater than 5.
29	RDWRSET	R/W	Determines if an access is a read access (if the flag is cleared) or a write access (if the flag is set). On read this flag will display the value most recently written by the host.
28:5	reserved		
4:0	INDEX	W	On write contains the index of the entry which is purpose for dynamic reconfiguration. Will be ignored on read.

Table 93. L2 Forwarding table reconfiguration register 1-2 (address 2A – 2Bh)

Address	Bit	Symbol	Access	Description
2Bh	31:0	ENTRY[63:32]	R/W	On write this field contains the new value to be applied to the entry with index INDEX from L2 Forwarding Table in the same format as described in Section 5.2.4. On read this field will display the value most recently written by the host if this most recent access had the RDWRSET set. If the most recent host access requested a read (RDWRSET not set), the field will display the table entry data once the access completes (as indicated by the VALID flag being cleared).
2Ah	31:25	ENTRY[31:25]	R/W	
2Ah	24:0	reserved	R	

6.1.3.3 VLAN Lookup table

Table 94. VLAN Lookup table reconfiguration register 0 (address 30h)

Bit	Symbol	Access	Description
31	VALID	R/W	By writing a value which has this flag set, the host triggers a dynamic change of the entry associated with the VLANID field of ENTRY. A write access is only accepted during times where this flag is cleared. Upon a read access, if this flag is found set, a dynamic reconfiguration is currently in progress.

Bit	Symbol	Access	Description
30	RDWRSET	R/W	Determines if an access is a read access (if the flag is cleared) or a write access (if the flag is set). On read this flag will display the value most recently written by the host.
29:28	reserved		
27	VALIDENT	W	In case of a write access, this flag determines if the respective entry should be marked valid. Marking an entry as invalid (i.e., clearing VALIDENT) has the effect, that the VLAN with the VLANID field of ENTRY will be deactivated on the switch. The flag will be ignored on read.
26:0	reserved		

Table 95. VLAN Lookup table reconfiguration register 1 to 2 (address 2D to 2Eh)

Address	Bit	Symbol	Access	Description
2Eh	31:0	ENTRY[36:5]	R/W	On write this field contains the new VLAN entry to be applied to the VLAN Lookup Table in the same format as described in Table 19. On read this field will display the value most recently written by the host if this most recent access had the RDWRSET set. For writing a new VLAN entry, first the ENTRY registers must be written, then the control register (address 30h) (RDWRSET set). For reading a VLAN entry, first the ENTRY registers must be written (only the VLANID field is evaluated). Then the control address (address 30h) is written (RDWRSET not set). When the VALID flag is found cleared, ENTRY will contain the full VLAN entry.
2Dh	31:27	ENTRY[4:0]		
2Dh	26:0	Reserved		

6.1.3.4 MAC Configuration Table

The register entries in this section are used to dynamically reconfigure the parameters defined in the MAC configuration table.

Table 96. MAC Configuration table reconfiguration register 0 (address 53h)

Bit	Symbol	Access	Description
31	VALID	W	By writing a value that has this flag set the host triggers a dynamic change of the contents of the MAC Configuration Table.
30	ERRORS	R	On read it has meaning at times when VALID is found reset. If found set on read, the most recent access resulted in an error (and did not update any entry of the MAC Configuration Table).
29	RDWRSET	R/W	Determines if an access is a read access (if the flag is cleared) or a write access (if the flag is set). On read this flag will display the value most recently written by the host.
28:3	Reserved	R	
2:0	PORTIDX	W	Specifies the port number which is affected by this dynamic reconfiguration.

Table 97. MAC Configuration reconfiguration register 1 to 8 (address 4Bh to 52h)

Address	Bit	Symbol	Access	Description
52h	31:0	ENTRY[242:211]	R/W	On write this field contains the new value to be applied to the entry with index PORTIDX from MAC Configuration Table in the same format as described in Table 22. On read, this field will display the value most recently written by the host if RDWRSET was set for the most recent access. If the most recent host access requested a read (RDWRSET not set), the field will display the table entry data once the access completes (as indicated by the VALID flag being cleared). The following parameters are re-configured: SPEED (if SPEED is set to 0h in the static configuration), DRPDTAG, DRPSOTAG, DRPSITAG, DRPUNTAG, RETAG, DYN_LEARN, EGRESS, INGRESS, MIRRCIE, INGMIRR, EGRMIRR, VLANPRIO, VLANID, TPDELIN,(if SPEED is set to 0h in the static configuration), TPDELOUT (if SPEED is set to 0h in the static configuration).
51h	31:0	ENTRY[210:179]	R/W	
50h	31:0	ENTRY[178:147]	R/W	
4Fh	31:0	ENTRY[146:115]	R/W	
4Eh	31:0	ENTRY[114:83]	R/W	
4Dh	31:0	ENTRY[82:51]	R/W	
4Ch	31:0	ENTRY[50:19]	R/W	
4Bh	31:13	ENTRY[18:0]	R/W	
4Bh	12:0	reserved		

6.1.3.5 Retagging Table

The register entries in this section are used to dynamically reconfigure the parameters defined in the Retagging table.

Table 98. Retagging table reconfiguration register 0 (address 3Ah)

Bit	Symbol	Access	Description
31	VALID	R/W	Indicates that the entry at position INDEX shall be enabled (in this case the host is supposed to have provided the data for the entry at ENTRY when asserted; the entry at position INDEX will be disabled if this flag is found de-asserted.
30	ERRORS	R	On read it has meaning at times when VALID is found reset. If found set on read, the most recent access resulted in an error because it was issued prior to completing the configuration load procedure.
29	VALIDENT	R/W	Indicates that the entry at position INDEX shall be enabled (in this case the host is supposed to have provided the data for the entry at ENTRY when asserted; the entry at position INDEX will be disabled if this flag is found de-asserted.
28	RDWRSET	R/W	Determines if an access is a read access (if the flag is cleared) or a write access (if the flag is set). On read this flag will display the value most recently written by the host.
27:6	reserved		
5:0	INDEX	W	On write contains the index of the entry which is purpose for dynamic reconfiguration.

Table 99. Retagging table reconfiguration register 1 to 2 (address 38h to 39h)

Address	Bit	Symbol	Access	Description
39h	31:0	ENTRY[40:9]	R/W	On write this field contains the new value to be applied to the entry with index INDEX from Retagging Table in the same format as described in Table 23. On read this field will display the value most recently written by the host if this most recent access had the RDWRSET set. If the most recent host access requested a read (RDWRSET not set), the field will display the table entry data once the access completes (as indicated by the VALID flag being cleared).
38h	31:23	ENTRY[8:0]	R/W	
38h	22:0	reserved	R/W	

6.1.3.6 General Parameters

The register entries in this section are used to dynamically reconfigure the parameters defined in the General Parameters table.

Table 100. General Parameters reconfiguration register 0 (address 46h)

Bit	Symbol	Access	Description
31	VALID	W	By writing a value that has this flag set the host triggers an update. The flag will always be found cleared on read.
30	ERRORS	R	On read it has meaning at times when VALID is found reset. If found set on read, the most recent write access resulted in an error because dynamic reconfiguration is not enabled as indicated by the MIRR_ PTACU flag being de-asserted.
29	MIRR_ERR	R	This flag is found set if the mirror port was not reconfigured. This happens if MIRR_PTACU is was not set and a mirror port reconfiguration was attempted.
28	RDWRSET	R/W	Determines if an access is a read access (if the flag is cleared) or a write access (if the flag is set). On read this flag will display the value most recently written by the host.
27:0	reserved	R	

Table 101. General Parameters reconfiguration register 1 to 11 (address 3Bh to 45h)

Address	Bit	Symbol	Access	Description
45h	31:0	ENTRY[329:298]	R/W	On write this field contains the new value to be applied to General Parameters in the same format as described in Table 28. On read this field will display the value most recently written by the host if this most recent access had the RDWRSET set. If the most recent host access requested a read (RDWRSET not set), the field will display the table data once the access completes (as indicated by the VALID flag being cleared). The following parameters are re-configured: MIRR_PORT, QUEUE_TS, EGRMIRRVID, EGRMIRRPCP, EGRMIRRDEI, REPLAY_PORT
44h	31:0	ENTRY [297:266]	R/W	
43h	31:0	ENTRY [265:234]	R/W	
42h	31:0	ENTRY [233:202]	R/W	
41h	31:0	ENTRY [201:170]	R/W	
40h	31:0	ENTRY [169:138]	R/W	
3Fh	31:0	ENTRY [137:106]	R/W	
3Eh	31:0	ENTRY [105:74]	R/W	
3Dh	31:0	ENTRY [73:42]	R/W	
3Ch	31:0	ENTRY [41:10]	R/W	
3Bh	31:22	ENTRY [9:0]	R/W	

Address	Bit	Symbol	Access	Description
3Bh	21:0	reserved	R	

6.1.3.7 VL Lookup table

SJA1105Q and SJA1105S only

The registers in this section are used for dynamic reconfiguration of the VL Lookup Table configuration.

Table 102. VL Lookup table reconfiguration register 0 (address 4Ah)

Bit	Symbol	Access	Description
31	VALID	R/W	By writing a value that has this flag set the host triggers an update. If this flag is found set on read, the switch is still busy processing the most recent update request.
30	ERRORS	R	If VALID and ERRORS are found set on read, the most recent access resulted in an error (and did not update any entry of the VL Lookup Table) because either it was issued prior to completing the configuration load procedure, or VLLUPFORMAT is set to 0, or the VL Lookup Table has not been loaded (i.e. there is no critical traffic enabled), or the host provided an index in INDEX that has not been loaded.
29	RDWRSET	R/W	Determines if an access is a read access (if the flag is cleared) or a write access (if the flag is set). On read this flag will display the value most recently written by the host.
28:10	reserved	R	
9:0	INDEX	W	On write contains the index of the entry which is purpose for dynamic reconfiguration.

Table 103. VL Lookup table reconfiguration register 1 to 3 (address 47h to 49h)

Address	Bit	Symbol	Access	Description
49h	31:0	ENTRY[71:40]	R/W	On write this field contains the new value to be applied to the entry with index INDEX from VL Lookup Table in the same format as described in Table 7 and Table 8. Only the fields EGRMIRR and INGRMIRR will be reconfigured. On read this field will display the value most recently written by the host if this most recent access had the RDWRSET set. If the most recent host access requested a read (RDWRSET not set), the field will display the table entry data once the access completes (as indicated by the VALID flag being cleared).
48h	31:0	ENTRY[39:8]	R/W	
47h	31:24	ENTRY[7:0]	R/W	
47h	23:0	reserved	R	

6.1.3.8 L2 Lookup Parameters

The register entries in this section are used to dynamically reconfigure the parameters defined in the L2 Lookup Parameters table (Table 24).

Table 104. L2 Lookup parameters reconfiguration register 0 (address 58h)

Bit	Symbol	Access	Description
31	VALID	R/W	By writing a value that has this flag set the host triggers an update. If this flag is found set on read, the switch is still busy processing the most recent update request. The flag will be evaluated only after CONFIGS is found asserted. An updated request issued prior to CONFIGS being found asserted will be processed (and keep the VALID flag asserted) until after CONFIGS gets asserted.
30	RDWRSET	R/W	Determines if an access is a read access (if the flag is cleared) or a write access (if the flag is set). On read this flag will display the value most recently written by the host.
29: 0	reserved	R	

Table 105. L2 Lookup table parameters reconfiguration register 1 to 4 (address 54h to 57h)

Address	Bit	Symbol	Access	Description
57h	31:0	ENTRY[105:74]	R/W	On write this field contains the new value to be applied to L2 Lookup Parameters in the same format as described in Table 24. On read this field will display the value most recently written by the host if this most recent access had the RDWRSET set. If the most recent host access requested a read (RDWRSET not set), the field will display the table data once the access completes (as indicated by the VALID flag being cleared).
56h	31:0	ENTRY[73:42]	R/W	
55h	31:0	ENTRY[41:10]	R/W	
54h	31:22	ENTRY[9:0]	R/W	
54h	21:0	reserved	R	

6.1.3.9 AVB Parameters

The register entries in this section are used to dynamically reconfigure the parameters defined in the AVB parameters table (Table 26).

Table 106. AVB Parameters reconfiguration register 0 (address 8007h)

Bit	Symbol	Access	Description
31	VALID	R/W	By writing a value that has this flag set the host triggers an update. If this flag is found set on read, the switch is still busy processing the most recent update request.
30	ERRORS	R	On read it has meaning at times when VALID is found reset. If found set on read, the most recent access resulted in an error (and did not update any entry of the AVB Parameters).
29	RDWRSET	R/W	Determines if an access is a read access (if the flag is cleared) or a write access (if the flag is set). On read this flag will display the value most recently written by the host.
28: 0	reserved	R	

Table 107. AVB Parameters reconfiguration register 1 to 4 (address 8003h to 8006h)

Address	Bit	Symbol	Access	Description
8006h	31:0	ENTRY[97:66]	R/W	On write this field contains the new value to be applied to AVB Parameters in the same format as described in Table 26. On read this field will display the value most recently written by the host if this most recent access had the RDWRSET set. If the most recent host access requested a read (RDWRSET not set), the field will display the table data once the access completes (as indicated by the VALID flag being cleared). From the AVB Parameters only the following parameters are re-configured: CAS_MASTER and L2CBS.
8005h	31:0	ENTRY[65:34]	R/W	
8004h	31:0	ENTRY[33:2]	R/W	
8003h	31:30	ENTRY[1:0]	R/W	
8003h	29:0	reserved	R	

6.1.3.10 Credit-Based Shaping

The register entries in this section are used to dynamically reconfigure the parameters defined in the Credit Based Shaping table (Table 27).

Table 108. Credit-Based shaping reconfiguration register 0 (address 37h)

Bit	Symbol	Access	Description
31	VALID	W	By writing a value that has this flag set the host triggers a dynamic change of the entry with index CBSIDX. The flag will always be found de-asserted on read.
30	RDWRSET	R/W	Determines if an access is a read access (if the flag is cleared) or a write access (if the flag is set). On read this flag will display the value most recently written by the host.
29	ERRORS	R	On read it has meaning at times when VALID is found reset. If found set on read, the most recent access resulted in an error (and did not update any entry of the Credit-Based Shaping Table.)
28:4	reserved	R	
3:0	CBSIDX	W	On write, this field specifies the index (0 to 15) of the 16 credit-based shaping blocks which is subject for dynamic reconfiguration.

Table 109. Credit Based Shaping reconfiguration register 1 to 5 (address 32h to 36h)

Address	Bit	Symbol	Access	Description
36h	31:0	ENTRY[133:102]	R/W	On write this field contains the new value to be applied to the entry with index CBSIDX from Credit-Based Shaping Table in the same format as described in Table 27. On read this field will display the value most recently written by the host if this most recent access had the RDWRSET set. If the most recent host access requested a read (RDWRSET not set), the field will display the table entry data once the access completes (as indicated by the VALID flag being cleared). The following parameters are re-configured: CBS_PORT CBS_PRIO CREDIT_LO, CREDIT_HI, SEND_SLOPE, IDLE_SLOPE.
35h	31:0	ENTRY[101:70]	R/W	
34h	31:0	ENTRY[69:38]	R/W	
33h	31:0	ENTRY[37:6]	R/W	
32h	31:26	ENTRY[5:0]	R/W	

Address	Bit	Symbol	Access	Description
32h	25:0	reserved	R	

6.1.3.11 L2 Forwarding Parameters

The following registers are used for reading back the parameters defined in the L2 Forwarding Parameters configuration block (Section 5.2.8). Note that writing is not supported.

Table 110. L2 Forwarding Parameters reconfiguration register 0 to 2 (address 8000h to 8002h)

Address	Bit	Symbol	Access	Description
8002h	31:0	ENTRY[82:51]	R	On read, this field returns the L2 Forwarding parameters. Fields PART_SPC[7] to PART_SPC[0] in ENTRY do not show the configured partitioning, but the actual space used at the instant of the read operation.
8001h	31:0	ENTRY[50:19]	R	
8000h	31:13	ENTRY[18:0]	R	
8000h	12:0	reserved	R	

6.2 Reset Generation Unit (RGU)

The RGU provides reset sources across the device and can be used to reset the device.

Table 111. Register overview

Address	Name	Access	Reset Value
100440h	RESET_CTRL	W	00000000h
1007FDh	UNIT_DISABLE	R/W	00000000h

Table 112. Reset control register (addr. 100440h)

Bit	Symbol	Access	Value	Description
31:9	reserved	R	0h	
8	SWITCH_RST	R/W	0	Main reset for all functional modules
7	CFG_RST	R/W	0	Resets all chip-configuration
6	reserved			
5	CAR_RST	R/W	0	Resets the clock and reset control logic
4	OTP_RST	R/W	0	Initiates an OTP read-cycle to read out the product configuration settings
3	WARM_RST	R/W	0	Perform a warm reset
2	COLD_RST	R/W	0	Perform a cold reset
1	POR_RST	R/W	0	Perform a power-on reset
0	reserved			

The reset control register exposes the implemented sequencing of internal reset signals. Activating a reset signal associated with a lower bit number implies resetting all units with higher bit numbers as well.

The bits in the reset control register are self-clearing.

Table 113. Unit disable register for RGU (addr. 1007FDh)

Bit	Symbol	Access	Value	Description
31:1	reserved	R	0h	
0	DISABLE_FLAG	R/W	0	when this bit is set to 1, access to all registers of this unit (except for this register) is inhibited

6.3 Clock Generation Unit (CGU)

The clock generation unit (CGU) generates and distributes the internal core, SGMII, MII, RMII and RGMII clocks.

The CGU generates multiple internal clocks to drive the internal core and the xMII ports. Depending on the operating mode, selected clocks are used to drive the internal xMII interface and transmit clock pins (configured as TX_CLK, REF_CLK or TXC).

A block diagram of the CGU is shown in Figure 14. PLL0 generates a 125 MHz clock for the switch core and, optionally, RGMII. PLL1 generates a 50 MHz clock for RMII. The IDIVx divider is configurable per port and can divide the input clock down to 2.5 MHz. After reset, PLL0 is automatically set to provide a 125 MHz clock for the switch core and PLL1 is disabled. PLL1 must be manually enabled when a port is configured for RMII. The SGMII is hardwired to PLL0 and does not need further CGU configuration.

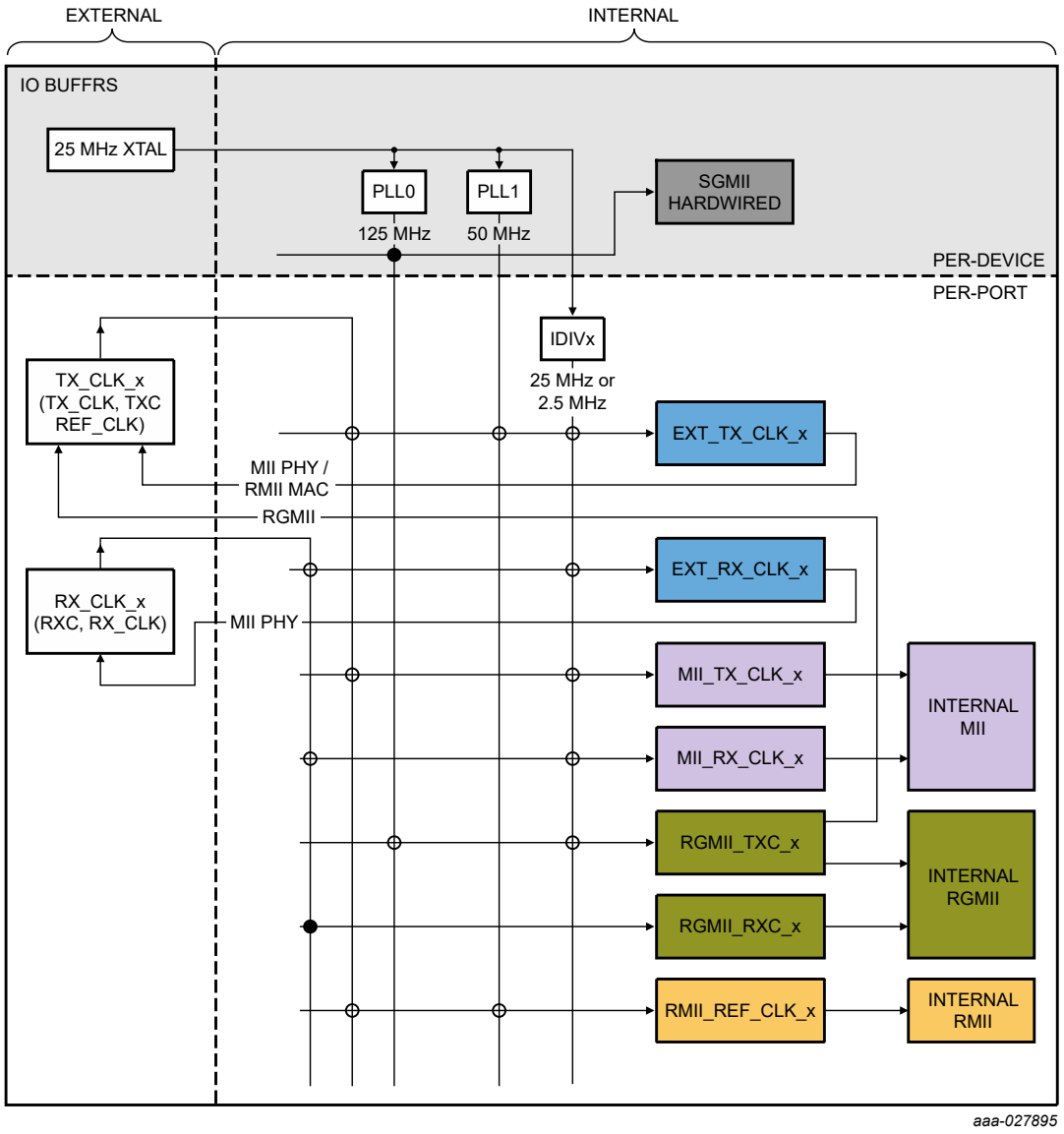


Figure 14. CGU clocking scheme

Loading the static configuration into the device alone is not sufficient to send or receive traffic. Additionally, the clocking of the xMII interfaces has to be set up through the CGU.

The CGU is organized as a matrix, which can forward input clocks (e.g. from a physical clock input such as RXC or a PLL) to various clock sinks. Clock sinks can have multiple purposes. In Figure 14, they appear colored to indicate in which mode they are relevant. Some sinks are used to clock internal parts of the device (e.g. the MII logic, which is shown in violet), while other sinks drive clock pins (e.g. TXC).

Clock sinks and clock sources (except the IO pins) can be configured. For sinks, the source can be selected (CLKSRC field). For sources, advanced functionality can be configured, such as the settings for the integer dividers (IDIVs).

For the sake of completeness Figure 14 shows RGMII_RXC_x. This clock sink is hard-wired and is not configurable. Hence there is no associated configuration register.

CGU registers and addresses are listed in Table 114.

Table 114. CGU Register overview

Address	Name	Access	Reset Value
100005h	RFRQ	R/W	00000000h
100006h	XO66M_0_C	R	0000002Ch
100007h	PLL_0_S	R	00000000h
100008h	PLL_0_C	R/W	0A040040h
100009h	PLL_1_S	R	00000000h
10000Ah	PLL_1_C	R/W	0A000083h
10000Bh	IDIV_0_C	R/W	0A000000h
10000Ch	IDIV_1_C	R/W	0A000000h
10000Dh	IDIV_2_C	R/W	0A000000h
10000Eh	IDIV_3_C	R/W	0A000000h
10000Fh	IDIV_4_C	R/W	0A000000h
100013h	MII_TX_CLK_0	R/W	11000000h
100014h	MII_RX_CLK_0	R/W	11000000h
100015h	RMII_REF_CLK_0	R/W	11000000h
100016h	RGMII_TX_CLK_0	R/W	11000000h
100017h	EXT_TX_CLK_0	R/W	11000000h
100018h	EXT_RX_CLK_0	R/W	11000000h
100019h	MII_TX_CLK_1	R/W	12000000h
10001Ah	MII_RX_CLK_1	R/W	12000000h
10001Bh	RMII_REF_CLK_1	R/W	12000000h
10001Ch	RGMII_TX_CLK_1	R/W	12000000h
10001Dh	EXT_TX_CLK_1	R/W	12000000h
10001Eh	EXT_RX_CLK_1	R/W	12000000h
10001Fh	MII_TX_CLK_2	R/W	13000000h
100020h	MII_RX_CLK_2	R/W	13000000h
100021h	RMII_REF_CLK_2	R/W	13000000h
100022h	RGMII_TX_CLK_2	R/W	13000000h
100023h	EXT_TX_CLK_2	R/W	13000000h
100024h	EXT_RX_CLK_2	R/W	13000000h
100025h	MII_TX_CLK_3	R/W	14000000h
100026h	MII_RX_CLK_3	R/W	14000000h
100027h	RMII_REF_CLK_3	R/W	14000000h
100028h	RGMII_TX_CLK_3	R/W	14000000h
100029h	EXT_TX_CLK_3	R/W	14000000h
10002Ah	EXT_RX_CLK_3	R/W	14000000h
10002Bh	MII_TX_CLK_4	R/W	15000000h

Address	Name	Access	Reset Value
10002Ch	MII_RX_CLK_4	R/W	15000000h
10002Dh	RMII_REF_CLK_4	R/W	15000000h
10002Eh	RGMII_TX_CLK_4	R/W	15000000h
10002Fh	EXT_TX_CLK_4	R/W	15000000h
100030h	EXT_RX_CLK_4	R/W	15000000h

6.3.1 PLL Setup

After reset, PLL0 provides the 125 MHz clock used for the digital core, SGMII and RGMII. For RMII, PLL1 must be set to output 50 MHz by setting PSEL = 1h, MSEL = 1h and NSEL = 0h.

Table 115. PLL_x_S status registers 0 and 1 (addr. 100007h and 100009h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
31:1	reserved	R	0h	
0	LOCK	R		PLL lock indicator
			0*	not locked
			1	locked

Table 116. PLL_x_C control registers 0 and 1 (addr. 100008h and 10000Ah)

For R/W elements, reset values are indicated by ''*

Bit	Symbol	PLL_0_C		PLL_1_C		Description
		Access	Value	Access	Value	
31:29	reserved	R	0h	R	0h	
28:24	PLLCLKSRC	R	0Ah	R	0Ah	input clock selection; select XO66M_0 (CLKSRC = 0Ah) as 25 MHz source.
23:16	MSEL	R	04h	R	00h	feedback divider value; the actual value used for the divider is M = MSEL + 1
15:14	reserved	R	0h	R	0h	
13:12	NSEL	R	0h	R/W	0h*	pre-divider value; the actual value used for the divider is N = NSEL + 1
11	AUTOBLOCK	R		R/W		block clock automatically when settings are being changed to prevent glitches in the output clock:
			0		0*	disabled
			-		1	enabled
10	reserved	R	0	R	0	
9:8	PSEL	R	0h	R/W	0h*	post divider value; the actual value used for the divider is P = PSEL + 1
7	DIRECT	R	0	R	1	direct clock output control
6	FBSEL	R		R/W		PLL feedback select

Bit	Symbol	PLL_0_C		PLL_1_C		Description
		Access	Value	Access	Value	
			1		0	disabled
			-		1*	enabled
5:3	reserved	R	0h	R/W	0h*	
2	P23EN	R/W		R/W		enable additional phase outputs of PLL_x
			0*		0*	disable 120° and 240° output
			1		1	enable 120° and 240° output
1	BYPASS	R		R/W		bypass select
			0		0	disabled
			-		1*	enabled
0	PD	R		R/W		power down select
			0		0	enabled
			-		1*	disabled

6.3.2 Clock Dividers

Table 117. IDIV_x_C control registers (address 10000Bh to 10000Fh)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
31:29	Reserved	R/W	0h	
28:24	CLKSRC	R/W		internal clock selection:[1]
			00h..09h	reserved
			0Ah*	XO66M_0
			0B..0Fh	reserved
23:12	reserved	R/W	0h	
11	AUTOBLOCK	R/W		block output clock automatically when frequency is changing to prevent glitches:
			0*	disabled
			1	enabled (recommended when clock source is being changed)
10	reserved	R/W	0h	
9:2	IDIV	R/W	0h*	divide by (1 + IDIV)
1	reserved	R	0	
0	PD	R/W		IDIVx clock power down and disable output
			0*	IDIVx clock enabled
			1	IDIVx clock disabled

[1] Invalid values are ignored and the existing values are retained.

6.3.3 Clock Sinks

Table 118. MIIx clock control registers (address 100013h to 100030h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
31:29	Reserved	R/W	0h	
28:24	CLKSRC	R/W		internal clock selection:[1]
			00h	TX_CLK_0
			01h	RX_CLK_0
			02h	TX_CLK_1
			03h	RX_CLK_1
			04h	TX_CLK_2
			05h	RX_CLK_2
			06h	TX_CLK_3
			07h	RX_CLK_3
			08h	TX_CLK_4
			09h	RX_CLK_4
			0Ah	XO66M_0
			0Bh	PLL0
			0Ch	PLL0_120
			0Dh	PLL0_240
			0Eh	PLL1
			0Fh	PLL1_120
			10h	PLL1_240
			11h	IDIV0
			12h	IDIV1
			13h	IDIV2
			14h	IDIV3
			15h	IDIV4
23:12	reserved	R/W	0h	
11	AUTOBLOCK	R/W		Block output clock automatically when frequency is changing to prevent glitches:
			0*	disabled
			1	enabled (recommended when clock source is being changed)
10:1	reserved	R/W	0h	
0	PD	R/W		MIIx clock power down and disable output
			0*	MIIx clock enabled
			1	MIIx clock disabled

[1] Invalid values are ignored and the existing values are retained.

Table 119. Clock selection matrix

'd' indicates the reset value; 'a' indicates alternative clock sources; all other values are invalid

	Clock Selection (via CLKSRC)																			
CLKSRC value	**00h**	**01h**	**02h**	**03h**	**04h**	**05h**	**06h**	**07h**	**08h**	**09h**	**0Ah**	**0Bh**	**0Ch**	**0Dh**	**0Eh**	**0Fh**	**10h**	**11h**	**12h**	**13h**	**14h**	**15h**
Internal Clock	**TX_CLK_0**	**RX_CLK_0**	**TX_CLK_1**	**RX_CLK_1**	**TX_CLK_2**	**RX_CLK_2**	**TX_CLK_3**	**RX_CLK_3**	**TX_CLK_4**	**RX_CLK_4**	**XO66M_0**	**PLL0**	**PLL0_120**	**PLL0_240**	**PLL1**	**PLL1_120**	**PLL1_240**	**IDIV0**	**IDIV1**	**IDIV2**	**IDIV3**	**IDIV4**
MII_TX_CLK_0	a																	d				
MII_RX_CLK_0		a																d				
RMII_REF_CLK_0	a																	d				
RGMII_TX_CLK_0												a	a	a				d				
EXT_TX_CLK_0															a	a	a	d				
EXT_RX_CLK_0																		d				
MII_TX_CLK_1			a																d			
MII_RX_CLK_1				a															d			
RMII_REF_CLK_1			a																d			
RGMII_TX_CLK_1												a	a	a					d			
EXT_TX_CLK_1															a	a	a		d			
EXT_RX_CLK_1																			d			
MII_TX_CLK_2					a															d		
MII_RX_CLK_2						a														d		
RMII_REF_CLK_2					a															d		
RGMII_TX_CLK_2												a	a	a						d		
EXT_TX_CLK_2															a	a	a			d		

	Clock Selection (via CLKSRC)																			
CLKSRC value	**00h**	**01h**	**02h**	**03h**	**04h**	**05h**	**06h**	**07h**	**08h**	**09h**	**0Ah**	**0Bh**	**0Ch**	**0Dh**	**0Eh**	**0Fh**	**10h**	**11h**	**12h**	**13h**	**14h**	**15h**
Internal Clock	**TX_CLK_0**	**RX_CLK_0**	**TX_CLK_1**	**RX_CLK_1**	**TX_CLK_2**	**RX_CLK_2**	**TX_CLK_3**	**RX_CLK_3**	**TX_CLK_4**	**RX_CLK_4**	**XO66M_0**	**PLL0**	**PLL0_120**	**PLL0_240**	**PLL1**	**PLL1_120**	**PLL1_240**	**IDIV0**	**IDIV1**	**IDIV2**	**IDIV3**	**IDIV4**
EXT_RX_CLK_2																				d		
MII_TX_CLK_3							a														d	
MII_RX_CLK_3								a													d	
RMII_REF_CLK_3							a														d	
RGMII_TX_CLK_3												a	a	a							d	
EXT_TX_CLK_3															a	a	a				d	
EXT_RX_CLK_3																					d	
MII_TX_CLK_4									a													d
MII_RX_CLK_4										a												d
RMII_REF_CLK_4									a													d
RGMII_TX_CLK_4												a	a	a								d
EXT_TX_CLK_4															a	a	a					d
EXT_RX_CLK_4																						d

6.4 Auxiliary Configuration Unit (ACU)

The auxiliary configuration unit (ACU) controls the I/O characteristics and provides auxiliary functionality.

Table 120. Register overview

Address	Name	Access	Reset Value
100800h	CFG_PAD_MII0_TX	R/W	12121212h
100801h	CFG_PAD_MII0_RX	R/W	02020212h
100802h	CFG_PAD_MII1_TX	R/W	12121212h
100803h	CFG_PAD_MII1_RX	R/W	02020212h
100804h	CFG_PAD_MII2_TX	R/W	12121212h
100805h	CFG_PAD_MII2_RX	R/W	02020212h
100806h	CFG_PAD_MII3_TX	R/W	12121212h
100807h	CFG_PAD_MII3_RX	R/W	02020212h
100808h	CFG_PAD_MII4_TX	R/W	12121212h
100809h	CFG_PAD_MII4_RX	R/W	02020212h
100810h	CFG_PAD_MII0_ID	R/W	00002323h
100811h	CFG_PAD_MII1_ID	R/W	00002323h
100812h	CFG_PAD_MII2_ID	R/W	00002323h
100813h	CFG_PAD_MII3_ID	R/W	00002323h
100814h	CFG_PAD_MII4_ID	R/W	00002323h
100840h	CFG_PAD_MISC	R/W	00120412h
100880h	CFG_PAD_SPI	R/W	12040407h
100881h	CFG_PAD_JTAG	R/W	02000000h
100900h	PORT_STATUS_MII0	R	0031311Fh
100901h	PORT_STATUS_MII1	R	0031311Fh
100902h	PORT_STATUS_MII2	R	0031311Fh
100903h	PORT_STATUS_MII3	R	0031311Fh
100904h	PORT_STATUS_MII4	R	0031311Fh
100A00h	TS_CONFIG	R/W	00000065h
100A01h	TS_STATUS	R	00000000h
100BC0h	PROD_CFG	R	-
100BC3h	PROD_ID	R	-
100BFDh	UNIT_DISABLE	R/W	00000000h

6.4.1 Pad configuration registers

Table 121. Registers CFG_PAD_MIIx_TX

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
31:29	reserved	R	0	
28:27	D32_ OS	R/W		Pad output stage speed selection. Pins TXD2, TXD3
			0h	Very low noise / Low Speed
			1h	Low noise / Medium Speed
			2h*	Medium noise / Fast Speed
			3h	High Noise / High Speed
26	reserved	R	0	Reserved
25:24	D32_IPUD	R/W		Pad input stage (weak) pull-up/-down selection. Pins TXD2, TXD3
			0h	Pull-up
			1h	Repeater
			2h*	Plain input
			3h	Pull-down
23:21	reserved	R	0	Reserved
20:19	D10_ OS	R/W		Pad output stage speed selection. Pins TXD1, TXD0
			0h	Very low noise / Low Speed
			1h	Low noise / Medium Speed
			2h*	Medium noise / Fast Speed
			3h	High Noise / High Speed
18	reserved	R	0	Reserved
17:16	D10_IPUD	R/W		Pad input stage (weak) pull-up/-down selection Pins TXD1, TXD0
			0h	Pull-up
			1h	Repeater
			2h*	Plain input
			3h	Pull-down
15:13	reserved	R	0	Reserved
12:11	CTRL_ OS	R/W		Pad output stage speed selection. Pins TX_EN, TX_ER
			0h	Very low noise / Low Speed
			1h	Low noise / Medium Speed
			2h*	Medium noise / Fast Speed
			3h	High Noise / High Speed

Bit	Symbol	Access	Value	Description
10	reserved	R	0	Reserved
9:8	CTRL_IPUD	R/W		Pad input stage (weak) pull-up/-down selection Pins TX_EN, TX_ER
			0h	Pull-up
			1h	Repeater
			2h*	Plain input
			3h	Pull-down
7:5	reserved	R	0	Reserved
4:3	CLK_ OS	R/W		Pad output stage speed selection. Pins TX_CLK
			0h	Very low noise / Low Speed
			1h	Low noise / Medium Speed
			2h*	Medium noise / Fast Speed
			3h	High Noise / High Speed
2	CLK_IH	R/W		Pad input stage hysteresis selection Pins TX_CLK
			0*	non Schmitt
			1	Schmitt
1:0	CLK_IPUD	R/W		Pad input stage (weak) pull-up/-down selection Pins TX_CLK
			0h	Pull-up
			1h	Repeater
			2h*	Plain input
			3h	Pull-down

Table 122. Registers CFG_PAD_MIIx_RX

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
31:27	reserved	R	0h	
26	D32_IH	R/W		Pad input stage hysteresis selection Pins RXD3, RXD2
			0*	non Schmitt
			1	Schmitt
25:24	D32_IPUD	R/W		Pad input stage (weak) pull-up/-down selection Pins RXD3, RXD2
			0h	Pull-up
			1h	Repeater
			2h*	Plain input

Bit	Symbol	Access	Value	Description
			3h	Pull-down
23:19	reserved	R	0h	
18	D10_IH	R/W		Pad input stage hysteresis selection Pins RXD1, RXD0
			0*	non Schmitt
			1	Schmitt
17:16	D10_IPUD	R/W		Pad input stage (weak) pull-up/-down selection Pins RXD1, RXD0
			0h	Pull-up
			1h	Repeater
			2h*	Plain input
			3h	Pull-down
15:11	reserved	R	00	Reserved
10	CTRL_IH	R/W		Pad input stage hysteresis selection Pins RX_DV, RX_ER
			0*	non Schmitt
			1	Schmitt
9:8	CTRL_IPUD	R/W		Pad input stage (weak) pull-up/-down selection Pins RX_DV, RX_ER
			0h	Pull-up
			1h	Repeater
			2h*	Plain input
			3h	Pull-down
7:5	reserved	R	0	Reserved
4:3	CLK_ OS	R/W		Pad output stage speed selection. Pins RX_CLK
			0h	Very low noise / Low Speed
			1h	Low noise / Medium Speed
			2h*	Medium noise / Fast Speed
			3h	High Noise / High Speed
2	CLK_IH	R/W		Pad input stage hysteresis selection
			0*	non Schmitt
			1	Schmitt
1:0	CLK_IPUD	R/W		Pad input stage (weak) pull-up/-down selection
			0h	Pull-up
			1h	Repeater
			2h*	Plain input
			3h	Pull-down

Table 123. Registers CFG_PAD_MIIx_ID

Bit	Symbol	Access	Value	Description
31:16	reserved	R	0h	
15	RXC_STABLE_OVR	R/W	0	RXC Internal Delay stability detection override
14:10	RXC_DELAY	R/W	8h	RXC Internal Delay value (8h == 81°) The delay in degree phase is 73.8° + delay_tune×0.9°
9	RXC_BYPASS	R/W	1	RXC Internal Delay bypass (when set) **Note**: The Tunable Delay Line (TDL) expects a stable RXC clock. In case the frequency has changed (e.g. during auto-negotiation), the TDL must be temporarily disabled by setting RXC_BYPASS=1. RXC must be stable when RXC_BYPASS is deasserted.
8	RXC_PD	R/W	1	RXC Internal Delay power-down (when set)
7	TXC_STABLE_OVR	R/W	0	TXC Internal Delay stability detection override
6:2	TXC_DELAY	R/W	8h	TXC Internal Delay value (8h == 81°) The delay in degree phase is 73.8° + delay_tune×0.9°
1	TXC_BYPASS	R/W	1	TXC Internal Delay bypass (when set) **Note**: The TDL expects a stable TXC clock. In case the frequency needs to be changed (e.g. CGU settings where changed), the TDL must be temporarily disabled by setting TXC_BYPASS=1.
0	TXC_PD	R/W	1	TXC Internal Delay power-down (when set)

Table 124. Register CFG_PAD_MISC (address 100840h)

Bit	Symbol	Access	Value	Description
31:24	reserved	R	0	Reserved
23:21	reserved	R	0	Reserved
20:19	PTPCLK_OS	R/W		Pad output stage speed selection:
			0h	Very low noise / Low Speed
			1h	Low noise / Medium Speed
			2h*	Medium noise / Fast Speed
			3h	High Noise / High Speed
18	PTPCLK_IH	R/W		Pad input stage hysteresis selection
			0*	non Schmitt
			1	Schmitt
17:16	PTPCLK_ IPUD	R/W		Pad input stage (weak) pull-up/-down selection
			0h	Pull-up
			1h	Repeater
			2h*	Plain input
			3h	Pull-down

Bit	Symbol	Access	Value	Description
15:13	reserved	R	0	Reserved
12:11	reserved	R	0	Reserved
10	RSTN_IH	R/W		Pad input stage hysteresis selection:
			0	non Schmitt
			1*	Schmitt
9:8	RSTN_ IPUD	R/W		Pad input stage (weak) pull-up/-down selection
			0h	Pull-up
			1h	Repeater
			2h*	Plain input
			3h	Pull-down
7:6	reserved	R	0	Reserved
5	CLKOUT_EN	R/W		Pad output stage enable (active low):
			0*	Enabled
			1	Disabled
4:3	CLKOUT_OS	R/W		Pad output stage speed selection:
			0h	Very low noise / Low Speed
			1h	Low noise / Medium Speed
			2h*	Medium noise / Fast Speed
			3h	High Noise / High Speed
2	reserved	R	0	Reserved
1:0	CLKOUT_ IPUD	R/W		Pad input stage (weak) pull-up/-down selection
			0h	Pull-up
			1h	Repeater
			2h*	Plain input
			3h	Pull-down

Table 125. Registers CFG_PAD_SPI (address 100880h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
31:29	reserved	R	0	
28:27	SDO_ OS	R/W		Pad output stage speed selection:
			0h	Very low noise / Low Speed
			1h	Low noise / Medium Speed
			2h*	Medium noise / Fast Speed
			3h	High Noise / High Speed
26	reserved	R	0	Reserved

Bit	Symbol	Access	Value	Description
25:24	SDO _IPUD	R/W		Pad input stage (weak) pull-up/-down selection
			0h	Pull-up
			1h	Repeater
			2h*	Plain input
			3h	Pull-down
23:19	reserved	R	0	Reserved
18	SDI_IH	R/W		Pad input stage hysteresis selection:
			0	non Schmitt
			1*	Schmitt
17:16	SDI_ IPUD	R/W		Pad input stage (weak) pull-up/-down selection
			0h*	Pull-up
			1h	Repeater
			2h	Plain input
			3h	Pull-down
15:11	reserved	R	0h	
10	SSN_IH	R/W		Pad input stage hysteresis selection:
			0	non Schmitt
			1*	Schmitt
9:8	SSN_ IPUD	R/W		Pad input stage (weak) pull-up/-down selection
			0h*	Pull-up
			1h	Repeater
			2h	Plain input
			3h	Pull-down
7:3	reserved	R	0h	
2	SCK_IH	R/W		Pad input stage hysteresis selection:
			0	non Schmitt
			1*	Schmitt
1:0	SCK_ IPUD	R/W		Pad input stage (weak) pull-up/-down selection
			0h	Pull-up
			1h	Repeater
			2h	Plain input
			3h*	Pull-down

Table 126. Registers CFG_PAD_JTAG (address 100881h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
31:26	reserved	R	0	
25:24	TDO_ IPUD	R/W		Pad input stage (weak) pull-up/-down selection
			0h	Pull-up
			1h	Repeater
			2h*	Plain input
			3h	Pull-down
23:18	reserved	R	0	
17:16	TDI_ IPUD	R/W		Pad input stage (weak) pull-up/-down selection
			0h*	Pull-up
			1h	Repeater
			2h	Plain input
			3h	Pull-down
15:10	reserved	R	0	
9:8	TRSTNTMS_ IPUD	R/W		Pad input stage (weak) pull-up/-down selection
			0h*	Pull-up
			1h	Repeater
			2h	Plain input
			3h	Pull-down
7:2	reserved	R	0	
1:0	TCK_ IPUD	R/W		Pad input stage (weak) pull-up/-down selection
			0h*	Pull-up
			1h	Repeater
			2h	Plain input
			3h	Pull-down

6.4.2 Port status registers

Table 127. Registers PORT_STATUS_MIIx (address 100900h to 100904h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
31:22	reserved	R	0	
21:20	RXC_ID_FREQ_MODE	R	11b	RXC Internal Delay frequency mode selected: 00b: 2.5MHz 01b: 25MHz 10b: 50MHz 11b: 125MHz

Bit	Symbol	Access	Value	Description
19:18	RXC_ID_CTL_MODE	R	00b	RXC Internal Delay operating mode: 00b: bypass mode 01b: delayed clock 1xb: output clock disabled
17	RXC_ID_STABLE	R	0	RXC Internal Delay started-up
16	RXC_ID_PD	R	1	RXC Internal Delay power-down (when set)
15:14	reserved	R	0	
13:12	TXC_ID_FREQ_MODE	R	11b	TXC Internal Delay frequency mode selected: 00b: 2.5MHz 01b: 25MHz 10b: 50MHz 11b: 125MHz
11:10	TXC_ID_CTL_MODE	R	00b	TXC Internal Delay operating mode: 00b: bypass mode 01b: delayed clock 1xb: output clock disabled
9	TXC_ID_STABLE	R	0	TXC Internal Delay started-up
8	TXC_ID_PD	R	1	TXC Internal Delay power-down (when set)
7:5	reserved	R	0	
4:3	SPEED	R	11b	Port speed setting: 00b: 10Mbit/s 01b: 100Mbits/s 1xb: 1Gbit/s
2:0	MODE	R	111b	Port mode setting: 000b: MII MAC mode 001b: RMII MAC mode 100b: MII PHY mode 101b: RMII PHY mode -10b: RGMII 011b: SGMII (only SJA1105 R/S, otherwise inactive) 111b: Inactive

6.4.3 Temperature Sensor

Table 128. Registers TS_CONFIG (address 100A00h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
31:7	reserved	R	0h	Reserved
6	PD	R/W	1*	Power down control: 0: Active 1: Power-down
5:0	THRESHOLD	R/W	25h*	Temperature threshold selection

Table 129. Registers TS_STATUS (address 100A01h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
31:1	reserved	R	0	Reserved
0	EXCEEDED	R	0	Temperature detection status: 0: Below threshold 1: Above threshold

Table 130. Temperature threshold selection (selected via bits THRESHOLD)

Reset values are indicated by ''*

Bit Value	Temp (°C)	Bit Value	Temp (°C)	Bit Value	Temp (°C)	Bit Value	Temp (°C)	Bit Value	Temp (°C)
000000	invalid	001000	−11.4	010000	+25.6	011000	+63.3	100000	+102.5
000001	−45.7	001001	−6.1	010001	+30.9	011001	+67.9	100001	+106.9
000010	−41.7	001010	−2.1	010010	+36.4	011010	+72.6	100010	+111.4
000011	−37.5	001011	+2.1	010011	+42.0	011011	+77.4	100011	+116.0
000100	−33	001100	+6.5	010100	+46.1	011100	+82.4	100100	+120.7
000101	−28.4	001101	+11.0	010101	+50.2	011101	+87.5	100101*	+125.5
000110	−23.5	001110	+15.7	010110	+54.5	011110	+92.8	100110	+130.5
000111	−18.3	001111	+20.6	010111	+58.8	011111	+98.2	100111	+135.5

6.4.4 Other ACU registers

Table 131. PROD_CFG register (address 100BC0h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
31:1	reserved	R	0h	Reserved
0	DISABLE_TTETH	R		When asserted, time-triggered Ethernet features are disabled.

Table 132. PROD_ID register (address 100BC3h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
31:20	reserved	R	0h	reserved
19:4	PART_NR	R		9A84h: SJA1105P device configuration 9A85h: SJA1105Q device configuration 9A86h: SJA1105R device configuration 9A87h: SJA1105S device configuration
3:0	VERSION	R	1h	version number

Table 133. Unit disable register for ACU (addr. 100BFDh)

Bit	Symbol	Access	Value	Description
31:1	reserved	R	0h	
0	DISABLE_FLAG	R/W	0	When this bit is set to 1, access to all registers of this unit (except for this register) is inhibited.

6.5 SGMII Configuration (SGMII)

SJA1105R and SJA1105S only

SR: Standard Register

VR: Vendor-specific Register

Table 134. SGMII Register overview

Legend: SR - Standard Register, VR - Vendor-specific Register

Address	Name	Access	Reset Value	Group
1F0000h	BASIC_CONTROL	R/W	1140h	SR
1F0001h	BASIC_STATUS	R	0189h	SR
1F0002h	PHY_IDENTIFIER_1	R	B018h	SR
1F0003h	PHY_IDENTIFIER_2	R	02D0h	SR
1F0004h	AUTONEG_ADV	R/W	0020h	SR
1F0005h	AUTONEG_LP_BABL	R	0000h	SR
1F0006h	AUTONEG_EXPN	R	0000h	SR
1F000Fh	EXTENDED_STATUS	R	C000h	SR
1F8000h	DIGITAL_CONTROL_1	R/W	2400h	VR
1F8001h	AUTONEG_CONTROL	R/W	0000h	VR
1F8002h	AUTONEG_INTR_STATUS	R/W	000Ah	VR
1F8003h	TEST_CONTROL	R/W	0000h	VR
1F8005h	DEBUG_CONTROL	R/W	0000h	VR
1F8010h	DIGITAL_STATUS	R	0010h	VR
1F8011h	ICG_ERROR_CNT	R	0000h	VR
1F8030h	TX_BOOST_CONTROL	R/W	000Ah	VR
1F8031h	TX_ATTN_CONTROL	R/W	0000h	VR
1F8033h	TX_EDGE_CONTROL	R/W	0000h	VR
1F8051h	RX_EQ_CONTROL	R/W	0005h	VR
1F8090h	LEVEL_CONTROL	R/W	0230h	VR
1F80E1h	DIGITAL_CONTROL_2	R/W	0000h	VR
1F80E2h	DIGITAL_ERROR_CNT	R/W	0000h	VR

6.5.1 Standard registers

Table 135. BASIC_CONTROL register (address 1F0000h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
15	RESET	R/W		software reset process in which all internal blocks are reset, except the Management Interface block
			0*	reset complete (TX/RX clocks stable)
			1	trigger reset
14	LOOPBACK	R/W		Loopback of TX lanes back to the RX lanes
			0*	Loopback disabled
			1	Loopback enabled
13	SPEED_SELECT (LSB)	R/W		Speed selection. This bit forms the complete value together with bit 6.
			11	Reserved
			10*	1 Gbit/s
			01	100 Mbit/s
			00	10 Mbit/s
12	AUTONEG_ENABLE	R/W		Enables the Clause 37 auto-negotiation process.
			0	Auto-negotiation disabled
			1*	Auto-negotiation enabled
11	POWER_DOWN	R/W		SGMII power-down mode
			0*	Normal operation
			1	Power-down mode
10	reserved	R	0	
9	RE_AUTONEG	R/W		Restart Auto-negotiation; bit is cleared after restarting
			0*	No change
			1	Auto-negotiation process is initiated
8	DUPLEX_MODE	R/W		Duplex mode (only for AUTONEG_ENABLE = 0)
			0	Half duplex
			1*	Full duplex
7	reserved	R	0	
6	SPEED_SELECT (MSB)	R/W		See Bit 13 SPEED_SELECT (LSB)
5:0	reserved	R	0	

Table 136. BASIC_STATUS register (address 1F0001h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
15	100BASE-T4	R	0	Not able to perform 100BASE-T4

Bit	Symbol	Access	Value	Description
14	100BASE-X_FD Duplex	R	0	Not able to perform 100BASE-X Full Duplex
13	100BASE-X_HD	R	0	Not able to perform 100BASE-X Half Duplex
12	10MBPS_FD	R	0	Not able to perform 10 Mbit/s Full Duplex
11	10MBPS_HD	R	0	Not able to perform 10 Mbit/s Half Duplex
10	100BASE-T2_FD	R	0	Not able to perform 100BASE-T2 Full Duplex
9	100BASE-T2_HD	R	0	Not able to perform 100BASE-T2 Half Duplex
8	EXTENDED_STATUS	R	1	Extended status information available in Table 142
7	UN_DIR_ABL	R	1	PHY able to transmit from MII regardless of whether the PHY has determined that a valid link has been established
6	MF_PRE_SUP	R	0	PHY will not accept management frames with preamble suppressed
5	AUTONEG_CMPL	R		Auto-negotiation complete
			0*	The AN process is not complete
			1	The AN process is complete
4	REMOTE_FAULT	R		Remote fault Feature is not supported for SGMII
			0*	No remote fault detected
			1	Remote fault detected
3	AUTONEG_ABL	R	1	Able to perform auto-negotiation
2	LINK_STATUS	R		RX Link status
			0*	Link is down
			1	Link is up
1	reserved	R	0	
0	EXTENDED_REG	R	1	Extended register capabilities available

Table 137. PHY_IDENTIFIER_1 register (address 1F0002h)

Bit	Symbol	Access	Value	Description
15:0	PHY_ID	R	B018h	Bits 3 to 18 of Organizationally Unique IDentifier (OUI) 2C-06-00

Table 138. PHY_IDENTIFIER_2 register (address 1F0003h)

Bit	Symbol	Access	Value	Description
15:10	PHY_ID	R	00h	Bits 19 to 24 of Organizationally Unique Identifier (OUI) 2C-06-00
9:4	TYPE_NO	R	2Dh	Six-bit manufacturer type number
3:0	REVISION_NO	R	0	Four-bit manufacturer revision number

Table 139. AUTONEG_ADV register (address 1F0004h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
15	NEXT_PAGE	R	0	Next page feature is not supported for SGMII
14	reserved	R	0	
13:12	REMOTE_FAULT	R/W		This field indicates the fault signaling of the local device to be communicated to the link partner. Feature is not supported for SGMII
			00*	No Error
			01	Offline
			10	Link Failure
			11	Auto-negotiation Error
11:9	reserved	R	0	
7:8	PAUSE	R/W		Pause ability Feature is not supported for SGMII
			00*	No Pause
			01	Asymmetric Pause toward the link partner
			10	Symmetric Pause
			11	Symmetric Pause and Asymmetric Pause toward the local device
6	HALF_DUPLEX	R/W		Half-duplex mode advertisement Feature is not supported for SGMII
			0*	Half-duplex mode not advertised
			1	Half-duplex mode advertised
5	FULL_DUPLEX	R/W		Full-duplex mode advertisement; note that the switch only supports full duplex
			0	Full-duplex mode not advertised
			1*	Full-duplex mode advertised
4:0	reserved	R	0	

Table 140. AUTONEG_LP_BABL register (address 1F0005h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
15	NEXT_PAGE	R	0	Next page feature is not supported
14	ACK	R		ACK bit from the Link Partner
			0*	Link partner has not yet received the page sent by the local device
			1	Link partner has successfully received the page sent by the local device
13:12	REMOTE_FAULT	R		Fault signaling of the link partner Feature is not supported for SGMII

Bit	Symbol	Access	Value	Description
			00*	No Error
			01	Offline
			10	Link Failure
			11	Auto-negotiation Error
11:9	reserved	R	0	
7:8	PAUSE	R		Link partner Pause ability Feature is not supported for SGMII
			00*	No Pause
			01	Asymmetric Pause toward the link partner
			10	Symmetric Pause
			11	Symmetric Pause and Asymmetric Pause toward the local device
6	HALF_DUPLEX	R		Link partner half-duplex capability Feature is not supported for SGMII
			0*	Link partner is half-duplex capable
			1	Link partner is not half-duplex capable
5	FULL_DUPLEX	R		Link partner full-duplex capability
			0*	Link partner is full-duplex capable
			1	Link partner is not full-duplex capable
4:0	reserved	R	0	

Table 141. AUTONEG_EXPN register (address 1F0006h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
15:3	reserved	R	0	
2	NEXT_PAGE_ABL	R	0	Next page feature is not supported
1	PAGE_RECVD	R		This bit indicates that the local device received a page from the link partner
			0*	Local device did not receive a new page
			1	Local device received a new page
0	reserved	R	0	

Table 142. EXTENDED_STATUS register (address 1F000Fh)

Bit	Symbol	Access	Value	Description
15	1000BASE-X_FD	R	1	Can perform 1000BASE-X full duplex
14	1000BASE-X_HD	R	1	Can perform 1000BASE-X half-duplex
13	1000BASE-T_FD	R	0	Unable to perform 1000BASE-T full duplex

Bit	Symbol	Access	Value	Description
12	1000BASE-T_HD	R	0	Unable to perform 1000BASE-T half-duplex
11:0	reserved	R		

6.5.2 Vendor-specific registers

Table 143. DIGITAL_CONTROL_1 register (address 1F8000h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
15	VS_RESET	R/W		Vendor-specific software reset process in which all internal blocks are reset, except the Management Interface block and the CSR block
			0*	Reset complete (TX/RX clocks stable)
			1	Trigger reset
14	REMOTE_LOOPBACK	R/W		Loopback on the internal GMII port from RX to TX
			0*	Loopback disabled
			1	Loopback enabled
13	EN_VSMMD1	R/W		Enable Vendor-Specific MMD1
			0	VSMMD1 disabled
			1*	VSMMD1 enabled
12	reserved	R	0	
11	POWER_SAVE	R/W		Triggers the power-down mode by turning off the PHY Receiver and Transmitter, and without turning off MPLL
			0*	Normal operation
			1	Power save mode
10	CLOCK_STOP_EN	R/W		Clock stop enable
			0	The clock cannot be stopped during LPI mode
			1*	The PHY may stop the clock during LPI mode
9	MAC_AUTO_SW	R/W		Auto speed mode change after auto-negotiation (only in MAC mode) Note: the speed setting of the switch core must be manually adjusted (MAC Configuration Table)
			0*	After completion of auto-negotiation, speed has to switched through SW action
			1	After completion of auto-negotiation, speed is switched autonomously
8	INIT	R/W		Datapath initialization control
			0*	Normal operation/init. complete
			1	Flush/initialize the internal FIFOs
7:5	reserved	R	0	
4	TX_DISABLE	R/W		TX lane disable
			0	TX lane of PHY enabled

Bit	Symbol	Access	Value	Description
			1	TX lane of PHY disabled
3	AUTONEG_TIMER_OVRR	R/W		Override auto-negotiation timer
			0*	Use default value
			1	Override the default value
2	reserved	R/W	0	Do not overwrite with 1
1	BYP_POWERUP	R/W		Bypass power-up sequence
			0*	Normal power-up sequence
			1	Bypasses the normal flow of the power-up sequence. Will not wait for MPLL and TX or RX PLL
0	PHY_MODE_CONTROL	R/W		SGMII PHY mode control (only in PHY mode, PHY_MODE=1) Controls the source of the capabilities that are advertised
			0*	Config_Reg for Clause 37 auto-negotiation will be derived from the SGMII core as follows: Config_Reg[15] = SGMII_LINK, AUTONEG_CONTROL Config_Reg[12] = FULL_DUPLEX, AUTONEG_ADV Config_Reg[11:10] = SPEED_SELECT, BASIC_CONTROL
			1	Config_Reg for Clause 37 auto-negotiation will be derived from the switch core as follows: Config_Reg[15] = 1, if xMII Mode for port 4 is SGMII Config_Reg[12] = 1 Config_Reg[11:10] = SPEED according to MAC Configuration Table

Table 144. AUTONEG_CONTROL register (address 1F8001h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
15:9	reserved	R	0	
8	MII_CONTROL	R/W		Width of the MAC interface when the current SGMII speed mode is 10 Mbit/s or 100 Mbit/s
			0*	4-bit MII
			1	8-bit MII
7:5	reserved	R	0	
4	SGMII_LINK	R/W		SGMII Link Status: See PHY_MODE_CONTROL
			0*	Link is down
			1	Link is up
3	PHY_MODE	R/W		Transmit Configuration
			0*	MAC mode
			1	PHY mode
2:1	AUTONEG_MODE	R/W		Auto-negotiation mode

Bit	Symbol	Access	Value	Description
			00*	Clause 37 auto-negotiation for 1000BASE-X mode Not supported
			10	Clause 37 auto-negotiation for SGMII mode
			X1	reserved
0	reserved	R	0	

Table 145. AUTONEG_INTR_STATUS register (address 1F8002h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
15:5	reserved	R	0	
4	LINK_STATUS	R		Link status after auto-negotiation; only valid for AUTONEG_MODE = 10
			0*	Link down
			1	Link up
3:2	SPEED	R		Link speed after auto-negotiation; only valid for AUTONEG_MODE = 10
			00	10 Mbit/s
			01	100 Mbit/s
			10*	1 Gbit/s
			11	reserved
1	DUPLEX_MODE	R		Duplex mode after auto-negotiation; only valid for AUTONEG_MODE = 10
			0	Half Duplex
			1*	Full Duplex
0	COMPLETE	R/W		The bit is set upon completion of clause 37 auto-negotiation. The host must clear this bit by writing 0 to it.
			0*	Auto-negotiation not complete
			1	Auto-negotiation complete

Table 146. TEST_CONTROL register (address 1F8003h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
15:3	reserved	R	0	
2	TP_ENABLE	R/W		Test pattern enable
			0*	Test pattern disabled
			1	Test pattern will be enabled in the TX path after the current normal frame transmission is complete

Bit	Symbol	Access	Value	Description
1:0	TP_SELECT	R/W		Test pattern select; test pattern definitions are specified in IEEE Std 802.3ae, Annex 48A
			00*	High frequency test pattern
			01	Low frequency test pattern
			10	Mixed frequency test pattern
			11	Reserved

Table 147. DEBUG_CONTROL register (address 1F8005h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
15:5	reserved	R	0	
4	SUPRESS_LOS	R/W		Suppress loss of signal detection
			0*	Loss of signal will be considered for the receive link status
			1	Loss of signal will be ignored for the receive link status
3:1	reserved	R	0	
0	RESTART_SYNC	R/W		Restart Synchronization
			0*	The host must clear this bit to 0 before setting it to 1 next time to restart synchronization
			1	restarts the RX synchronization state machine

Table 148. DIGITAL_STATUS register (address 1F8010h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
15:7	reserved	R	0	
6	RXFIFO_OVF	R		RX clock rate compensation FIFO overflow
			0*	Normal operation
			1	overflow
5	RXFIFO_UNDF	R		RX clock rate compensation FIFO underflow
			0*	Normal operation
			1	FIFO underflow
4:2	PSEQ_STATE	R		Power up sequence state
			000	Wait for MPLL ON
			001	Wait for TXCLK
			010	Wait for RXCLK
			011	Wait for RX DPLL lock
			100*	Tx/RX Stable (Power_Good state)
			101	Wait for Tx/RX down (MPLL still ON)

Bit	Symbol	Access	Value	Description
			110	Wait for MPLL OFF
			111	MPLL OFF
1	LOOPBACK	R		Loopback active
			0*	Loopback disabled
			1	Loopback enabled
0	reserved	R	0	

Table 149. ICG_ERROR_CNT register (address 1F8011h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0	
7:0	ERROR_CNT	R	0*	Invalid code group count

Table 150. TX_BOOST_CONTROL register (address 1F8030h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
15:4	reserved	R	0	
3:0	TX_BOOST	R/W	Ah*	TX Boost control: if 0h: boost = 0 dB, else: $\text{boost} = -20 \times \log\left(1 - \frac{\text{TX\_BOOST}+0.5}{32}\right)\ \text{dB}$ *boost* can also be expressed as a factor: $\text{boost\_factor} = 1 - \frac{\text{TX\_BOOST}+0.5}{32}$ Note: for SGMII, TX Boost must be disabled by setting TX_BOOST to 0h.

Table 151. TX_ATTN_CONTROL register (address 1F8031h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
15:3	reserved	R	0	

Bit	Symbol	Access	Value	Description
2:0	TX_ATTN	R/W	0h*	Attenuation of the transmitter driver. Provides a selection of discrete factors for *attn_factor* b000: 16/16 b001: 14/16 b010: 12/16 b011: 10/16 b100: 9/16 b101: 8/16 b11x: reserved Attenuating the drive level does not use less power than using the non-attenuated (16/16) drive level. Changes while the transmitter is on might briefly cause unwanted transmit waveforms. See register LEVEL_CONTROL for the resulting differential amplitude.

Table 152. TX_EDGE_CONTROL register (address 1F8033h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	
1:0	TX_EDGERATE	R/W		TX Edge Rate
			00*	fast edge rate
			01	medium edge rate
			10	slow edge rate
			11	reserved

Table 153. RX_EQ_CONTROL register (address 1F8051h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	
2:0	RX_EQ_VAL	R/W	5h	RX Equalization Control. This field controls the internal linear equalizer boost. Note: must be set to 0h for SGMII operation.

Table 154. LEVEL_CONTROL register (address 1F8090h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
15:10	reserved	R	0	

Bit	Symbol	Access	Value	Description
9:5	LOS_LVL	R/W	11h*	Loss-of-Signal Level Control This field is used to control the loss-of-signal (LOS) detection threshold. The threshold is set by: $V_{\text{thresh}} = 1.21 \times \frac{(\text{LOS\_LVL}+1)}{(32\times16)}\ [V_{\text{dif}}]$ The Peak Level at which LOS is asserted is between the programmed threshold + 2 mV and the programmed threshold + 55 mV.
4:0	TX_LVL	R/W	1Fh*	TX Level Control This field is used to set the transmitter output level $\lvert V_{OD}\rvert$. The resulting differential output voltage at pins SGMII_TXN, SGMII_TXP is: $V_{\text{PP}} = \text{boost\_factor} \times \text{attn\_factor} \times \text{tx\_output}$ *boost_factor*: see TX_BOOST (Table 150) *attn_factor*: see TX_ATTN (Table 151) The raw differential amplitude before attenuation and boost is given by: $\lvert V_{\text{OD}}\rvert = 1.24 \times \frac{\left(48+\frac{\text{tx}_{\text{level}}}{2}\right)}{63.5}\ [V_{\text{dif}}]$ Note: setting the maximum TX amplitude greater than 1 V peak-to-peak differential results in overdrive (applying 1.2 V) to the thin-gate output transistors.

Table 155. DIGITAL_CONTROL_2 register (address 1F80E1h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
15:5	reserved	R	0	
4	TX_POL_INV[1]	R/W		TX polarity inversion For SGMII, TX_POL_INV must be set to 1
			1	Normal polarity
			0*	Data polarity is reversed on TX differential lines
3:1	reserved	R	0	
0	RX_POL_INV[1]	R/W		RX polarity inversion
			1	Data polarity is reversed on RX differential lines
			0*	Normal polarity

[1] For normal SGMII polarity, TX_POL_INV and RX_POL_INV must be set to normal polarity after power-on/reset - that is: TX_POL_INV = 1 and RX_POL_INV = 0.

Table 156. DIGITAL_ERROR_CNT register (address 1F80E2h)

Reset values are indicated by ''*

Bit	Symbol	Access	Value	Description
15:5	reserved	R	0	
4	ICG_EC_EN	R/W		Invalid code group error counter enable
			0*	counting is disabled
			1	counting is enabled
3:1	reserved	R	0	
0	COR	R/W		Clear on read
			0*	Do not clear counters on read
			1	Clear any error counter that is read

7 References

[1] SJA1105P/Q/R/S Data Sheet, NXP Semiconductors

[2] AH1704 SJA1105P/Q/R/S Application Hints, NXP Semiconductors

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