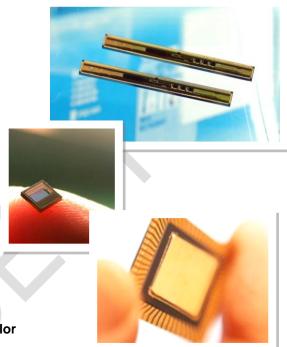
# Raydium <sup>瑞</sup> 鼎 科 技 股 份 有 限 公 司 Raydium Semiconductor Corporation



# WT030 Data Sheet

Single Chip Driver and touch controller with 16.7M color for 480RGBx480 OLED driver

Revision: 0.1

Date : Oct,26 2018



**Revision History** 

Version No.	Date	Description	Page	Modified By	Checked By
0.0	2018/10/11	First Release		Howard Hsiung	CN.Lin
0.1	2018/10/26	8000h D4: RGB555_SWAP	118	Howard Hsiung	CN.Lin

## **Table of Contents**

Tab	le of (	Conte	ents	
1		Gene	eral Description	
2		Featu	res	
3		Block	k Diagram10	
4		Pin D	Description	
	4.1		Power Supply Pins	
	4.2		Interface Pins	
	4.3		MIPI Interface Pins	
	4.4		Interface Logic Pins	
	4.5		Driver Output Pins (Pins for Panel)	
	4.6		DC/DC Convert Pins	
	4.7		Test Pins	
	4.8		TP Interface Pins (PWR/GND=VDDI_TP / VSSI)	
	4.9		TP Interface Pins (PWR/GND=VDDI_FLASH / VSSI)	
	4.10		TP Sensing Pins (Pins for Panel)	17
5		Func	tion Description	
	5.1		Interface Type Selection	
	5.2		3-wire/4-wire SPI Interface	
		5.2.1		
		5.2.2		
		5.2.3		
	5.3		Display Serial Interface (DSI)	
		5.3.1		
		5.3.2	1	
		5.3.3	1	
		5.3.4	1	
		5.3.5		
		5.3.6		
		5.3.7		
		5.3.8		
	5.4		Tearing Effect Output	
		5.4.1		
_		5.4.2		40
6	- 1	Com	mand	
	6.1		Command List	
	6.2		Command Description	
			NOP (0000h)	
			SWRESET(0100h): Software Reset	
			RDDID(0400h~0402h): Read Display ID	
			RDNUMED(0500h): Read Number of Errors on DSI	
			RDDPM (0A00h): Read Display Power Mode	
			RDDMADCTR (0B00h): Read Display MADCTR	
			RDDCOLMOD (0C00h): Read Display Pixel Format	
			RDDIM (0D00h): Read Display Image Mode	
			RDDSM (0E00h): Read Display Signal Mode	
			RDDSDR (0F00h): Read Display Self-Diagnostic Result	
			SLPIN (1000h): Sleep In	
			SLPOUT (1100h): Sleep Out	
			PTLON (1200h): Partial Display Mode On	
			NORON (1300h): Normal Display Mode On	
			INVOFF (2000H): Display Inversion Off	
			INVON (2100H): Display Inversion On	
			ALLPOFF (2200H): All Pixel Off	04

# Raydium

		ALLPON (2300H): All Pixel On	66
		DISPOFF (2800h): Display Off	
		DISPON (2900h): Display On	69
		CASET(2A00h~2A03h): Set Column Start Address	71
		RASET(2B00h~2B03h): Set Row Start Address	73
		RAMWR (2C00h): Memory Write	75
		PTLAR (3000h): Partial Area	
		PTLAR (3100h): Vertical Partial Area	79
		TEOFF (3400h): Tearing Effect Line OFF	
		TEON (3500h): Tearing Effect Line ON	
		MADCTR (3600h): Scan Direction Control	
		IDMOFF (3800h): Idle Mode Off	
		IDMON (3900h): Enter_idle_mode	
		COLMOD (3A00h): Interface Pixel Format	
		RAMWRC (3C00h): Memory Continuous Write	
		STESL(4400h): Set_Tear_Scanline	
		GSL (4500h): Get_Scanline	
		DSTBON (4F00h): Deep Standby Mode On	
		WRDISBV (5100h): Write Display Brightness	
		RDDISBV (5200h): Read Display Brightness	
		WRCTRLD (5300h): Write Display Control	
		RDCTRLD (5400h): Read Display Control	
		WRRADACL (5500h): RAD_ACL Control	
		IMGEHCCTR (5800h): Set_color_enhance	
		IMGEHCCTR (5900h): Read_color_enhance	
		OPSCTR (5E00h): OPS CTR	
		OPSCTR2 (5F00h): OPS CTR2	
		WRHBMDISBV (6300h): Write HBM Display Brightness	
		RDHBMDISBV (6400h): Read HBM Display Brightness	
		HBM_Mode (6600h): Set_HBM_Mode	
		Deep_Idle_Mode (6700h): Set_Deep Idle Mode	
		COLSET (7000~7F00h): Interface Pixel Format Set	
		COLOPT (8000h): Interface Pixel Format Option	
		RDDDBS(A100h): Read_DDB_Start	
		RDDDBC(A800h): Read DDB Continous	
		RDFCS(AA00h): Read First Checksum	
		RDCCS(AF00h): Read Continue Checksum	
		SetDISPMode (C200h): set_DISP Mode	126
		SetDSPIMode (C400h): set_DSPI Mode	127
		RDID1 (DA00h): ID1 Code	130
		RDID2 (DB00h): ID2 Code	131
		RDID3 (DC00h): ID3 Code	132
		(FE00h): CMD Mode Switch	133
		(FF00h): Read CMD Status	135
7		Electrical Characteristics	7
	7.1	Absolute Maximum Ratings	137
	7.2	ESD Protection Level	
	7.3	Latch-Up Protection Level	
	7.4	DC Characteristics	
		7.4.1 Basic Characteristics.	
	7.5	MIPI Characteristics.	
	, .5	7.5.1 High-Speed Receiver Specification	
		7.5.2 Forward high speed transmissions	
		7.5.3 Data to Clock Timing Definitions	
		7.5.4 Low power transceiver specifications	
	7.6	AC Characteristics	
	7.0	7.6.1 Serial Interface Characteristics	
		7.6.2 DSI Timing Characteristics	145

# Raydium

	7.6.3	Reset Timing(RESX)	14	18
	7.6.4	<u> </u>	(ESET)	
7.7		<b>U</b> ,		





### 1 General Description

The WT030 device is a single-chip solution for LTPS AMOLED that incorporates gate drivers and is capable of 480RGBx480, 400RGBx400, 360RGBx480, 320RGBx320, 320RGBx480, 272RGBx480, 240RGBx240, 240RGBx320, 180RGBx360, 180RGBx540, 128RGBx432with internal GRAM. It includes a 2,764,800 bits internal memory, a timing controller with glass interface level-shifters and a glass power supply circuit.

The WT030 supports 30CH touch-controller SOC IC with I2C serial interface for capacitive touch panel applications

The WT030 supports MIPI Interface, 8-bit system interfaces, serial peripheral interfaces (SPI), dual serial peripheral interfaces (Dual-SPI). The specified window area can be updated selectively, so that moving pictures can be displayed simultaneously independent of the still picture area.

The WT030 is also able to make gamma correction settings separately for RGB dots to allow benign adjustments to panel characteristics, resulting in higher display qualities. The IC possesses internal GRAM that stores  $480 \times 480 \times 1/2 \times 24$  bits for 16.77M-color images. A deep standby mode is also supported for lower power consumption.

This LSI is suitable for wearable device applications, including I-watch and smart band.

### 2 Features

### ■ Single chip AMOLED controller/driver with display RAM

### ■ Touch

- ARM Cortex-M0 32-bit micro-processor
- Support 64KB External Flash
- On chip 4KB data memory
- On chip Sensing memory and Baseline memory
- Support serial wire debug interface with 2 watch points and 4 break points
- Support in-system-programming
- I2C-compatible serial interface
- ➤ Power management unit Normal / IDLE mode / Wake up mode/ Standby mode
- Sensing mode Node Self Scan for charge sensing / Parallel Scan(non driving)
- Support Node base compensation
- 30 Sensing channels for Self Mode

### ■ Display resolution option

- > 480RGB x 480
- > 400RGB x 400
- > 360RGB x 480
- > 320RGB x 320
- > 320RGB x 480
- > 272RGB x 480
- > 240RGB x 240
- > 240RGB x 320
- > 180RGB x 360
- > 180RGB x 540
- > 128RGB x 432

### ■ Display data RAM (frame memory): 2,764,800 bits

### Display mode (Color mode)

- Full color mode: 16.7M-colors
- ldle mode: 16.7M-colors, 4096-colors, 8-colors

### ■ Interface

- 8-bits 80-series MPU interface
- Serial peripheral interface (SPI)
- Dual serial peripheral interface (Dual-SPI)
- MIPI Display Serial Interface (1 clock and 2 data lane pairs)
  - Support 1lane/2lane (1lane: 500Mbps)
  - Maximum total bit rate is 500Mbps of 2 data lanes 24-bit data format/ 360Mbps of 2 data lanes 18-bit data format/ 320Mbps of 2 data lanes 16-bit data format

### Abundant color display and drawing functions

- Programmable y-correction function for 16.7 million color display
- Individual gamma correction setting for RGB dots



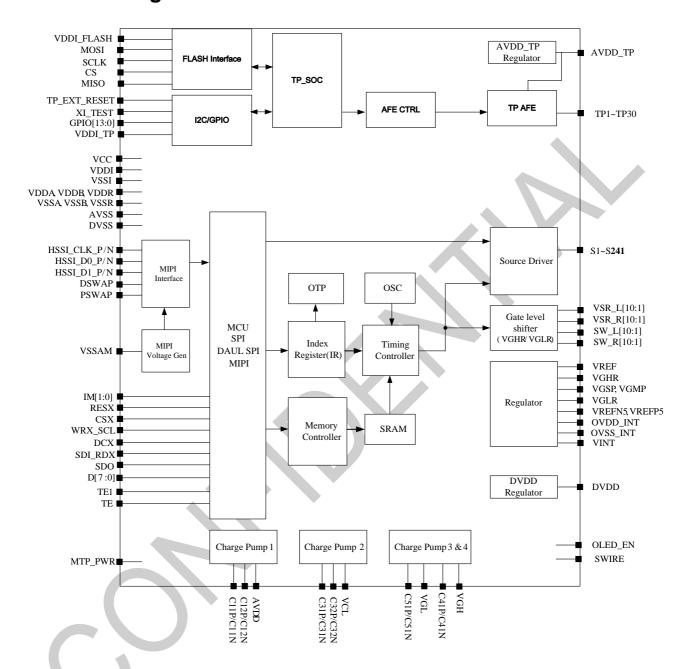
- Partial display function
- Sunlight readable
- Temperature sensor and power IC control
  - Built-in temperature sensor.
  - LUT mapping can be programmed by registers
- Control power IC by one-wire interface
- Low Frame Rate Select
- Internal OLED power mode
- On chip
  - VREFP5/VREFN5/VREFP5\_2 voltage generator for panel voltage
  - VGHR/VGLR voltage for gate control signal
  - Internal oscillator for display clock
  - Source output MUX 1-6 with 240ch source output pins
  - Source output MUX 1-5, MUX 1-10 for hyper plus
  - Supports gate control signals to gate driver in the panel
- Built-in OTP function to adjust panel setting
- Logic / interface power supply voltage VDDI = 1.65V ~ 1.95V
- Analog power supply voltage VDD = 2.7V ~ 3.6V
- Output voltage levels
  - ➤ Positive gate driver voltage range for VGHR: 3 ~ 10.5V (Max<=VGH-0.3v)
  - ➤ Negative gate driver voltage range for VGLR: -2V ~ -9.5V (Min>=VGL+0.3v)
  - VREFP5 & VREFP5\_2 panel voltage range: 0~5V (Max<=AVDD-0.3v)</p>
  - VREFN5 panel voltage range : -0.5~-4.5V (Min>=VCL+0.3v)
  - > Step-up 1,2 output voltage range for AVDD: 4.5 ~ 6.5V, VCL: -3.5 ~ -5.0V
  - Gamma high/low voltage range for VGMP: 2.0V ~ 6.0V (Max<=AVDD-0.5v) , VGSP: 0V, 0.2125V ~ 4.5V</p>
- Low voltage detection (VDDA / VDDI) for abnormal power off
- Package: COF
- Chip size evaluation: 8970um x 2800um(including scribe line)



### **■**Power Supply Specifications

No.	Item		Description		
1	Source Driver		241 pins (480 x RGB)		
2	gate control timing Le	vel shift	VGHR-VGLR		
5	Input Voltage	VDDI	1.65 ~ 1.95V		
		VCC	Connect to VDDI or VDD(VCI)		
		VDD (VDDA/VDDB/VDDR)	2.70 ~ 3.60V		
6	OLED drive voltages	AVDD	4.5V ~ 6.5V		
		VGHR	3V ~ 10.5V (Max<=VGH-0.3v)		
		VGLR	-2V ~ -9.5V (Min>=VGL+0.3v)		
		VREFP5 & VREFP5_2	0V ~ 5V (Max<=AVDD-0.3v)		
		VREFN5	-0.5V ~ -4.5V (Min>=VCL+0.3v)		
		OVDD_INT (BVP3D)	2~4.9v (Max<=AVDD-0.3v)		
		OVSS_INT (BVP3D)	-0.4 ~ -4.0V (Min>=VCL+0.3v)		
7	Internal step-up circuits	AVDD	VCI x2.0(dual), x3.0(single)		
	Circuits	VCL	VCI x -1.0(dual), x-2.0(single)		
		VGH	VCI x2, x3, x4		
		VGL	VCI x-2, x-3, x-4		
		TPPUMP	VCI x2.0(dual), x3.0(single)		

### 3 Block Diagram



#### Interface

The WT030 supports MIPI DSI interface. MIPI DSI can access both internal command and display data.

### Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a drive voltage, which corresponds to grayscale level set in the  $\gamma$  correction register. The WT030 displays 16.7M colors at the maximum.

### Power Supply Circuit

The power supply circuit generates supply voltages to OLED panel, VGH, VGL.

### **Timing Generating**

The timing controller generates timing signals for internal circuits such as the display timing.



### Oscillator

The WT030 incorporates RC oscillator circuit. The frame frequency is changeable by command settings.

### **Panel Driver Circuit**

The OLED display driver circuit consists of 241 source drivers (S1~S241). The gate signal consists of VSR\_R/L[1:10], SW\_R/L[1:10] and outputs either VGHR or VGLR level.

### **Touch Circuit**

The WT030 supports 30CH touch-controller SOC IC with I2C serial interface for capacitive touch panel applications



## 4 Pin Description

### 4.1 Power Supply Pins

Signal	I/O	Function		
VDDB	Р	Power supply for DC/DC converter  VDDB, VDDA and VDDR should be the same input voltage level		
VDDA	Р	Power supply for analog system and low voltage detection VDDB, VDDA and VDDR should be the same input voltage level		
VDDR	Р	Power supply for regulator system VDDB, VDDA and VDDR should be the same input voltage level		
VDDA_TP	Р	Power supply for TP circuit.  VDDB, VDDA , VDDA_TP and VDDR should be the same input voltage level		
VDDI	Р	Power supply for interface system except MIPI interface, and power supply for low voltage detection		
VDDI_TP	Р	Power supply for TP interface circuit		
VDDI_FLASH	Р	Power supply for TP FLASH circuit (1.65~1.95v)		
VCC	Р	Power supply for DVDD regulator		
VSSB	Р	System ground for DC/DC converter		
VSSA	Р	System ground for analog system		
VSSR	Р	System ground for regulator system		
VSSAM	Р	System ground for internal MIPI analog system		
VSSA_TP	Р	System ground for TP circuit		
VSSI	Р	System ground for interface system except MIPI interface		
DVSS	Р	System ground for internal digital system		
AVSS	Р	System ground for source OP system.		
MTP_PWR	Р	MTP programming power supply pin (7.5V typical) Must be left open or connected to DVSS in normal condition.		
AVDD_TP_PW R	Р	Power supply for AVDD_TP circuit. If not use, please leave it open.		



### 4.2 Interface Pins

Signal	I/O	Function
CSX	I	Chip select input pin ("Low" enable) in 80-series MPU I/F and SPI I/F. If not used, please connect to VDDI.
WRX_SCL	I	WRX : Writes strobe signal to write data when WRX is "Low" in 80-series MPU I/F. SCL: A synchronous clock signal in SPI I/F. If not used, please connect to VSSI.
D/CX	ı	Display data / command selection in 80-series MPU I/F and 4-wire SPI I/F. D/CX = "0" : Command D/CX = "1" : Display data or Parameter If not used, please connect to VSSI.
SDI_RDX	I/O	SDI: Serial input signal in SPI I/F. The data is input on the rising edge of the SCL signal. RDX: Reads strobe signal to write data when RDX is "Low" in 80-series MPU interface. If not used, please leave it Open.
SDO	0	Serial output signal in SPI I/F. The data is output on the rising/falling edge of the SCL signal. If the host places the SDI line into high-impedance state during the read interval, the SDI and SDO can be tied together. If not used, please open this pin.
D[7:0]	I/O	8-bit bi-directional data bus for 80-series MPU I/F and 8-bit input data bus for RGB I/F. These pins are not used for SPI, MIPI, please leave it Open.



### 4.3 MIPI Interface Pins

Signal	I/O	Function																		
HSSI_CLK_P HSSI_CLK_N	I		-These pins are DSI-CLK+/- differential clock signals if MIPI interface is usedIf not used, please connect these pins to VSSAM.																	
HSSI_D0_P HSSI_D0_N	I/O		-These pins are DSI-D0+/- differential data signals if MIPI interface is usedIf not used, please connect these pins to VSSAM.																	
HSSI_D1_P HSSI_D1_N	I/O	-These pins ar -If not used, pl			•	MIPI interfac	ce is used.													
		Pin Name	lect HSSI_D(	D/D1 data lan	HSSI_CLK_ P	and polarity in the state of th	n high speed HSSI_D1_P	Hinterface only.  HSSI_D1_N												
		DSWAP=0 PSWAP=0	DSI D0+	DSI D0-	DSI         DSI         DSI           CLK+         CLK-         D1+         D1-															
DSWAP PSWAP	NAP DSWAP=	1	ı	1	I	I	ı	ı	1	ı	1	1	ı	DSWAP=0 PSWAP=1	DSI D0-	DSI D0+	DSI CLK-	DSI CLK+	DSI D1-	DSI D1+
		DSWAP=1 PSWAP=0	DSI D1+	DSI D1-	DSI CLK+	DSI CLK-	DSI D0+	DSI D0-												
		DSWAP=1 PSWAP=1	DSI D1-	DSI D1+	DSI CLK-	DSI CLK+	DSI D0-	DSI D0+												
		If not used, please connect to VSSI.																		

NOTE: "1" = VDDI level, "0" = VSSI level.

### 4.4 Interface Logic Pins

Signal	I/O	Function							
RESX			This signal will reset the device and must be applied to properly initialize the chip.  Signal is active low.						
			election. The connections of IM[1	:0] which not shown in table are invalid.					
IM[1:0]	I	M[1:0] 00 01 10 11	Display Data MIPI / 3-wire SPI MIPI / 4-wire SPI MIPI / QUAD-SPI MCU 8-bit	Command  MIPI / 3-wire SPI  MIPI / 4-wire SPI  MIPI / QUAD-SPI  MCU 8-bit					



		Boost mode selection p	in.		
		BSTM	Mode		
BSTM	I	0	2 PWR(VDDI, VCI)  AVDD> internal CP  VCL> internal CP		
		1	Reserved		
TE	0	Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is output low.			
TE1	0	If not used, please oper			
SWIRE	0	O Swire protocol setting pin of Power IC, If not used, please open this pin.			
OLED_EN	0	Power IC enable control pin, If not used, please open this pin.			

NOTE: "1" = VDDI level, "0" = VSSI level.

### 4.5 Driver Output Pins (Pins for Panel)

Signal	I/O	Function
S1 ~ S241	0	Pixel electrode driving output.
SDMY[1] ~ SDMY[20]	0	Dummy Source, leave it Open.
VSR_L[10:1] VSR_R[10:1]	0	VSR control signals, Level shift output, (VGHR-VGLR)
SW_L[10:1] SW_R[10:1]	0	VSR control signals, Level shift output, (VGHR-VGLR)

### 4.6 DC/DC Convert Pins

Signal	I/O	Function
AVDD	0	Output voltage from step-up circuit 1, generated from VDDB. Connect a capacitor for stabilization.
		Output voltage from step-up circuit 3, generated from VDDB. Connect a capacitor for stabilization.



VGH	0	Output voltage from step-up circuit 4. Connect a capacitor for stabilization.	
VGL	0	Output voltage from step-up circuit 5. Connect a capacitor for stabilization.	
C11P, C11N C12P, C12N	Ю	Capacitor connection pins for the step-up circuit which generate AVDD.  Connect capacitor as requirement. When not in used, please open these pins.	
C31P, C31N C32P, C32N	Ю	Capacitor connection pins for the step-up circuit which generate VCL. Connect capacitor as requirement.	
C41P, C41N	Ю	Capacitor connection pins for the step-up circuit which generate VGH. Connect capacitor as requirement.	
C51P, C51N	Ю	Capacitor connection pins for the step-up circuit which generate VGL.  Connect capacitor as requirement.	
VGHR	0	Output voltage generated from VGH. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.	
VGLR	0	Output voltage generated from VGL. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.	
OVDD_INT (BVP3D)	0	Positive output voltage generated from AVDD. LDO output used for OLED panel display. Connect a capacitor for stabilization. When not in use, please open this pin.	
OVSS_INT (BVN3D)	0	Negative output voltage generated from VCL. LDO output used for OLED panel display Connect a capacitor for stabilization. When not in use, please open this pin.	
VGMP	0	Output voltage generated from AVDD. LDO output for positive gamma high voltage generator.	
VGSP	0	Output voltage generated from AVDD. LDO output for positive gamma low voltage generato	
VREF	0	Regulator output for internal reference voltage. Connect capacitor for stabilization.	
DVDD	0	Regulator output for logic system power. Connect a capacitor for stabilization.	
VREFP5	0	Regulator output for VREFP(0~5V)	
VREFP5_2	0	Regulator output for VREFP_2(0~5V)	
VREFN5	0	Regulator output for VREFN(-0.5~-5V)	
AVDD_TP	0	Regulator output for AVDD_TP (4.3~5V)	
TPPUMP	0	Output voltage from TPPUMP step-up circuit, generated from VDDB. Connect a capacitor for stabilization.	
C11P_TP, C11N_TP C12P_TP, C12N_TP	C11N_TP C12P_TP, C12P_TP, C12P_TP, C12P_TP, C12P_TP, C22P_TP, C3PACITION Connection pins for the step-up circuit which generate TPPUMP C3PACITION CONNECTION CONNECTI		
VCM O Output voltage generated from AVDD_TP. Connect a capacitor for stabilization.		Output voltage generated from AVDD_TP. Connect a capacitor for stabilization.	

### 4.7 Test Pins

Signal	I/O	Function
ANALOG_TEST	0	Test pin, not accessible to user. Must be left open.



1~3			
TEST1~3	Ю	Test pin, not accessible to user. Must be left open.	
TESTEN	I	Test pin, not accessible to user. Must be left open., Internal pull low	
EXTCLK	I	Test pin, not accessible to user. Must be left open.	
DUMMY	I	Dummy PAD, leave it open	

### 4.8 TP Interface Pins (PWR/GND=VDDI\_TP / VSSI)

Signal	I/O	Function			
TP_EXT_RESET	I	System reset (default: H), (Default : Internal Pull-High), If no use, please leave it open.  TP_EXT_RESET = "L": System reset  TP_EXT_RESET = "H": Normal operation			
XI_TEST	I	TEST mode (Default : Internal Pull-Low), If no use, please leave it open.  XI_TEST = "H": Enable test mode  XI_TEST= "L": Normal operation			
GPIO0	I/O	I <sup>2</sup> C clock (I2C_SCL) (internal pull -High), If no use, please leave it open. For I2C interface, this line must be connected to a positive supply via a pull-up resistor. The value of the resistor should be chosen to ensure that the rise time is within the limits set by the I2C specification. The value typically would fall within the ranges of 1.5k~10kohm.			
GPIO1	I/O	I <sup>2</sup> C data(I2C_SDA) (internal pull -High), If no use, please leave it open. For I2C interface, this line must be connected to a positive supply via a pull-up resistor. The value of the resistor should be chosen to ensure that the rise time is within the limits set by the I2C specification. The value typically would fall within the ranges of 1.5k~10kohm.			
GPIO2	0	INT output , If no use, please leave it open.			
GPIO3	I/O	RS232_TX/SWDIO (internal pull-High) , If no use, please leave it open.			
GPIO4	I/O	SWCLK(internal pull-High) , If no use, please leave it open.			
GPIO5	IO5 I/O HOLD(internal pull-High) , If no use, please leave it open.				
GPIO6	I/O WP(internal pull-High) , If no use, please leave it open.				
GPIO7	I/O	BOOT_DEVICE(internal pull -High) , If no use, please leave it open.			
GPIO8 ~ GPIO13	I/O	GPIO pins(internal pull-High), If no use, please leave it open.			

### 4.9 TP Interface Pins (PWR/GND=VDDI\_FLASH / VSSI)

Signal	I/O	Function	
CS	0	SPI Chip select to FLASH, If no use, please leave it open.	
SCLK	0	SPI serial clock to FLASH, If no use, please leave it open.	
MOSI	0	SPI data output to FLASH, If no use, please leave it open.	
MISO	I	SPI data input from FLASH (Internal Pull-Low) , If no use, please leave it open.	

### 4.10 TP Sensing Pins (Pins for Panel)



Signal	I/O	Function			
TP1~TP30	I/O	ensing channel pins (AVDD_TP ~ VSSA)			
TPDMYL1~18 TPDMYR1~18 TPDMY1~36 DUMMYL* DUMMYR*	0	Dummy pad , leave it open.			

Page18



## **5 Function Description**

### 5.1 Interface Type Selection

Interface type selection. The connections of IM[1:0] which not shown in table are invalid.

IM[1:0]	Display Data	Command
00	MIPI / 3-wire SPI	MIPI / 3-wire SPI
01	MIPI / 4-wire SPI	MIPI / 4-wire SPI
10	MIPI / QAD-SPI	MIPI / QAD-SPI
11	MCU 8-bit	MCU 8-bit





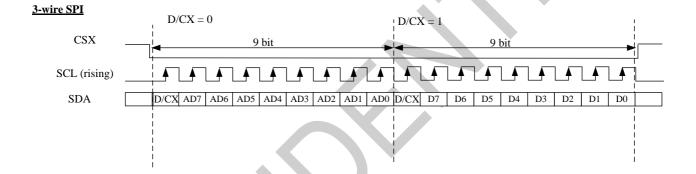
### 5.2 3-wire/4-wire SPI Interface

### 5.2.1 Write Cycle and Sequence

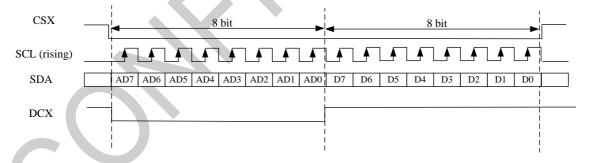
During a write cycle the host processor sends a single bit of data to the display module via the interface. The 3-wire/4-wire SPI interface utilizes CSX, SCL and SDA signals. SCL is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of SCL.

During the write sequence the host processor writes one or more bytes of information to the display module via the interface. The write sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. The 3-wire serial data contains DCX bit and a transmission byte. DCX bit is driven low while command information is on the interface and is pulled high when data is present.

The 3-wire/4-wire SPI interface write command sequences are described in the following figure.



#### 4-wire SPI





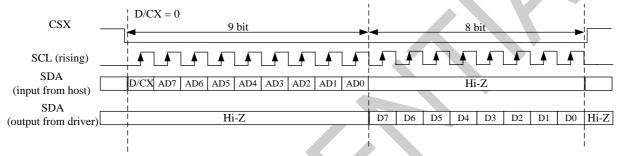
### 5.2.2 Read Cycle and Sequence

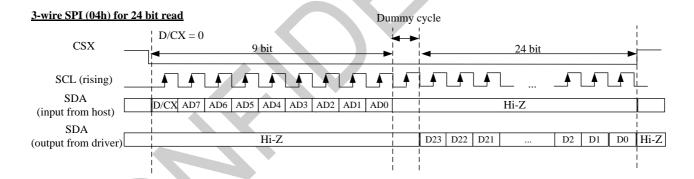
During a read cycle the host processor reads a single bit of data from the display module via the interface. The 3-wire/4-wire SPI interface utilizes CSX, SCL and SDA signals. SCL is driven from high to low then pulled back to high during the read cycle. The display module provides information during the read cycle while the host processor reads the display module information on the rising edge of SCL.

During the read sequence the host processor reads one or more bytes of information from the display module via the interface. The read sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. The 3-wire serial data contains DCX bit and a transmission byte. DCX is driven low while command information is on the interface and is pulled high when data is present.

The 3-wire/4-wire SPI interface read command sequences are described in the following figure.

#### 3-wire SPI (0Ah/0B/0Ch/0Dh/0Eh/0Fh/DAh/DBh/DCh) for 8 bit read







SDA

(output from driver)

#### 4-wire SPI (0Ah/0B/0Ch/0Dh/0Eh/0Fh/DAh/DBh/DCh) for 8 bit read D/CX = 0CSX 8 bit 8 bit SCL (rising) DCX SDA AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0 Hi-Z (input from host) SDA Hi-Z D6 D4 D3 D2 D0 Hi-Z D7 D5 D1 (output from driver) 4-wire SPI (04h) for 24 bit read Dummy cycle D/CX = 0CSX 24 bit 8 bit SCL (rising) DCX SDA AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0 Hi-Z (input from host)

D23 D22 D21

D2 D1

D0 Hi-Z

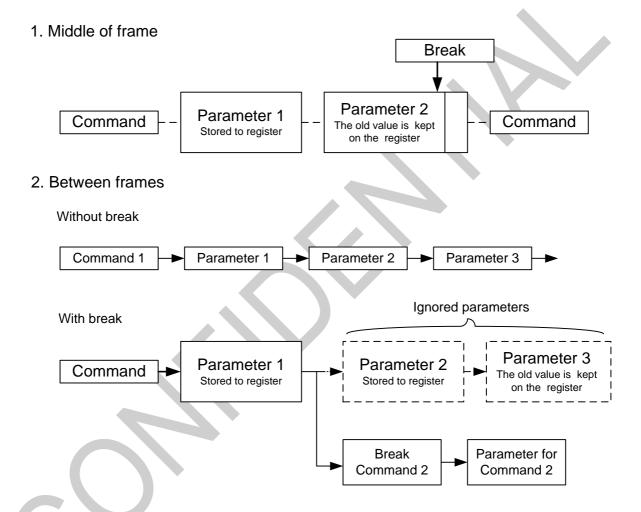
Hi-Z



### 5.2.3 Break and Pause Sequence

The host processor can break a read or write sequence by pulling the CSX signal high during a command or data byte. The display module shall reset its interface so it will be ready to receive the same byte when CSX is again driven low.

The host processor can pause a read or write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the read or write sequence at the point where the sequence was paused.



Break can be e.g. another command or noise pulse.



### 5.3 Display Serial Interface (DSI)

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

WT030 is capable of both Command Mode operation and Video Mode operation. Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a display module that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller.

The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface. Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode.

WT030 Video Mode architectures also include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to reduce power consumption.

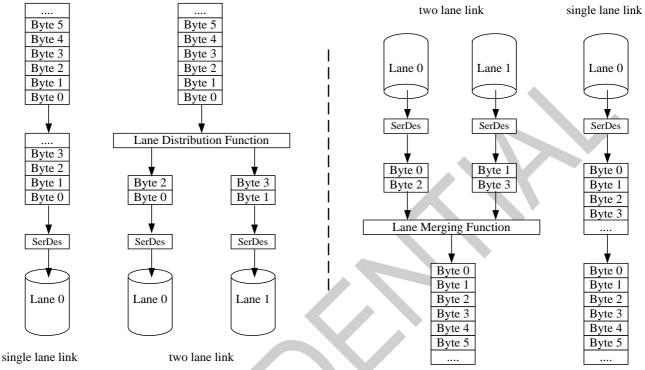
WT030 Configuration:

Lane Pair	MCU(Master) WT030(Slave)
Clock Lane	Unidirectional Lane
	Clock only
Data Lane 0	Bi-directional Lane
	Forward High-speed
	Bi-directional Escape Mode
	Bi-directional LPDT
Data Lane 1	Unidirectional Lane
	Forward High-Speed
	Escape Mode
	No LPDT



#### 5.3.1 DSI Protocol

On the transmitter side of a DSI Link, parallel data, signal events, and commands are converted to packets. These packets are sent across the serial Link. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands.

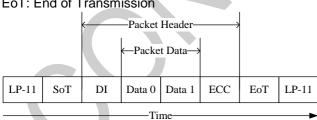


There are two kinds of packets, short packet and long packet.

Short packet structure: LP-11: low power mode

SoT: start of transmission DI: data identification

Data 0, Data1: packet data ECC: error correction code EoT: End of Transmission





#### DI structure:

Virtual Channel: these two bits identify the data as directed to one of four virtual channels

Data Type: It specifies the packet structure and packet format

Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

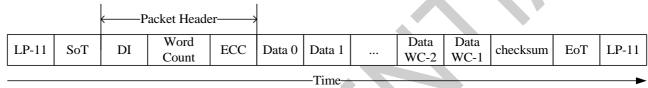
Long packet structure: LP-11: low power mode SoT: start of transmission DI: data identification

Word Count: the number of data bytes of packet data

ECC: error correction code

Checksum: The 16-bit CRC generator to check packet data. If the calculated checksum of receiver are equal to the packet data, the packet data is correct. If the calculated checksum of receiver are not equal, the packet data are not correct.

EoT: end of transmission





### 5.3.2 Processor to Peripheral Transactions

Processor to Peripheral Direction Packet Data Types

Data Type	Data Type	Description	Packet
	binary	•	Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission packet (EoTp)	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	reserved	Short
32h	11 0010	reserved	Short
03h	00 0011	reserved	Short
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
04h	00 0100	reserved	Short
14h	01 0100	Generic READ, 1 parameter	Short
24h	10 0100	Generic READ, 2 parameters	Short
05h	00 0101	DCS Short WRITE, no parameters	Short
15h	01 0101	DCS Short WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
29h	10 1001	Generic Long Write	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6	Long
		Format	
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long



### Sync Event, Data Type = xx 0001

Sync Events are all short packets and time-accurately. They can perform like the start and end of sync pulses. To represent timing information as accurately as possible, a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Hence, a V Sync End event implies an H Sync Start event for the last line of the VSA. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode.

#### EoT packet

This short packet is used to indicate the end of a high speed (HS) transmission. This packet will enhance overall syntem reliability. Although the main objective of the EoTp is to enhance robustness during HS transmission mode, WT030 can detect and interpret arriving EoTps regardless of transmission mode (HS or LP modes)

#### Color Mode Off / On Command

They are short packet commands to switch video display module between normal display mode and low-color mode for power saving.

### Generic short write / read packet

Generic Short WRITE command is a Short packet type for sending generic data to the peripheral. Generic READ request is a Short packet requesting data from the peripheral.

#### DCS commands

### DCS short write command

DCS short write command is used to write a single data byte command to display module. If there is a valid parameter byte, data type bit 4 shall be set to 1. If there is no valid parameter byte, data type bit 4 shall be set to 0 and the parameter byte shall be 00h.

#### DCS read commands

The commands are used to request data from s display module.

### DCS Long Write / write\_LUT command

The commands are used to send larger blocks of data to a display module.

### Maximum return packet size

This command specifies the maximum size of the payload in a long packet transmission from a display module to host processor.

#### **Null Packet**

This is a mechanism for keeping the data lane(s) in high speed mode while sending dummy data.

### Blanking Packet

A Blanking packet is used to convey blanking timing information in a Long packet. The packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Blanking packets may contain arbitrary data as payload.

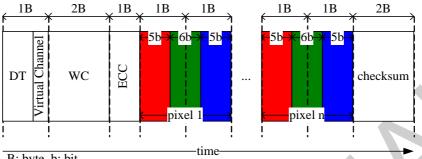
#### Generic Long Write

This is used to transmit arbitrary blocks of data from a host processor to a peripheral.



Packed Pixel Stream, 16-bit Format, Data Type: 00 1110

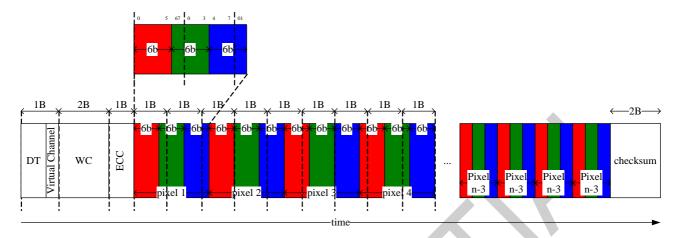
The pixel format is five bits red, six bits green and five bits blue. The green component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.





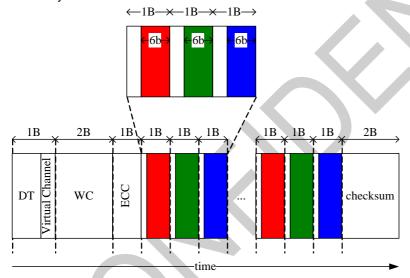
Packet pixel stream, 18-bit format, Data Type: 01 1110

The pixel format is six bits red, six bits green and six bits blue. Within a color component, the LSB is sent first, the MSB last.



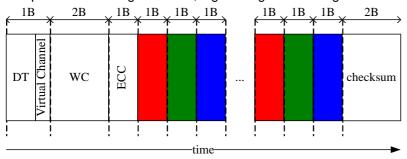
Packet pixel stream, 18-bit format in three bytes, Data Type: 10 1110

This is 18-bit pixel lossely packed format, each R, G or B color component is six bits but shifted to the upper bits of byte.





Packet pixel stream, 24-bit format, Data Type: 11 1110
The pixel format is eight bits red, eight bits green and eight bits blue.





### 5.3.3 Peripheral-to-Processor LP Transmission

All Command Mode systems require bidirectional capability for returning READ data, acknowledge, or error information to the host processor. Multi-Lane systems shall use Lane 0 for all peripheral-to-processor transmissions. Reverse-direction signaling shall only use low power mode transmission.

Packet structure for peripheral-to-processor transaction is the same as for the processor-to-peripheral direction. For the processor-to-peripheral direction, two basic packet formats are the same as the peripheral-to-processor direction: Short and Long packet structure. BTA shall take place after every peripheral-to-processor transaction. This returns bus control to the host processor following the completion of the LP transmission from the peripheral.

There are four basic types of peripheral-to-processor transactions.

Tearing Effect: It is a Trigger message sent to convey display timing information to the host processor. Acknowledge: It is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication.

Acknowledge and Error Report: It is a Short packet sent if any errors were detected in preceding transmissions from the host processor.

Response to Read Request: It may be a Short or Long packet that returns data requested by the preceding READ command from the processor.

Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as follows:

Following a non-Read command: If no errors were detected, the peripheral shall respond with Acknowledge.

Following a Read request: The peripheral shall send the requested READ data if no errors were detected and stored since the last peripheral to host communication.

Following a Read request: If only a single-bit ECC error was detected and corrected, the peripheral shall send the requested READ data in a Long or Short packet and a 4-byte Acknowledge and Error Report packet in the same LP transmission.

Following a non-Read command: If only a single-bit ECC error was detected and corrected, the peripheral shall respond to BTA by sending a 4-byte Acknowledge and Error Report packet.

Following a Read request: If multi-bit ECC errors were detected and not corrected, the peripheral shall send a 4-byte Acknowledge and Error Report packet without sending Read data.

Following a non-Read command: If multi-bit ECC errors were detected and not corrected, the peripheral shall not execute the command, and shall send a 4-byte Acknowledge and Error Report packet.

Following any command: If SoT Error, SoT Sync Error, the VC of DSI or the ID of DSI Invalid or DSI protocol violation was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge and Error Report response.

Following any command: If EoT Sync Error or LP Transmit Sync Error is detected, or a checksum error is detected in the payload, the peripheral shall send a 4-byte Acknowledge and Error Report packet.



### 5.3.4 Error Report Format

The following table shows the bit assignment for all error report.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	HS Receive Timeout Error
6	False Control Error
7	Reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	reserved
14	reserved
15	reserved



5.3.5 Peripheral-to-Processor Transaction – Detail Format Description

The following list is the complete set of peripheral-to-processor data types.

Data type, hex	Data type binary	Description	Packet size
02h	00 0010	Acknowledge and error report	short
08h	00 1000	reserved	short
11h	01 0001	GEN short read reponse, 1byte returned	short
12h	01 0010	GEN short read reponse, 2bytes returned	short
1Ah	01 1010	Generic long read reponse	long
1Ch	01 1100	DCS long read reponse	long
21h	10 0001	DCS short read reponse, 1byte returned	short
22h	10 0010	DCS short read reponse, 2bytes returned	short

Acknowledge and error report: It is sent with BTA asserted when a reportable error is detected in the preceding, or earlier, transmission from the host processor.

Generic Short Read Response: This is the short-packet response to Generic READ Request. Packet composition is the Data Identifier (DI) byte, two bytes of payload data and an ECC byte. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

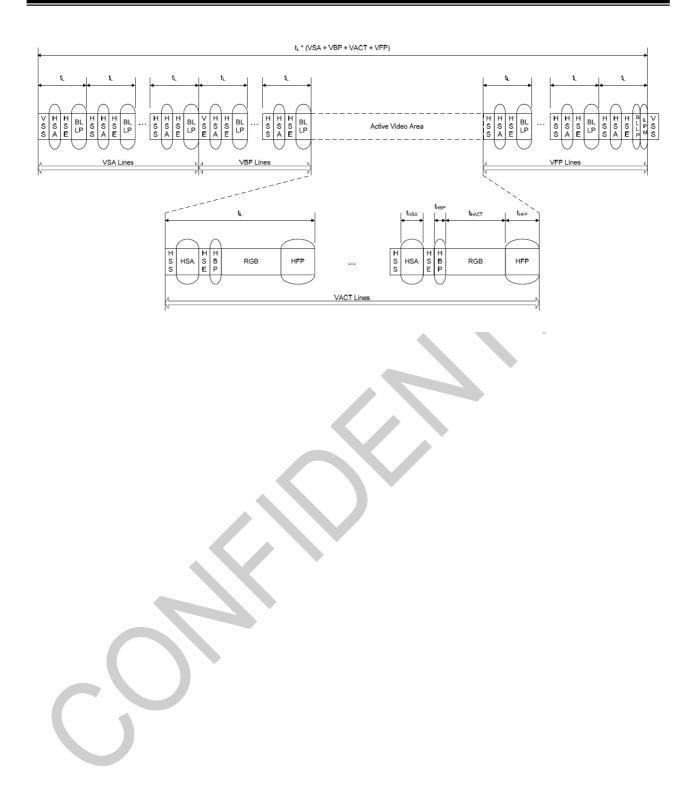
Generic long read reponse: This is the long-packet response to Generic READ Request. Packet composition is DI followed by a two-byte Word Count, an ECC byte, N bytes of payload, and a two-byte Checksum. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

DCS long read reponse: This is a Long packet response to DCS Read Request. Packet composition is DI followed by a two-byte Word Count, an ECC byte, N bytes of payload, and a two-byte Checksum. If the DCS command itself is possibly corrupt, due to uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

DCS short read reponse: This is the short-packet response to DCS Read Request. Packet composition is DI, two bytes of payload data and an ECC byte. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge and Error Report packet shall be sent.

#### 5.3.6 DSI Video Mode Interface Timing







### 5.3.7 Error Correction Code (ECC)

ECC shall always be generated and appended in the Packet Header from the host processor. Peripherals with Bidirectional Links shall also generate and send ECC.

The number of parity or error check bits required is given by the Hamming rule, which uses parity to correct a single-bit error or detect a two-bit error, but are not capable of doing both simultaneously. DSI uses Hamming-modified codes where an extra parity bit is used to support both single error correction as well as two-bit error detection.

Since Packet Headers are fixed at four bytes (twenty-four data bits and eight ECC bits), P6 and P7 of the ECC byte are unused and shall be set to zero by the transmitter. The receiver shall ignore P6 and P7 and set both bits to zero before processing ECC.

The parity bits of ECC are defined as below:

P7 = 0

P6 = 0

P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

The table below shows a compact way to specify the encoding of parity and decoding of syndromes.

### **ECC Parity Generation Rules:**

Data Bit	P7	P6	P5	P4	P3	P2	P1	P0	Hex
0	0	0	0	0	0	1	1	1	0x07
1	0	0	0	0	1	0	1	1	0x0B
2	0	0	0	0	1	1	0	1	0x0D
3	0	0	0	0	1	1	1	0	0x0E
4	0	0	0	1	0	0	1	1	0x13
5	0	0	0	1	0	1	0	1	0x15
6	0	0	0	1	0	1	1	0	0x16
7	0	0	0	1	1	0	0	1	0x19
8	0	0	0	1	1	0	1	0	0x1A
9	0	0	0	1	1	1	0	0	0x1C
10	0	0	1	0	0	0	1	1	0x23
11	0	0	1	0	0	1	0	1	0x25
12	0	0	1	0	0	1	1	0	0x26
13	0	0	1	0	1	0	0	1	0x29
14	0	0	1	0	1	0	1	0	0x2A
15	0	0	1	0	1	1	0	0	0x2C
16	0	0	1	1	0	0	0	1	0x31
17	0	0	1	1	0	0	1	0	0x32
18	0	0	1	1	0	1	0	0	0x34
19	0	0	1	1	1	0	0	0	0x38
20	0	0	0	1	1	1	1	1	0x1F
21	0	0	1	0	1	1	1	1	0x2F
22	0	0	1	1	0	1	1	1	0x37
23	0	0	1	1	1	0	1	1	0x3B



#### **5.3.8** Notice

- 1. We recommend users to stay in STOP state for 500ns when switching from LPDT to HSDT.
- 2. We recommend users to adopt EoTp to enhance overall robustness of the system during HSDT.



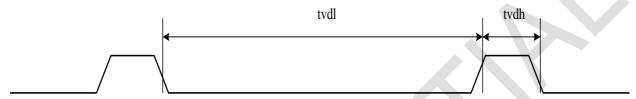


#### 5.4 Tearing Effect Output

The tearing effect output line supplies to the HOST a panel synchronization signal. This signal can be enabled or disabled by the set\_tear\_off (34h) and set\_tear\_on (35h) commands. The mode of the tearing effect signal is defined by the parameter of the set\_tear\_on (35h) and set\_tear\_scanline(44h) commands. The signal can be used by the HOST to synchronize internal VSYNC when displaying video images.

#### 5.4.1 Tearing Effect Line Mode

Mode 1, the tearing effect output signal consist of V-sync information only:



tvdh = The LCD display is not updated from the frame memory. tvdl = The LCD display is updated from the frame memory.

Mode 2, the tearing effect output signal consist of V-sync and H-sync information:



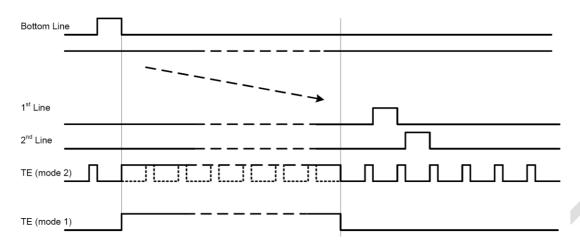
thdh = The LCD display is not updated from the frame memory. thdl = The LCD display is updated from the frame memory.

Mode 3, this mode turn on the tearing effect output signal when vertical scanning reachs line N.



N = The N-th scanning line which set by register N[15:0] of command STESL(44h).



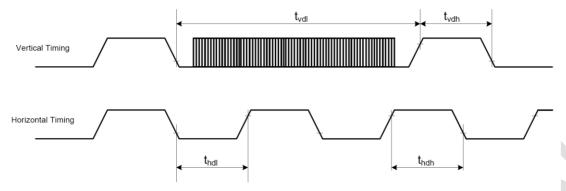


Note. During Sleep In mode, the tearing effect output signal is active low.



#### 5.4.2 Tearing Effect Line Timing

The tearing effect signal is described as below:

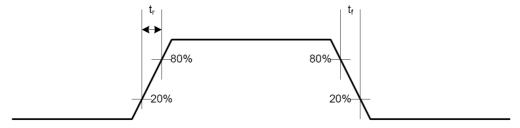


AC characteristics of Tearing Effect Signal (Frame Rate = 60.5Hz)

Symbol	Parameter	Тур.	Unit	Description
tvdl	Vertical timing low duration			1*frame time- tvdh
tvdh	Vertical timing high duration			tvdh =V Porch time if STS[15:0]=0. tvdh =31* line time if STS[15:0] not equal to 0.
thdl	Horizontal timing low duration			1* line time- 32*PCLK
thdh	Horizontal timing high duration	1.45	us	32*PCLK

#### Notes:

- 1. The timings apply when MADCTL B4=0 and B4=1
- 2. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the HOST and should be used as shown below to avoid tearing effect:

The Tearing Effect output line supplies to the HOST a panel synchronization signal. This signal can be enabled or disabled by the set\_tear\_off(34h), set\_tear\_on(35h) commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command. The signal can be used by the HOST to synchronize internal VSYNC when displaying video images.

TEON (35h)	TELOM (35h, 1 <sup>st</sup> bit)	TE signal Output
0	*	GND
1	0	TE (Mode 1)
1	1	TE (Mode 2)



# 6 Command

#### 6.1 Command List

Co	mman	nd											Default	
Page	1	Para.	W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP
CMD1	00h	-	w	NOP			<u>I</u>	No Arg	gument	<u>I</u>			-	-
CMD1	01h	-	W	Software reset				No Arg	gument				-	-
CMD1	04h	1st						ID1	[7:0]				00h	<b>)</b> -
CMD1	04h	2nd	R	Read display identification				ID2	[7:0]				80h	-
CMD1	04h	3rd		information				ID3	<u> </u>	_			00h	-
CMD1	05h	-	R	Read number of the errors on					7:0]				00h	-
CMD1	0Ah	1st	R	DSI Read display power mode	BSTON	IDMON	PTLON	SLPOUT	NORON	DISPON			08h	-
CMD1	0Bh	1st	R	Read display MADCTR	-	MX	-	-	RGB	-	-	_	00h	-
CMD1	0Ch	1st	R	Read display pixel format	SPI_IFPF_	VIPF2	VIPF1	VIPF0		IFPF2	IFPF1	IFPF0	77h	_
CMD1	0Dh	1st	R	Read display image mode	SEL 0		INVON	ALLPON	ALLPOFF	0	0	0	00h	-
	0Eh					0						ERR		-
CMD1		1st	R	Read display signal mode Read display self-diagnostic	TEON	М	0	0	0	0	0	checksum_	00h	-
CMD1	0Fh	1st	R	result	0	0	0	0	0	0	0	comp	00h	-
CMD1	10h	-	W	Sleep-in				No Arg	gument				-	-
CMD1	11h	-	W	Sleep-out				No Arg	gument				-	-
CMD1	12h	-	W	Partial display mode on				No Arg	gument				-	-
CMD1	13h	-	W	Normal display mode on				No Arg	gument				-	-
CMD1	20h	-	W	Display inversion off				No Arg	gument				-	-
CMD1	21h	•	W	Display inversion on	·			No Arg	gument				-	-
CMD1	22h	-	W	All pixel off				No Arg	gument				-	-
CMD1	23h	-	W	All pixel on				No Arg	gument				-	-
CMD1	28h	-	W	Display off				No Arg	gument				-	-
CMD1	29h	-	W	Display on				No Arg	gument				-	-
CMD1		1st	W					sc	[9:8]				00h	-
CMD1	ا ۔ ا	2nd	W					sc	[7:0]				00h	-
CMD1	2Ah	3rd	W	Set column start address				EC	[9:8]				01h	-
CMD1		4th	w					EC	[7:0]				8Fh	-
CMD1		1st	W					SP	[9:8]				00h	-
CMD1	i	2nd	w					SP	[7:0]				00h	-
CMD1	2Bh	3rd	w	Set row start address				EP	[9:8]				01h	-
CMD1		4th	w					EP	[7:0]				8Fh	-
CMD1	2Ch		w	Memory write				No Arg	gument				-	-
CMD1		1st	w					SR	[9:8]				00h	-
CMD1		2nd	W					SR	[7:0]				00h	-
CMD1	30h	3rd	w	Partial area				ER	[9:8]				01h	-
CMD1		4th	w						 [7:0]				8Fh	-
CMD1		1st	W						: - :[9:8]				00h	-
CMD1		2nd	w						[7:0]				00h	-
CMD1	31h	3rd	W	Vertical partial area					[9:8]				01h	-
CMD1		4th	w						[7:0]				8Fh	-
CMD1	34h	-	w	Tearing effect line off					gument				•	-
CMD1	35h	-	w	Tearing effect line on	0	0	0	0	0	SKIP M[1]	SKIP_M[0]	TELOM	00h	-
CMD1	36h	-	w	Scan direction control		-	I		TR[7:0]		1[0]	1	00h	-
CMD1	38h	-	w	Idle mode off					gument				-	-
CMD1	39h	-	w	Enter idle mode					gument				-	-
CMD1	3Ah	_	w	Interface Pixel Format	SPI_IFPF_	VIPF2	VIPF1	VIPF0	0	IFPF[2]	IFPF[1]	IFPF[0]	77h	-
CIMIDI	JAII		**	Interface Fixer Fulfilat	SEL	VITTZ	VIITI	VIITU	U	IFFF[2]	ir-re[i]	ir F F[V]	7711	_



CMD1         3Ch         -           CMD1         44h         1st           CMD1         45h         2nd           CMD1         45h         2nd           CMD1         45h         -           CMD1         51h         -           CMD1         52h         -           CMD1         53h         -           CMD1         56h         -           CMD1         56h         -           CMD1         58h         -           CMD1         63h         -           CMD1         64h         -           CMD1         66h         -           CMD1         70h         2nd           CMD1         70h         2nd	W W R R W W R W W W W W W W W W	Memory Continuous Write  Set tear scan-line  Get scan line  Deep standby  Write display brightness  Read display brightness  Write CTRL display  Read CTRL display  Write RAD_ACL function  Read RAD_ACL function  Set color enhancement  OPS CTR  OPS CTR2  Write HBM display brightness  Read HBM display brightness	0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0	BCTRL BCTRL 0 0 0 0 0 0 0 0 0	STS[ STS]  GTS[ GTS]  0  DBV  0  0  0  0  0	15:8] [7:0] (15:8] [7:0] 0 [7:0] [7:0] DD DD 0 0	0 0 0 0 0 0 SLR_EN	RAD_A	ACL[1:0] SLR_LEVE	00h 00h 00h 00h 00h 00h 00h 28h 28h 00h 00h	
CMD1         44h           CMD1         45h           CMD1         45h           CMD1         51h           CMD1         51h           CMD1         52h           CMD1         53h           CMD1         54h           CMD1         56h           CMD1         56h           CMD1         59h           CMD1         5Fh           CMD1         5Fh           CMD1         63h           CMD1         66h           CMD1         66h           CMD1         67h           CMD1         70h           CMD1         70h           CMD1         3rd	W R W W R W R W R W R W R W R W R W W R	Get scan line  Deep standby Write display brightness Read display brightness Write CTRL display Read CTRL display Write RAD_ACL function Read RAD_ACL function Set color enhancement Read color enhancement OPS CTR OPS CTR2 Write HBM display brightness Read HBM display brightness	0 0 0 0 0	0 0 0 0 0 0	BCTRL  BCTRL  0  0  0  0	STS GTS  GTS 0 DBV DBV 0 0 0 0	[7:0] [15:8] [7:0] 0 [7:0] [7:0] [7:0] DD DD 0	0 0 0	0 0 RAD_/ RAD_/ SLR_LEVE	0 0 ACL[1:0] ACL[1:0]  SLR_LEVE	00h 00h 00h 00h 00h 00h 28h 28h 00h	- - - - -
CMD1	R R W W R W R W R W R W R W R W W W W W	Deep standby Write display brightness Read display brightness Write CTRL display Read CTRL display Write RAD_ACL function Read RAD_ACL function Set color enhancement Read color enhancement OPS CTR OPS CTR2 Write HBM display brightness Read HBM display brightness	0 0 0 0 0	0 0 0 0 0 0	BCTRL  BCTRL  0  0  0  0	GTS	[15:8] [7:0] 0 [7:0] [7:0] DD DD 0 0	0 0 0	0 0 RAD_/ RAD_/ SLR_LEVE	0 0 ACL[1:0] ACL[1:0]  SLR_LEVE	00h 00h 00h 00h 00h 28h 28h 00h	- - - -
CMD1 45h	R W W R W R W R W R W R W W W W	Deep standby Write display brightness Read display brightness Write CTRL display Read CTRL display Write RAD_ACL function Read RAD_ACL function Set color enhancement Read color enhancement OPS CTR OPS CTR2 Write HBM display brightness Read HBM display brightness	0 0 0 0 0	0 0 0 0 0 0	BCTRL  BCTRL  0  0  0  0	O DBV DBV O O O O O O O	[7:0] 0 [7:0] [7:0] DD DD 0 0	0 0 0	0 0 RAD_/ RAD_/ SLR_LEVE	0 0 ACL[1:0] ACL[1:0]  SLR_LEVE	00h 00h 00h 00h 28h 28h 00h	- - -
CMD1 4Fh - CMD1 51h - CMD1 52h - CMD1 53h - CMD1 55h - CMD1 55h - CMD1 56h - CMD1 58h - CMD1 59h - CMD1 5Fh - CMD1 5Fh - CMD1 63h - CMD1 64h - CMD1 66h CMD1 67h CMD1 70h CMD1	W R W R W R W R W R W W W W W	Write display brightness Read display brightness Write CTRL display Read CTRL display Write RAD_ACL function Read RAD_ACL function Set color enhancement Read color enhancement OPS CTR OPS CTR2 Write HBM display brightness Read HBM display brightness	0 0 0 0 0	0 0 0 0 0 0	BCTRL  BCTRL  0  0  0  0	0 DBV DBV 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 [[7:0] [7:0] DD DD 0 0	0 0 0	0 0 RAD_/ RAD_/ SLR_LEVE	0 0 ACL[1:0] ACL[1:0]  SLR_LEVE	00h 00h 00h 28h 28h 00h	
CMD1 51h - CMD1 52h - CMD1 53h - CMD1 54h - CMD1 55h - CMD1 56h - CMD1 58h - CMD1 59h - CMD1 5Fh - CMD1 5Fh - CMD1 63h - CMD1 64h - CMD1 66h CMD1 67h CMD1 67h CMD1 70h CMD1 70h CMD1 70h CMD1 3rd	W R W R W W W W W W W	Write display brightness Read display brightness Write CTRL display Read CTRL display Write RAD_ACL function Read RAD_ACL function Set color enhancement Read color enhancement OPS CTR OPS CTR2 Write HBM display brightness Read HBM display brightness	0 0 0 0 0	0 0 0 0 0 0	BCTRL  BCTRL  0  0  0  0	DBV	[7:0] [7:0] DD DD 0 0	0 0 0	0 0 RAD_/ RAD_/ SLR_LEVE	0 0 ACL[1:0] ACL[1:0]  SLR_LEVE	00h 00h 28h 28h 00h 00h	-
CMD1 52h - CMD1 53h - CMD1 54h - CMD1 55h - CMD1 56h - CMD1 58h - CMD1 59h - CMD1 5Fh - CMD1 63h - CMD1 64h - CMD1 66h CMD1 67h CMD1 67h CMD1 70h CMD1 70h CMD1 70h CMD1 3rd	R W R W R W R W R W W W W	Read display brightness Write CTRL display Read CTRL display Write RAD_ACL function Read RAD_ACL function Set color enhancement Read color enhancement OPS CTR OPS CTR2 Write HBM display brightness Read HBM display brightness	0 0 0 0 0	0 0 0 0 0 0 0 ops2_ratio	0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	[7:0] DD DD 0 0	0 0 0	0 RAD_A RAD_A SLR_LEVE	0 ACL[1:0] ACL[1:0] SLR_LEVE	00h 28h 28h 00h 00h	-
CMD1 53h - CMD1 54h - CMD1 55h - CMD1 56h - CMD1 58h - CMD1 59h - CMD1 5Fh - CMD1 63h - CMD1 64h - CMD1 66h CMD1 67h CMD1 70h CMD1 70h CMD1 70h CMD1 3rd	W R W R W R W R W W W W W	Write CTRL display Read CTRL display Write RAD_ACL function Read RAD_ACL function Set color enhancement Read color enhancement OPS CTR OPS CTR2 Write HBM display brightness Read HBM display brightness	0 0 0 0 0	0 0 0 0 0 0 0 ops2_ratio	0 0 0 0 0	0 0 0 0	DD DD 0 0 0	0 0 0	0 RAD_A RAD_A SLR_LEVE	0 ACL[1:0] ACL[1:0] SLR_LEVE	28h 28h 00h 00h	-
CMD1 54h - CMD1 55h - CMD1 56h - CMD1 58h - CMD1 59h - CMD1 5Fh - CMD1 63h - CMD1 64h - CMD1 66h CMD1 67h CMD1 67h CMD1 70h CMD1 70h CMD1 3rd	R W R W W W W W	Read CTRL display Write RAD_ACL function Read RAD_ACL function Set color enhancement Read color enhancement OPS CTR OPS CTR2 Write HBM display brightness Read HBM display brightness	0 0 0 0 0	0 0 0 0 0 0 0 ops2_ratio	0 0 0 0 0	0 0 0 0 0	0 0 0	0 0 0	0 RAD_A RAD_A SLR_LEVE	0 ACL[1:0] ACL[1:0] SLR_LEVE	28h 00h 00h	
CMD1 55h - CMD1 56h - CMD1 58h - CMD1 59h - CMD1 5Fh - CMD1 63h - CMD1 64h - CMD1 66h CMD1 67h CMD1 67h CMD1 70h CMD1 70h CMD1 3rd	W R W R W W W W	Write RAD_ACL function Read RAD_ACL function Set color enhancement Read color enhancement OPS CTR OPS CTR2 Write HBM display brightness Read HBM display brightness	0 0 0 0	0 0 0 0 0 0 ops2_ratio	0 0 0 0	0 0 0	0 0	0	RAD_/ RAD_/ SLR_LEVE	ACL[1:0] ACL[1:0] SLR_LEVE	00h 00h	-
CMD1 56h - CMD1 58h - CMD1 59h - CMD1 5Eh - CMD1 5Fh - CMD1 63h - CMD1 64h - CMD1 66h CMD1 67h CMD1 70h CMD1 70h CMD1 3rd	R W R W W R W	Read RAD_ACL function Set color enhancement Read color enhancement OPS CTR OPS CTR2 Write HBM display brightness Read HBM display brightness	0 0 0	0 0 0 0 ops2_ratio	0 0 0 0	0 0	0	0	RAD_A	ACL[1:0] SLR_LEVE	00h	-
CMD1 58h - CMD1 59h - CMD1 5Eh - CMD1 5Fh - CMD1 63h - CMD1 64h - CMD1 66h CMD1 67h CMD1 70h 2nd CMD1 70h 3rd	W R W W W R	Set color enhancement Read color enhancement OPS CTR OPS CTR2 Write HBM display brightness Read HBM display brightness	0 0 0	0 0 0 ops2_ratio	0 0 0	0	0		SLR_LEVE	SLR_LEVE		-
CMD1 59h - CMD1 5Eh - CMD1 5Fh - CMD1 63h - CMD1 64h - CMD1 66h CMD1 67h CMD1 70h 2nd CMD1 70h 3rd	R W W R W	Read color enhancement  OPS CTR  OPS CTR2  Write HBM display brightness  Read HBM display brightness	0	0 0 ops2_ratio	0	0		SLR_EN			00h	-
CMD1 5Eh - CMD1 5Fh - CMD1 63h - CMD1 64h - CMD1 66h CMD1 67h CMD1 1st CMD1 70h 2nd CMD1 3rd	W W W R W	OPS CTR  OPS CTR2  Write HBM display brightness Read HBM display brightness	0	0 ops2_ratio	0		0			LU		
CMD1 5Fh - CMD1 63h - CMD1 64h - CMD1 66h CMD1 67h CMD1 1st CMD1 70h 2nd CMD1 3rd	W W R W	OPS CTR2 Write HBM display brightness Read HBM display brightness		ops2_ratio		_	U	SLR_EN			00h	-
CMD1 5Fh - CMD1 63h - CMD1 64h - CMD1 66h CMD1 67h CMD1 1st CMD1 70h 2nd CMD1 3rd	W W R W	OPS CTR2 Write HBM display brightness Read HBM display brightness		ops2_ratio		0	0	0			00h	_
CMD1 63h - CMD1 64h - CMD1 66h CMD1 67h CMD1 1st CMD1 70h 2nd CMD1 3rd	W R W	Write HBM display brightness Read HBM display brightness	<u> </u>	2		ops2_ratio			ops2_mod		_	_
CMD1 64h - CMD1 66h CMD1 67h CMD1 1st CMD1 70h 2nd CMD1 3rd	R W	Read HBM display brightness	STS[7:0]				$\vdash$					
CMD1 66h  CMD1 67h  CMD1 1st  CMD1 70h 2nd  CMD1 3rd	w	1 1 1									00h	$\vdash$
CMD1 67h  CMD1 1st  CMD1 70h 2nd  CMD1 3rd	w			1	1				l		00h	$\vdash$
CMD1 1st CMD1 70h 2nd CMD1 3rd		HBM enable	-	-	-	-	-	-	HBM_en	-	00h	
CMD1 70h 2nd CMD1 3rd	w	Deep idle enable	-	-	-	-	-	-	-		00h	
CMD1 3rd	•••	COLSET				R_000	00[7:0]				00h	
	w	COLSET				G_000	00[7:0]				00h	
	W	COLSET				B_000	00[7:0]				00h	
CMD1 1st	w	COLSET				R_000	01[7:0]				00h	
CMD1 71h 2nd	w	COLSET				G_000	01[7:0]				00h	
CMD1 3rd	w	COLSET				B_000	01[7:0]				FFh	
CMD1 1st	w	COLSET				R_001	10[7:0]				00h	
CMD1 72h 2nd	w	COLSET				G_001	10[7:0]				FFh	
CMD1 3rd	w	COLSET									00h	
CMD1 1st	w	COLSET									00h	
CMD1 73h 2nd	w	COLSET									FFh	
CMD1 3rd	w	COLSET									FFh	
CMD1 1st	w	COLSET			,						FFh	
CMD1 74h 2nd	w	COLSET									00h	
CMD1 3rd	w	COLSET									00h	
CMD1 1st	w	COLSET									FFh	
CMD1 75h 2nd		COLSET										
CMD1 3rd	w	COLSET										
CMD1 3rd CMD1 1st	-	COLSET										
CMD1 76h 2nd	W	COLSET										
CMD1 3rd	W	COLSET										
CMD1 1st	w	COLSET										
CMD1 77h 2nd	W	COLSET									FFh	
CMD1 3rd	W	COLSET									FFh	
CMD1 1st	W	COLSET									00h	<del>                                     </del>
CMD1 78h 2nd	W	COLSET									00h	<b> </b>
CMD1 3rd	W	COLSET									00h	
CMD1 1st	W	COLSET									00h	
CMD1 79h 2nd	W	COLSET				G_100	01[7:0]				00h	
CMD1 3rd	W	COLSET				B_100	01[7:0]				FFh	
CMD1 1st	W	COLSET				R_101	10[7:0]				00h	
CMD1 7Ah 2nd	W	COLSET				G_101	10[7:0]				FFh	
CMD1 3rd	W	COLSET				B_101	10[7:0]				00h	
CMD1 1st	W	COLSET				R_101	11[7:0]				00h	
CMD1 7Bh 2nd	W	COLSET				G_101	11[7:0]				FFh	
CMD1 3rd	W	COLSET				B_101	11[7:0]				FFh	



1	i i	i		I	1									
CMD1		1st	W	COLSET					00[7:0]				FFh	
CMD1	7Ch	2nd	W	COLSET				G_11	00[7:0]				00h	
CMD1		3rd	W	COLSET				B_110	00[7:0]				00h	
CMD1		1st	W	COLSET				R_110	01[7:0]				FFh	
CMD1	7Dh	2nd	W	COLSET				G_11	01[7:0]				00h	
CMD1		3rd	W	COLSET				B_110	01[7:0]				FFh	
CMD1		1st	W	COLSET				R_11	10[7:0]				FFh	
CMD1	7Eh	2nd	W	COLSET				G_11	10[7:0]				FFh	
CMD1		3rd	W	COLSET				B_11	10[7:0]				00h	
CMD1		1st	W	COLSET				R_11	11[7:0]				FFh	
CMD1	7Fh	2nd	W	COLSET				G_11	11[7:0]				FFh	
CMD1		3rd	W	COLSET				B_11	11[7:0]				FFh	
CMD1	80h	1st	w	COLOPT	-	RGB111_o pt	-	-	RGB4bit_ en	gray256_cc or[2]	ol gray256_o olor[1]	gray256_ color[0]	07h	
CMD1		1st	R					SID	[7:0]				D0h	-
CMD1		2nd	R					SID[	15:8]				01h	-
CMD1	A1h	3rd	R	Read DDB				MID	[7:0]				80h	-
CMD1		4th	R					MID	[15:8]				90h	-
CMD1		5th	R		1	1	1	1	1	1	1	1	FFh	-
CMD1		1st	R					SID	[7:0]			>	D0h	-
CMD1		2nd	R					SID[	15:8]				01h	-
CMD1	A8h	3rd	R	Read DDB Continuous				MID	[7:0]				80h	-
CMD1		4th	R					MID	15:8]		_		90h	-
CMD1		5th	R		1	1	1	1	1	1	1	1	FFh	-
CMD1	AAh	-	R	Read first checksum				FCS	[7:0]				00h	-
CMD1	AFh	-	R	Read continuous checksum				CCS	[7:0]				00h	-
CMD1	C2h			Set_DSIP Mode	0	0	0	0	0	0	DM1	DM0	00h	-
CMD1	C4h			Set_DSPI Mode	SPI_WRA M	0	DSPI_CFG 1	DSPI_CFG 0	0	0	0	DSPI_EN	00h	-
CMD1	DAh	-	R	Read display identification				ID1	[7:0]			•	00h	-
CMD1	DBh	-	R	information				ID2	[7:0]				80h	-
CMD1	DCh		R	(the same as 04h)				ID3	[7:0]				00h	-
CMD1	FEh	-	w	Write CMD mode page	0	0	0		С	MD_Page[4	:0]	_	00h	-
CMD1	FFh	-	R	Read CMD page Status	0	0	0		CI	MD_Status[4	1:0]		00h	-



# 6.2 Command Description

# NOP (0000h)

0000Н					NOP (	<b>No Op</b>	eration	1)					
Inst/Para	R/W	Ado	Iress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
ilisvi ala	17/77	MIPI	Other	D10 0	"	Do	D3	DŦ		02			TILX
NOP	W	00h	0000h				No Arg	gumen	t				
Description	Th	is comm	and is an	empty comr		does i		e any	effect o	on the o	display	modul	e.
Restriction	None												
			itus						ilabilit	:y			
				le On, Idle I									
		No	rmal Mod	le On, Idle I	Mode C	n, Sle	ep Out	Yes					
		Pa	rtial Mode	e On, Idle M	lode O	ff, Slee	p Out	Yes					
Register Availability		Pa	rtial Mode	e On, Idle M	lode O	n, Slee	p Out	Yes	;				
Availability		Sle	ep In					Yes	3				
					<u> </u>								
			St	atus		Г	Default	Value					
				wer On Sec	quence		V/A	Value					
			sv	V Reset		1	N/A						
Default			HV	V Reset		N	N/A						
						1							
Flow Chart	None												



# SWRESET(0100h): Software Reset

0100H				SW	/RESE	T(Soft	ware Re	eset)					
		Add	dress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SWRESET	W	01h	0100h				No Arg	umen	t				
Description	paramete	ers to the	ir S/W Re	set default v	alues.	(See d	efault ta	bles ii	n each				
Restriction		comman	d cannot							nters S	leep-In	mode.	. Do not
			atus							y			
		No	rmal Mod	de On, Idle I	Mode C	Off, Sle	ep Out	Yes					
Register						-							
Availability							_						
			ep In	e On, idle iv	lode O	No Argument  en, it causes software reset. It resets the commands s. (See default tables in each command description.  uring Sleep Out sequence. ame period until the WT030 enters Sleep-In mode. Example of the command description.  Availability  e Off, Sleep Out Yes  e On, Sleep Out Yes  on, Sleep Out Yes  on, Sleep Out Yes  Yes  Default Value							
		Sit	зер ш		7			163	)				
			St	atus			Default '	Value	!				
			Po	wer On Sec	quence	) I	N/A						
Default			SV	V Reset		ı	N/A						
			HV	W Reset		I	N/A						
Flow Chart			Display Set 0 to S	y whole blank screen Commands W Default Value pp In Mode						Pro See	ommand aramete Display Action Mode		



#### RDDID(0400h~0402h): Read Display ID

0400H							RDDI	D						
		Add	ress											
Inst/Para	R/W	MIPI	Other	D15	5-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
			0400h	х	[	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	00
RDDID	R	04h	0401h	х		ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	80
			0402h	х		ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	00
Description	The 2 <sup>nd p</sup> The 3 <sup>rd</sup> pa Note: Co	arameter arameter mmands	(ID1): the (ID2): the (ID3): the RDID1/2/3 spectively.	Modu Modu (DAh	ıle/driv le/driv	ver ver ver ID	sion ID		espon	d to the	param	neter 1	, 2, 3 of	f
Restriction	_													
		Statu	IS						Availa	ability				
		Norn	nal Mode	On, Id	lle Mo	de Off	, Sleep	Out	Yes					
Register		Norn	nal Mode	On, Id	lle Mo	de On	, Sleep	Out	Yes					
Availability		-	al Mode (		_		<u> </u>		Yes					
			al Mode (	On, Idl	e Mod	de On,	Sleep	Out	Yes					
		Slee	o In						Yes					
		Status				ult Val	ue	Refe	re MTI	D				
Default		Power	On Seque	ence	_	value			:00h / I		h / ID3	=00h		
		SW Res	set		MTP	value		ID1=	:00h / I	D2=80	h / ID3	=00h		
		HW Re	set		MTP	value		ID1=	00h / I	D2=80	h / ID3	=00h		
Flow Chart		ID1[  Send 2nd ID2[	paramet 7:0] d parame 7:0]	ter							Para Dis Ac Mo	gend mand meter play tion ode uentia		



# RDNUMED(0500h): Read Number of Errors on DSI

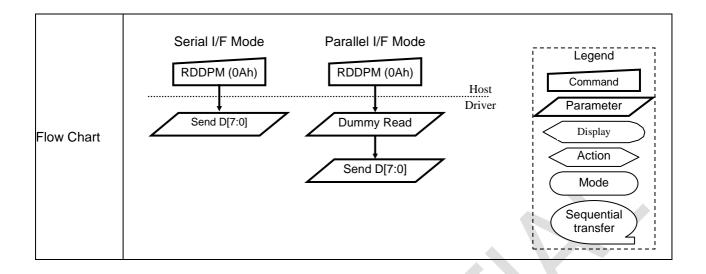
0500H						RDNU	MED						
		Add	lress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDNUMED	R	05h	0500h	х	D7	D6	D5	D4	D3	D2	D1	D0	00
Description	the bits D[60] I D[7] is s D[70] I sent the	is below bits are to set to "1" bits are s e first par	elling a nu if there is et to "0"s ameter in	ng a number umber of the overflow wit (as well as F formation (= MIPI DSI or	parity on the parity of the pa	errors. 0] bits. //(0Eh) ad fun	's D0 ar	e set ' compl	'0" at the	ne sam	e time)	after t	
Restriction	-									X			
Register Availability		N P P	lormal Mo	ode On, Idle ode On, Idle de On, Idle de On, Idle	Mode	On, S Off, SI	leep Ou	ut Yeut Yeut Yeut Yeut	vailabi es es es es	lity			
Default			P	tatus ower On Se W Reset W Reset	quenc	е	Defaul 00h 00h 00h	t Valu	e				
Flow Chart	RDE	P[7:0]=	paramete					Lege Comm Param Displ Actic Mod Seque	neter ay on de	7			



# RDDPM (0A00h): Read Display Power Mode

0A00H				RDD	PM (R	ead D	isplay	Powe	r Mod	e)			
Inst/Para	R/W	Add	dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IIISI/Pala	R/VV	MIPI	Othe		יט	D6	DS	D4	D3	DZ	וט	DU	ПЕЛ
RDDPM	R	0Ah	0A00	h x	D7	D6	D5	D4	D3	D2	D1	D0	08
	This co	mmand	indicat	es the cur	rent st	atus of	the di	splay a	as des	cribed	in the	table b	elow:
	Bi	t Sym	nbol	Descripti	on			omme					
	D7	BST	ON	Booster Vo	Itage S	tatus	'0'	=Booste	er off				
	D6	IDMC	ON	Idle Mode (	On/Off		'0'	= Idle N = Idle N	lode Of	f			
Description	D5	PTLC	ON	Partial Mod	le On/O	ff	'0'	= Partia	al Mode				
2 coonpact	D4	SLPC		Sleep In/Oເ			'0'	= Sleep	ln .				
	D3	NOR	ON	Display No On/Off	rmal Mo	ode	'1' '0'	= Norm = Partia	al Displ	ay, ay			
	D2	DISC	N	Display On	/Off		'1'	= Displ = Displ	ay On,				
	D1 D0	Rese Rese					0						
		Rese	iveu				10						
		_											
			Status		_					<u>Availa</u>	bility		
			Norma	al Mode C	n, Idle	• Mode	Off,	Sleep	Out	Yes			
Register			Norma	al Mode C	n, Idle	• Mode	On,	Sleep	Out	Yes			
Availability			Partia	I Mode O	n, Idle	Mode	Off, S	leep C	Out '	Yes			
				I Mode O	n, Idle	Mode	On, S	leep C		Yes			
		Ļ	Sleep	In					,	Yes			
			S	tatus			Def	fault V	alue				
Defect				ower On	Seque	nce	081						
Default			S	W Reset			180	1					
			Н	W Reset			08h	1					







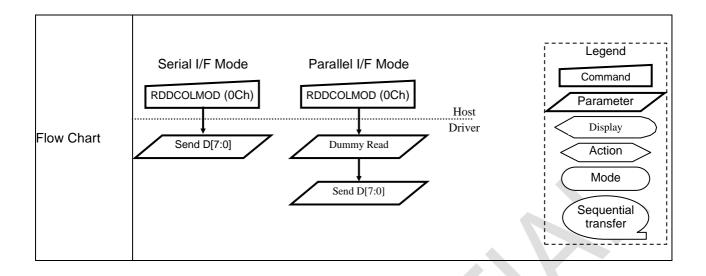
# RDDMADCTR (0B00h): Read Display MADCTR

0B00H			F	RDDMAD	CTR (	Read	Displa	y MAI	OCTR)	)			
		Addı											
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	d in the table	D0	HEX
RDDMADCTR	R	0Bh	0B00h	X	D7	D6	D5	D4	D3	D2	D1	D0	00
	This com	mand in	dicates	the curre	nt stat	us of t	he disp	olay as	descr	ibed ir	the ta	ble be	low:
	Bit	Symbo	N.	Description	on.		Com	ment					
			)	Column A		<u> </u>		creasin	g in ho	rizontal			
	D6	MX		Incremen	ıt		1: D	ecreasi	ng in h	orizonta			
Description	D3 othe	RGB	_	RGB/BG	R Orde	r	11′=	BGR, "(	)"=RGE	3			
Description	rs	Reserv	/ed	-			-						
											•	d able bel	
			tatus							ailabi	lity		
		N	ormal N	lode On	Idle N	lode C	Off, SI	ер Оі	ıt Ye	S			
Register		N	ormal N	lode On	Idle N	/lode C	On, Sle	ер Оі	ıt Ye	S			
Availability		P	artial M	ode On,	ldle M	ode O	ff, Sle	ep Ou	t Ye	es			
		P	artial M	ode On,	ldle M	ode O	n, Sle	ep Out	t Ye	s			
		S	leep In						Ye	s			
		01.1						4.11				1	
		Statu						ault Va	alue			-	
Default				equence	;		00h					_	
		SW	Reset				00h						
		HW	Reset				00h	l					
Flow Chart	RDD	MADCTR Send D[7	(0Bh)		DDMAD(	I/F Mo	$\neg$	Ho: Driv		P2	ommand aramete Display Action Mode		



# RDDCOLMOD (0C00h): Read Display Pixel Format

0C00H			R	DDCOLM	OD (R	ead Di	splay	Pixel	Forma	at)			
		Addr	ess	_									
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDCOLMOD	R	0Ch	0C00h	Х	SPI_I FPF	VIPF[ 01	VIPF[ 01	VIPF[ 01	0	IFPF[2	]IFPF[1]	IFPF[0]	77
	This could be seen as a country of the seen as	IFPF_SE IFPF_SE used DPI rol Interf B bit/pixel port IF: SI B bit/pixel poort IF: S B bit/pixel	sets the L(3Ah-B L(3Ah-B interface ace Cole (256 cole P13/SP14 (256 cole SP13/SP1 (8 colors	pixel forma (7) = 1: The (7) = 0: The (7) then the (8) (8) (7) (8) (8) (8) (8) (8) (9) (8) (8) (8) (8) (8) (8) (8) (8) (8) (8	e VIPF e IFPF corresp 56 Gra	[2:0] pi [2:0] pi pondin	xel for xel for g bits	mat us mat us	ed by ed by	eter a	PI inte PI / M	rface CU inte	erface
	16bit	oport IF: \$ /pixel (65, /pixel (262 /pixel (16.	536 colo 2,144 co	ors) lors)				1 1 1	0 1		1 0 1		
		5	Status						Av	ailabi	litv		
				Mode On,	dle M	ode O	ff, Sle	ep Out			,		
Register		ì	Normal I	Mode On,	dle M	ode O	n, Sle	ep Out	Ye	s			
Availability		I	Partial M	lode On, lo	dle Mo	de Off	, Slee	p Out	Ye	s			
		1	Partial M	lode On, lo	dle Mo	de On	, Slee	p Out	Ye	s			
		3	Sleep In						Ye	s			
			atus					ault Va	alue				
Default				Sequence			77h					4	
			/ Reset				77h					4	
		HV	V Reset				77h						





# RDDIM (0D00h): Read Display Image Mode

0D00H				RDDIM	(Read	d Disp	lay Ima	age M	ode)				
		Ade	dress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDIM	R	0Dh	0D00h	х	D7	D6	D5	D4	D3	D2	D1	D0	00
	The disp	olay mo	dule returr	ns the disp	olay im	age m	ode st	atus.				1	
	Bit D7	Sym	bol	Descri	ption		Comr	nent					
	D6	Rese	erved				'0'		:- 6			V	
Description	D5	INVO	N	Inversi	on On	/Off	"0" =	Inversi Inversi	on is C	Off			
Description	D4	ALLO	NC	All Pix	el On		'1' = V	Normal White o	lisplay				
	D3	ALLO	OFF	All Pix	el Off			Normal Black d		ıy	•		
	D2~ D0	Rese	erved				'000'			,			
			-										
			Status Normal M	ode On I	dlo Ma	odo Ot	f Sloc	n Out		ilabilit	: <b>y</b>		
D '. (		-	Normal M					•					
Register Availability		-	Partial Mo			$\overline{}$		•	Yes				
		-	Partial Mo						Yes				
			Sleep In				<u> </u>		Yes				
		St	tatus				Def	ault Va	alue			1	
			ower On	Sequence	<b>)</b>		00h						
Default		SI	W Reset				00h	1					
		H	W Reset				00h						
Flow Chart	R	DDIM (0D	0h)	RI	DDIM (0) ummy R	Dh)		Host  Driver			Com Para Dis	gend mmand meter splay ction ode uential nsfer	



# RDDSM (0E00h): Read Display Signal Mode

0E00H		-		RDDS	SM (Re	ead Dis	play S	Signal	Mode)				
		Add	dress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDSM	R	0Eh	0E00h	x	D7	D6	D5	D4	D3	D2	D1	D0	00
	The disp			rns the D	isplay	l Signal	Mode.						
	Bit	Sym		Descript	tion			ment					
	D7	TEON	N	Tearing E On/Off				On, "0"					
	D6	TELC	M	Tearing e mode	effect lin	е		mode1 mode2					
Description	D5	Rese					'0'						
Booonplion	D4 D3	Rese Rese					'0'		<i>-</i>				
	D2	Rese					,0,						
	D1	Rese					'0'						
	D0	Error	on DSI	Error on	DSI		'0' = 1 '1' = 1	No Erro Error	r				
		3	Status						Ava	ailabili	ty		
		ı	Normal I	Mode On	, Idle N	Node C	ff, Sle	ep Ou	t Yes	5			
Register		ı	Normal I	Mode On	, Idle N	/lode C	n, Sle	ep Out	Yes	5			
Availability		F	Partial M	lode On,	ldle M	ode Of	f, Slee	p Out	Yes	3			
		F	Partial M	lode On,	ldle M	ode O	n, Slee	p Out	Yes	5			
		\$	Sleep In						Yes	3			
		S	status		<u> </u>		D	efault '	Value				
Default		P	ower O	n Sequer	nce		00	)h					
Doradit		S	W Rese	t			00	)h					
		H	IW Rese	t			00	)h					
						/E 5.4				 !	L	egend	
	Se	rial I/F	Mode	Pa	arallel	/F Mod	le —				Co	mmand	$\exists \   \  $
	F	RDDSM (0	DEh)		RDDSN	И (0Eh)					Pai	rameter	
								Host Drive			Г	Display	$\leq$
Flow Chart		Send D[7	7:0]		Dumm	y Read	7	Diive	L	 	$\rightarrow$	Action	$\langle \cdot   \cdot  $
											$\geq$		$< \Box$
					Send 1	D[7:0]	7			!		Mode	$\mathcal{I} \mid$
						- [, ]				!	Sec	quential	
												ansfer	4
										<u> </u>			<del></del>



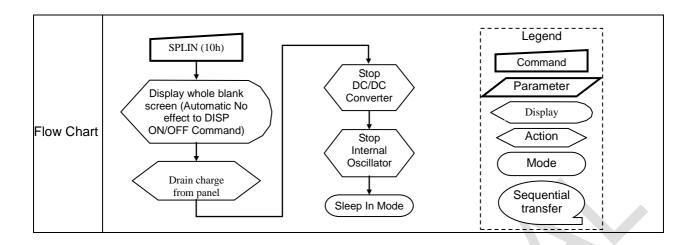
# RDDSDR (0F00h): Read Display Self-Diagnostic Result

0F00H			R	DDSDR	(Read	Displa	y Self	-Diagno	ostic F	Result)			
		Ado	dress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDSDR	R	0Fh	0F00h	Х	0	0	0	0	0	0	0	checksu m_comp	00
	The dis	splay m	odule retu	irns the	self-dia	agnostic	result	s follow	ing a S	Sleep C	out con	nmand.	
	Bit	t Syr		escription				Comm	nent				
	DO	) Res	served ch	necksum_	_comp			'0'					
Description													
,													
			Status							ailabili	ty		
			Normal					<u> </u>					
Register			Normal										
Availability			Partial N			_		-					
			Partial M Sleep In		i, idle i	Wode (	on, Sie	ep Out	Ye				
		Į	Sieep iii			<del>/</del>			16	<b>.</b>			
		-	Status	. 0				Default	Value				
Default		-	Power O	·	ence			00h					
			SW Rese					00h 00h					
			UAA VESE	FL				7011					
		Opriol I/	T Mada		Davalla	1 1/E NA	1 -					egend	
		Seriai i/i	F Mode		Paralle	II/F Mo	ode			; ; ;	С	ommand	$\exists \   \  $
	L	RDDSD	R (0Fh)		RDDS	STR (0Fh	)	11			Pa	arameter	
			,					Hos Driv				Display	
Flow Chart	/	Send I	D[7:0]		Dun	nmy Read	$\mathcal{I}$			 		Action	>
						<u> </u>				!		Mode	
				_	Sen	d D[7:0]	_/			; ;	SF	equentia	$\begin{bmatrix} & & & & & & & & & & & & & & & & & & &$
										 		ransfer	3
										<u> </u>			



# SLPIN (1000h): Sleep In

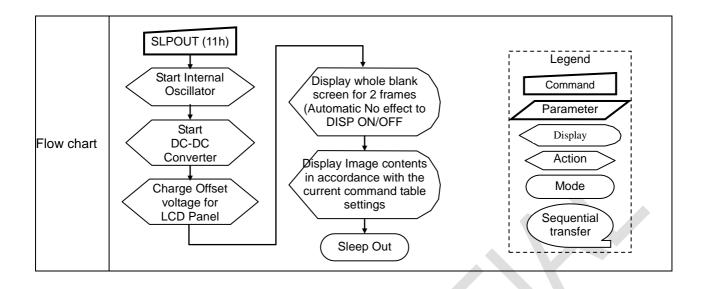
1000H					S	LPIN (	Sleep	ln)					
		Ad	dress										
Inst/Para	R/W	MIDI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
SLPIN	W	10h	1000h				No A	rgume	nt				
Description	In this m scannin values. After Sle display a Out-mo	node the g is stoemer in contract the green and the green	I causes to be DC/DC popped. The command information an internation in the command an internation in the command in the comman	converted e control l , user car tion is vali	r is sto Interfac n send id durir	pped, I ce such PCLK, ng 2 fra	nterna n as reg HS ar nmes if	l displa gisters nd VS i	y oscil is still nforma	lator is workin	stopping and	ed, and keeps i	l panel ts blank
Restriction	Sleep Ir It must v stabilize It must v	n Mode wait 5m e. wait 12	I has no e can only nsec befo Omsec af nand can	be exit by re sending ter sendin	the Signext	leep O comma	ut Com and for	nmand the su	(11h). pply vo	oltages	and cl	ock cir	
			01-1				<u> </u>			- *1 - 1. *1*	4		
		-	Status	Mode On	Idlo N	lodo C	off Clo	on Ou		ailabili	ty		
								<u> </u>	_	-			
Register		-		Mode On			•	•		-			
Availability				lode On,				<u> </u>		5			
				lode On,	Idle M	ode O	n, Slee	p Out	Yes	5			
			Sleep In						Yes	3			
Default			SW	us /er On Se Reset Reset	quence	e S	Default Bleep Ir Bleep Ir Bleep Ir	n Mode n Mode	)				





# SLPOUT (1100h): Sleep Out

1100H					SLPC	UT (S	leep O	ut)					
		Add	Iress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	W	11h	1100h				No A	Argum	ent				
Description	module a	re enable	d. The ho	ost proce	essor s	ends P	CLK, I	HS and	d VS in	format	ion to	display	,
Restriction	is not in S command circuits to The host sending a the registe display de	Sleep mod I before so stabilize processo I Sleep-Ir ers when evice who he displa	de. The he cending and the commar exiting the loading ymodule	ost proc nother c ait 120 m nd. The c ne Sleep g the reg is not in	essor romman nilliseco display mode isters i	must wond. This  onds af  modul  There  f the fa	ait five s delay fter ser e loads shall r ctory c	millise  allows  ading a  s the d  not be  default	econds s the s a Sleep isplay any ab and re	after supply volume of Out commodule on ormal egister volume of the ormal egister volume egister vo	ending voltage ommar e's defa Il visua values	this and the same the	clock  ore lues to t on the e same
		Sta	itus						Avail	ability			
			rmal Mod	le On, lo	dle Mo	de Off	Sleep	Out	Yes	<u></u>			
Register		No	rmal Mod	de On, Id	dle Mo	de On,	Sleep	Out	Yes				
Availability		Par	tial Mod	e On, Id	le Moc	le Off,	Sleep	Out	Yes				
		Par	tial Mod	e On, Id	le Mod	le On,	Sleep	Out	Yes				
		Sle	ep In						Yes			the display to display Normal Mod	
Default			SW	us er On S Reset Reset	equenc	се	Defaul Sleep Sleep Sleep	In Mod In Mod	le le				





# PTLON (1200h): Partial Display Mode On

1200H				PTI	LON (P	artial [	Display	Mode	On)				
Inst/Para	R/W		ress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
PTLON	W	12h	1200h				No	Argum	ent				
Description	Display To leave written.	Mode we Partial The hoses for two	rindow is Display st proces	he displa describ Mode, t ssor cont after this	ed by the Northian	he Part mal Dis o send	ial Area play M PCLK,	a (30h) ode Or HS an	comma n (13h) d VS in	and. comma formati	and sho on to d	uld be isplay	
Restriction	This cor	nmand	has no e	effect wh	en Part	ial Disp	olay Mo	de is a	Iready	active.			
Register Availability		1	Normal No		n, Idle n, Idle N	Mode (	On, Slee	ep Out	t Yes Yes	i i	У		
Default			Power SW R HW R	On Sec	quence	No No	fault Va rmal di rmal di rmal di	splay n splay n	node O	n			
Flow Chart	Refer to	Partial	Area (30	Dh)									



# NORON (1300h): Normal Display Mode On

1300H				NORON (No	rmal I	Displ	ay Mo	de O	n)				
		Add	ress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NORON	W	13h	1300h			No /	Argun	nent		l		•	
Description	as Partia The hos	al Displa t proces	ay mode ssor sen	he display modulo ds PCLK, HS and nand is sent whe	l VS i	nform	ation	to Ty <sub>l</sub>	oe 2 d	lisplay	/ mod	lules t	wo
Restriction	This cor	nmand	has no e	ffect when Norma	al Dis	play r	node	is alre	eady a	active			
		_	Status							abilit	y		
		<u> </u>	Normal I	Mode On, Idle M	ode C	Off, S	leep (	Out	Yes				
Register			Normal I	Mode On, Idle M	ode (	On, SI	leep (	Out	Yes				
Availability		I	Partial M	lode On, Idle Mo	de O	ff, Sle	еер О	ut	Yes				
		ı	Partial M	lode On, Idle Mo	de O	n, Sle	еер О	ut	Yes				
		3	Sleep In						Yes				
			Sta	tus	D	efault	Value	9					
Default				ver On Sequence			Displ						
				Reset			Displ						
			HW	Reset	N	ormal	Displ	ay Mo	ode O	n			
Flow Chart	Refer to	the des	scription	of Partial Area (3	000h)	)							



# INVOFF (2000H): Display Inversion Off

2000H				IN	VOFF (	Displa	y Inve	rsion (	Off)				
		Addres	SS			Τ			T				
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVOFF	W	20h	2000h		1	1	No A	rgumer	nt	•		•	
				the displa		le to sto	op inve	erting th	ne ima				
		1 1	Input Ima	age	1				ı	D II	isplay I I	Pane	 
Description								> .					
Restriction	This o	commar	nd has no	effect whe	n the di	splay r	nodule	e is not	inverti	ng the	displa	y imag	e.
			Status		1.11. 5	L. J. 6	" 01-			ilabilit	У		
D				I Mode On									
Register Availability				I Mode On Mode On,					Yes				
			-	Mode On,		_			Yes				
			Sleep		Talo III	<u> </u>	., 0.00	p Gut	Yes				
Default		7	P S	tatus ower On S W Reset W Reset	equenc	e D	isplay isplay	Value Inversi Inversi Inversi	on off				
Flow Chart			INVC	Inversion Or Mode DFF (20h) Inversion OF Mode								Legend Commar Paramet Display Action Mode	er



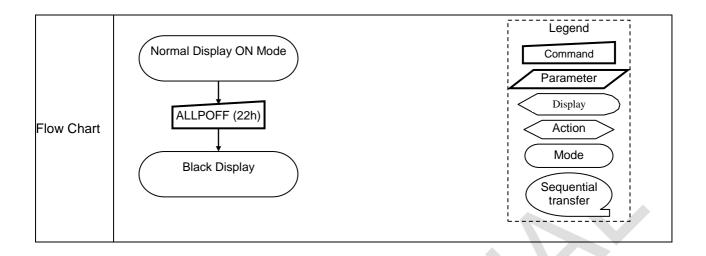
# INVON (2100H): Display Inversion On

2100H				IN	VON (I	Display	/ Invers	sion O	n)				
		Add	dress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVON	W	21h	2100h			•	No	Argum	ent	ı			
			causes the		/ modu	le to inv	vert the	image	data o	nly on t	he disp	olay dev	vice.
		Inp	ut Image						!	Display	Panel		-
					_			_					_
Description					_			_					_
							$\geq$						_
					<u> </u>			_					_
	+	+++	+++	++	<del></del>								_
Restriction	This cor	mmand l	has no eff	ect whe	n modu	ıle is alı	ready ir	n invers	sion on	mode.			
			<b>.</b>							1 1114			
			Status Normal M	ode On	Idle M	lode O	ff Slee	n Out	Yes	ability			
Daniela			Normal M						Yes				
Register Availability			Partial Mo	-		_			Yes				
			Partial Mo						Yes				
			Sleep In				•		Yes				
			Status			De	fault V	alue					
Default				On Seq	uence		splay Ir						
			SW Re				splay Ir splay Ir						
			·			'							
									1		egend	<b>-</b>	
		Display Iı N	nversion O Mode	FF )					į		mmand		
			T						_	Par	ameter		
		INV	_ <b>↓</b> ON (21h)						į	$\leq$ _D	isplay	$\supset$	
Flow Chart		<u> </u>	T	l					 	$\leq$ A	ction	>	
		Display I	nversion C	ON					į	$\overline{}$	/lode	$) \parallel$	
			Mode						 	Sec	quential		
									į	tra	ansfer	$\exists \ data$	



# ALLPOFF (2200H): All Pixel Off

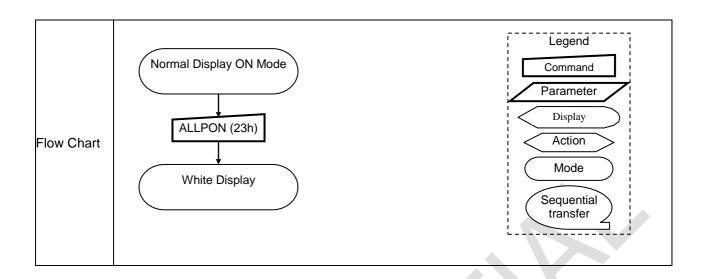
2200H						ALLPO	)EE						
220011		Ι Δ.	-1 -1		I	ALLF	JFF	I	ı	I	ı	ı	I
L 1/1D	D 44/	A	ddress	D45.0	D.7	<b>D</b> 0	DE	<b>D</b> 4	<b>D</b> 0	<b>D</b> 0	D.4	<b>D</b> 0	. IEV
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
ALLPOFF	W	22h	2200h				No A	rgumer	nt				
Description	On/Of	f regist ommar	nd turns the er can be on the does not the d	n or off. change an			·	ut mod		olay P		Displa	y •
Restriction	this m	ode. Th	n", "Normal ne display p tial Mode C	anel is sho	wing th								
			Status						Availa	bility			
Pogistor				Mode On, I					Yes Yes				
Register Availability				Mode On, I lode On, Id					Yes				
				lode On, Id					Yes				
			Sleep In	,			<u> </u>		Yes				
Default	)		SW F	r On Seque	ence	Disp Disp	ault Va blay Inv blay Inv blay Inv	ersion ersion	off				





# ALLPON (2300H): All Pixel On

2300H						ALLP	ON						
Inst/Para	R/W	Ac MIPI	dress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
ALLPON	W	23h	2300h			I	No <i>i</i>	Argum	ent		I	I	
Description	On/Off I This con	els Off",	turns the discan be on o does not chut Image  "Normal Disdisplay pan I Mode On" o	or off.  ange an  splay Moel is sho	ode On	r status	•	ode Or	Displa	ay Pa	nel	ed to le	ave
Restriction	-												
Register Availability		1 1 1 1	Status Normal Mo Normal Mod Partial Mod Sleep In	de On, I le On, Id	dle Mo	de On de Off,	, Sleep Sleep	Out Out	Availa Yes Yes Yes Yes	ability			
Default			Status Power C SW Res HW Res	et .	ence	Disp Disp	ault Val blay Inv blay Inv blay Inv	ersion ersion	off				





# DISPOFF (2800h): Display Off

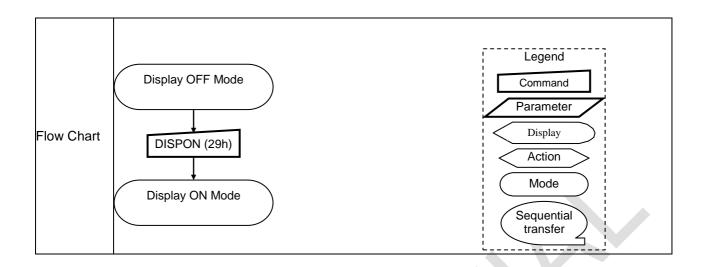
2800H					DISP	OFF (E	Display	Off)					
		Ad	dress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPOFF	W	28h	2800h		l .	1	No A	Argume	nt		l .	1	
			d causes t			le to sto	op disp	laying t	he ima	ge data	on the	displa	у
		Inp	ut Image						D	isplay	Panel		
	$\vdash$	++	+++	+++	_			$\dashv$	++	++	++	++	_
Description						_		$\exists$		$\dashv$	+	+	_
Description								$\exists$		$\pm$	#	$\pm$	_
					_			$\exists$		$\pm \pm$			_
	$\vdash$				_			$\exists$	++	++	++		_
									Ţ				
Restriction	This c	ommano	d has no e	effect whe	n modu	ıle is al	ready ir	n displa	y off m	ode.			
		ī									_		
			Status	Mode On	Idlo M	lodo O	ff Sloo	n Out	Yes	ability			
Decistes				Mode On					Yes				
Register Availability				lode On,		_		•	Yes				
				lode On,		_			Yes				
			Sleep In		Talo III	<b>Juo 0</b> 11	., O.OOF	- Cut	Yes				
			Stat	tus		De	fault Va	alue					
Default				ver On Se	quence		splay O						
				Reset Reset			splay O splay O						
							spiay C						
										<u> </u>	Legen	d	!
			isplay On I	Mode	)						Comma	nd	
				/	,						Parame	ter	
		Γī	DISPOFF (:	28h)							Display		!
Flow Chart		Ľ	1	2011)						$ \cdot $	Action		
			<u> </u>								Mode		!
		( Di	splay OFF	Mode	)						Sequen	tial	
				/							transfe		
										١			



# DISPON (2900h): Display On

2900H		DISPON (Display On)												
Inst/Para	R/W		dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
		MIPI	Other			_			_					
DISPON	W	29h	9h 2900h No Argume					ent						
	This command causes the display module to start displaying the image data on the display device. No status bits are changed.											У		
Description		Input Image								Display	Panel			
Restriction	This co	ommano	d has no e	effect wh	en mod	dule is a	lready	in displ	ay on m	node.				
	Status Availability													
Register Availability		Normal Mode On, Idle Mode Off, Sleep Out							Yes					
		Normal Mode On, Idle Mode On, Sleep Out								Yes				
		Partial Mode On, Idle Mode Off, Sleep Out								Yes				
	Partial Mode On, Idle Mode On, Sleep Out								Yes					
	Sleep In								Yes					
Default	Status Default Value Power On Sequence Display Off SW Reset Display Off HW Reset Display Off													







Description

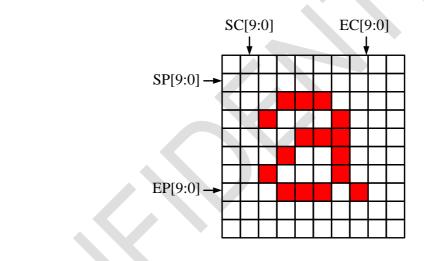
Restriction

#### CASET(2A00h~2A03h): Set Column Start Address

2A00H	CASET												
Inst/Para	R/W	Address		D45.0	7	Do	נ	D.4	Do	Do	D4	D0	LIEV
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CASET	W	2Ah	2A00h	х	1	-	-	-	-	1	SC9	SC8	00
			2A01h	х	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00
			2A02h	х	-	-	-	-	-	-	EC9	EC8	01
			2A03h	х	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	8F

This command defines the column extent of the frame memory accessed by the host processor with the read\_memory\_continue and write\_memory\_continue commands.

This command makes no change on the other driver status. The values of SC[9:0] and EC[9:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.



(1) SC[9:0] always must be equal to or less than EC[9:0].

(2) The SC[9:0] and EC[9:0]-SC[9:0]+1 must can be divisible by 2.

Register
Availability

Register
Partial Mode On, Idle Mode Off, Sleep Out
Partial Mode On, Idle Mode Off, Sleep Out
Partial Mode On, Idle Mode Off, Sleep Out
Partial Mode On, Idle Mode On, Sleep Out
Partial Mode On, Idle Mode On, Sleep Out
Sleep In
Yes



	Chatria	Default Value						
Default	Status	SC[9:0]	EC[9:0]					
	Power On Sequence	0000h	018Fh					
	SW Reset	0000h	018Fh					
	HW Reset	0000h	018Fh					
Flow Chart	CASET  1st & 2nd Param 3rd & 4th Param  RASET  1st & 2nd Param 3rd & 4th Param  RAMWR  RAMWR  D1[B:0],D2[B:0  Any Com	eter: SC[9:0] eter: EC[9:0]  (2Bh)  eter: SP[9:0] eter: EP[9:0]  (2Ch)  Data ]Dn[B:0]	Legend Command Parameter Display Action Mode Sequential transfer					

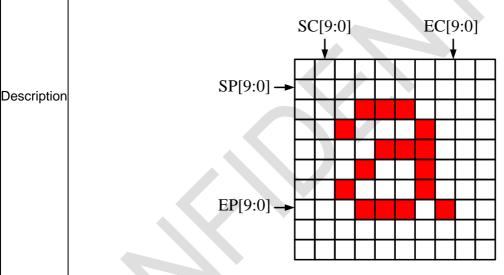


#### RASET(2B00h~2B03h): Set Row Start Address

2B00H						RASET							
/5	D 444	Add	Iress	D45.0	D.7	<b>D</b> 0	5.5	D.4	Do	D.C.	D.4	D.o.	
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
			2B00h	х	ı	-	-	ı	ı	ı	SP9	SP8	00
RASET	W	2Bh	2B01h	х	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	00
KASET	VV	2011	2B02h	х	ı	-	-	-	ı	1	EP9	EP8	01
			2B03h	х	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	8F

This command defines the page extent of the frame memory accessed by the host processor with the write\_memory\_continue and read\_memory\_continue command.

This command makes no change on theother driver status. The values of SP[9:0] and EP[9:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.



(1) SP[9:0] always must be equal to or less than EP[9:0]

Restriction (2) The SP[9:0] and EP[9:0]-SP[9:0]+1 must can be divisible by 2.

	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
Register	Normal Mode On, Idle Mode On, Sleep Out	Yes
Availability	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes



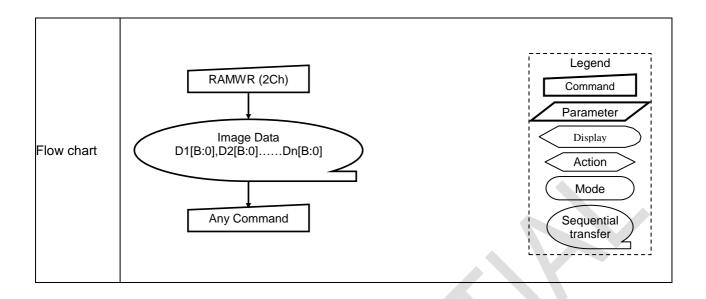
	Status	Defa	ault Value
	Sidius	SP[9:0]	EP[9:0]
Default	Power On Sequence	0000h	018Fh
	SW Reset	0000h	018Fh
	HW Reset	0000h	018Fh
Flow Chart	CASET (2Ah)  1st & 2nd Parameter: 3rd & 4th Parameter:  RASET (2Bh)  1st & 2nd Parameter: 3rd & 4th Parameter: 3rd & 4th Parameter:  RAMWR (2Ch)  Image Data D1[B:0],D2[B:0]	SC[9:0] EC[9:0] SP[9:0] EP[9:0] Dn[B:0]	Legend Command Parameter Display Action Mode Sequential transfer



# RAMWR (2C00h): Memory Write

2C00H						RAN	IWR						
		Ac	dress										
Inst/Para	R/W			D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
			2C00h	Χ	0	0	1	0	1	1	0	0	2C
			1 <sup>st</sup> Pixel	Х	D <sub>1</sub> 7	D₁6	D₁5	D <sub>1</sub> 4	D₁3	D <sub>1</sub> 2	D <sub>1</sub> 1	D <sub>1</sub> 0	
RAMWR	W	2Ch	:	Х	:	:	:	:	:	:		:	
			N <sup>th</sup> Pixel	Х	D <sub>N</sub> 7	D <sub>N</sub> 6	D <sub>N</sub> 5	D <sub>N</sub> 4	D <sub>N</sub> 3	D <sub>N</sub> 2	D <sub>N</sub> 1	D <sub>N</sub> 0	
Description		startin	transfers g at the pi										
Restriction	write loc	ation.	e should f Otherwise vritten to u	, data wr	itten w	ith RAI							
Restriction	write loc	ation.	Otherwise	, data wr	itten w d locati	ith RAI			nd any	followir	ng RAN		
Restriction	write loc	ation.	Otherwise	, data wr	itten w	ith RAI			nd any		ng RAN		
Restriction	write loc	ation.	Otherwise	, data wr ındefined	itten w d location	ith RAN	MWR(2	2Ch) ar	nd any	followir	ng RAN		
	write loc	ation.	Otherwise vritten to u	, data wr indefined Mode On	Statu	ith RAN	off, Slee	ep Out	nd any	followir vailabili	ng RAN		
Register	write loc	ation.	Otherwise vritten to u	, data wr indefined Mode On	Statu , Idle N	ith RAN	MWR(2	2Ch) an	nd any	followir vailabili Yes	ng RAN		
Register	write loc	ation.	Normal No	, data wr indefined Mode On Mode On	Statu , Idle N , Idle N	ith RANons.  s  Mode C  Mode C	off, Slee	ep Out	nd any	vailabili Yes Yes	ng RAN		
Restriction Register Availability	write loc	ation.	Normal No	, data wr indefined Mode On Mode On	Statu , Idle N , Idle N	ith RANons.  s  Mode O  Mode O  Iode O	off, Slee	ep Out	nd any	vailabili Yes Yes Yes	ng RAN		
Register	write loc	ation.	Normal No	, data wr indefined Mode On Mode On	Statu  , Idle M , Idle M , Idle M	ith RANons.  s  Mode O  Mode O  Iode O	off, Slee	ep Out	nd any	railabili Yes Yes Yes Yes	ng RAN		
Register	write loc	ation.	Normal No	, data wr indefined Mode On Mode On Mode On	Statu  , Idle M , Idle M , Idle M	ith RANons.  s  Mode O  Mode O  Iode O	off, Slee	ep Out ep Out ep Out	nd any	vailabili Yes Yes Yes Yes Yes	ng RAN		
Register Availability	write loc	ation. (ads is v	Normal No	, data wr indefined Mode On Mode On Mode On	Statu  Statu  I, Idle M  I, Idle M  I, Idle M  Sleep	ith RAI ons.  s  Mode C  lode C  lode O  In	MWR(2	ep Out ep Out ep Out ep Out	Av Av	railabili Yes Yes Yes Yes Yes	ty		
Register	write loc	ation. (ads is v	Normal No	, data wr indefined Mode On Mode On Mode On Sequence	Statu  Statu  I, Idle M  I, Idle M  I, Idle M  Sleep	ith RAI ons.  s  Mode C  Mode C  Iode O  In	MWR(2	ep Out ep Out ep Out	Av Av	railabili Yes Yes Yes Yes Yes et rand	ty lomly		







#### PTLAR (3000h): Partial Area

3000H					P	TLAR (	Partial	Area)					
Inst/Para	R/W	Add MIPI	ress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HE
		IVIIFI	3000h	Х	_	_	_	_	_	_	SR9	SR8	00
			3000h	X	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
PTLAR	W	30h	3002h	X	-	-	-	-	-	-	ER9	ER8	01
			3003h	х	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	8F
	Row (I If End Star SR[	ER), as d Row > t Row	h this co illustrate Start Ro	d in the							Partia Area	al	
escription		<b>9:0] -</b> d Row <	Start Ro	ow .								Partial	
	ER	[9:0]	<b>→</b>								}	Area	
			=		_	_	_	_	_	+-			
		[9:0]	→ Start Ro								}	Partial Area	



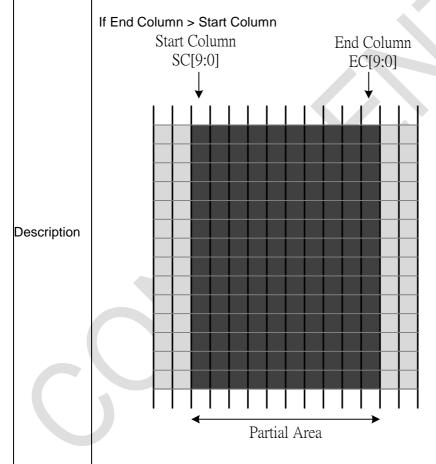
	Status		Availability	
	-	On, Idle Mode Off, Sleep Ou		
Register		On, Idle Mode On, Sleep Ou		
Availability	-	On, Idle Mode Off, Sleep Out		
		On, Idle Mode On, Sleep Out		
	Sleep In		Yes	
		<b>5</b>		
	Status	Default Value		
		SR[9:0]	ER[9:0]	
Default	Power On Sequence	0000h	018Fh	
	SW Reset	0000h	018Fh	
	HW Reset	0000h	018Fh	
Flow chart	PTLAR (30h)  1st & 2nd Parameter: SR[9:0]  3rd & 4th Parameter: ER[9:0]  PTLON (12h)  Partial Mode  Note: B=23	Partial Mode  DISPOFF (28h  NORON (13h)  Partial Mode OF  Image Data D1[B:0],D2[B:0]Dn[B:0]  DISON (29h)	Legend Command Parameter Display Action	
	100 · D=20			



#### PTLAR (3100h): Vertical Partial Area

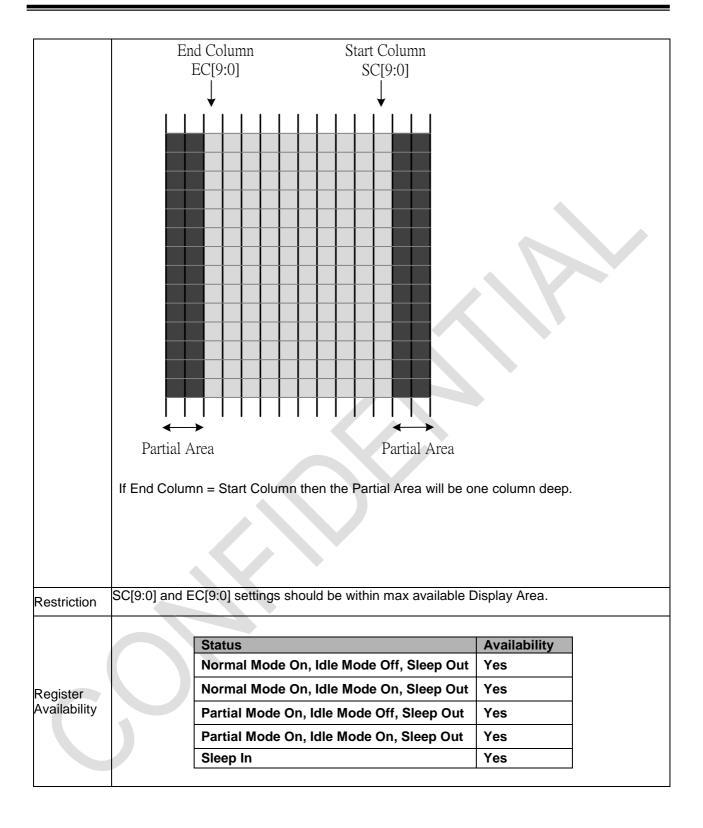
3100H		PTLAR (Partial Area)											
Inst/Para	R/W	Add	ress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IIISVFala	IT/VV	MIPI	Other	ס-פום	זט	D6	מם	D4	ט	DZ	וט	טם	ПЕЛ
			3100h	х	ı	-	ı	ı	ı	ı	-	SC8	00
PTLAR	W	31h	3101h	х	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00
FILAR	VV	3111	3102h	х	1	-	-	-	-	i	-	EC8	01
			3103h	х	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	8F

This command defines the Vertical Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Column (SC) and the second the End Column (EC), as illustrated in the following figure.



If End Column < Start Column







		Default Value	
	Status	SC[9:0]	EC[9:0]
Default	Power On Sequence	0000h	018Fh
	SW Reset	0000h	018Fh
	HW Reset	0000h	018Fh
Flow chart	1. To Enter Partial Mod  PTLAR (30h)  1st & 2nd Parameter: SR[9:0]  3rd & 4th Parameter: ER[9:0]  PTLON (12h)  Partial Mode  Note: B=23	Partial Mode  DISPOFF (28  NORON (13h  Partial Mode C  Image Data D1[B:0],D2[B:CDn[B:0]  DISON (29h	Optional to prevent tearing effect image display  h)  Legend  Command  Parameter  Display  Action  Mode  Sequential transfer



# TEOFF (3400h): Tearing Effect Line OFF

3400H				TEC	OFF (T	earing	Effec	t Line	OFF)				
Inst/Para	R/W	Addı		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
movi ara		MIPI	Other	2100									112/
TEOFF	W	34h	3400h				No A	rgume	nt				
Description	This line.	comman	d turns o	ff the disp	olay mo	odule's	Tearir	ng Effe	ct outp	out sigi	nal on	the TE	signal
Restriction	This	comman	d has no	effect wh	en the	Tearir	ng Effe	ct outp	out is a	lready	off.		
			Status							Availak	nility		
				I Mode O	n, Idle	Mode	Off, S	leep (		es	Jiiley		
Register			Norma	Mode O	n, Idle	Mode	On, S	leep (	Out \	es			
Availability			Partial	Mode Or	ı, idle	Mode	Off, SI	еер О	ut \	es .			
			Partial	Mode Or	, Idle	Mode	On, SI	еер О		es .			
			Sleep I	n					)	es_			
Default				Status Power ( SW Res HW Res	set	quence		Defau OFF OFF OFF	lt Valu	е			
Flow Chart		TE	EOFF (34)	n)							Com Para Dis Acc Mo	gend mand meter splay ction ode uential nsfer	



#### TEON (3500h): Tearing Effect Line ON

3500H		TEON (Tearing Effect Line ON)												
Inst/Para	a R/	۸۸/	Addr	ess	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IIISVFaia	a   N/	vv [	MIPI	Other	D15-6	יט	DO	D3	D4	DS	D2	וט	DU	HEX
TEON	٧	٧	35h	3500h	Х	0	0	0	0	0	SKIP_ M[1]	SKIP_ M[0]	TELOM	00

Bit	Symbol	Description	Comment
D2			01 : only refresh frame active
	SKIP_M[1:0]	Output mode of TE signal for	10 : only the frame before refresh
D1	OKII _IVI[1.0]	skip frame area	frame active
			00/11 : reserved
D0	TELOM	Output made of TE signal	0:only V-blanking
DU	TELOW	Output mode of TE signal	1:V-blanking +H-blanking

This command turns on the tearing Effect output signal on the TE signal line. The TE signal is not affected by changing MADCTR (36h) B4 (Line Address Order).

The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.

If TELOM = 0:

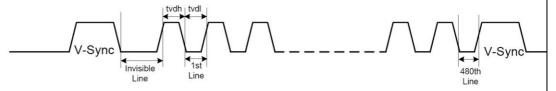
The Tearing Effect Output line consists of V-Blanking information only.



#### Description

If TELOM = 1:

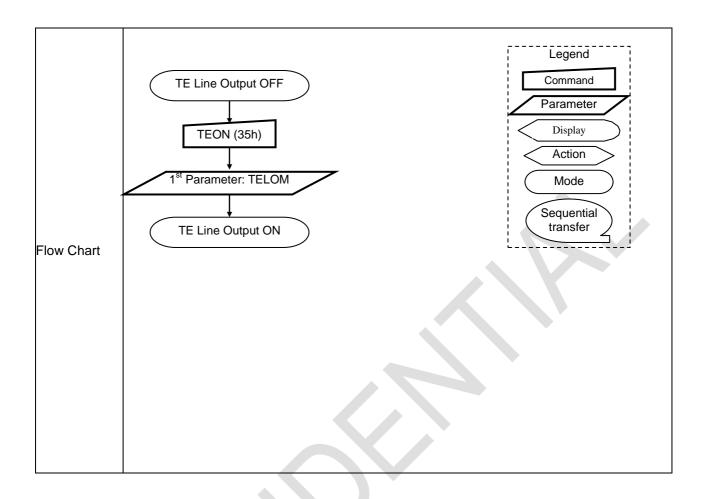
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information.



The Tearing Effect Output line shall be active low when the display module is in Sleep mode.



Restriction	This command has no effect when Tearing Effect output is alr	eady ON.
	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
Register	Partial Mode On, Idle Mode Off, Sleep Out	Yes
vailability	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
)efault	Status Power On Sequence OFF SW Reset HW Reset OFF	





# MADCTR (3600h): Scan Direction Control

3600H				MA	ADCTR	(Scan	Directi	ion Co	ntrol)				
Inst/Para	R/W	Add MIPI	ress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MADCTR	W	36h	3600h	Х	D7	D6	D5	D4	D3	D2	D1	D0	00
Description		e on the	other drambol served  Berved served served	RGB/B	n Addres	D. Ser		Ccc   0:	mment Increasi Decreas =BGR, Display Pa In Frame F	ng in ho sing in h "0"=RGE	rizontal orizonta 3		kes no
Restriction													
Register Availability			Normal Partial	l Mode O l Mode O Mode Or Mode Or n	n, Idle n, Idle I	Mode (	On, Sle	ep Out	t Yes t Yes Yes	; ;	у		



	Status	Default Value	
Dofoult	Power On Sequence	00h	
Default	SW Reset	00h	
	HW Reset	00h	
ilow chart	MADCTR (36h)  1 <sup>st</sup> Parameter	Legend Command Parameter Display Action Mode Sequential transfer	



# IDMOFF (3800h): Idle Mode Off

3800H				II	OMOF	F (Idle	Mode	Off)					
		Ad	ldress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDMOFF	W	38h	3800h				No A	rgume	nt				
Description	This c	ommano	d causes th	e display ı	module	e to exi	it Idle r	node.		•			
Restriction	This c	ommano	d has no eff	ect when	the dis	play m	odule	is not	in Idle	mode.			
		ı	Otatus		_		_	_	<u> </u>	:1 = l= :1:4			
			Status Normal M	ode On, I	dle Mo	ode Or	າ		Yes	ilabilit	. <b>y</b>		
Register			Partial Mo						Yes				
Availability			Sleep Out	, Sleep Ir	1				No				
				Status Power Or	Sogn	lonco		fault V Mode					
Default				SW Rese		lence		Mode					
				HW Rese	et		ldle	e Mode	Off				
					•				 !	Le	egend		
	<	Idle m	node ON	<b>)</b>					!		mmand	$\neg$	
	<b>(</b>									Pai	rameter		
		IDMC	)FF (38h)	1						( 1	Display	<b>-</b>	
Flow Chart		1		J					! ! !		Action	$\leq$	
	<	Idle m	ode OFF	<b>\</b>							Mode		
				,					!	800	quential		
									; ! !		ansfer	'	
												<del></del> !	



# IDMON (3900h): Enter\_idle\_mode

3900H					Ent	ter_idle	e_mod	le					
		Add	ress										
Inst/Para	R/W			D15-8	D7	D6	D5	D4	D3	D2	D1	D0	НЕХ
		MIPI	Other										
IDMON	W	39h	3900h			I	No A	Argum	ent		^	1	
			auses the										
			or express								devic	e using	the
	INIOR OF		he R, G a		or com	ponen	ts in th	e inpu	ımage		nel Di	onlov	
		ın	put Imag	je '						Pa 		spiay	
								-					
								/ .					
Description													
I													
	Color	R7 R6	6 R5 R4 R3	R2 R1 R0		G7 G6 G	5 G4 G3	G2 G1	G0	B7 B6	B5 B4 E	33 B2 B1	В0
	Black	0XXX	XXXX			XXXXX	XX			0XXX	XXXX		
	Blue	0XXX	XXXX			XXXXX	XX			1XXXX	XXXX		
	Red		XXXX			XXXXX				0XXX			
	Magei		XXXX			XXXXX				1XXXX			
	Green		XXXX			1XXXXX				0XXX			
	Cyan		XXXX			1XXXXX				1XXXX			
	Yellov		XXXX			1XXXXX				0XXXX			
	White	IXXX	XXXX			1XXXXX	**			1XXXX	<b>XXXX</b>		
Restriction	This cor	mmand h	as no effe	ct when	modul	e is alr	eady ir	n idle o	n mod	e.			
IXESHICHOH													
		84	tatus						Avai	lability	,		
			ormal Mo	de On.	Idle M	ode Of	f		Yes	iability	/		
Register			artial Mod						Yes				
Availability			eep out,						No				
									1 -				



Default	Status Power On Sequence SW Reset HW Reset	Default Value Idle Mode Off Idle Mode Off Idle Mode Off	
Flow Chart	IDMON (39h) Idle mode ON	Comm Param Disp Acti Mod Seque trans	neter lay on de



#### COLMOD (3A00h): Interface Pixel Format

3A00H				CC	DLMOE	(Inter	face Pi	xel Fo	rmat)				
Inst/Para	R/W	Add	ress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IIISVFala	IN/VV	MIPI	Other	D13-6	<i>D1</i>	Do	D3	υ4	DS	DZ	וט	Do	IILA
COLMOD	W	3Ah	3A00h	Х	SPI_IFPF_ SEL	VIPF[2]	VIPF[1]	VIPF[0]	0	IFPF[2]	IFPF[1]	IFPF[0]	77

This command sets the pixel format for the RGB image data used by the interface. The IFPF[2:0] pixel format used by the MIPI/ MCU interface.

If SPI\_IFPF\_SEL(3Ah-D7) = 1: The VIPF[2:0] pixel format used by the SPI interface If SPI\_IFPF\_SEL(3Ah-D7) = 0: The IFPF[2:0] pixel format used by the SPI interface

Control Interface Color Format	IFPF[2]	IFPF[1]	IFPF[0]
SPI 8 bit/pixel (256 colors); SPI 256 Gray (Support IF: SPI3/SPI4)	0	0	1
SPI 8 bit/pixel (256 colors); SPI 3-3-2 (Support IF: SPI3/SPI4)	0	1	0
SPI 3 bit/pixel (8 colors); SPI 1-1-1 (Support IF: SPI3/SPI4)	0	1	1
16bit/pixel (65,536 colors)	1	0	1
18bit/pixel (262,144 colors)	1	1	0
24bit/pixel (16.7M colors)	1	1	1

#### SPI 1-1-1

RGB 1-1-1 Bit	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	0	0	0	0	0	0	0x2C for GRAM Write
1st RAM Data Write	1	х	х			B1[0]	R2[0]		B2[0]	1,2 pixel Data Write
2nd RAM Data Write	1	х	x		G3[0]	B3[0]	R4[0]	G4[0]	B4[0]	3,4 pixel Data Write
3rd RAM Data Write	1	х	х			B5[0]	R6[0]	G6[0]	B6[0]	5,6 pixel Data Write
So on										

Description

RGB 3-3-2 Bit	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	0	0	0	0	0	0	0x2C for GRAM Write
1st RAM Data Write	1	R1[2]						B1[1]	B1[0]	1st pixel Data Write
2nd RAM Data Write	1	R2[2]					G2[0]	B2[1]	B2[0]	2nd pixel Data Write
3rd RAM Data Write	1	R3[2]						B3[1]	B3[0]	3rd pixel Data Write
So on										

#### SPI 256 Gray

RGB 256 Gray	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	0	0	0	0	0	0	0x2C for GRAM Write
1st RAM Data Write	1									1st pixel Data Write
2nd RAM Data Write	1	P2[7]								2nd pixel Data Write
3rd RAM Data Write	1	P3[7]								3rd pixel Data Write
So on										

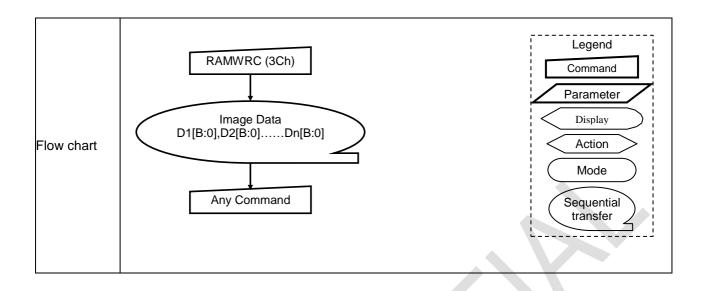


Restriction	-		
	Status		Availability
	Normal Mode On, Idle Mod	e Off, Sleep Out	Yes
Register	Normal Mode On, Idle Mod	e On, Sleep Out	Yes
Availability	Partial Mode On, Idle Mode	Off, Sleep Out	Yes
	Partial Mode On, Idle Mode	On, Sleep Out	Yes
	Sleep In		Yes
	Status	Default Va	alue
	Power On Sequence	77h	
Default	SW Reset	77h	
	HW Reset	77h	
Flow chart	Example :  16-bits/Pixel Mode  COLMOD (3Ah)  1st Parameter (06h)  18-bits/Pixel Mode		Legend  Command  Parameter  Display  Action  Mode  Sequential transfer



# RAMWRC (3C00h): Memory Continuous Write

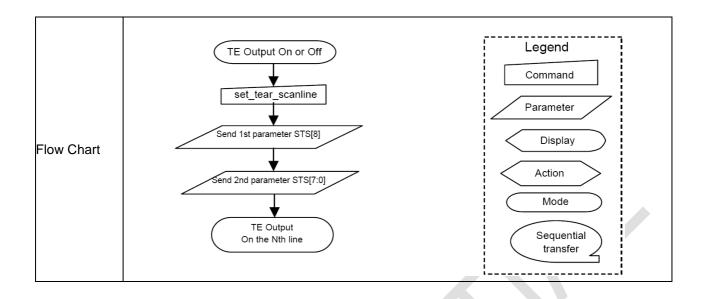
3C00H						RA	MWRC						
		Ac	dress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
			3C00h	Х	0	0	1	1	1	1	0	0	3C
			1 <sup>st</sup> Pixel	Х	D <sub>1</sub> 7	D₁6	D₁5	D₁4	D₁3	D <sub>1</sub> 2	D <sub>1</sub> 1	D <sub>1</sub> 0	
RAMWRC	W	3Ch	:	Х	:	:	:	:	:	÷	:	:	
			N <sup>th</sup> Pixel	Х	D <sub>N</sub> 7	D <sub>N</sub> 6	D <sub>N</sub> 5	D <sub>N</sub> 4	D <sub>N</sub> 3	D <sub>N</sub> 2	D <sub>N</sub> 1	D <sub>N</sub> 0	
Description	memor write_r	ry cont nemor	nd transfer inuing from y_start co	m the pix mmand.	kel loca	ation fol	lowing	the pre	vious v	vrite_m	emory_	_continu	ue or
Restriction	write lo	ocation	. Otherwis	se, data									
	comma	ands is	written to	undefin	ed loca	ations.		(2011) &					
	comma	ands is	s written to	undefin	ed loca			(2011) 6		vailabil			
	Comma	ands is		undefin	ed loca	ations.			A				
	COMM	ands is	Norma		Sta	ations.	Off, Sle	eep Ou	t	vailabil			()
Register Availability	COMM	ands is	Norma	I Mode (	Sta  On, Idle	ations.  atus  Mode  Mode	Off, Sle	eep Ou	t t	vailabil Yes			(()
Register	Comma	ands is	Norma Norma Partial	I Mode (	Sta On, Idle On, Idle	ations.  Mutus  Mode  Mode	Off, Sle	eep Ou	t t	vailabil Yes Yes			()
Register	Comma	ands is	Norma Norma Partial	I Mode (	Sta On, Idle On, Idle	ations.  Mode  Mode  Mode  Mode	Off, Sle	eep Ou	t t	vailabil Yes Yes Yes			(()
Register	Comma	ands is	Norma Norma Partial	I Mode (	Sta On, Idle On, Idle On, Idle	ations.  Mode  Mode  Mode  Mode	Off, Sle	eep Ou	t t	Yes Yes Yes Yes Yes			(()
Register	Comma	ands is	Norma Norma Partial Partial	I Mode (I Mode	Sta On, Idle On, Idle On, Idle Slee	ations.  Mode  Mode  Mode  Mode  p In	Off, Sle On, Sle Off, Sle	eep Outeep Out	t t	vailabil Yes Yes Yes Yes Yes	ity		(()
Register	COMM	ands is	Norma Norma Partial Partial	I Mode (I Mode	Sta On, Idle On, Idle On, Idle Slee	ations.  Mode  Mode  Mode  Mode  Pp In	Off, Ske On, Ske Off, Sle On, Ske	eep Outeep Outee	t t	Yes Yes Yes Yes Yes Yes Yes	ity		
Register Availability	COMM	ands is	Norma Norma Partial Partial Partial St Power Or	I Mode (I Mode	Sta On, Idle On, Idle On, Idle Slee	ations.  Mode  Mode  Mode  Mode  p In	Off, Sle On, Sle Off, Sle	peep Outeep Oute	t t ault Valmory is	Yes Yes Yes Yes Yes Yes Yes on the sector of	ity ity		





# STESL(4400h): Set\_Tear\_Scanline

4400H					STESI	_(Set_	Γear_S	canlin	e)				
Inst/Para	R/W	Add	ress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IIISI/Paia	K/VV	MIPI	Other	ס-פוט	וטו	D6	DS	D4	D3	DZ	וטו	50	ПЕХ
OTEOL	107	4.41	4400h	Х	STS[15]	STS[14]	STS[13]	STS[12]	STS[11]	STS[10]	STS[9]	STS[8]	00
STESL	W	44h	4401h	х	STS[7]	STS[6]	STS[5]	STS[4]	STS[3]	STS[2]	STS[1]	STS[0]	00
Description	the dis B4. Th Line m	splay rea ne Tearin node. al Time	aches lin ng Effect	n the disp e N. The t Line On	TÉ sigr has on	nal is n	ot affec	eted by hat des tvd	changi scribes	ng set_ the Tea	_addres	ss_mod ffect O tvdh	de bit utput
Restriction													
Register Availability			Norma Partial	I Mode O I Mode O Mode Or Mode Or n	n, Idle n, Idle I	Mode Mode (	On, Sle	eep Ou	it Yes	s s	ty		
Default				Status Power Or SW Rese HW Rese	et .	ence	STS STS	ault Val [15:0]= [15:0]= [15:0]=	:16'h00 :16'h00	000			





# GSL (4500h): Get\_Scanline

4500H					GSI	_(Get_	Scanli	ne)					
		Add	dress										HEX
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
			4500h	Х	GTS[15]	GTS[14]	GTS[13]	GTS[12]	GTS[11]	GTS[10]	GTS[9]	GTS[8]	0x
GSL	R	45h	4501h	х	GTS[7]	GTS[6]	GTS[5]	GTS[4]	GTS[3]	GTS[2]	GTS[1]	GTS[0]	xx
Description	numbe first sc	er of sca an line i	turns the on lines on s defined Mode, th	a display as the firs	device at line o	is def of V-Sy	ined as nc and	· VSYN is den	NC + V oted a	BP + V s Line	ACT +		
Restriction	-							X					
		ļ	Status							ilabili	ty		
Danistan		-		Mode On			<del>-</del>						
Register Availability		-		Mode On, lode On,					_				
		-		lode On,	_			<del>•</del>	Yes				
		-	Sleep In					•	Yes	<b>;</b>			
Flow Chart		Send 1s	get_scanline  Wait 3us  Dummy Read  t parameter GTS				Com Para  L An S	gend nmand ameter Display ction Mode equential transfer					



# DSTBON (4F00h): Deep Standby Mode On

4F00H				DS	STBON	l(Deep	Stand	by Mod	le On)				
		Add	r000						,				
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DSTBON	W	4Fh	4F00h	х	0	0	0	0	0	0	0	DSTB	00
Description	DSTB: Notes: 1. To e 2. For	="1", ent : exit Deep MIPI IF,	er deep  Standb  if deep	to enter standby by Mode standby I to GND	mode , input mode i	low pul s used,	se mor	e than (	SSI_CI	_K_P/N			
Restriction	_												
			Status Norma	I Mode (	On, Idl	e Mode	Off, S	leep O		vailabil	ity		
Register		=	Norma	I Mode (	On, Idl	e Mode	On, S	leep O	ut Ye	s			
Availability		-	Partial	Mode C	n, Idle	Mode	Off, SI	eep Ou	ıt Ye	es			
		-	Partial	Mode C	n, Idle	Mode	On, SI	еер Ои	ıt Ye	es			
		<u> </u>	Sleep I	n					Ye	es.			
		3	Status					Default	Value				
Default		ı	Power C	n Sequ	ence		(	)0h					
Doraum			SW Res	et			(	)0h					
		I	HW Res	et			(	)0h					
Flow chart		Parar	TBON (4F	B=1	)					Pr	Legend Command		



# WRDISBV (5100h): Write Display Brightness

5100H						W	RDISB	V					
		Add	ress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRDISBV	W	51h	5100h	x	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	00
		ciple rela	is used to					st brigh	tness ar	nd FFh v	/alue me	eans the	highest
Description													
Restriction	The d	isplay s	upplier o	annot u	se this	comm	and for	tuning					
Register Availability			Norma Partial Partial Sleep Status	Il Mode Il Mode Mode ( Mode (	On, Idle	e Mode	e On, S Off, Sl	Bleep O	out Yout Yout Yout You	es es es	lity	<b>—</b>	
Default			SW Res		uence			00h 00h 00h					
Flow chart		Para	RDISBV (5	/[7:0]						P	Display Action Mode equenti	d er	



# RDDISBV (5200h): Read Display Brightness

5200H						RDI	DISBV						
Inst/Para	R/W	Add MIPI	dress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDISBV	R	52h	5200h	х	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	00
Description	This com In princip brightnes	ole relat	returns bi ionship is	ightness v that 00h v	alue. /alue me	eans the	e lowest	brightn	ess and	I FFh va	llue mea	ans the	highest
Restriction	-												
		-	01.1										
		-	Status	l Mode O	n Idle	Mode	Off SI	een Oı		ailabili s	ty		
Register		-		Mode O									
Availability		-		Mode Or	-			<u> </u>		s			
		=	Partial	Mode Or	ı, Idle N	Mode (	On, Sle	ep Ou	t Ye	s			
			Sleep I	n					Ye	S			
			Status					efault '	Value				
		-		n Seque	nce			)h				4	
Default		_	SW Res					Oh				-	
		Ľ	HW Res	et			0	)h					
	RDD	DISBV (	52hH)	>		Lege							
				Host Driver	L	Comm							
		n d n a ram				Disp	=	,					
Flow Chart	Se	nd param DBV[7:0				Acti							
					(	Mod	de						
						Seque							
					`	trans							



# WRCTRLD (5300h): Write Display Control

5300H						W	RCTRL	.D					
		Add	ress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRCTRLD	W	53h	5300h	х	0	0	BCTR	0	DD	0	0	0	28
		∟ _: Brightr	l ness cont nming co	rol ,1=en	able		<u> </u>						
Description													
Restriction	The d	isplay s	upplier o	annot u	se this	comm	and for	tuning		¥			
Register Availability Default			Norma Partial Partial Sleep Status	Il Mode Il Mode Mode ( Mode ( In	On, Idle On, Idle On, Idle	e Mode	e On, S	Sleep O	Out Yout Yout Yout You	es es es	lity		
Flow chart			CCTRLD (5	53h)				28h			Legend Commander Parameter Display Action Mode Gequentitransfer	er al	



# RDCTRLD (5400h): Read Display Control

5400H						RDC	TRLD						
Inst/Para	R/W	Add MIPI	dress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCTRLD	R	54h	5400h	Х	0	0	BCTRL	0	DD	0	0	0	28
Description	BCTRL: DD: Disp	Brightn blay dim	ess contr iming cor	ol ,1=enab ntrol ,1=ena	ole able								
Restriction	-								_				
Register Availability			Norma Partial	I Mode O I Mode O Mode Or Mode Or n	n, Idle ı, Idle I	Mode Mode (	On, Sle	eep Ou	it Ye	s s	ty		
Default		ļ	Status Power C SW Rese		nce		28	efault ' Bh Bh Bh	Value				
Flow Chart		nd param BCTRL		Host Driver	(	Lege Comn Paran Disp Acti Mo	neter olay on de						



# WRRADACL (5500h): RAD\_ACL Control

5500H						WRR	ADACI	-					
In at/Dana	DAM	Add	dress	D45.0	D7	DC	Dr	D4	Do	D0	D4	D0	LIEV
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRRADACL	W	55h	5500h	Х	0	0	0	0	0	0	RAD_A	CL[1:0]	00
Description	RAD_A	CL[1:0]	=11, Ena	o control F ble Raydiu able Raydiu	ım ACL	function	١.	on for A	CL (Aut	o Curre	nt Limit)		
Restriction	-												
			01-1										
			Status Norma	l Mode O	n. Idle	Mode	Off. SI	eep Ou		ailabili s	ity		
Register		-		l Mode O				· ·					
Availability		=		Mode Or					_	s			
		-	Partial	Mode Or	, Idle I	Mode C	n, Sle	ep Out	Ye	s			
			Sleep I	n					Ye	S			
								>					
		3	Status				D	efault \	Value				
		I	Power C	n Seque	nce		00	)h					
Default		_	SW Res					0h					
			HW Res	et			00	)h					
Flow Chart	Se	nd param	eter /	Host Driver	<	Lege Comm Param Disp Action Moo	neter lay						



#### IMGEHCCTR (5800h): Set\_color\_enhance

5800H					WI	RCE (se	et_colo	r_enha	nce)				
Inst/Para	R/W	Add	dress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
movi did	10,77	MIPI	Other	D 10 0	<i></i>	50	50	54	D0				
WRCE	W	58h	5800h	Χ	0	0	0	0	0	SLR_EN	SLR_LEV EL1	SLR_LEV EL0	00
	Bit			Des	cription	1			Valu	e			
		R_EN		Sun	light Re		ole		'0' : c	disable; nable			
Description	SL	R_LEV	EL[1:0]	Sun Enh	light Rea	adable ent Leve	el		0~2	2, low to h	nigh		
Description													
Restriction	-												
Register Availability			Norm Partia	al Mod al Mod Il Mod	de On, e On, I	Idle Mo	ode On, de Off,	Sleep (Sleep C	Out	Yes Yes Yes Yes Yes Yes Yes	bility		
Flow Chart		Com Pars  L Ar Si	mand imeter Display Stion Mode	)									



# IMGEHCCTR (5900h): Read\_color\_enhance

5900H					RDCI	E (set_	color_c	enhano	:e)						
		bbA	ress												
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
RDCE	R	59h	5900h	х	0	0	0	0	0	SLR_EN	SLR_LEV	SLR_LE	00		
											LLI	VLLO	l		
	Bit				scriptio				Value		SLR_EN SLR_LEV SLR_LE VELO  able; cole  www.to.high  availability fes fes fes fes				
	SLI	R_EN			nlight Renancem	eadable ent Ena	able		'0' : dis '1': ena						
	SLI	R_LEVE	L[1:0]		nlight Re	eadable ent Lev	⁄el		0~2,	low to hi	gh				
Description															
Restriction	-														
		[	Status							Availal	oility				
			_	l Mode						Yes					
Register Availability				I Mode						Yes		_			
Availability				Mode C						Yes		-			
			Sleep I		m, idie	Wode	On, Si	eep Ot		Yes		-			
Flow Chart		Action Mc Seq	eter play												



# OPSCTR (5E00h): OPS CTR

5E00H					C	PSCTI	R (OPS	S ctrl)					
		Add	dress					Param	eter				
Instruction	R/W	MIPI	Others	D15-D8	3 D7	D6	D5	D4	D3	D2	D1	D0	HEX
OPSCTR	W	5Eh	5E00h	00h	0	0	0	0	0	0	0	ops_en	00
	Е	Bit			Descrip	tion			_	alue			
Description		PS_EN	N		OPS Po	wer Cor	trol En	able		: disable			
Restriction	-												
			Statu		. On Id	lo Mod	- Off	Cloop (		Availab	oility		
			-	al Mode						Yes		-	
Register Availability				al Mode	-		_	•		Yes Yes	<u> </u>	+	
rtranability				al Mode						Yes		1	
			Sleep		,		7			Yes		1	
												<b>-</b>	
			Status					Default	Valu	2			
		- 1		On Sequ	uence			00h	Valu				
Default		-	SW Res					00h					
			HW Res	set			(	00h					
										Legend			
		W	/RCABCM	B(5Eh)					=	Command			
Flow chart	_	New	Display L	uminanc	re )					Display Action Mode equentia transfer			



# OPSCTR2 (5F00h): OPS CTR2

5F00H					OI	PSCTR	2 (OPS	CTR2)					
Instruction	R/W	Add	dress					Param	eter				
instruction	K/VV	MIPI	Others	D15-D8	3 D7	D6	D5	D4	D3	D2	D1	D0	HEX
OPSCTR2	W	5Fh	5F00h	00h	0	ops2_rat o2	ops2_rat o1	i ops2_rati o0	0	0	ops2_mo de	ops2_en	00
	_												
		3it			Descri	otion				<b>lue</b> : disabl	0.		
Description		OPS2_E	N		OPS C	ontrol En	able		'1':	enable	,		
		OPS2_N	MODE		OPS M	ode				: Luma RGB N			
		OPS2_F	RATIO[2:	0]	OPS R	atio			0~	7: 0, 1/	8,7/8		
Restriction	-												
			Statu	S						Availal	oility	1	
				al Mode	On, Ic	lle Mod	e Off,	Sleep C		'es	<b>,</b>		
Register			Norm	al Mode	On, Ic	lle Mod	e On,	Sleep C	Out Y	'es			
Availability			-	al Mode						'es			
				al Mode	On, Id	e Mode	On, S	leep O		es		_	
			Sleep	) IN					ן ו	'es		]	
			Status					Default	Value			-	
		Ī		On Sequ	uence			00h	Value				
Default			SW Res	set			(	00h					
			HW Res	set			(	00h					
								-				1	
		_							_	Leger	<b>—</b>		
			RDCABCI	MB(5Fh)				ł	=	Comma Parame			
		_	Send Pai	romotor		7		-  -		Display	<b>=</b>		
Flow chart	_		CMB[		_/				$\geq$	Action			
										Mode			
								į	S	equent			
								į		transfe			



# WRHBMDISBV (6300h): Write HBM Display Brightness

6300H	WRHBMDISBV												
Inst/Para	R/W	Address											
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRHBMDIS BV	W	63h	6300h x DBV_HBM[7:0]							00			
	This command is used to adjust brightness value in HBM mode if hbm_gidx_type=1.(0xC840h)												
Restriction	1. The display supplier cannot use this command for tuning 2. DBV_HBM[7:0] setting value must be greater than G_ratio_to2 (0xAC60h )/ G_ratio_to3 (0x5530h ) value.												
Register Availability			Status						A	Availability			
					Mode On, Idle Mode Off, Sleep Out								
		Normal Mode On, Idle Mode On, Sleep Out								Yes			
			Partial Mode On, Idle Mode Off, Sleep Out							Yes			
		Partial Mode On, Idle Mode On, Sleep Out Sleep In								Yes Yes			
	100 III												
Default	Status Default Value												
			Power On Sequer										
			SW Reset				00h						
			HW Re	set				00h					
Flow chart	Parameter DBV_HBM[7:0]  Commar  Parameter DBV_HBM[7:0]  Mode  Sequent										Display Action Mode	d der	



# RDHBMDISBV (6400h): Read HBM Display Brightness

6400H						RDHB	MDISB	V					
In at/Dana	DAM	Add	dress	D45.0	D7	DC	DE	D4	Do	D0	D4		LIEV
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDHBMDISB V	R	64h	6400h	х		•		DBV_H	BM[7:0	)]	•		00
Description	This com	nmand	returns bı	rightness v	alue in	HBM mo	doe.						
Restriction	-								_				
			Status				011 01			ailabili	ity		
		-		I Mode O									
Register Availability		-		I Mode O									
Availability		-		Mode Or									
		-		Mode Or	i, idle i	Mode (	on, Sie	ep Ou					
			Sleep I	<u>n</u>	<del>-</del>				Ye	S			
			Status			X		efault	Value			1	
				n Seque	nce			Oh	Value			1	
		_	SW Res	<del></del>			00	0h				=	
Default		ī	HW Res	et			00	0h					
							l					_	
Flow Chart	Se	nd param	neter	<u>Hos</u> t Driver	[ 	Lege Comm Param Disp Acti Mod	neter lay on de						



## HBM\_Mode (6600h): Set\_HBM\_Mode

						Se	tHbmM	lode					
In at/Dava	DAM	Add	dress	D45.0	D.7	DC	De	D.4	Do	Do	D4	Do	HEX
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
SetHbmMode	W	66h	6600h	Х	0	0	0	0	0	0	HBM_en	0	00
Description	and deep i	dle)	, This co										
Restriction	under	displa	y area										
			Statu	S						Availa	bility		
					de On,	Idle Mo	de On			Yes			
Register			Partia	al Mod	e On, l	dle Mod	de On			Yes			
Availability			Sleep	In, SI	eep Ou	ıt				No			



## Deep\_Idle\_Mode (6700h): Set\_Deep Idle Mode

						SetD	eepldle	eMode					
Leat/Dave	D 44/	Add	dress	D45.0	D.7	Do	De	D.4	Do	Do	D.4	Do	HEX
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
SetDeepIdleMo de	W	67h	6700h	х	0	0	0	0	0	0	0	DEEP_I DLE_EN	00
	norma	l, idle a _ldle_e	n = 1, T and HBN n = 0, T	И)				•					
Restriction	under	display	y area										
			Statu	s						Availa	bility		
					de On,	Idle Mo	de On			Yes			
Register			Partia	al Mod	e On, I	dle Mod	de On			Yes			
Availability			Sleep	In, Sl	eep Ou	ıt	-	-		No			



# COLSET (7000~7F00h): Interface Pixel Format Set

7000H ~ 7F00H				COLS	ET (In	terface	e Pixel	Forma	it Set)				
		Add	Iress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
			7000h	х				R_000	00[7:0]				00
7000h	W	70h	7001h	х				G_000	00[7:0]				00
			7002h	х				B_000	00[7:0]				00
			7100h	х				R_000	01[7:0]				00
7100h	W	71h	7101h	х				G_000	01[7:0]				00
			7102h	х				B_000	)1[7:0]				FF
			7200h	х				R_00	10[7:0]		>		00
7200h	W	72h	7201h	х				G_00 <sup>2</sup>	10[7:0]	<b>&gt;</b>			FF
			7202h	х				B_001	0[7:0]				00
			7300h	х				R_00°	11[7:0]				00
7300h	W	73h	7301h	х				G_00 <sup>2</sup>	11[7:0]				FF
			7302h	х		X		B_001	1[7:0]				FF
			7400h	X				R_010	00[7:0]				FF
7400h	W	74h	7401h	х				G_010	00[7:0]				00
			7402h	х				B_010	00[7:0]				00
		_	7500h	х				R_010	01[7:0]				FF
7500h	W	75h	7501h	х				G_010	01[7:0]				00
			7502h	х				B_010	)1[7:0]				FF
			7600h	х				R_01′	10[7:0]				FF
7600h	W	76h	7601h	х				G_01	10[7:0]				FF
			7602h	х				B_011	0[7:0]				00
			7700h	х				R_01′	11[7:0]				FF
7700h	W	77h	7701h	х				G_01	11[7:0]				FF
			7702h	х	B_0111[7:0]							FF	
			7800h	х				R_100	00[7:0]				00
7800h	W	78h	7801h	х				G_100	00[7:0]				00
			7802h	х				B_100	00[7:0]				00
			7900h	х				R_100	01[7:0]				00
7900h	W	79h	7901h	х				G_100	01[7:0]				00
			7902h	х				B_100	)1[7:0]				FF

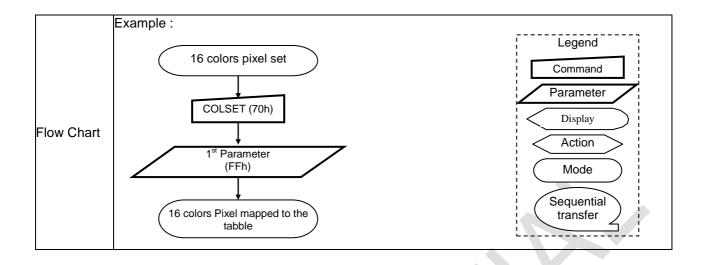


			7A00h	Х	R_1010[7:0]	00
7A00h	W	7Ah	7A01h	Х	G_1010[7:0]	FF
			7A02h	Х	B_1010[7:0]	00
			7B00h	Х	R_1011[7:0]	00
7B00h	W	7Bh	7B01h	Х	G_1011[7:0]	FF
			7B02h	Х	B_1011[7:0]	FF
			7C00h	Х	R_1100[7:0]	FF
7C00h	W	7Ch	7C01h	Х	G_1100[7:0]	00
			7C02h	Х	B_1100[7:0]	00
			7D00h	Х	R_1101[7:0]	FF
7D00h	W	7Dh	7D01h	Х	G_1101[7:0]	00
			7D02h	Х	B_1101[7:0]	FF
			7E00h	Х	R_1110[7:0]	FF
7E00h	W	7Eh	7E01h	Х	G_1110[7:0]	FF
			7E02h	Х	B_1110[7:0]	00
			7F00h	Х	R_1111[7:0]	FF
7F00h	W	7Fh	7F01h	Х	G_1111[7:0]	FF
			7F02h	х	B_1111[7:0]	FF



Т	his command set	the 1-1-1	color form	at map di	re	ctly to	ctly to 24 bits by CI
	RGB111 color mapping	R[7:0]	<b>G</b> [7:0]	B[7:0]			
	0000 (70h)	R_0000[7:0]	G_0000[7:0]	B_0000[7:0]		]	
	0001 (71h)	R_0001[7:0]	G_0001[7:0]	B_0001[7:0]		1	
	0010 (72h)	R_0010[7:0]	G_0010[7:0]	B_0010[7:0]		1	
	0011 (73h)	R_0011[7:0]	G_0011[7:0]	B_0011[7:0]			1
	0100 (74h)	R_0100[7:0]	G_0100[7:0]	B_0100[7:0]		]	
	0101 (75h)	R_0101[7:0]	G_0101[7:0]	B_0101[7:0]			
Description	0110 (76h)	R_0110[7:0]	G_0110[7:0]	B_0110[7:0]			
Josephon	0111 (77h)	R_0111[7:0]	G_0111[7:0]	B_0111[7:0]			
	1000 (78h)	R_1000[7:0]	G_1000[7:0]	B_1000[7:0]			
	1001 (79h)	R_1001[7:0]	G_1001[7:0]	B_1001[7:0]			
	1010 (7Ah)	R_1010[7:0]	G_1010[7:0]	B_1010[7:0]			
	1011 (7Bh)	R_1011[7:0]	G_1011[7:0]	B_1011[7:0]			
	1100 (7Ch)	R_1100[7:0]	G_1100[7:0]	B_1100[7:0]			
	1101 (7Dh)	R_1101[7:0]	G_1101[7:0]	B_1101[7:0]			
	1110 (7Eh)	R_1110[7:0]	G_1110[7:0]	B_1110[7:0]			r I
	1111 (7Fh)	R_1111[7:0]	G_1111[7:0]	B_1111[7:0]			
						l	l
Restriction							
					_		
	Status						Availability
		Mode On,			_	-	·
Register Availability		Mode On,		<u> </u>		•	· -
wanability		ode On, l					-
		ode On, I	die Mode	On, Sleep		Out	Out Yes Yes
	Sleep In						res
E	xample :						Default Value
	Status			R_0000		0[7:0]	D[7:0] G_0000[7:0]
Default		r On Sequ	ience	00	_		
	SW R			001			
	HW R			00		_	h 00h







# **COLOPT (8000h): Interface Pixel Format Option**

8000H				COLO	PT (Ir	terface	Pixe	l For	mat Op	tion)			
Inst/Para	R/W	Add	ress	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IIISVFaia	IN/VV	MIPI	Other	D13-6	יט	D0	טט	D4	DS	DZ		DU	TIEX
COLOPT	W	80h	8000h	Х	Х	RGB111 _opt		RGB 565_ swap	ı en	gray256_ color[2]	gray256_ color[1]	gray256_ color[0]	07



This command sets the 1-1-1/256 gray color format option used by SPI interface.

RGB111\_opt = 0 (80h-B6):

Supporting in IFPF[2:0]=011 case setting by 3A00h (interface pixel format is SPI 1-1-1).

RGB 1-1-1 Bit	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	0	0	0	0	0	0	0x2C for GRAM Write
1st RAM Data Write	1	х	x	R1[0]	G1[0]	B1[0]	R2[0]	G2[0]	B2[0]	1,2 pixel Data Write
2nd RAM Data Write	1	х	х	R3[0]	G3[0]	B3[0]	R4[0]	G4[0]	B4[0]	3,4 pixel Data Write
3rd RAM Data Write	1	х	х	R5[0]	G5[0]	B5[0]	R6[0]	G6[0]	B6[0]	5,6 pixel Data Write
So on										

 $RGB111_{opt} = 1 (80h-B6)$ :

Supporting in IFPF[2:0]=011 case setting by 3A00h (interface pixel format is SPI 1-1-1).

# Description

RGB 1-1-1 Bit	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	0	0	0	0	0	0	0x2C for GRAM Write
1st RAM Data Write	1	x	R1[0]	G1[0]	B1[0]	x	R2[0]	G2[0]	B2[0]	1,2 Pixel Data Write
2nd RAM Data Write	1	x	R3[0]	G3[0]	B3[0]	X	R4[0]	G4[0]	B4[0]	3,4 Pixel Data Write
3rd RAM Data Write	1	x	R5[0]	G5[0]	B5[0]	x	R6[0]	G6[0]	B6[0]	5,6 Pixel Data Write
So on										

 $RGB4bit_en = 0 (80h-B3)$ :

Supporting in IFPF[2:0]=011 case setting by 3A00h (interface pixel format is SPI 1-1-1). Three bits per pixel formats map directly to 24bits by CMD 7000h-7700h

R	GB 1-1-1 Bit	DCX	<b>D</b> [7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
	CMDWR	0	0	0	0	0	0	0	0	0	0x2C for GRAM Write
1st R	AM Data Write	1	x	x	P1[2]	P1[1]	P1[0]	P2[2]	P2[1]	P2[0]	1,2 Pixel Data Write
2nd R	AM Data Write	1	x	x	P3[2]	P3[1]	P3[0]	P4[2]	P4[1]	P4[0]	3,4 Pixel Data Write
3rd R.	AM Data Write	1	x	x	P5[2]	P5[1]	P5[0]	P6[2]	P6[1]	P6[0]	5,6 Pixel Data Write
	So on										

Example:

 $P1[2:0] = 3'b101 = \{ R_0101[7:0], G_0101[7:0], B_0101[7:0] \}$ 

CMD 7500h-7502h



RGB4bit\_en = 1(80h-B3):

Supporting in IFPF[2:0]=011 case setting by 3A00h (interface pixel format is SPI 1-1-1).

Four bits per pixel formats map directly to 24bits by CMD 7000h-7F00h

our bito por pixor re										
RGB 1-1-1 Bit	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	0	0	0	0	0	0	0x2C for GRAM Write
1st RAM Data Write	1	P1[3]	P1[2]	P1[1]	P1[0]	P2[3]	P2[2]	P2[1]	P2[0]	1,2 Pixel Data Write
2nd RAM Data Write	1	P3[3]	P3[2]	P3[1]	P3[0]	P4[3]	P4[2]	P4[1]	P4[0]	3,4 Pixel Data Write
3rd RAM Data Write	1	P5[3]	P5[2]	P5[1]	P5[0]	P6[3]	P6[2]	P6[1]	P6[0]	5,6 Pixel Data Write
So on										

Example:

 $P1[3:0] = 4'b1101 = \{ R_1101[7:0], G_1101[7:0], B_1101[7:0] \}$ 

CMD 7D00h-7D02h

gray256\_color(80h-B[2:0]):

Supporting in IFPF[2:0]=001 case setting by 3A00h (interface pixel format is SPI 256 Gray). This command sets the valid red, green and blue 256 grayscale

#### Description

gray256_color[2:0]	Red grayscale	Green grayscale	Blue grayscale
000	00000000	00000000	00000000
001	00000000	00000000	P[7:0]
010	00000000	P[7:0]	00000000
011	00000000	P[7:0]	P[7:0]
100	P[7:0]	00000000	00000000
101	P[7:0]	00000000	P[7:0]
110	P[7:0]	P[7:0]	00000000
111	P[7:0]	P[7:0]	P[7:0]

RGB565\_swap(80h-B4):

Supporting in IFPF[2:0]=101 case setting by 3A00h. (interface pixel format is 16bit/pixel)

This command sets little-endian pixel mode

Example:

RGB565\_swap=0: R4 R3 R2 R1 R0 G5 G4 G3, G2 G1 G0 B4 B3 B2 B1 B0 RGB565 swap=1: G2 G1 G0 B4 B3 B2 B1 B0, R4 R3 R2 R1 R0 G5 G4 G3

Restriction

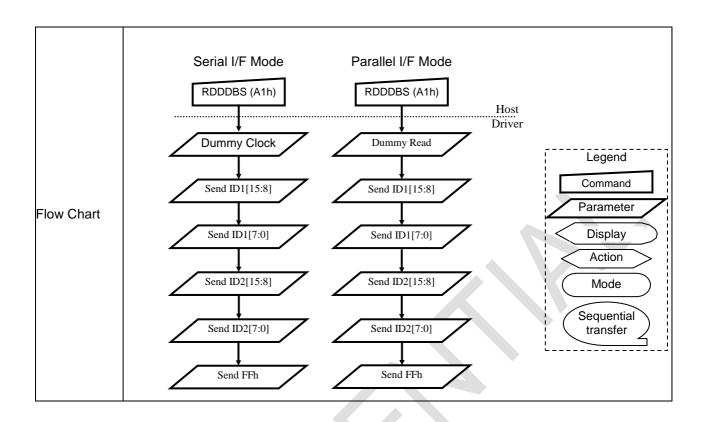


	Status	Availability	
	Normal Mode On, Idle Mo		
Register	Normal Mode On, Idle Mo	de On, Sleep Out Yes	
Availability	Partial Mode On, Idle Mod	•	
	Partial Mode On, Idle Mod	· ·	
	Sleep In	Yes	
	•		
	Status	Default Value	
	Power On Sequence	07h	
Default	SW Reset	07h	
	HW Reset	07h	
	TIW Keset	O/II	
Flow chart	8 colors Pixel Mode  COLOPT (80h)  1st Parameter (0Fh)  16 colors Pixel Mode	Legend Command Parameter Display Action Mode Sequentia transfer	



# RDDDBS(A100h): Read\_DDB\_Start

A100H		Address												
Inst/Para	R/W			D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
			A100h	х	SID[7]	SID [6]	SID [5]	SID [4]	SID [3]	SID [2]	SID [1]	SID [0]	D0	
			A101h	х	SID[15]	SID[14]	SID[13]	SID[12]	SID[11]	SID[10]	SID[9]	SID[8]	01	
RDDDBS	R	A1h	A102h	х	MID[7]	MID[6]	MID[5]	MID[4]	MID[3]	MID[2]	MID[1]	MID[0]	80	
			A103h	х	MID[15]	MID[14]	MID[13]	MID[12]	MID[11]	MID[10]	MID[9]	MID[8]	90	
			A104h	Х	1	1	1	1	1	1	1	SID [0]   SID[8]   MID[0]   1   1   1   1   1   1   1   1   1	FF	
Description	1 <sup>st</sup> 2 <sup>nd</sup> 3 <sup>rd</sup> 4 <sup>th</sup> 5 <sup>th</sup>	parameter: Supplier ID code parameter: Module ID parameter: Module ID Exit code (FFh).  Status  Availability												
Restriction														
Register Availability		•	Nor Nor Part	us mal Mod mal Mod ial Mod	de On, le	dle Mo	de On, le Off, S	Sleep C	Out YOut YOut Y	es es	lity			
				ep In	· ·		<u> </u>			es				
												_		
		Statu	s			Defau	ult Value	e 						
						After	MTP	В	Sefore M	1TP				
Default		Powe	r On Se	equence		MTP	Value	0	1h, D0h	n, 90h, 6	60h, FF	h		
		SW R	Reset			MTP	Value	0	1h, D0h	SID [2] SID [1] SID  SID[10] SID[9] SID  MID[2] MID[1] MID  MID[10] MID[9] MID  1 1 1  Availability  Yes  Yes  Yes  Yes	h			
		HW F	Reset			MTP	Value	0	1h, D0h	n, 90h, 6	60h, FF	[1] SID [0] [1] SID[8] [1] MID[8] [1] [1] M		





# RDDDBC(A800h): Read DDB Continous

A800H						F	RDDDB	С					
		Add	Iress										
Inst/Para	R/W	MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	[2] SID [1] SID [10] SID[9] SID [2] MID[1] MID [10] MID[9] MID [10] 1 [10] mode/revision [10] mode/revision [10] mode/revision	D0	HEX
			A800h	х	SID[7]	SID [6]	SID [5]	SID [4]	SID [3]	SID [2]	SID [1]	SID [0]	D0
			A801h	Х	SID[15]	SID[14]	SID[13]	SID[12]	SID[11]	SID[10]	SID[9]	SID[8]	01
RDDDBC	R	A8h	A802h	Х	MID[7]	MID[6]	MID[5]	MID[4]	MID[3]	MID[2]	MID[1]	MID[0]	80
			A803h	Х	MID[15]	MID[14]	MID[13]	MID[12]	MID[11]	MID[10]	MID[9]	MID[8]	90
			A804h	Х	1	1	1	1	1	1		1	FF
Description	Note: block Note: 1. Se 2. Re	Paran For us t maxii ad 0x/	neter 0x se exan mum re 11, retu		n "Exit C ket size es SID[7	code", tf =3 7:0], SID	nis mea 0[15:8],	ns that  MID[7:0	there is	no moi	re data i	in the D	DB
Restriction	DDB comm	Contin nand (F	ue RDDDB		fine the								
			Ctot			<u> </u>			A	veileki	1:4.		
			Stat	mal Mod	de On.	ldle Mo	de Off.	Sleep		vallabi 'es	lity		
Register	4			mal Mod						es			
Availability			Part	ial Mod	e On, lo	dle Mod	le Off,	Sleep C	out Y	es			
			Part	ial Mod	e On, Id	dle Mod	le On, S	Sleep C	ut Y	es			
			Slee	p In					Y	es			



	Status	Default Value	e
	Status	After MTP	Before MTP
Default	Power On Sequence	MTP Value	01h, D0h, 90h, 60h, FFh
	SW Reset	MTP Value	01h, D0h, 90h, 60h, FFh
	HW Reset	MTP Value	01h, D0h, 90h, 60h, FFh
Flow Chart	RDDDBC(A	A8h)	Legend  Command  Parameter
	RDDDBS I D1[7:0] D2[7:0], ···, [	ļ,	Display Action Mode
			Sequential transfer



# RDFCS(AA00h): Read First Checksum

AA00H							RDFCS	5					
Inst/Para	R/W	Add	dress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDFCS	R	AAh	AA00h	х	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0	00
Description	Set" a regist	area ers (no ss to th	ot includ	rns the f de "Manu me mem	ufacture	: Comm	and Se						
Restriction	area			to wait î					rite acc	ess on	"User C	ommar	nd Set"
	١.,	01-1							1	1 - 1 - 11 4 - 1		_	
	-			On Idl	e Mode	Off S	leen Oi	ıt		liability			
Register													
Availability	<u> </u>						•		Yes				
				-					Yes				
		Sleep	In						Yes				
Default		Partial Mode On, Idle Mode On, Sleep Out Sleep In  Status Power On Sequence O0h S/W Reset H/W Reset O0h											
Flow Chart	Status Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes  Status Power On Sequence S/W Reset Ooh												



# RDCCS(AF00h): Read Continue Checksum

AF00H							RDCCS	3					
Inst/Para	R/W	Add MIPI	dress Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCCS	R	AFh	AF00h	х	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0	00
Description	the fir	st sum h	as calc	rns the outline the control of the c	om "Us	er Com	mand S	et" area	a registe	ers and	the fran	-	
Restriction				to wait 3 e there								ommar	nd Set"
		Statu							Availa	ability			
				de On, lo					Yes				
Register Availability				de On, lo					Yes				
Availability				e On, Id					Yes				
				e On, Id	ie woa	e On, S	leep O	ut					
		Siee	p in						res				
Default		Partial Mode On, Idle Mode On, Sleep Out Sleep In  Status Power On Sequence S/W Reset H/W Reset  O0h  O0h  O0h											
Flow Chart		5	[	Send Pa	rameter					P	Legend Command aramete Display Action Mode equential transfer		



## SetDISPMode (C200h): set\_DISP Mode

C200H		MIPI   Other												
Inst/Para	R/W		C	)15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
SetDISPMode	W			X	0	0	0	0	0	0	DM1	DM0	00	
	_		0_00											
Description					-		selection	n	2'b00: inte 2'b01: rese 2'b10: rese 2'b11: exte	erved erved ernal timi	ing (VSY	/NC +		
Restriction	Note: (1)If	video r	node, nee	ed to	set DM[	1:0] = 2	?'b11.							
			Status		_	_				Availa	bilitv			
					de On,	ldle Mo	de Off,	Slee	p Out		,	7		
Register			Norma	l Mo	de On,	ldle Mo	de On,	Slee	p Out	Yes				
Availability			Partial	Mod	e On, le	dle Mod	de Off,	Sleep	p Out	Yes				
	<b>(</b>		Partial	Mod	e On, l	dle Mod	de On, S	Sleep	Out	Yes				
			Sleep	In						Yes				
Flow Chart		Com Pars  L A Si	mend mand Display Display Mode Dequential transfer											

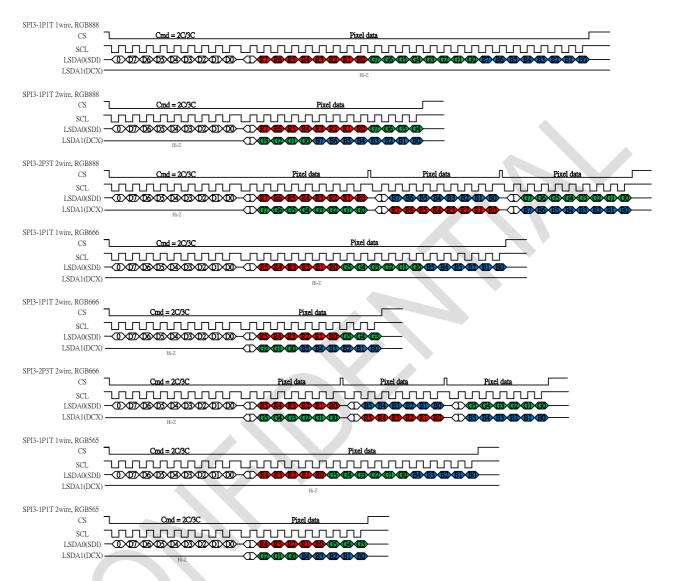


# SetDSPIMode (C400h): set\_DSPI Mode

C400H		,				Set	DSPI n	node	9					
Inst/Para	R/W		dress Other	D15-8	D7	D6	D5	D4	4	D3	D2	D1	D0	HEX
SetDSPIMode	W	C4h	C400h	x	SPI_WR AM	0	DSPI_C FG1	DSP FG		0	0	0	DSPI_E N	00
					<u>I</u>		rui	10					I IN	
		Bit		Des	cription					disable		_		
	1	DSPI_EN	l	DAU	IL SPI MC	DE Enal	ole			enable				
		DSPI_CF	G[1:0]	DAU	IL SPI MC	DE Sele	ction		10 11	: 1P1T f	or 1 wire or 2 wire or 2 wire ed			
Description	:	SPI_WR#	AM	SPI/S Maki befo	command SPINK int ing sure to re host wi SPINK int	erfaces. o set SPI rites SRA	_WRAM=	1		disable SPI inte	rface wr	ite RAM	enable	
Restriction	Note	e: detail	ed DAUL	. SPI f	formats	are des	scribed a	at ne	ext p	oage.				
			Status								Availa	bility		
							de Off,		-	-	Yes			
Register Availability				-			de On,				Yes			
Availability							de Off,				Yes			
					e On, I	dle Mo	de On,	Slee	рO	ut	Yes			
			Sleep	ln							Yes			
Flow Chart	4	Para  D  Ac	mand  Display  Stion  Mode  equential transfer	>										

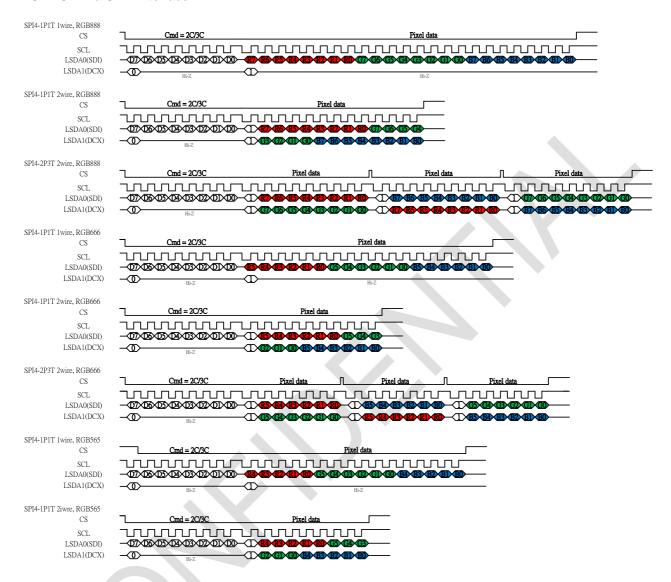


#### DUAL SPI via SPI3 interface:





#### DUAL SPI via SPI4 interface:





# RDID1 (DA00h): ID1 Code

DA00h						W	RDID								
Instruction	R/W	Ad	dress					Paran	neter						
instruction	IK/ VV	MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
WRDID	R	DAh	DA00h	00h				ID1	[7:0]				00		
	This	comma	and is for I	Module M	anufad	cture N	lumbe	r							
		ı	Bit		Desc	ription				Dat	a		]		
Description		ID1	[7:0]	Module				r							
			• •												
Restriction															
				Status					A۱	/ailabil	ity				
		Norma	al Mode O	n, Idle Mo	de Of	f, Slee	p Out			Yes					
Register		Norma	al Mode O	n, Idle Mo	de Or	n, Slee	p Out			Yes					
Availability		Partia	l Mode O	n, Idle Mo	de Off	, Slee	o Out			Yes					
		Partia	I Mode O	n, Idle Mo	de On	, Slee	Out			Yes					
				Sleep Ir						Yes					
		1											1		
			Status					Defau	lt Value	9					
							0x	DAh /	0XDA	00h					
Default		Pow	er On Sec	quence				0x	00h						
			S/W Res	et				0x	00h						
			H/W Res	et				0x	00h						



RDID2 (DB00h): ID2 Code

DB00h															
Instruction	R/W	Ad	dress					Paran	neter						
instruction	K/VV	MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
WRDID	R	DBh	DB00h	00h				ID2	[7:0]				80		
	This	s comm	and is for	Module/E	Oriver '	Versio	n Num	ber							
		ı	Bit		Desc	ription				Dat	a				
Description		ID2	2[7:0]	Module/	Driver	Versior	n Numb	er		7					
	!			I				<u> </u>					<b>_</b>		
Restriction															
				Status					A	vailabil	ity				
		Norma	al Mode O	n, Idle Mo	de Of	f, Slee	p Out			Yes					
Register		Norma	al Mode O	n, Idle Mo	de Or	n, Slee	p Out			Yes					
Availability		Partia	l Mode O	n, Idle Mo	de Off	, Slee	o Out			Yes					
		Partia	l Mode O	n, Idle Mo	de On	, Slee	o Out			Yes					
				Sleep In	1					Yes					
													•		
			Status					Defau	lt Value	9					
			Olalus				0x	DBh /	0XDB(	00h					
Default		Pow	er On Sec	quence				0x	80h						
			S/W Res	et				0x	80h						
			H/W Res	et				0x	80h						
			_			_		_		_	_	_	-		



RDID3 (DC00h): ID3 Code

DC00h						WI	RDID								
Instruction	R/W	Ad	dress					Paran	neter						
Instruction	IN/ WW	MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
WRDID	R	DCh	DC00h	00h				ID3	[7:0]				00		
	This	comma	ind is for I	Module / D	Oriver	ID									
Description		E	Bit		Desc	ription				Dat	a				
Description		ID3	5[7:0]	N	lodule	/Driver	ID								
Restriction															
		Status Availability													
				Status					A۱	/ailabil	ity				
		Norma	al Mode O	n, Idle Mo	de Of	f, Slee	p Out			Yes					
Register		Norma	al Mode O	n, Idle Mo	de Or	n, Slee	p Out			Yes					
Availability		Partia	l Mode Oı	n, Idle Mo	de Off	, Slee	o Out			Yes					
		Partia	l Mode Or	n, Idle Mo	de On	, Slee	o Out			Yes					
				Sleep In						Yes					
													,		
			Status					Defau	lt Value	Э					
			Olalus				0x	DCh /	0xDC0	)0h					
Default		Pow	er On Sed	quence				0x	00h						
	1		S/W Res	et				0x	00h						
			H/W Res	et				0x	00h						



## (FE00h): CMD Mode Switch

FE00H			N	MAUCCTI	R (Mar	ufactu	re Cor	nman	d Set C	ontrol	)					
Instruction	D //4/	Add	dress					Param	neter							
instruction	R/W	MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX			
CMD Mode Switch	W	FEh	FE00h	00h	-	-	-		CME	)_Page	e[4:0]		00			
			and is u s sets.	sed to sw	itch the	e Manu	facture	Comn	nand P	ages a	nd Use	r				
	CI	MD_Pa	ge[4:0]	Hex '	Value				Descr	iption	$\nearrow$					
		000	00	00h (c	default)	Us	er Com	mand S	Set (UCS	S = CMI	D1)					
		000	01	0	1h	Ма	nufactu	ire Com	mand S	Set Page	e0					
		011	00	00	Ch	Ма	nufactu	ire Com	ommand Set Page0 ommand Set Page0 extension ommand Set Page Panel ID ommand Set Page Gamma1 ommand Set Page Gamma2 ommand Set Page Gamma3 ommand Set Page VSR							
		010	11	Ol	Bh	Ма	nufactu	ire Com	CMD_Page[4:0] 000  mmand Pages and User  Description  Set (UCS = CMD1)  mmand Set Page0  mmand Set Page0 extension  mmand Set Page Panel ID  mmand Set Page Gamma1  mmand Set Page Gamma2  mmand Set Page Gamma3  mmand Set Page OPS  mmand Set Page OPS  mmand Set Page DBC							
Description	00011 03h Manufacture Command Set Page Gamma2 01101 0Dh Manufacture Command Set Page Gamma3 00100 04h Manufacture Command Set Page VSR 00101 05h Manufacture Command Set Page OPS 00110 06h Manufacture Command Set Page DBC															
		000	11	0:	3h	Ma	nufactu	ire Com	nmand S	Set Page	e Gamm	na2				
		011	01	10	Oh	Ma	nufactu	ire Com	nmand S	Set Page	e Gamm	na3				
		001	00	0.	4h	Ma	nufactu	ire Com	mand S	Set Page	e VSR					
		001	01	0:	5h	Ma	nufactu	ire Com	mand S	Set Page	e OPS					
		001	10	0	6h	Ma	nufactu	ire Com	nmand S	Set Page	e DBC					
		100	00	10	0h	Ма	nufactu	ire Com	nmand S	Set ( CN	ID3_TP	)				
Restriction	-															
				Sta	itus					Availal	oility					
		Nori	mal Mod	e On, Idle	Mode	Off, SI	еер Оі	ut		Yes	3					
Register		Nori	mal Mod	e On, Idle	Mode	On, SI	еер О	ut		Yes	S					
Availability		Par	tial Mod	e On, Idle	Mode	Off, Sl	еер Ои	ıt		Yes	3					
		Par	tial Mod	e On, Idle	Mode	On, Sl	eep Ou	ıt		Yes	3					
				Slee	p In					Yes	6					



	Status	Default Value
	Status	FEh / FE00h
Default	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h
Flow Chart	Legend Command Parameter Display Action Mode Sequential transfer	

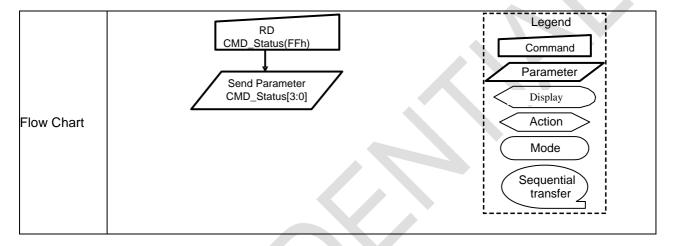


# (FF00h): Read CMD Status

FF00H	MAUCCTR (Manufacture Command Set Control)													
Instruction	DAM	Add	dress					Param	eter					
mstruction	R/W	MIPI	Others	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
RD CMD Status	R	FFh	FF00h	00h	-	-	-		CMD	_Statu	s[4:0]		00	
		nis command is used to switch the Manufacture Command Pages and User												
		mands												
	CN		tus[4:0]	Hex	Value				Descr					
		000	000		default)				Set (UCS					
		000	001	(	)1h	Ma	ınufactu	ire Com	mand S	Set Page	e0			
		011	100	C	)Ch	Ma	ınufactu	ire Com	mand S	Set Page	e0 exter	nsion		
		010	011	(	)Bh	Ma	ınufactu	ire Com	mand S	Set Page	Panel	ID		
Description		000	010	(	)2h	Ma	Manufacture Command			mand Set Page Gamma1				
		000	D11	03h Manufa			Manufacture Command Set Page Gamma2							
		011	101	0Dh I			ınufactu	ire Com	mand S	Set Page	e Gamm	na3		
		001	100	(	04h	Ma	ınufactu	re Com	mand S	Set Page	e VSR	3R		
		001	101	(	)5h	Ma	ınufactu	ire Com	mand S	Set Page	e OPS			
		001	110		06h	Ma	inufactu	ire Com	mand S	Set Page	e DBC			
		100	000	,	10h	Ma	ınufactu	ire Com	mand S	Set ( CN	ID3_TP	)		
Restriction	-													
				Sta	itus					Availal	oility			
		Nori	mal Mod	e On, Idle	Mode	Off, S	еер О	ut		Yes	S			
Register		Nori	mal Mod	e On, Idle	Mode	On, S	еер Оі	ut		Yes	S			
Availability	Availability Partial Mode On, Idle Mode Off, Sleep Out Yes													
		Par	tial Mod	e On, Idle	Mode	On, Sl	eep Ou	ıt		Yes	S			
				Slee	p In				Yes					



	Status	Default Value
	Status	FFh / FF00h
Default	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h
		3011





# 7 Electrical Characteristics

## 7.1 Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When WT030 is used out of the absolute maximum ratings, the WT030 may be permanently damaged. To use the WT030 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the WT030 will malfunction and cause poor reliability.

item	Symbol	Value	Unit
Power supply voltage	VDDI	-0.3 ~ + 5.5	V
Power supply voltage	VDD (VDDA, VDDB, VDDR)	-0.3 ~ + 5.5	V
Cumply valtage (NAV)	AVDD- AVSS	-0.3 ~ + 6.6	V
Supply voltage (MV)	AVSS- VCL	-0.3 ~ + 5.0	V
Supply voltage (HV)	VGH- VGLX	-0.3 ~ + 33	V
Input voltage	VIN	-0.3 ~ VDDI+ 0.3	V
Output voltage	VO	-0.3 ~ VDDI+ 0.3	V
Operating temperature	Topr	-40 ~ + 85	°C
Storage temperature	Tstg	-55 ~ + 125	°C

#### Notes:

If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation. Therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

#### 7.2 ESD Protection Level

Model	Test Condition	Level
Human Body Mode	R = 1.5  kohm  / C = 100  pF	Pass 3KV
Machine Mode	R = 0 ohm / C = 200 pF	Pass 300V

# 7.3 Latch-Up Protection Level

The device will not latch up at trigger current levels less than ±200 mA.



## 7.4 DC Characteristics

#### 7.4.1 Basic Characteristics

	Symbol	Condition	Min.	Тур.	Max.	Unit	Related Pins
Parameter							
Analog Power Supply Voltage	VDD	Operation Voltage	2.7	2.8	3.6	V	Note 1
I/O pin Power Supply Voltage	VDDI	I/O supply voltage	1.65	1.8	1.95	V	Note 1,2
70 pili Fowei Supply Voltage							
ogic High level input voltage	VIH	VDDI = 1.65V ~ 3.3V	0.8* VDDI	-	VDDI	V	Note 3
ogic Low level input voltage	VIL	VDDI = 1.65V ~ 3.3V	0.0	-	0.2* VDDI	V	Note 3
ogic High level Output voltage	VOH	lout = -1 mA	0.8* VDDI	-	VDDI	V	Note 3
ogic Low level Output voltage	VOL	lout = +1 mA	0.0	-	0.2* VDDI	V	Note 3
Logic High level input current (Except MIPI)	IIHD	Vin=0~VDDI			1	uA	Note 3
Logic Low level input current (Except MIPI)	IILD	Vin=0~VDDI	-1			uA	Note 3
_ogic High level input current (MIPI)	IIHD	Vin=0~VDDI			1	uA	Note 3
Logic Low level input current (MIPI)	IILD	Vin=0~VDDI	-1			uA	Note 3
AVDD booster voltage	AVDD		4.5		6.5	V	Note 3
/CL booster voltage	VCL		-3.5		-5	V	Note 3
VGH booster voltage	VGH		AVDD		2AVDD	V	Note 3
VGL booster voltage	VGL		VCL		VCL -AVDD	V	Note 3
Voltage difference between VGH and VGL	VGHL	VGH-VGL			30	V	Note 3
Gamma reference voltage	VGMP _		2.0		6.0	V	Note 3,4
Gamma reference voltage	VGSP		0.0		4.5	V	Note 3
_							
OSC	Fosc		20.24	22	23.76	MHz	
Channel deviation voltage	$V_{DEV}$	Sout ≥ AVDD-1.0V, and 0V < Sout ≤ 1.0V				mV	TBD
Channel deviation voltage	$V_{DEV}$	1.0V < Sout < AVDD-1.0V				mV	TBD

#### Notes

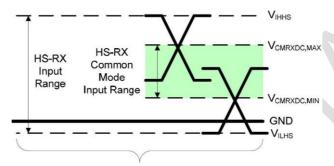
- 1. VDD means VDDA, VDDB, VDDB. And VSS means VSSA, VSSB, AVSS, VSSAM. VDDB, VDDA and VDDR should be the same input voltage level and larger than VDDI voltage.
- 2. Recommend VDDI=1.8V for power saving.
- 3. Ta(ambient temperature) ranges from -30 $^{\circ}$ C to 85 $^{\circ}$ C.
- 4. VGMP <= AVDD 0.5V



### 7.5 MIPI Characteristics

## 7.5.1 High-Speed Receiver Specification

#### DC Specifications



High Speed Receiver

Parameter	Description	Min	Nom	Max	Units	Note
VCMRX(DC)	Common-mode voltage HS receive mode	70		330	m∨	1,2
VIDTH	Differential input high threshold			70	mV	
VIDTL	Differential input low threshold	-70			mV	
VIHHS	Single-ended input high voltage			460	mV	1
VILHS	Single-ended input low voltage	-40			mV	1
ZID	Differential input impedance	80	100	125	Ω	

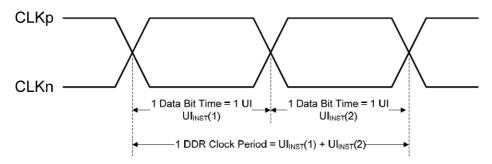
#### Notes:

- 1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
- 2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz



### 7.5.2 Forward high speed transmissions

### **DDR Clock Definition**



Clock Parameter	Symbol	Min	Тур	Max	Units	Notes
UI instantaneous	UI <sub>INST</sub>	2		12.5	ns	1,2

#### Notes:

- 1. This value corresponds to a minimum 80 Mbps data rate.
- 2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

### **Data-Clock Timing Specifications**

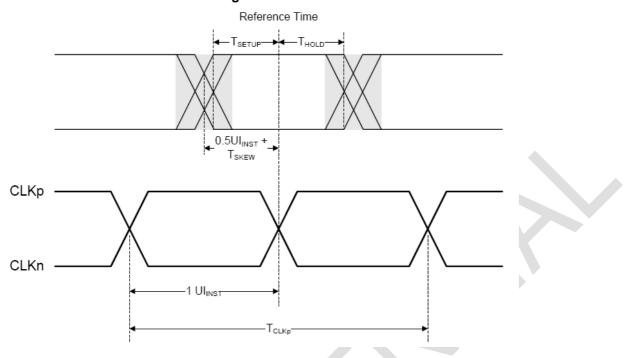
Parameter	Symbol	Min	Тур	Max	Units	Notes
Data to Clock Skew [measured at transmitter]		-0.15		0.15	UI <sub>INST</sub>	1
Data to Clock Setup Time [receiver]	T <sub>SETUP[RX]</sub>	0.15			UI <sub>INST</sub>	2
Clock to Data Hold Time [receiver]	T <sub>HOLD[RX]</sub>	0.15			UI <sub>INST</sub>	2

#### Notes:

- 1. Total silicon and package delay budget of 0.3\*UI<sub>INST</sub>
- 2. Total setup and hold window for receiver of  $0.3^*UIINST$



# 7.5.3 Data to Clock Timing Definitions





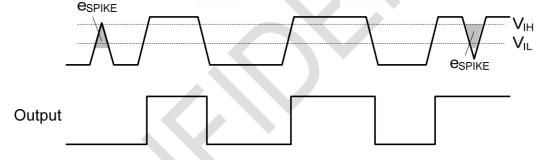
### 7.5.4 Low power transceiver specifications

Parameters	Symbol	Condition	Min	Тур	Max	Unit
Logic high level input voltage	VIHCD	Contention Detection (Lane_D0)	450		1350	mV
Logic low level input voltage	VILCD	Contention Detection (Lane_D0)	0		200	mV
Logic high level input voltage	VIH-LPRX	LP-Rx (Lane_CK, Lane_D0, Lane_D1)	880	-	1350	mV
Logic low level input voltage	VIL-LPRX	LP-Rx (Lane_CK, Lane_D0, Lane_D1	0		550	mV
Logic low level input voltage	VIL-ULPS	LP-Rx ULPS (Lane_CK, Lane_D0, Lane_D1)	0		300	mV
Logic high level input voltage	VOH-LPTX	Contention Detection (Lane_D0)	1.1	1.2	1.3	V
Logic low level input voltage	VOL-LPTX	Contention Detection (Lane_D0)	-50	0	50	mV
eSPIKE <sup>(1.2.3)</sup>	Fig. 2	Input pulse rejection			300	V.ps

#### Notes:

Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 State. An impulse less than this will not change the receiver state.

In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers. Input Glitch Rejection of Low Power Receivers as follow.

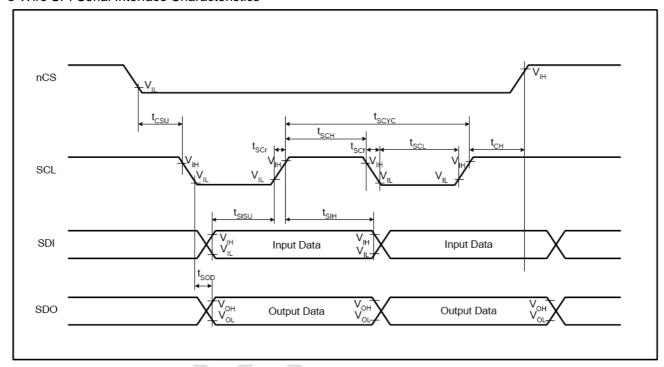




### 7.6 AC Characteristics

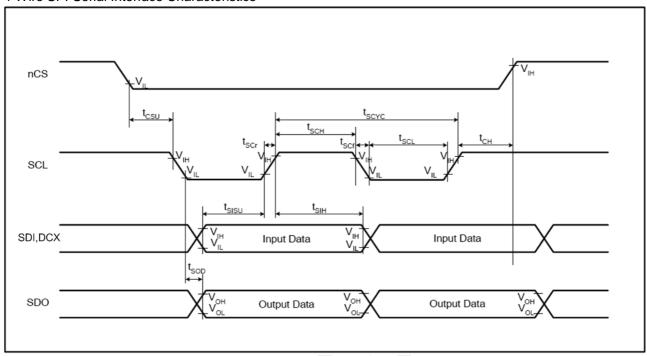
### 7.6.1 Serial Interface Characteristics

3-Wire SPI Serial Interface Characteristics





### 4-Wire SPI Serial Interface Characteristics



Signal	Symbol	Parameter	MIN	MAX	Unit	Description
	T <sub>SCYC</sub>	Clock cycle (Write)	20		ns	
	T <sub>SCYC</sub>	Clock cycle (Read)	300		ns	
	T <sub>SCH</sub>	Clock "H" pulse width (Write)	9		ns	
SCL	T <sub>SCH</sub>	Clock "H" pulse width (Read)	140		ns	
SCL	T <sub>SCL</sub>	Clock "L" pulse width (Write)	9		ns	-
	T <sub>SCL</sub>	Clock "L" pulse width (Read)	140		ns	
	T <sub>SCr</sub>	Clock rise time		2	ns	
	$T_{SCf}$	Clock fall time		2	ns	
nCS	T <sub>CSU</sub>	Chip select setup time	10		ns	
1103	T <sub>CH</sub>	Chip select hold time	10		ns	-
SDI (SDA)	$T_{SISU}$	Data input setup time	5		ns	
SDI (SDA)	T <sub>SIH</sub>	Data input hold time	5		ns	_
SDO (SDA)	T <sub>SOD</sub>	Data output setup time		120	ns	
3DO (3DA)	T <sub>SOH</sub>	Data output hold time	5		ns	-

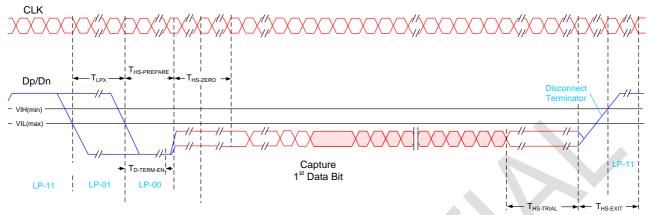
Note: Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

Note: Ta = -30 to 70 °C, VDDI=1.65V to 1.95V, VDD=2.7V to 3.6V, GND=0V

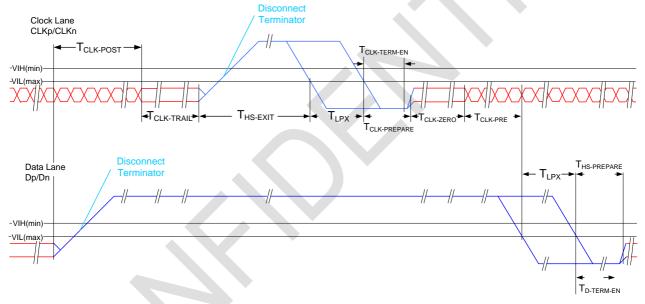


## 7.6.2 DSI Timing Characteristics

### **HS Data Transmission Burst**



### HS clock transmission



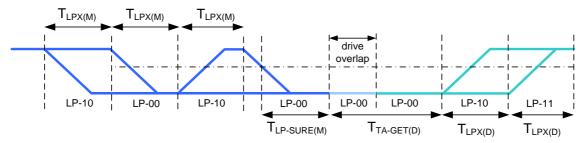


**Timing Parameters:** 

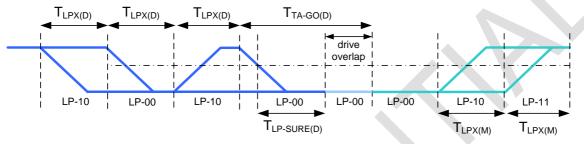
Parameter	Description	Min	Тур	Max	Unit
T <sub>CLK-POST</sub>	Time that the transmitter continues to send HS clock after the last associated Data	60ns + 52*UI	7.5		ns
	Lane has transitioned to LP Mode. Interval				
	is defined as the period from the end of				
	T <sub>HS-TRAIL</sub> to the beginning of T <sub>CLK-TRAIL</sub> .				
T <sub>CLK-TRAIL</sub>	Time that the transmitter drives the HS-0	60			ns
	state after the last payload clock bit of a HS				
	transmission burst.				
T <sub>HS-EXIT</sub>	Time that the transmitter drives LP-11 following a HS burst.	300			ns
T <sub>CLK-TERM-EN</sub>	Time for the Clock Lane receiver to enable	Time for Dn to		38	ns
	the HS line termination, starting from the	reach V <sub>TERM-EN</sub>			
	time point when Dn crosses V <sub>IL,MAX</sub> .				
T <sub>CLK-PREPARE</sub>	Time that the transmitter drives the Clock	38		95	ns
	Lane LP-00 Line state immediately before				
	the HS-0 Line state starting the HS				
	transmission.				
T <sub>CLK-PRE</sub>	Time that the HS clock shall be driven by	8			UI
	the transmitter prior to any associated Data				
	Lane beginning the transition from LP to				
	HS mode.				
T <sub>CLK-PREPARE</sub>	T <sub>CLK-PREPARE</sub> + time that the transmitter	300			ns
+ T <sub>CLK-ZERO</sub>	drives the HS-0 state prior to starting the				
	Clock.				
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable	Time for Dn to		35 ns +4*UI	
	the HS line termination, starting from the	reach V <sub>TERM-EN</sub>			
	time point when Dn crosses V <sub>IL,MAX</sub> .				
T <sub>HS-PREPARE</sub>	Time that the transmitter drives the Data	40ns + 4*UI		85 ns + 6*UI	ns
	Lane LP-00 Line state immediately before				
	the HS-0 Line state starting the HS				
_	transmission	445 40			
T <sub>HS-PREPARE</sub>	T <sub>HS-PREPARE</sub> + time that the transmitter	145ns + 10*UI			ns
+ T <sub>HS-ZERO</sub>	drives the HS-0 state prior to				
_	transmitting the Sync sequence.	00 4*!!!	-		
T <sub>HS-TRAIL</sub>	Time that the transmitter drives the flipped	60ns + 4*UI			ns
	differential state after last payload data bit				
	of a HS transmission burst				



### **Turnaround Procedure**



Bus turnaround (BAT) from MPU to display module timing



Bus turnaround (BAT) from display module to MPU timing

#### Low Power Mode:

Parameter	Description	Min	Тур	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns	1,2
$T_{TA\text{-SURE}(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T <sub>LPX(M)</sub>		2*T <sub>LPX(M)</sub>	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns	1,2
$T_{TA\text{-}GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		5*T <sub>LPX(D)</sub>		ns	2
$T_{TA\text{-}GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		4*T <sub>LPX(D)</sub>		ns	2
T <sub>TA-SURE(D)</sub>	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T <sub>LPX(D)</sub>		2*T <sub>LPX(D)</sub>	ns	2

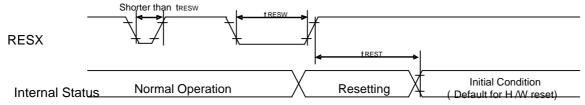
### NOTE:

2. Transmitter-specific parameter

<sup>1.</sup> T<sub>LPX</sub> is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.



### 7.6.3 Reset Timing(RESX)



Reset input timing:

VDDI=1.65 to 1.95V, VDD=2.7 to 3.6V, AGND=DGND=0V, Ta=-40 to  $85^{\circ}$ C

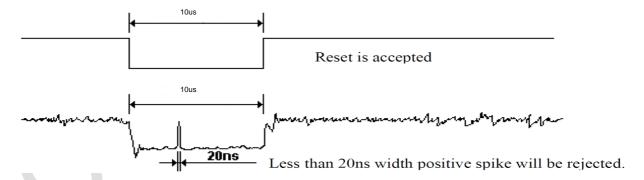
Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t <sub>RESW</sub>	*1) Reset low pulse width	RESX	10	-	-	-	μS
t <sub>REST</sub>	*2) Depot complete time	-	-	-	5	When reset applied during Sleep in mode	ms
	*2) Reset complete time	-		-	120	When reset applied during Sleep out mode	ms

Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5µs and 10µs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX. Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.



## 7.6.4 Reset Timing(TP\_EXT\_RESET)

(VDDI=1.65 to 1.95V, VDD=2.7 to 3.6V, AGND=DGND=0V, Ta=-30 to  $85^{\circ}$ C)

Symbol	Item	Min	Тур	Max	Units	Conditions
tRES	Reset low-level width	1	-	ı	ms	
trRES	Reset rise time	-	-	10	us	

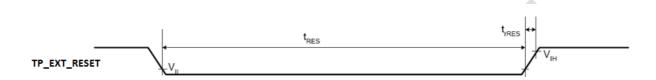


Figure 1 Reset Operation



# 7.7 I2C timing Characteristics

The I2C is always configured in the Slave mode. The definition of I2C timing is as following.

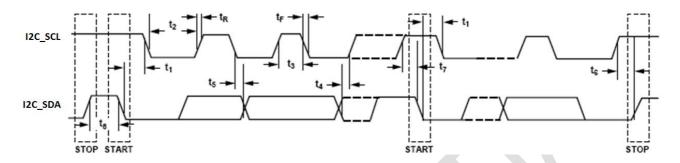


Figure 2 I2C timing Diagram

# **I2C AC Timing Specification**

(VDDI=1.65 to 1.95V, VDD=2.7 to 3.6V, AGND=DGND=0V, Ta=-30 to  $85^{\circ}$ C)

Symbol	Item	Min	Тур	Max	Units	Conditions
fSCL	I2C_SCL frequency	ì	ı	400	KHz	
t1	Start condition hold time, tHD; STA	0.6			us	
t2	Clock low period, tLOW	1.3	1	-	us	
t3	Clock high period, tHIGH	0.6	-	-	us	
t4	Data setup time, tSU; DAT	100	-	-	ns	
t5	Data hold time, tHD; DAT	120	ı	-	ns	
t6	Stop condition setup time, tSU; STO	0.6	ı	-	us	
t7	Start condition setup time, tSU; STA	0.6	ı	-	us	
t8	Bus-free time between stop and start conditions, tBUF	1.3	ı	-	us	
tR	Clock/data rise time	-	1	300	ns	
tF	Clock/data fall time	-	-	300	ns	
Cb	Capacitive load for each bus line			400	pF	

NOTE: All values are referred to VIH and VIL level of VDDI

NOTE: WT030 support I2C interface and the slave address is 39h.