Product Specification

1.28" AMOLED

MODEL NAME: U128BLX03.2

AUO Product P/N: 95.01U22.200

< ◆ >Preliminary Specification
< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2021/5/3	1~32	First edition
1.0	2021/11/12	31	Update drawing

Contents

1 General Specification

1.1 Physical Specifications

	Item	Description	Remark
1	Screen Size (inch)	1.28”	
2	Display Mode	AMOLED	
3	Display Resolution	416x416	
4	Active Area (mm*mm)	32.45 (H)× 32.45(V)	
5	Frame rate (normal mode)	45 (Hz)	
6	Pixel Configuration	Hyper R.G.B	
7	Display Color (M)	16.7	
8	Brightness (nits)	350	
9	Interface	MIPI	CMD Mode
10	Driver IC	WT030	
11	Outline Dimension (mm*mm*mm)	34.65 (H) ×34.96 (V) × 0.7 max.(T)	Glass only

1.2 FPC Pin Assignment

Main FPC Pin assignment — AMOLED Panel Input/Output Signal Interfac

FPCA recommended connector: AXG230144 / AXG230144KV1

Main board recommended connector: AXG130144 / AXG130144KV1

#	Pin_name	I/O	Description
1	VDDIO	Power	Power supply for interface system except MIPI interface
2	VDDIO	Power	Power supply for interface system except MIPI interface
3	VCI	Power	Driver analog power supply (Power IC need to follow AUO’s suggestion)
4	VCI	Power	Driver analog power supply (Power IC need to follow AUO’s suggestion)
5	CSX	I	SPI Enable Signal
6	SCL	I	SPI Clock signal
7	DCX	I	SPI CMD/Data selection signal
8	SDI	I/O	SPI data signal
9	SDO	O	SPI Output signal
10	RESX	I	Device reset signal (0 : enable ; 1 : Disable)
11	TE	O	Vsync (vertical sync) signal output from panel to avoid tearing effect
12	SWIRE	O	SWIRE signal for PWR IC control

13	ELVSS	Power	AMOLED negative power supply (Power IC need to follow AUO's suggestion)
14	ELVSS	Power	AMOLED negative power supply (Power IC need to follow AUO's suggestion)
15	ELVSS	Power	AMOLED negative power supply (Power IC need to follow AUO's suggestion)
16	ELVDD	Power	AMOLED positive power supply (Power IC need to follow AUO's suggestion)
17	ELVDD	Power	AMOLED positive power supply (Power IC need to follow AUO's suggestion)
18	ELVDD	Power	AMOLED positive power supply (Power IC need to follow AUO's suggestion)
19	TP_RES	I	TP Reset signal
20	TP_SCL	I	TP Clock signal
21	TP_SDA	I	TP Data signal
22	TP_INT	I	TP initial signal
23	GND	Power	Ground
24	DSI_D0P	I/O	MIPI positive data signal
25	DSI_D0N	I/O	MIPI negative data signal
26	GND	Power	Ground
27	DSI_CLKP	I	MIPI positive clock signal
28	DSI_CLKN	I	MIPI negative clock signal
29	GND	Power	Ground
30	NC	-	Floating

Note 1: I = input; O = output; P = Power; I/O = input / Output; NC= No Connection

Note 2: AUO suggest only use MIPI I/F, and pin of SPI I/F is connected as below.
(SCL & DCX & SDI & SDO pin is GND, and CSX is connected to VDDIO.)

1.3 Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remark
Digital Power Supply	VDDIO	-0.3	1.95	V	
Analog Power Supply	VCI	-0.3	5	V	
ELVDD power Supply	ELVDD	-	5.0	V	
ELVSS power Supply	ELVSS	-5.0	-	V	

Note : If the module exceeds the absolute maximum ratings, it may be damaged permanently.

2 DC Characteristics

2.1 Display DC Characteristics

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Digital Power Supply		VDDIO	1.65	1.8	1.95	V	Note1
Analog power Voltage		VCI	3.27	3.3	3.33	V	Note1
ELVDD power Supply		ELVDD	3.27	3.3	3.33	V	Note1
ELVSS power Supply		ELVSS	-3.33	-3.3	-3.27	V	Note1
			-3.75	-3.7	-3.65	V	Note2
Input Signal Voltage	**H Level**	VIH	0.8* VDDIO	-	VDDIO	V	Note1
	L Level	VIL	0	-	0.2* VDDIO	V	
Output Signal Voltage	**H Level**	VOH	0.8* VDDIO	-	VDDIO	V	Note1
	L Level	VOL	0	-	0.2* VDDIO	V	Note1

Note 1: The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during the operation. To prevent the noise, a bypass capacitor must be inserted into the line closed to the power pin.

Note 2: The Voltage of HBM mode

2.2 Display Only Power Consumption

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Panel Power	Normal	P_{OLED}	ELVDD:3.3V ELVSS:-3.3V	--	--	97.7	mW	Note1
		I_{OLED}		--	--	14.8	mA	Note1
	HBM	P_{OLED}	ELVDD:3.3V ELVSS:-3.7V	--	--	285.6	mW	Note 2
		I_{OLED}		--	--	40.8	mA	Note 2
IC	Normal	P_{VCI}	VCI : 3.3V	--	10.6	11.6	mW	Note3
		I_{VCI}		--	3.20	3.50	mA	Note3
		P_{VDDIO}	VDDIO :1.8V	--	2.92	3.46	mW	Note3
		I_{VDDIO}		--	1.62	1.92	mA	Note3
	Idle 15Hz	P_{VCI}	VCI : 3.3V	--	3.07	3.73	mW	Note4,6
		I_{VCI}		--	0.93	1.13	mA	Note4,6
		P_{VDDIO}	VDDIO :1.8V	--	1.39	1.57	mW	Note4,6
		I_{VDDIO}		--	0.77	0.87	mA	Note4,6
	Idle 5Hz	P_{VCI}	VCI : 3.3V	--	2.97	3.63	mW	Note5,6
		I_{VCI}		--	0.90	1.10	mA	Note5,6
		P_{VDDIO}	VDDIO :1.8V	--	1.39	1.57	mW	Note5,6
		I_{VDDIO}		--	0.77	0.87	mA	Note5,6
	Sleep	P_{VCI}	VCI : 3.3V	--	--	0.24	mW	
		I_{VCI}		--	--	0.072	mA	
		P_{VDDIO}	VDDIO :1.8V	--	--	0.45	mW	
		I_{VDDIO}		--	--	0.25	mA	
	HBM	P_{VCI}	VCI : 3.3V	--	11.9	13.2	mW	Note7
		I_{VCI}		--	3.60	4.00	mA	Note7
		P_{VDDIO}	VDDIO :1.8V	--	2.92	3.46	mW	Note7
		I_{VDDIO}		--	1.62	1.92	mA	Note7

Note 1: Based on L255 (350nits) full white pattern

Note 2: Based on L255 full white pattern at HBM mode

Note 3: Based on black pattern. MIPI-DSI frame rate 45Hz command mode.

Note 4: Based on black pattern. MIPI-DSI frame rate 15Hz command mode.

Note 5: Based on black pattern. MIPI-DSI frame rate 5Hz command mode.

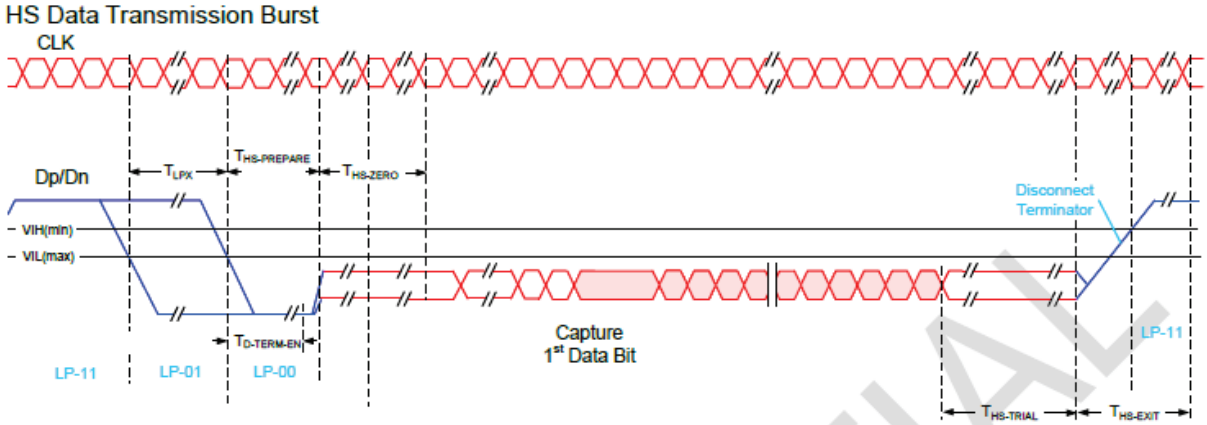
Note 6: VCI Current must < 2 mA at Idle mode & deep Idle mode in the condition of 10% pixel-on.

Note 7: Based on black pattern.

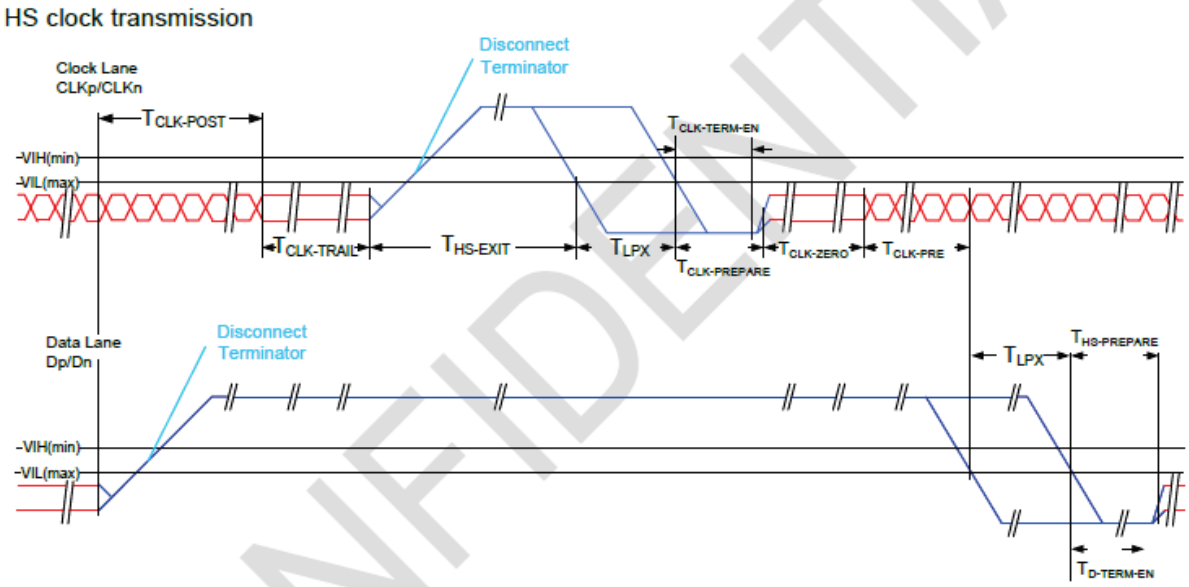
3 AC Characteristics

3.1 MIPI Interface Characteristics

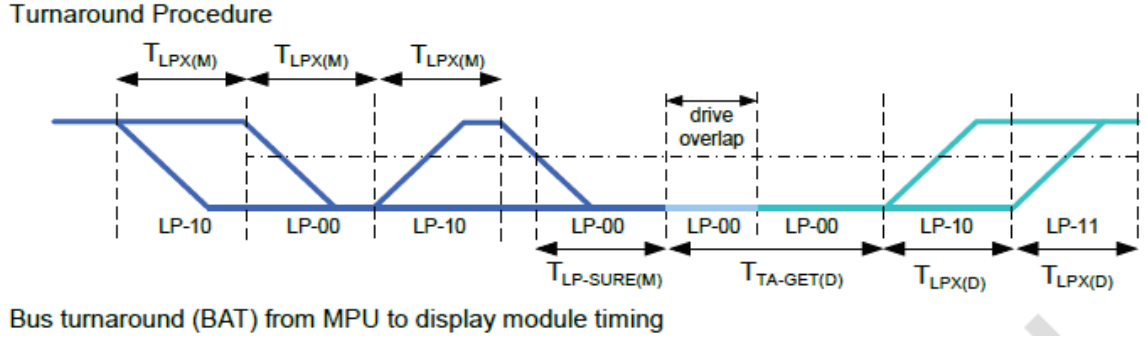
3.1.1 HS Data Transmission Burst



3.1.2 HS clock transmission

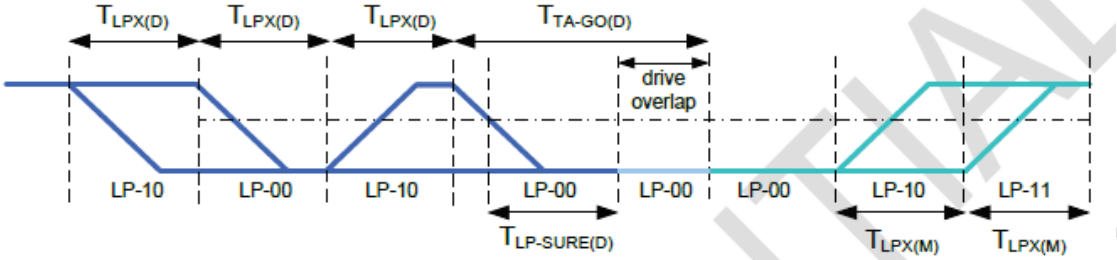


3.1.3 Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing

3.1.4 Bus turnaround (BAT) from MPU to display module timing



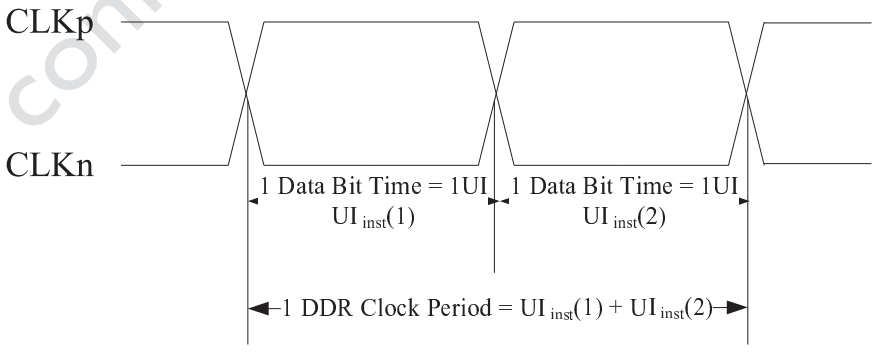
Bus turnaround (BAT) from display module to MPU timing

3.1.5 Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			Ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			Ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			Ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	Ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	Ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			Ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to Reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns

$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			Ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			Ns
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	Ns
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		2*$T_{LPX(M)}$	Ns
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	Ns
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		5*$T_{LPX(D)}$		Ns
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		4*$T_{LPX(D)}$		Ns
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		2*$T_{LPX(D)}$	Ns

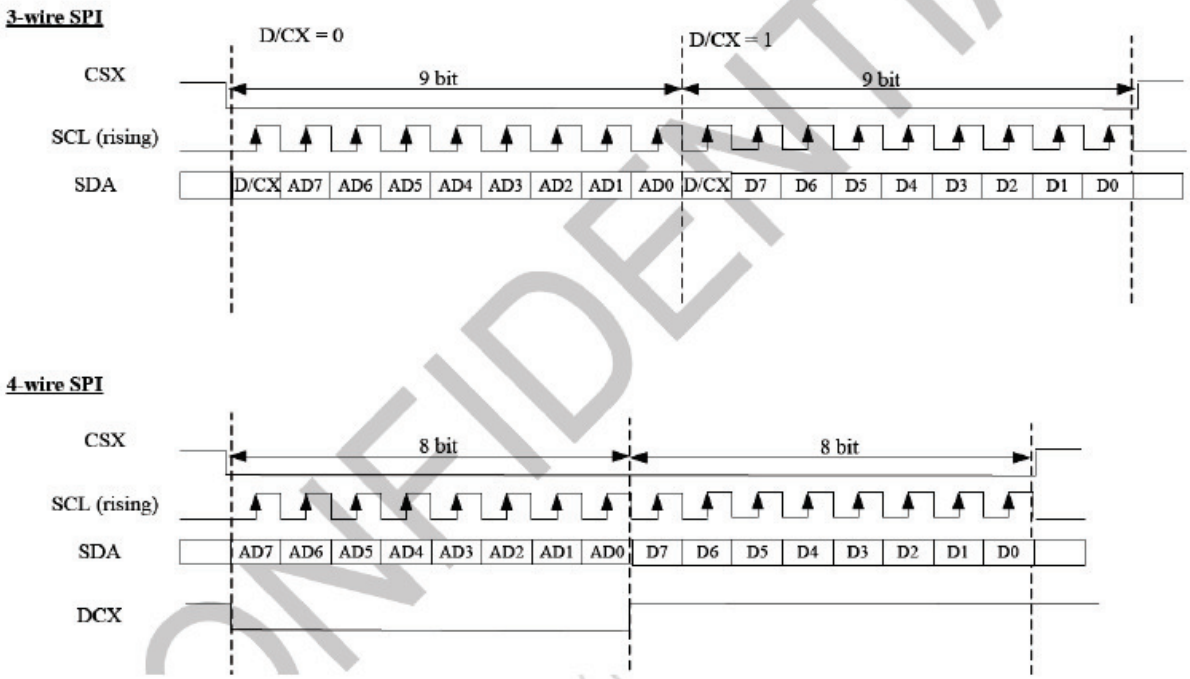
3.1.6 DDR Clock Definition



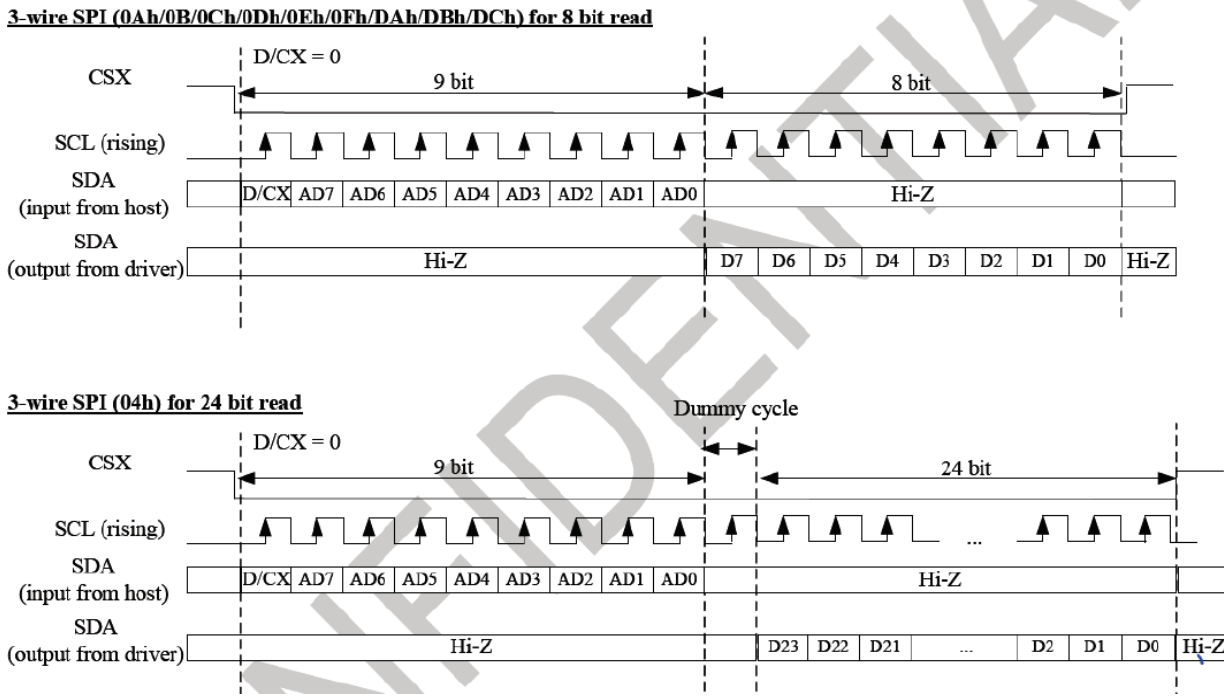
Clock Parameter	Symbol	Min	Typ	Max	Units
UI instataneous	UI_{inst}	2		12.5	ns

3.2 SPI Interface Characteristics

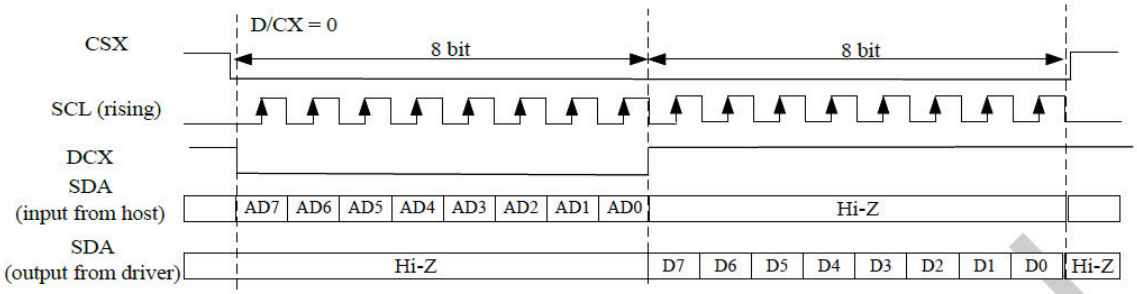
3.2.1 Write Cycle in SPI I/F



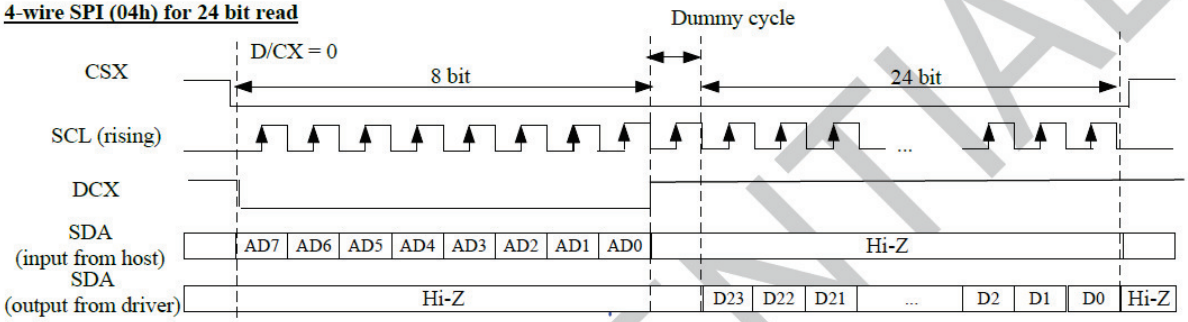
3.2.2 Read Cycle in SPI I/F



4-wire SPI (0Ah/0B/0Ch/0Dh/0Eh/0Fh/DAh/DBh/DCh) for 8 bit read

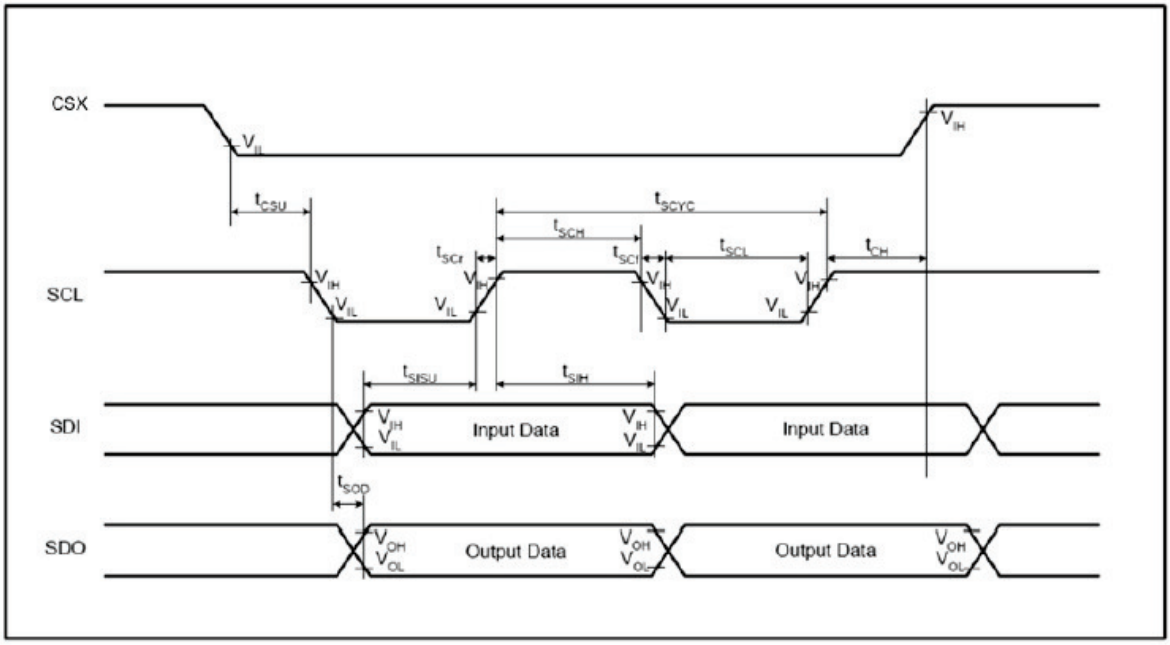


4-wire SPI (04h) for 24 bit read

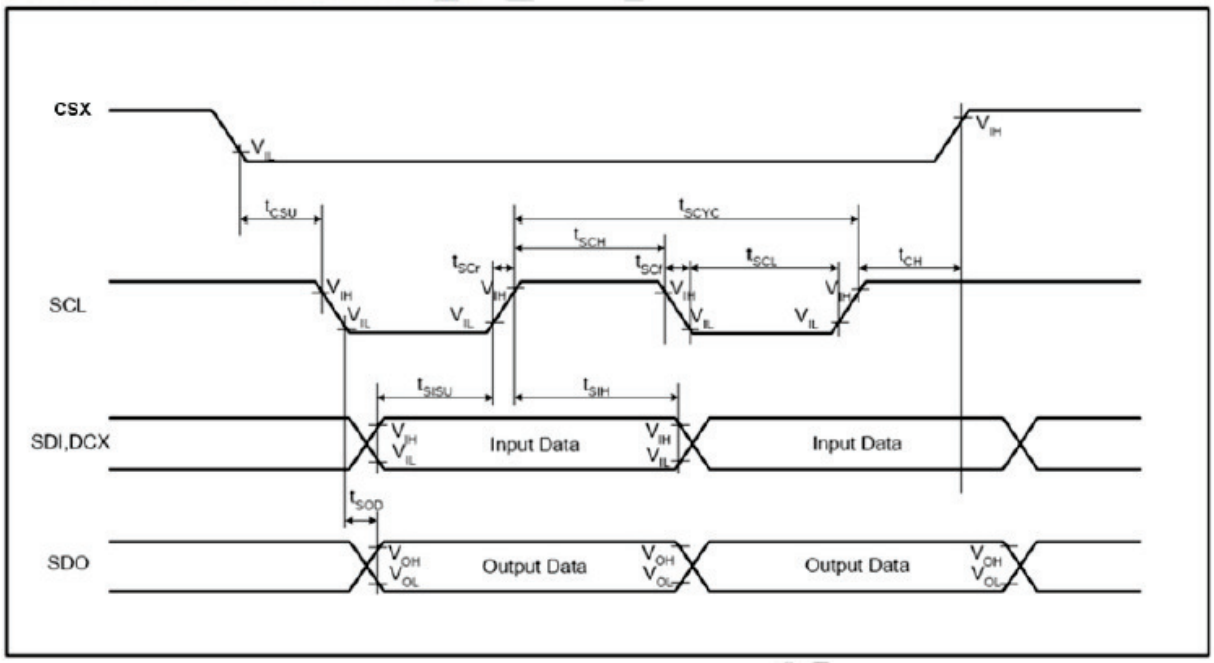


3.2.3 Serial Interface Characteristics

3-Wire SPI Serial Interface Characteristics



4-Wire SPI Serial Interface Characteristics

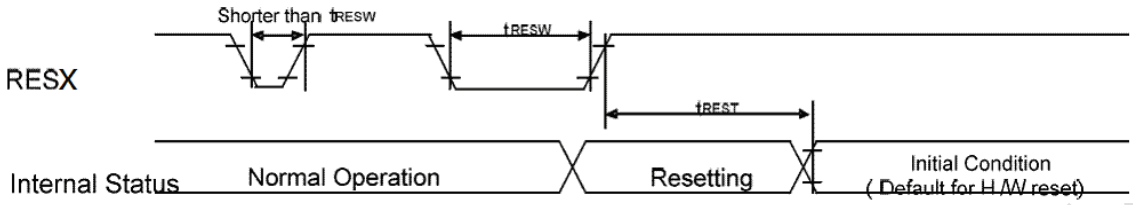


Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCL	T_{SCYC}	Clock cycle (Write)	20		ns	-
	T_{SCYC}	Clock cycle (Read)	300		ns	
	T_{SCH}	Clock "H" pulse width (Write)	9		ns	
	T_{SCH}	Clock "H" pulse width (Read)	140		ns	
	T_{SCL}	Clock "L" pulse width (Write)	9		ns	
	T_{SCL}	Clock "L" pulse width (Read)	140		ns	
	T_{SCr}	Clock rise time		2	ns	
	T_{SCf}	Clock fall time		2	ns	
CSX	T_{CSU}	Chip select setup time	10		ns	-
	T_{CH}	Chip select hold time	10		ns	
SDI (SDA)	T_{SISU}	Data input setup time	5		ns	-
	T_{SIH}	Data input hold time	5		ns	
SDO (SDA)	T_{SOD}	Data output setup time		120	ns	-
	T_{SOH}	Data output hold time	5		ns	

Note: Logic high and low levels are specified as 20% and 80% of VDDIO for Input signals. Note: Ta = -30 to 70°C, VDDIO=1.65V to 3.3V, VCI=2.7V to 3.6V, GND=0V

3.3 Display RESET Timing Characteristics

3.3.1 Reset input timing



3.3.2 Timing Parameters

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	μs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

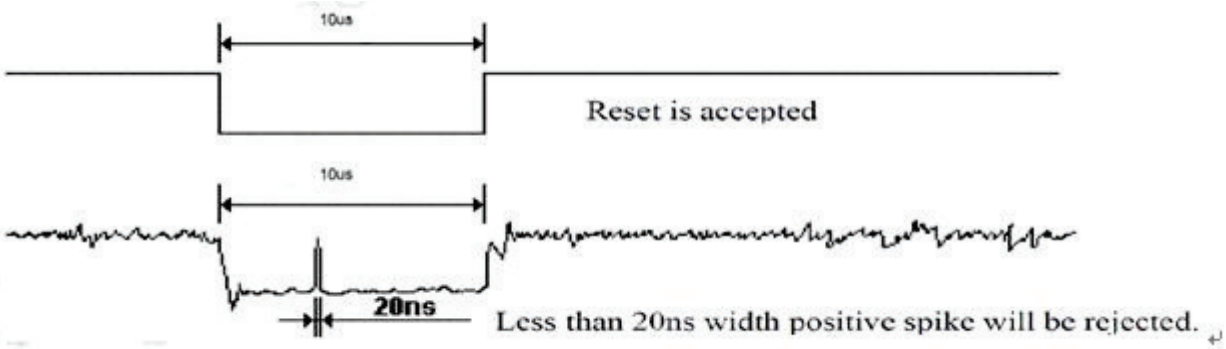
RESX Pulse	Action
Shorter than 5μs	Invalid Reset
Longer than 10μs	Valid Reset
Between 5μs and 10μs	Reset Initialigation Precedure

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

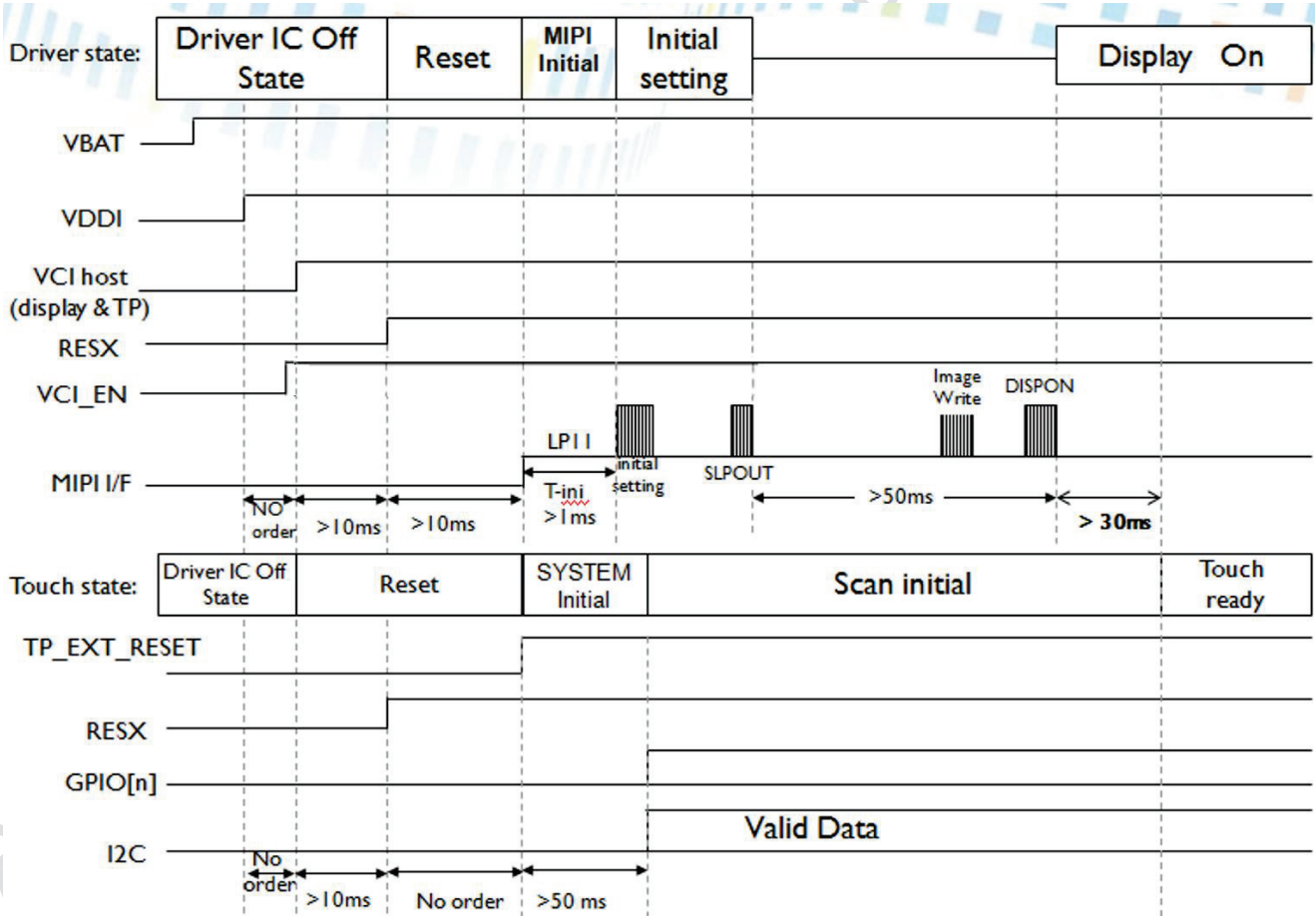
Note 4. Spike Rejection also applies during a valid reset pulse as shown below:

Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

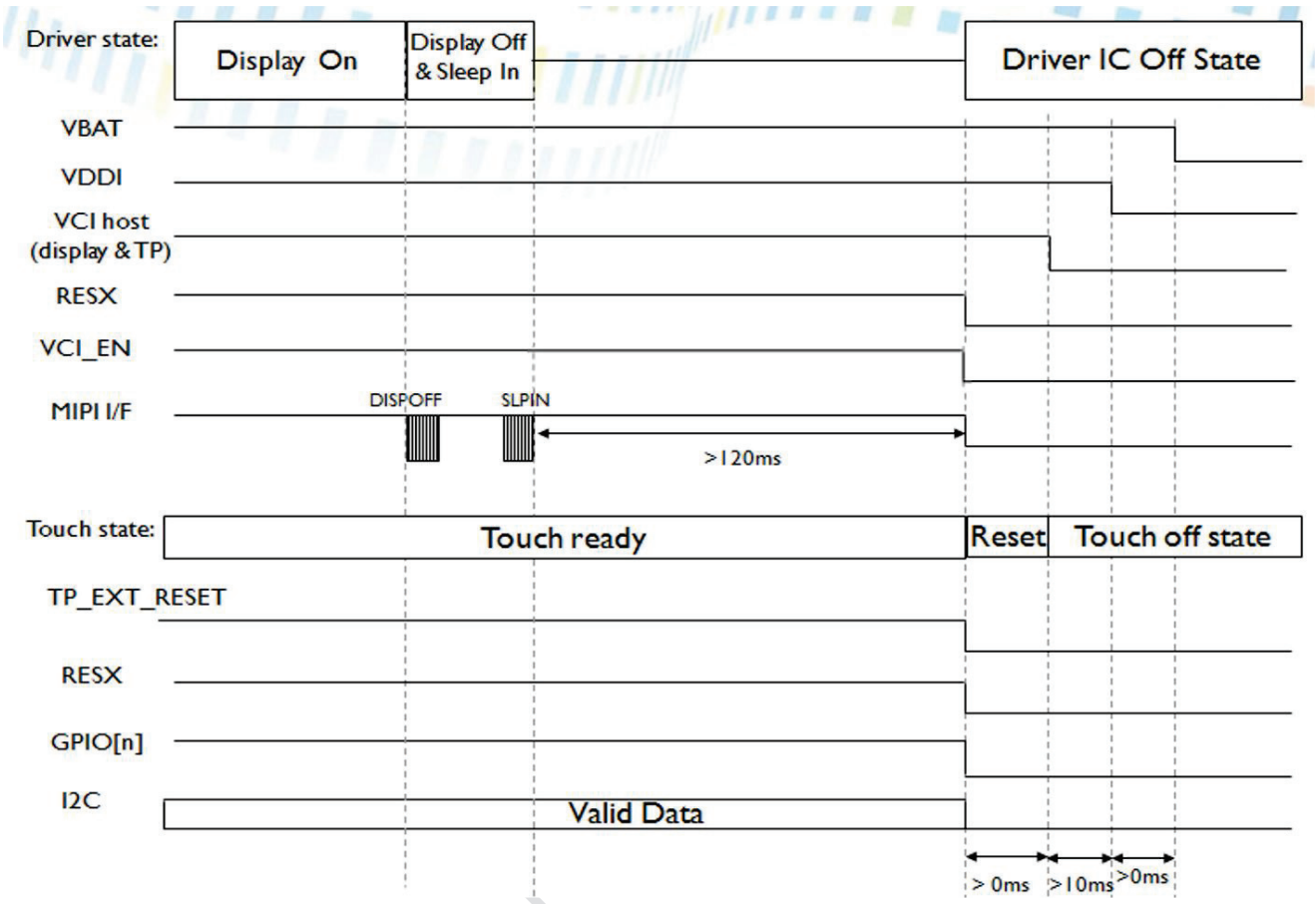


3.4 Operating Sequence

3.4.1 Power on sequence

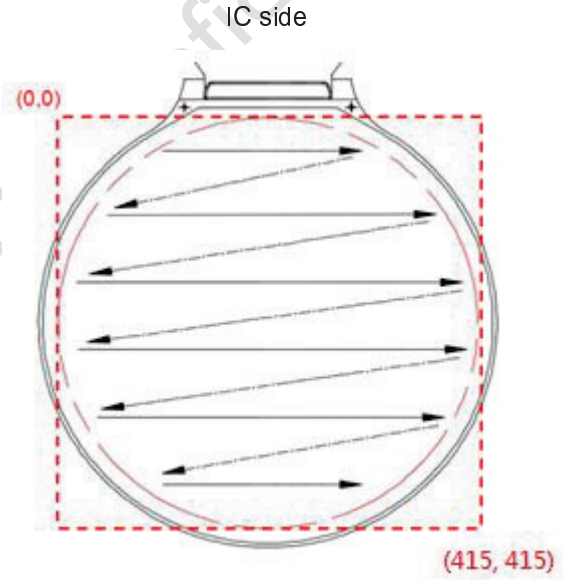


3.4.2 Power off sequence



3.5 Display Scan Direction & Coordinate

3.5.1 Scan direction



Panel Start Point = (0 , 0)

Panel End Point = (415 , 415)

3.5.2 Coordinate

Y	start_X	end_X	Total	Y	start_X	end_X	Total	Y	start_X	end_X	Total
0	194	221	28	30	100	315	216	60	61	354	294
1	183	232	50	31	98	317	220	61	60	355	296
2	176	239	64	32	96	319	224	62	59	356	298
3	170	245	76	33	95	320	226	63	58	357	300
4	165	250	86	34	93	322	230	64	57	358	302
5	161	254	94	35	92	323	232	65	56	359	304
6	156	259	104	36	90	325	236	66	56	359	304
7	153	262	110	37	89	326	238	67	55	360	306
8	149	266	118	38	88	327	240	68	54	361	308
9	146	269	124	39	86	329	244	69	53	362	310
10	143	272	130	40	85	330	246	70	52	363	312
11	140	275	136	41	83	332	250	71	51	364	314
12	137	278	142	42	82	333	252	72	50	365	316
13	134	281	148	43	81	334	254	73	49	366	318
14	132	283	152	44	80	335	256	74	49	366	318
15	129	286	158	45	78	337	260	75	48	367	320
16	127	288	162	46	77	338	262	76	47	368	322
17	125	290	166	47	76	339	264	77	46	369	324
18	122	293	172	48	75	340	266	78	45	370	326
19	120	295	176	49	73	342	270	79	45	370	326
20	118	297	180	50	72	343	272	80	44	371	328
21	116	299	184	51	71	344	274	81	43	372	330
22	114	301	188	52	70	345	276	82	42	373	332
23	112	303	192	53	69	346	278	83	41	374	334
24	110	305	196	54	68	347	280	84	41	374	334
25	108	307	200	55	67	348	282	85	40	375	336
26	106	309	204	56	65	350	286	86	39	376	338
27	105	310	206	57	64	351	288	87	39	376	338
28	103	312	210	58	63	352	290	88	38	377	340
29	101	314	214	59	62	353	292	89	37	378	342

Y	start_X	end_X	Total	Y	start_X	end_X	Total	Y	start_X	end_X	Total
90	36	379	344	120	19	396	378	150	8	407	400
91	36	379	344	121	19	396	378	151	8	407	400
92	35	380	346	122	18	397	380	152	8	407	400
93	34	381	348	123	18	397	380	153	7	408	402
94	34	381	348	124	18	397	380	154	7	408	402
95	33	382	350	125	17	398	382	155	7	408	402
96	32	383	352	126	17	398	382	156	6	409	404
97	32	383	352	127	16	399	384	157	6	409	404
98	31	384	354	128	16	399	384	158	6	409	404
99	31	384	354	129	15	400	386	159	6	409	404
100	30	385	356	130	15	400	386	160	6	409	404
101	29	386	358	131	15	400	386	161	5	410	406
102	29	386	358	132	14	401	388	162	5	410	406
103	28	387	360	133	14	401	388	163	5	410	406
104	28	387	360	134	13	402	390	164	5	410	406
105	27	388	362	135	13	402	390	165	4	411	408
106	26	389	364	136	13	402	390	166	4	411	408
107	26	389	364	137	12	403	392	167	4	411	408
108	25	390	366	138	12	403	392	168	4	411	408
109	25	390	366	139	12	403	392	169	4	411	408
110	24	391	368	140	11	404	394	170	3	412	410
111	24	391	368	141	11	404	394	171	3	412	410
112	23	392	370	142	11	404	394	172	3	412	410
113	23	392	370	143	10	405	396	173	3	412	410
114	22	393	372	144	10	405	396	174	3	412	410
115	22	393	372	145	10	405	396	175	3	412	410
116	21	394	374	146	9	406	398	176	2	413	412
117	21	394	374	147	9	406	398	177	2	413	412
118	20	395	376	148	9	406	398	178	2	413	412
119	20	395	376	149	8	407	400	179	2	413	412

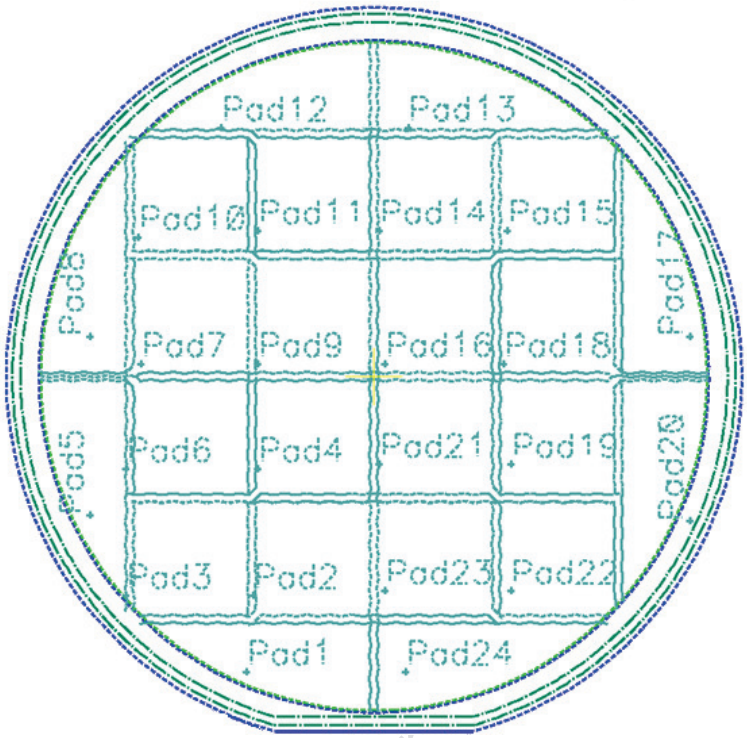
Y	start_X	end_X	Total	Y	start_X	end_X	Total	Y	start_X	end_X	Total
180	2	413	412	210	0	415	416	240	3	412	410
181	2	413	412	211	0	415	416	241	3	412	410
182	2	413	412	212	0	415	416	242	3	412	410
183	1	414	414	213	0	415	416	243	3	412	410
184	1	414	414	214	0	415	416	244	3	412	410
185	1	414	414	215	0	415	416	245	3	412	410
186	1	414	414	216	0	415	416	246	4	411	408
187	1	414	414	217	0	415	416	247	4	411	408
188	1	414	414	218	0	415	416	248	4	411	408
189	1	414	414	219	0	415	416	249	4	411	408
190	1	414	414	220	0	415	416	250	4	411	408
191	1	414	414	221	0	415	416	251	5	410	406
192	1	414	414	222	1	414	414	252	5	410	406
193	1	414	414	223	1	414	414	253	5	410	406
194	0	415	416	224	1	414	414	254	5	410	406
195	0	415	416	225	1	414	414	255	6	409	404
196	0	415	416	226	1	414	414	256	6	409	404
197	0	415	416	227	1	414	414	257	6	409	404
198	0	415	416	228	1	414	414	258	6	409	404
199	0	415	416	229	1	414	414	259	6	409	404
200	0	415	416	230	1	414	414	260	7	408	402
201	0	415	416	231	1	414	414	261	7	408	402
202	0	415	416	232	1	414	414	262	7	408	402
203	0	415	416	233	2	413	412	263	8	407	400
204	0	415	416	234	2	413	412	264	8	407	400
205	0	415	416	235	2	413	412	265	8	407	400
206	0	415	416	236	2	413	412	266	9	406	398
207	0	415	416	237	2	413	412	267	9	406	398
208	0	415	416	238	2	413	412	268	9	406	398
209	0	415	416	239	2	412	411	269	9	406	398

Y	start_X	end_X	Total	Y	start_X	end_X	Total	Y	start_X	end_X	Total
270	10	405	396	300	22	393	372	330	40	375	336
271	10	405	396	301	22	393	372	331	41	374	334
272	10	405	396	302	23	392	370	332	41	374	334
273	11	404	394	303	23	392	370	333	42	373	332
274	11	404	394	304	24	391	368	334	43	372	330
275	11	404	394	305	24	391	368	335	44	371	328
276	12	403	392	306	25	390	366	336	45	370	326
277	12	403	392	307	25	390	366	337	45	370	326
278	12	403	392	308	26	389	364	338	46	369	324
279	13	402	390	309	27	388	362	339	47	368	322
280	13	402	390	310	27	388	362	340	48	367	320
281	14	401	388	311	28	387	360	341	49	366	318
282	14	401	388	312	28	387	360	342	49	366	318
283	14	401	388	313	29	386	358	343	50	365	316
284	15	400	386	314	29	386	358	344	51	364	314
285	15	400	386	315	30	385	356	345	52	363	312
286	15	400	386	316	31	384	354	346	53	362	310
287	16	399	384	317	31	384	354	347	54	361	308
288	16	399	384	318	32	383	352	348	55	360	306
289	17	398	382	319	32	383	352	349	56	359	304
290	17	398	382	320	33	382	350	350	57	358	302
291	18	397	380	321	34	381	348	351	58	357	300
292	18	397	380	322	34	381	348	352	59	356	298
293	18	397	380	323	35	380	346	353	60	355	296
294	19	396	378	324	36	379	344	354	61	354	294
295	19	396	378	325	36	378	343	355	62	353	292
296	20	395	376	326	37	378	342	356	63	352	290
297	20	395	376	327	38	377	340	357	64	351	288
298	21	394	374	328	39	376	338	358	65	350	286
299	21	394	374	329	39	376	338	359	66	349	284

Y	start_X	end_X	Total	Y	start_X	end_X	Total	Y	start_X	end_X	Total
360	67	348	282	380	92	323	232	400	129	286	158
361	68	347	280	381	93	322	230	401	132	283	152
362	69	346	278	382	95	320	226	402	135	280	146
363	70	345	276	383	96	319	224	403	137	278	142
364	71	344	274	384	98	317	220	404	140	275	136
365	72	343	272	385	100	315	216	405	143	272	130
366	73	342	270	386	101	314	214	406	146	269	124
367	75	340	266	387	103	312	210	407	150	265	116
368	76	339	264	388	105	310	206	408	153	262	110
369	77	338	262	389	107	308	202	409	157	258	102
370	78	337	260	390	108	307	200	410	161	254	94
371	80	335	256	391	110	305	196	411	165	250	86
372	81	334	254	392	112	303	192	412	170	245	76
373	82	333	252	393	114	301	188	413	177	238	62
374	83	332	250	394	116	299	184	414	184	231	48
375	85	330	246	395	118	297	180	415	194	221	28
376	86	329	244	396	120	295	176				
377	88	327	240	397	122	293	172				
378	89	326	238	398	125	290	166				
379	91	324	234	399	127	288	162				

4 Touch Performance

4.1 Touch Sensor Drawing



4.2 Touch pattern design

Item	TP sensor
Number of touch panel sensors	24

4.3 Touch Specifications

4.3.1 TP performance

No.	Item		Spec.	Remark
1	Multi-Finger		2	
2	Report Rate		≧90Hz	
3	Performance	Accuracy (at Ø 9 mm)	Non-border ≦ 1.5mm, Border ≦ 2mm	
		Linearity (at Ø 9 mm)	Non-border ≦ 1.5mm, Border ≦ 2mm	
		Jitter (at Ø 9 mm)	Non-border ≦ 1.5mm, Border ≦ 2mm	

4.3.2 Waterproof

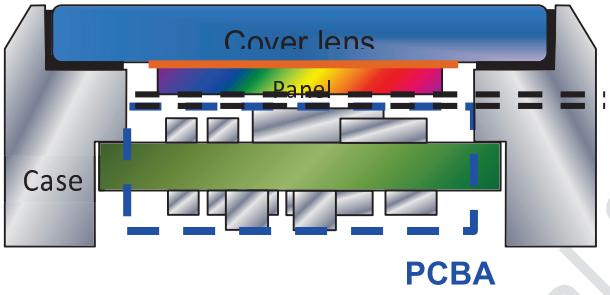
Item	Condition	Judgment	Remark
Waterproof (Anit-Water)	1000 ul	No touch is detected (without report any coordinates)	
Waterproof (Moisture)	100 ul	Touch function work	

4.3.3 Design requirements of in-cell touch

Cover lens design - Type: Glass, $\varepsilon \geqq 7.6$, Thickness: $\leqq$ 1.5mm

System gap $\geqq 0.3$mm

The system gap base on 1.1mm cover lens、stainless housing and smart watch application.



System gap:

1. the gap between bottom of AMOLED module and system parts/component.
2. The gap excludes system part thickness tolerance.

5 Optical Specifications

5.1 General optical specification

Item		Abbr.	Min.	Typ.	Max.	Unit	Remark
Optical Characteristic		Brightness	315	350	385	nits	Note 3
Contrast ratio		@25deg	10000	--	--		Note 4
Brightness Uniformity		350nits	85	--	--		Note 5
Viewing angle CR>1600		Top	80°	--	--	deg	Note 6
		Bottom	80°	--	--	deg	
		Left	80°	--	--	deg	
		Right	80°	--	--	deg	
Color	White	CIE1931 x	0.28	0.30	0.32		Note 7
	White	CIE1931 y	0.29	0.31	0.33		
	Red	CIE1931 x	0.652	0.682	0.712		
	Red	CIE1931 y	0.287	0.317	0.347		
	Green	CIE1931 x	0.190	0.230	0.270		
	Green	CIE1931 y	0.690	0.730	0.770		
	Blue	CIE1931 x	0.115	0.145	0.175		
	Blue	CIE1931 y	0.003	0.033	0.063		
NTSC		CIE x , y	90	110	--	%	
Life time	LT95	25°C	150	--	--	hrs	Note 8
Crosstalk	L128△CT	Vertical	--	--	110	%	Note 9
Flicker			--	--	-30	db	Note 10
Gamma		γ	1.9	2.2	2.5		Note 11

Note 1: Ambient temperature =25 ºC±2 ºC, measured by CA-310

Note 2: To be measured in the dark room.

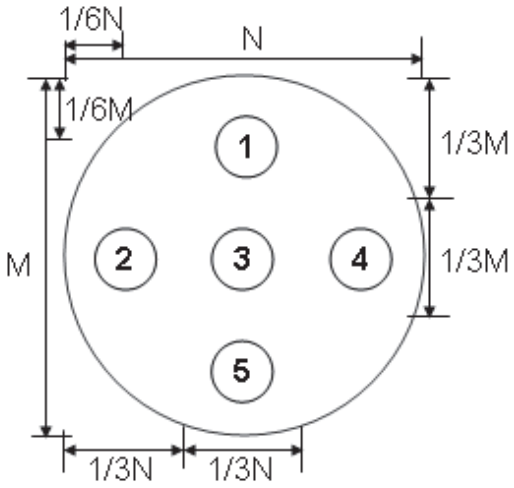
Note 3: The brightness measurement shall be done at the center of the display with a full white image.

Note 4: Definition of contrast ratio:

Contrast ratio is calculated with the following formula:

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when OLED is at “White” state}}{\text{Photo detector output when OLED is at “Black}}$$

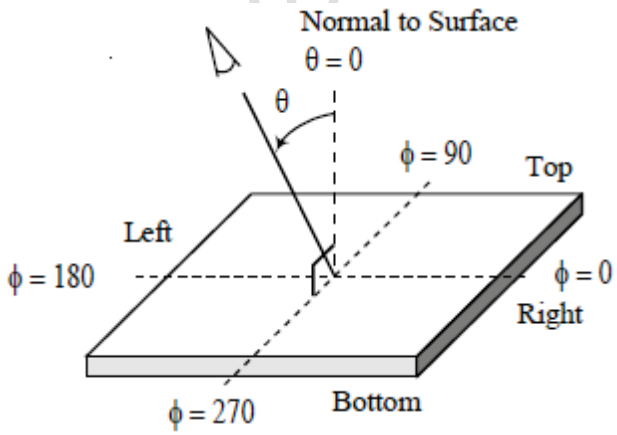
Note 5: Uniformity. Refer to figure as below



- △Bp = Bp (Min.) / Bp (Max.)×100 (%)
- Bp (Max.) = Maximum brightness in 5 measured spots
- Bp (Min.) = Minimum brightness in 5 measured spots.

Note 6: Definition of viewing angle :

The optical performance is specified as the driver IC located at =270°



Note 7: The color chromaticity should be based on sample performance because new OLED material should be verified later.

Note 8: Time to 95% Luminance

To measure the burn-in effect, a test pattern with white background applied to the AMOLED display at 100% loading

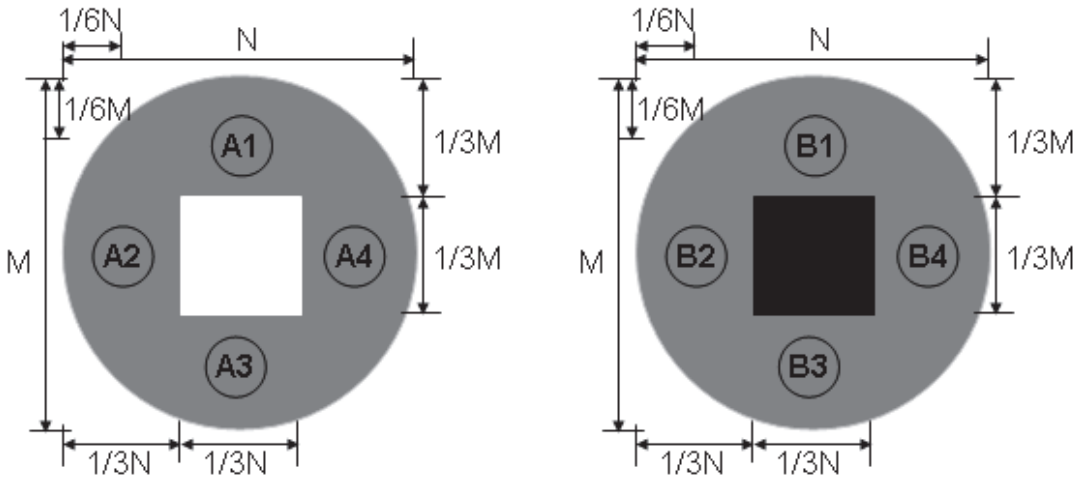
Note 9: Cross-talk

- There should be no visible cross-talk in normal direction of the display when the two ”Cross-talk Test Patterns ” below are loaded.
- Measurement equipment: DMS-803 or similar equipments

- The point should be marked is, the background of Cross-talk Test Pattern-“gray “ are defined as middle gray scale . For example, RGB 24bit “gray” defined as below:

R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

- △Bpn = Bpn (gray) / Bpn (white)
  Which n means the dot No. In the Cross-talk Test Pattern ;
  Bpn (gray) means the brightness of the No.n spots in Cross-talk Test Pattern A and B;
  Bpn (white) means the brightness of the No.n spots in Full white Test Pattern;
- △Bp (Max.) = Maximum value in A1~A4 and B1~B4.
- △Bp (Min.) = Minimum value in A1~A4 and pB1~B4.
- △CT=△Bp (Max.)/ △Bp(Min.).
- △CT must be less than 1.10



Note 10: Flicker

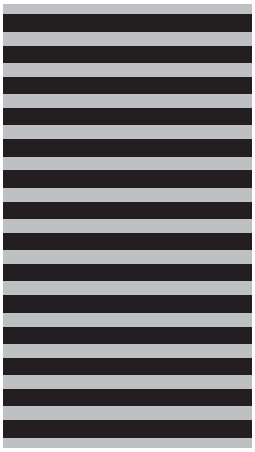
The flicker level is defined using Fast Fourier Transformation (FTT) as follows:

$$Flic\,\mathrm{ker} = 20\log_{10}\left(2\frac{f_{FFTC}(n)}{f_{FFTC}(0)}\right) + FS(Hz) \quad \text{(dB)}$$

where fFFTC(n) is the nth FFT coefficient, and fFFTC(0) is the 0th FFT coefficient which is DC component. FS(Hz) is the flicker sensitivity as a function of frequency.

The flicker level shall be measured with the test pattern in below.

The gray leves of test pattern is 128.

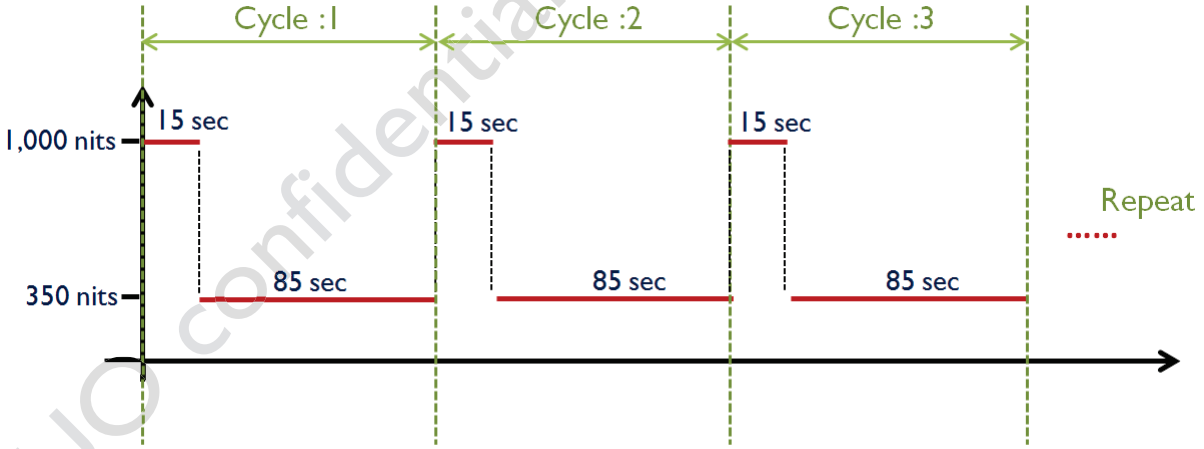


Note 11 : Gamma spec. is based on Gray level 255, 250, 244, 240, 232, 224, 206, 192, 160, 128, 95, 63, 47 & 31.

5.2 HB mode Optical Specifications

Item		Abbr.	Min.	Typ.	Max.	Unit	Remark
Optical Characteristic		Brightness	900	1000	1100	nits	
Life time	LT95	25°C	150	--	--	hrs	Note 1

Note 1 : HB mode lifetime test rule as below :



6 Reliability Test Items

6.1 Reliability Test

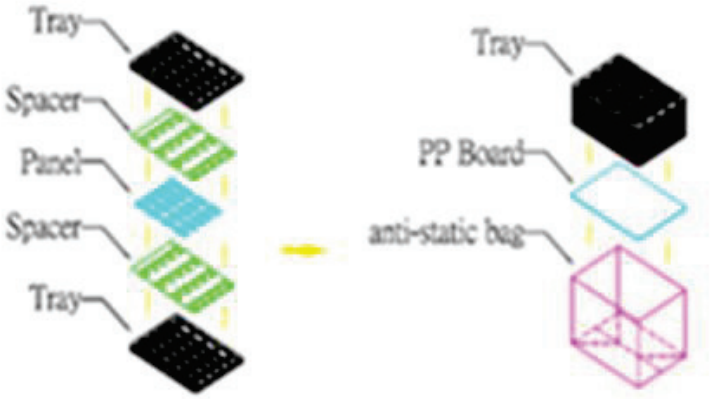
Category	No.	Test items		Conditions	Amount	Remark
Reliability (Environment)	1	High Temp. Operation		Ta= 60°C 240 hrs	5 pcs	
	2	High Temp. Storage		Ta= 70 °C 240 hrs	5 pcs	Non-operation
	3	Low Temp. Operation		Ta= -20 °C 240 hrs	5 pcs	
	4	Low Temp. Storage		Ta= -30 °C 240 hrs	5 pcs	Non-operation
	5	High Temp./Humi. Operation		Ta= 60 °C. 90% RH 240 hrs	5 pcs	
	6	Thermal Shock		-40 °C ~70 °C, Dwell for 30 min. 100 cycles.	5 pcs	Non-operation
	7	ESD	Contact mode	± 4KV; discharge time:10; Interval:1sec; Criteria: B	5 pcs	Test model：IEC61000-4-2，150pf，330ohm
			Air mode	± 8KV; discharge time:10;Interval:Discharge; Criteria: B	5 pcs	

Judge Criteria: No functional defect.

6.2 Drop test

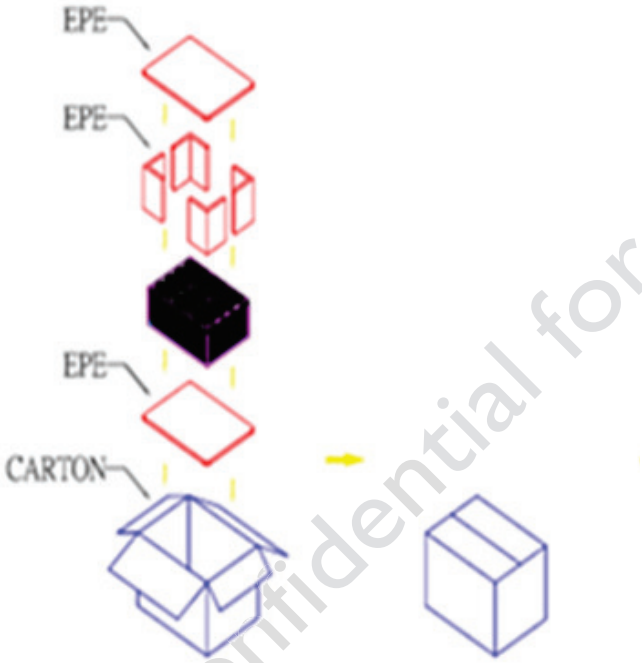
Test items	Conditions	Remark
Drop Test	Drop the packing from 76cm height, 6 surfaces, 3 edges and 1 corner.	Box

7 Packing



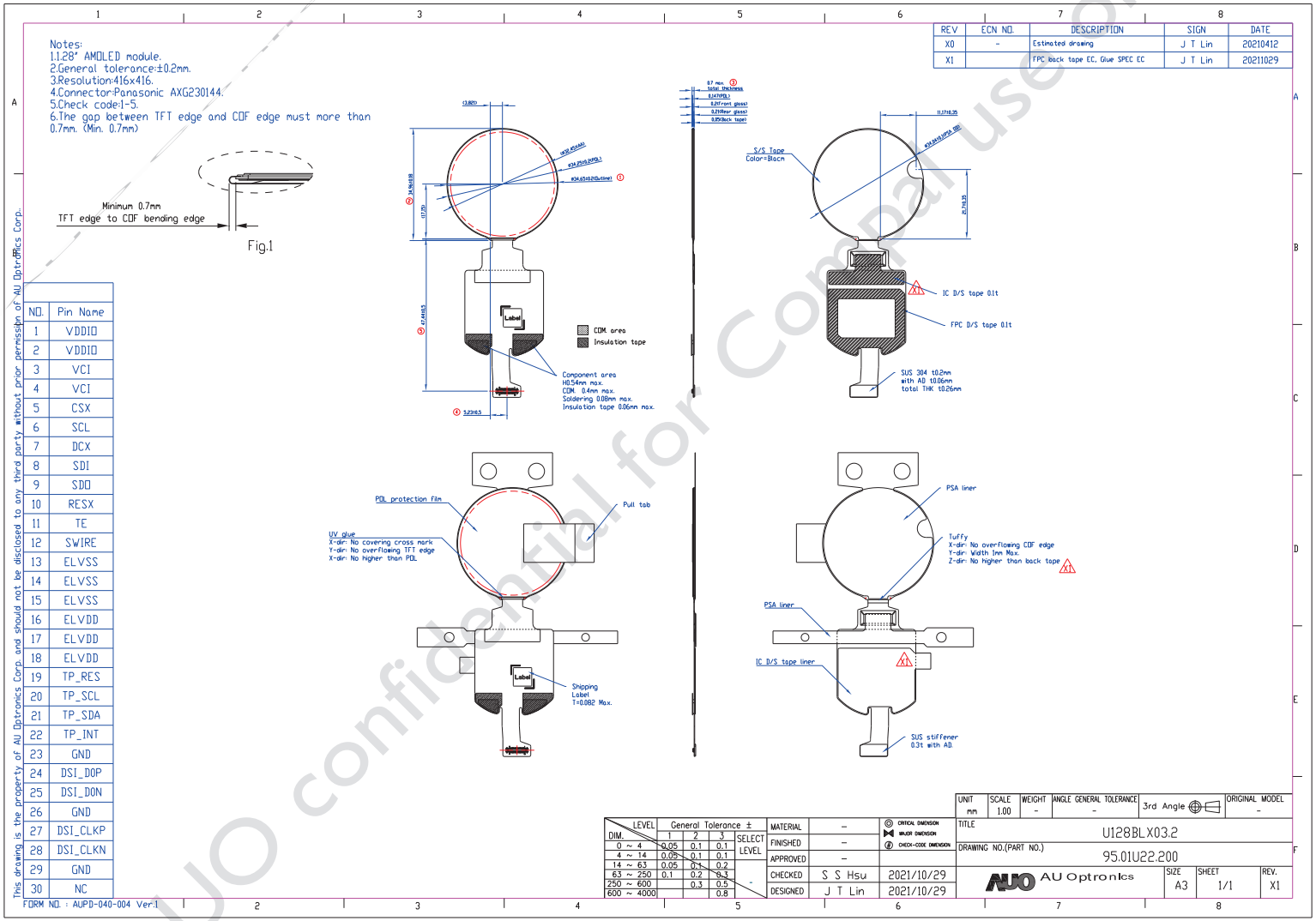
1 tray for 16pcs Panels

1 set for 24+1pcs trays =384Panels



Carton DIM：
550*410*274mm

8 Outline Dimension



9 Precaution

Please pay attention to the following items when you use the OLED Modules(Panel):

1. Do not twist or bend the module(panel) and prevent the unsuitable external force for display during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module(panel) with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module(panel).
5. Less EMI: it will be more safety and less noise.
6. Please operate module(panel) in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Please be sure to turn-off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dew drop may lead to destruction. Please wipe off any moisture before using module(panel).
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module(panel) to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with AMOLED display module(panel).
15. Static electricity will damage the module(panel), please do not touch the module(panel) without any grounded device.
16. Please avoid any static electricity damage (ESD) during producing and operating.
17. Do not disassemble and reassemble the module(panel) by self.
18. Be careful do not touch the rear side directly.
19. No strong vibration or shock. It will cause module(panel) broken.
20. Storage the modules(panel) in suitable environment with regular packing.
21. Be careful of injury from a broken display module(panel).
22. Please avoid the pressure adding to the surface (front or rear side) of modules(panel), because it will cause the display non-uniformity or other function issue.
23. Touch code is decided by (1) cover lens type, (2) lens lamination parameters, and (3) customers' hardware/software setting. Please be noted if above factors was changed, AUO need new samples to re-adjusted touch code.
24. Please take some protective action at the interface between rear side of panel and system hardware.
25. Please avoid any reflection material to cause the light radiated from rear side or broadside of panel.
26. Please NOTICE to keep the flatness between system board and AMOLED display, it will be much safer during the module drop test.