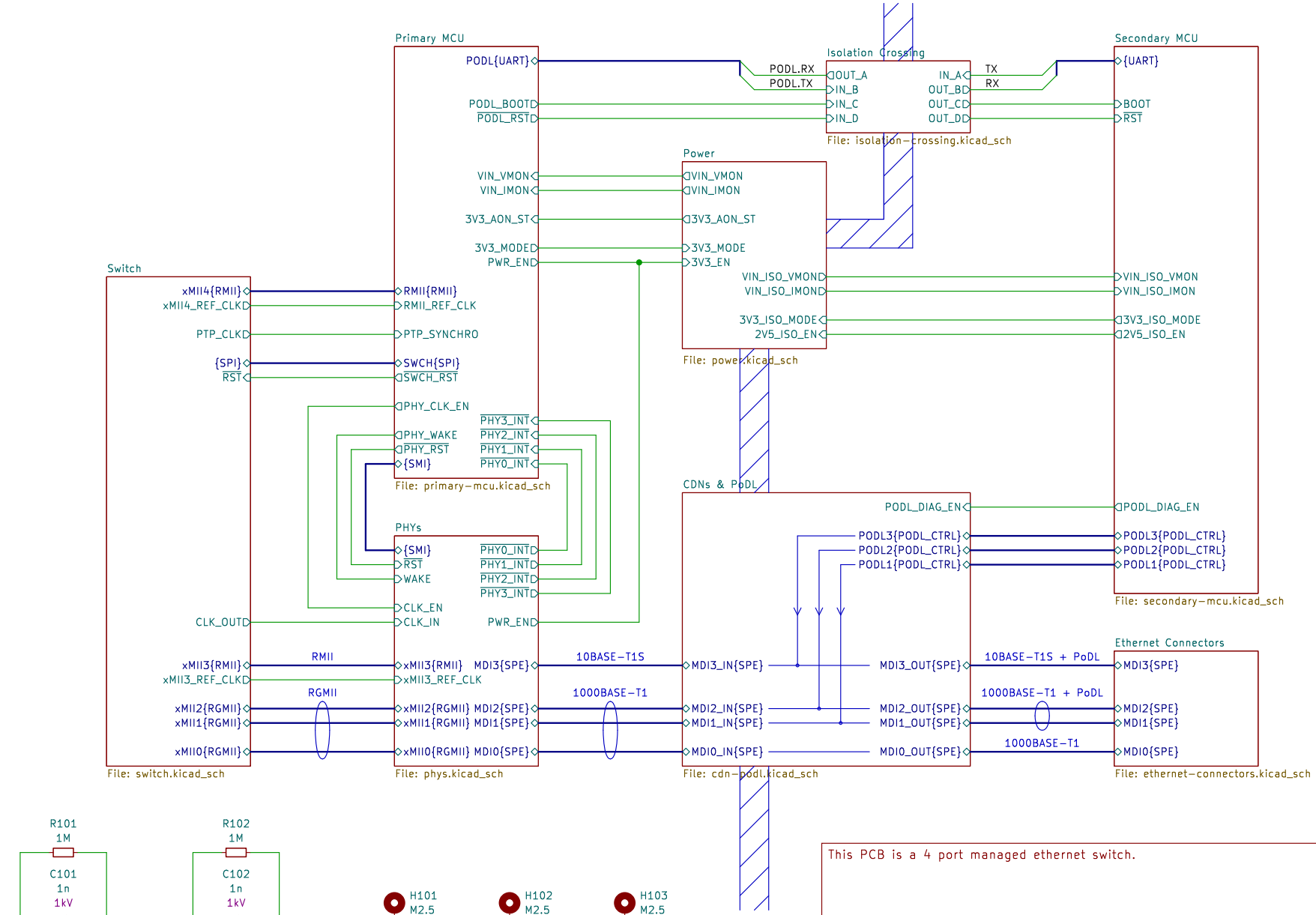
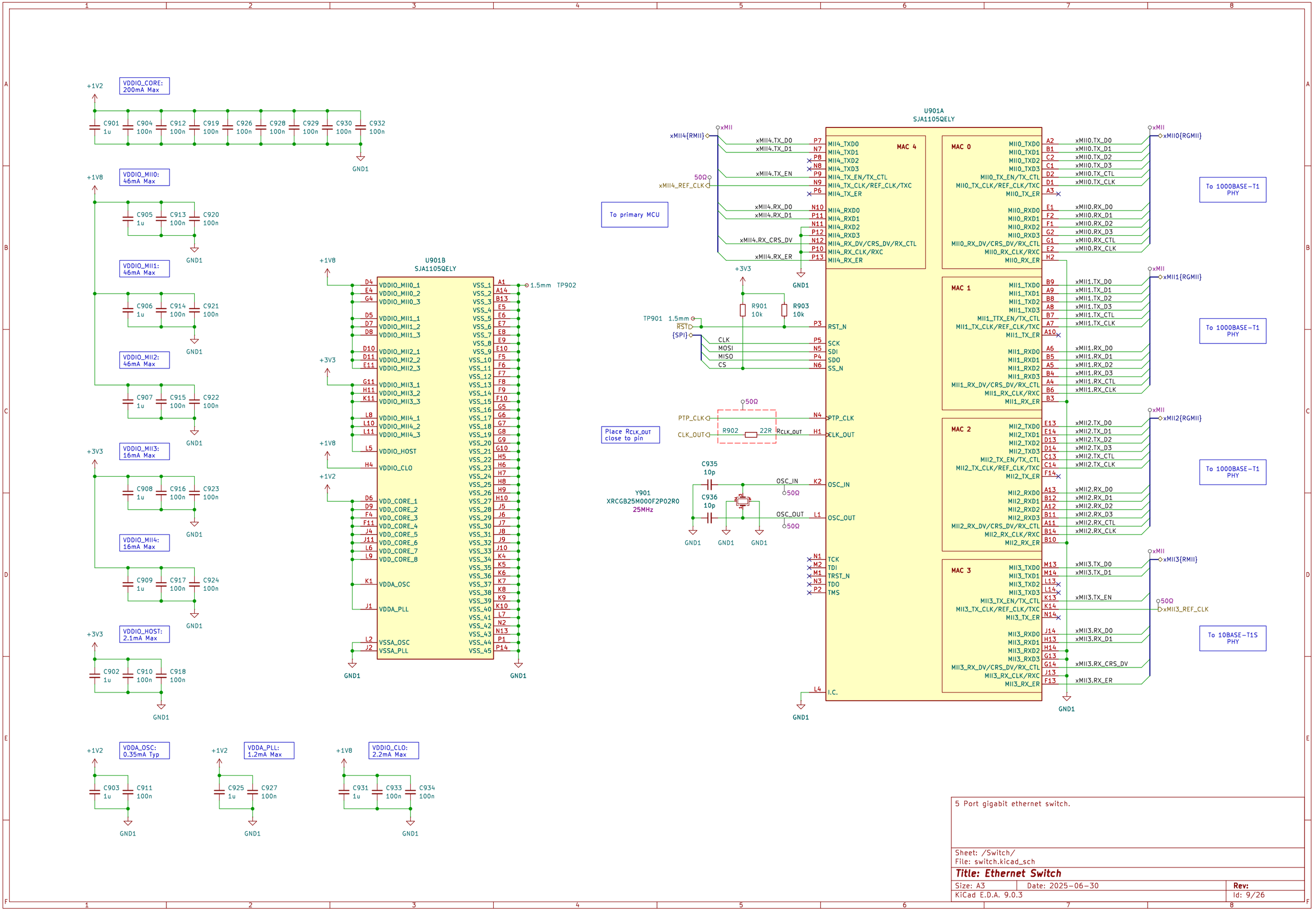

Primary MCU
PODL{UART}
PODL_BOOT
PODL_RST
VIN_VMON
VIN_IMON
3V3_AON_ST
3V3_MODE
PWR_EN
PHY_CLK_EN
PHY_WAKE
PHY_RST
{SMI}
PHY3_INT
PHY2_INT
PHY1_INT
PHY0_INT
File: primary-mcu.kicad_sch
Isolation Crossing
PODL.RX
PODL.TX
OUT_A
IN_B
IN_C
IN_D
IN_A
OUT_B
OUT_C
OUT_D
TX
RX
File: isolation-crossing.kicad_sch
Secondary MCU
{UART}
BOOT
RST
File: secondary-mcu.kicad_sch
Power
VIN_VMON
VIN_IMON
3V3_AON_ST
3V3_MODE
3V3_EN
VIN_ISO_VMON
VIN_ISO_IMON
3V3_ISO_MODE
2V5_ISO_EN
File: power.kicad_sch
Switch
xMII4{RMII}
xMII4_REF_CLK
PTP_CLK
{SPI}
RST
RMII{RMII}
RMII_REF_CLK
PTP_SYNCHRO
SWCH{SPI}
SWCH_RST
File: switch.kicad_sch
PHYs
{SMI}
RST
WAKE
CLK_EN
CLK_IN
PHY0_INT
PHY1_INT
PHY2_INT
PHY3_INT
PWR_EN
File: phys.kicad_sch
CDNs & PoDL
PODL_DIAG_EN
PODL3{PODL_CTRL}
PODL2{PODL_CTRL}
PODL1{PODL_CTRL}
MDI3_IN{SPE}
MDI2_IN{SPE}
MDI1_IN{SPE}
MDI0_IN{SPE}
MDI3_OUT{SPE}
MDI2_OUT{SPE}
MDI1_OUT{SPE}
MDI0_OUT{SPE}
File: cdn-podl.kicad_sch
Ethernet Connectors
MDI3{SPE}
MDI2{SPE}
MDI1{SPE}
MDI0{SPE}
File: ethernet-connectors.kicad_sch
RMII
RGMII
xMII3{RMII}
xMII3_REF_CLK
xMII2{RGMII}
xMII1{RGMII}
xMII0{RGMII}
MDI3{SPE}
MDI2{SPE}
MDI1{SPE}
MDI0{SPE}
10BASE-T1S
1000BASE-T1
10BASE-T1S + PoDL
1000BASE-T1 + PoDL
1000BASE-T1
R101
1M
C101
1n
1kV
R102
1M
C102
1n
1kV
GND1
GND2
SHIELD
H101
M2.5
H102
M2.5
H103
M2.5
This PCB is a 4 port managed ethernet switch.
Sheet: /
File: switch_main_v4.kicad_sch
Title: Switch V4 Top Level Schematic
Size: A4
Date: 2025-06-30
Rev:
KiCad E.D.A. 9.0.3
Id: 1/26

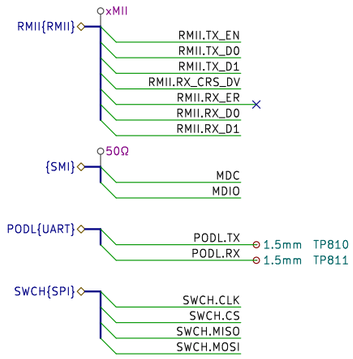


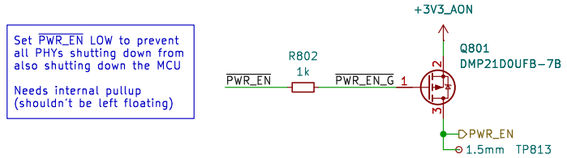
5 Port gigabit ethernet switch.

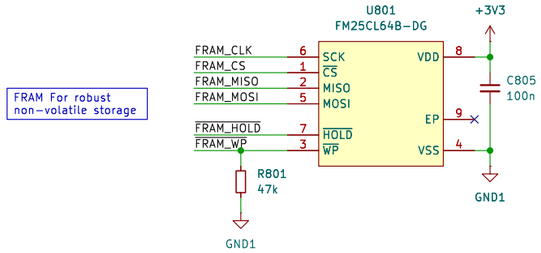
Sheet: /Switch/
File: switch.kicad_sch

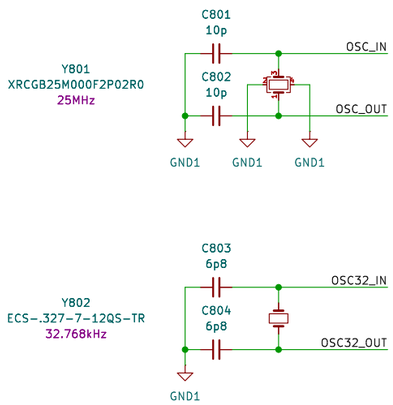
Title: Ethernet Switch

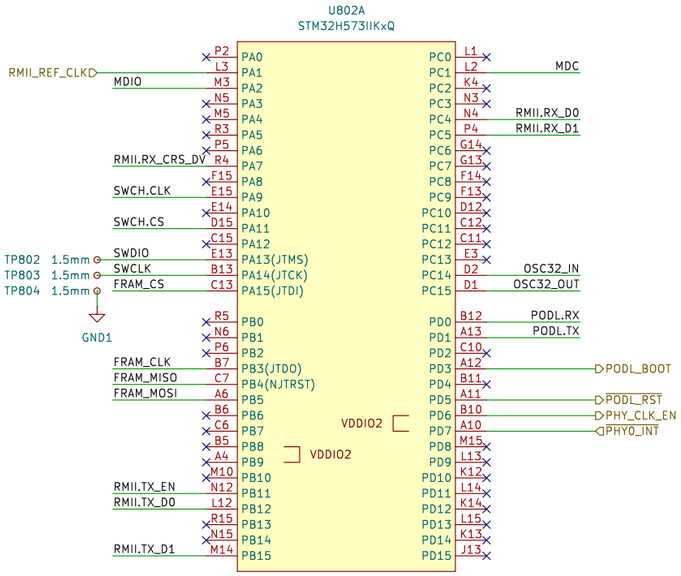
Size: A3	Date: 2025-06-30	**Rev:**
KiCad E.D.A. 9.0.3		Id: 9/26

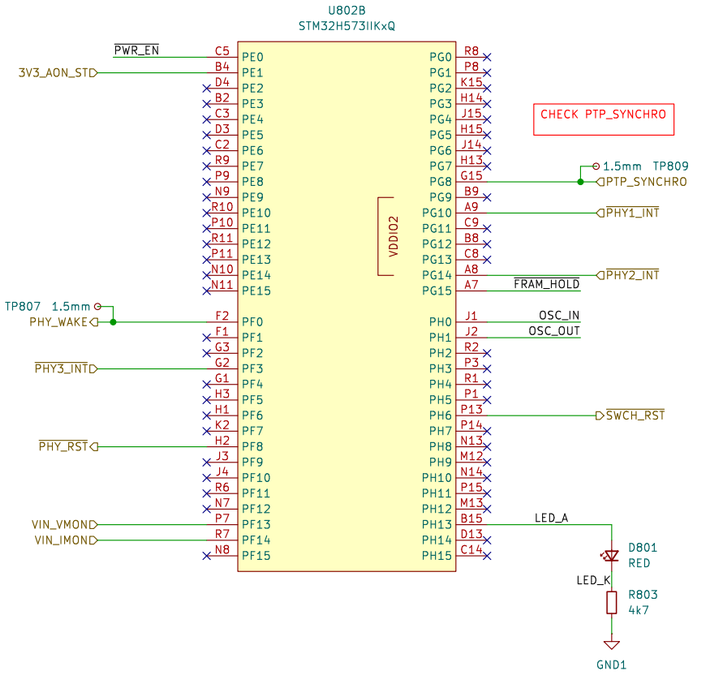


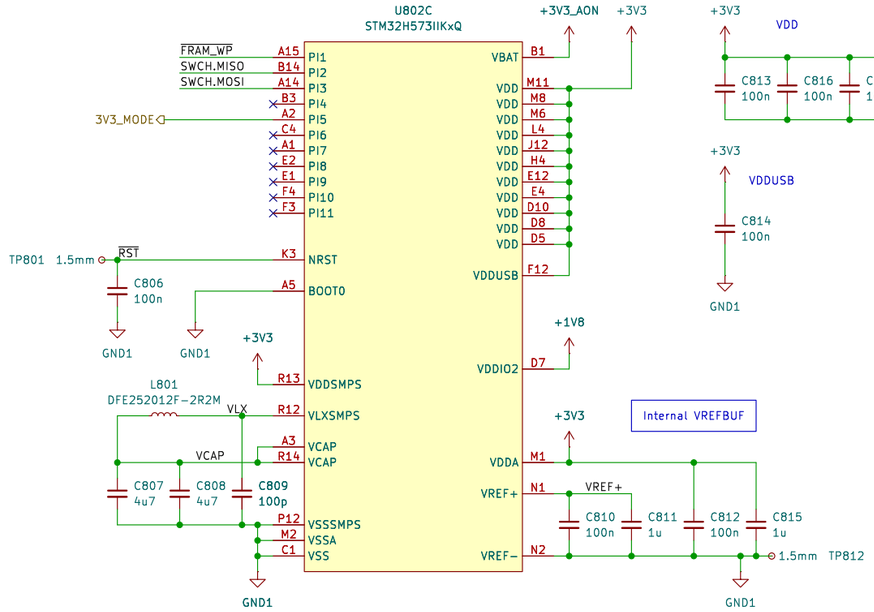


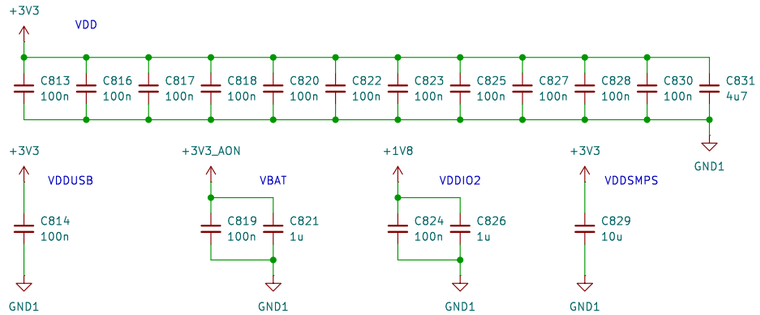










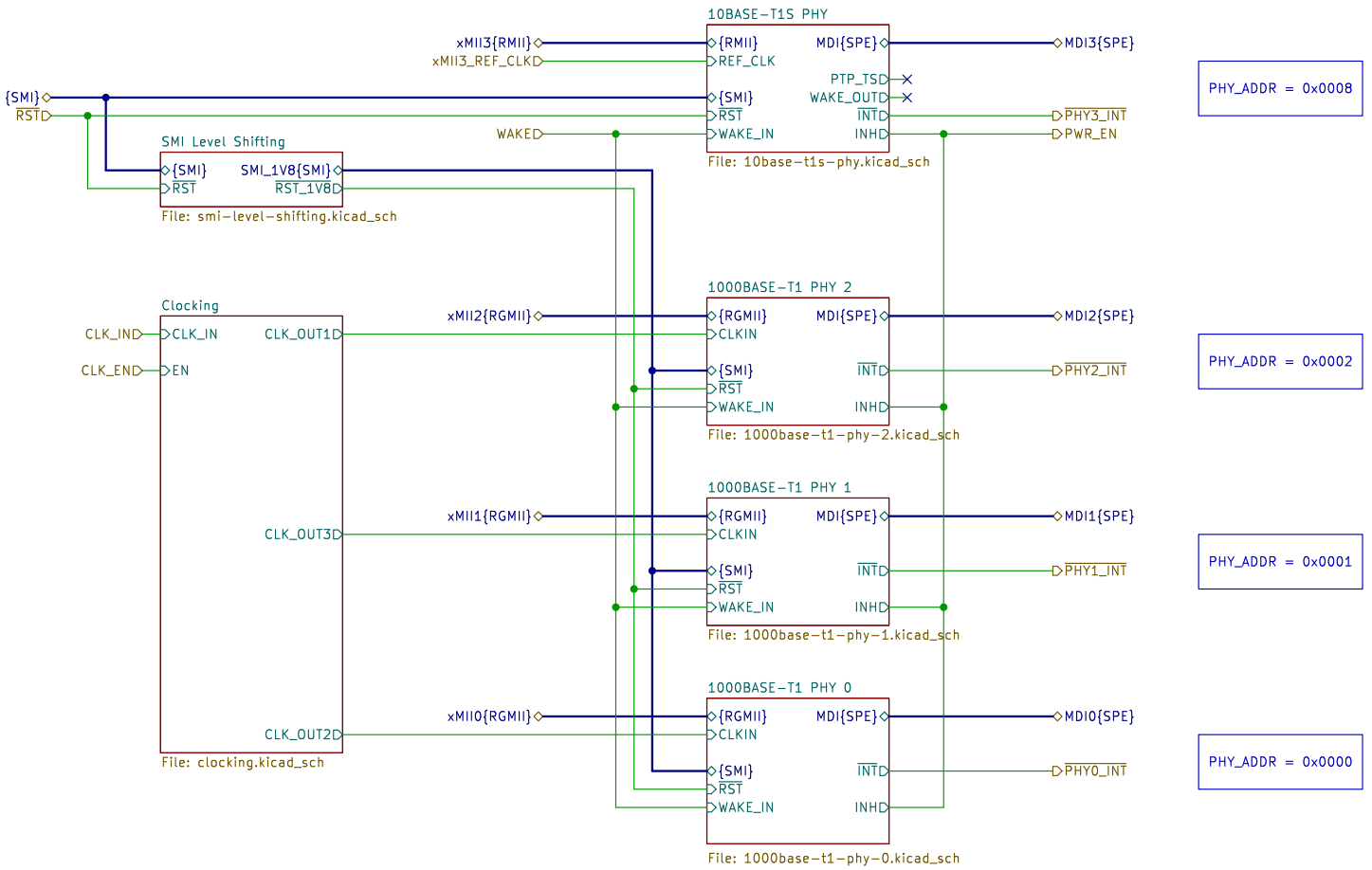


This microcontroller is responsible for managing the ethernet switch and PHYs.
It also runs algorithms like MSTP.

Sheet: /Primary MCU/
File: primary-mcu.kicad_sch

Title: Primary MCU

Size: A3	Date: 2025-06-30	**Rev:**
KiCad E.D.A. 9.0.3		Id: 8/26

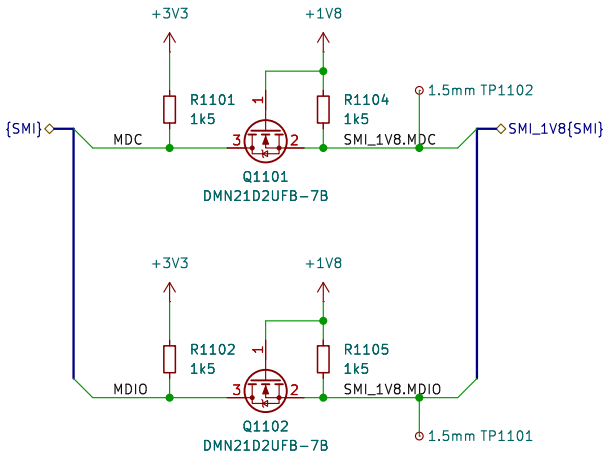


Ethernet PHYs and supporting circuitry.

Sheet: /PHYs/
File: phys.kicad_sch

Title: PHYs

Size: A4	Date: 2025-06-30	**Rev:**
KiCad E.D.A. 9.0.3		Id: 10/26



The 1000BASE-T1 PHYs operate at a 1V8 logic level (to save RGMII power), but the SMI and RST pins operate at a 3V3 logic level.

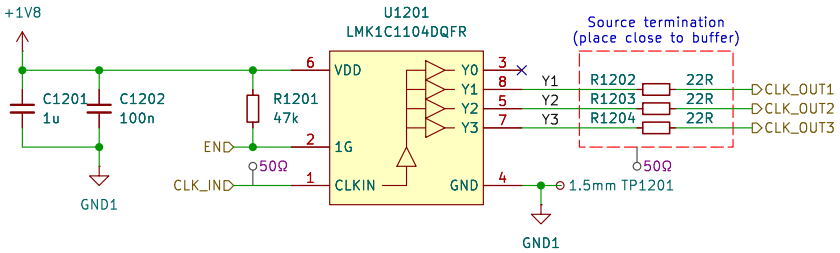
Level shifting is used to allow communication.

Converts 3.3V PHY management signals to 1.8V.

Sheet: /PHYs/SMI Level Shifting/
File: smi-level-shifting.kicad_sch

Title: SMI Level Shifting

Size: A4	Date: 2025-06-30	**Rev:**
KiCad E.D.A. 9.0.3		Id: 11/26

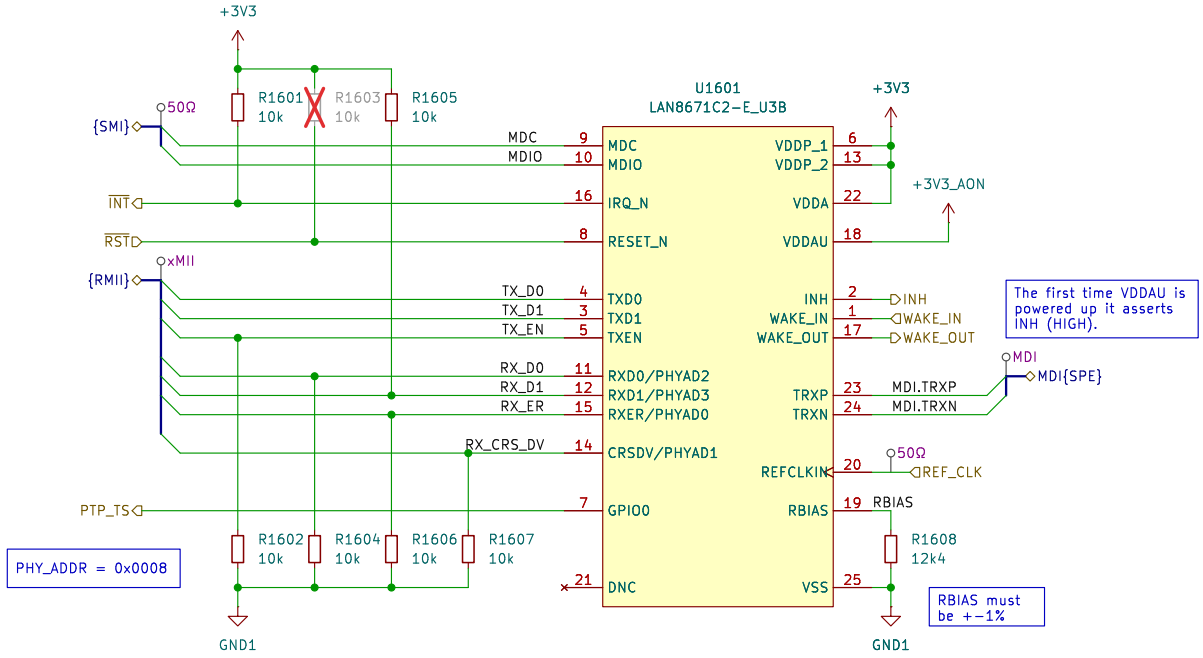


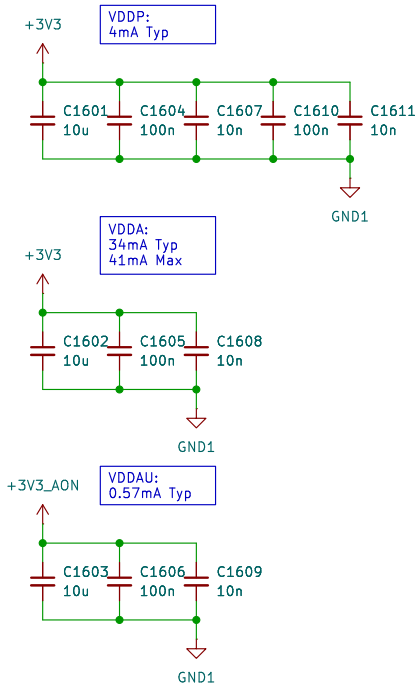
Receives a 25MHz clock from the switch and distributes it to the 3 1000BASE-T1 PHYs.

Sheet: /PHYs/Clocking/
File: clocking.kicad_sch

Title: Clock Buffer

Size: A4	Date: 2025-06-30	**Rev:**
KiCad E.D.A. 9.0.3		Id: 12/26

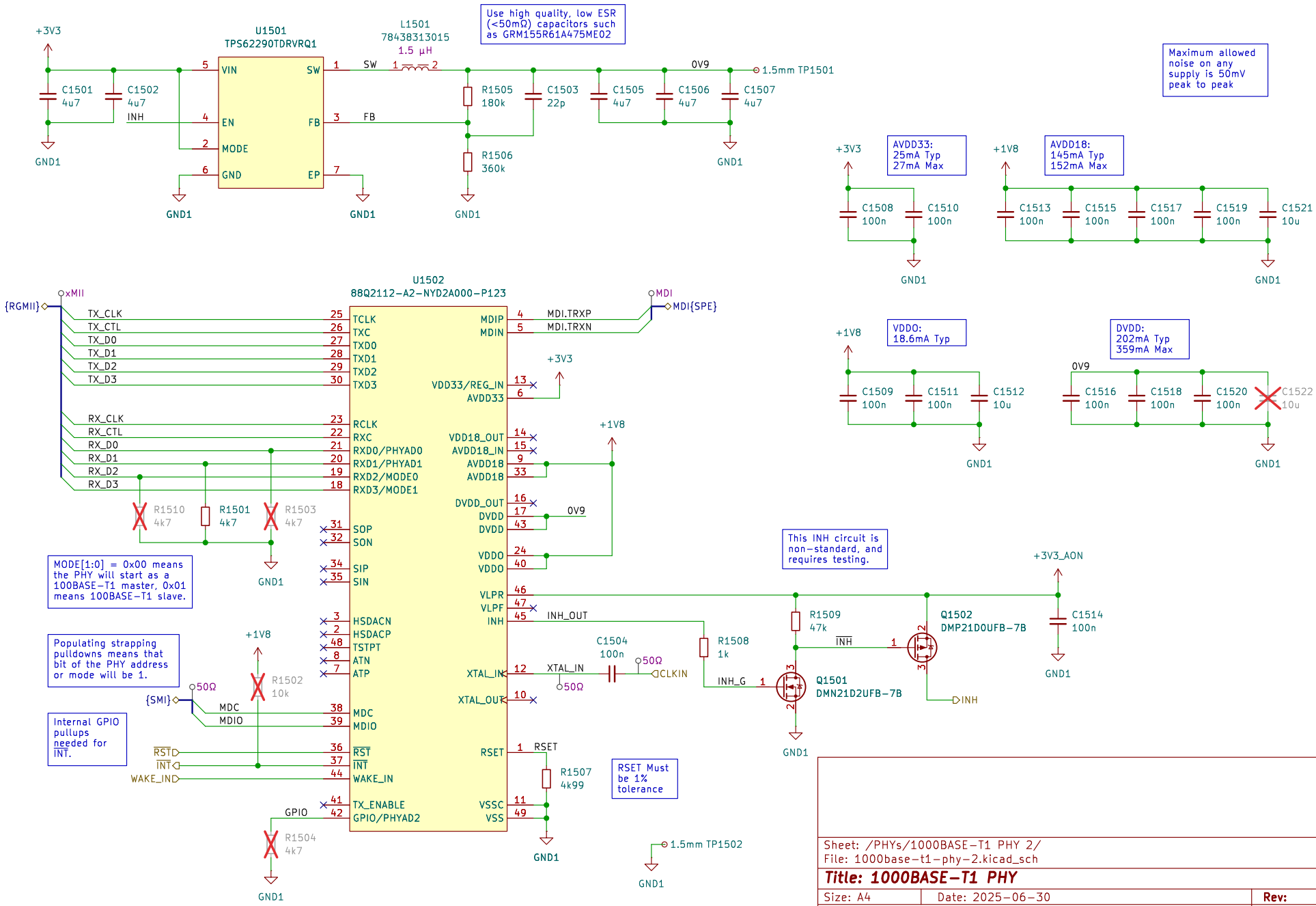


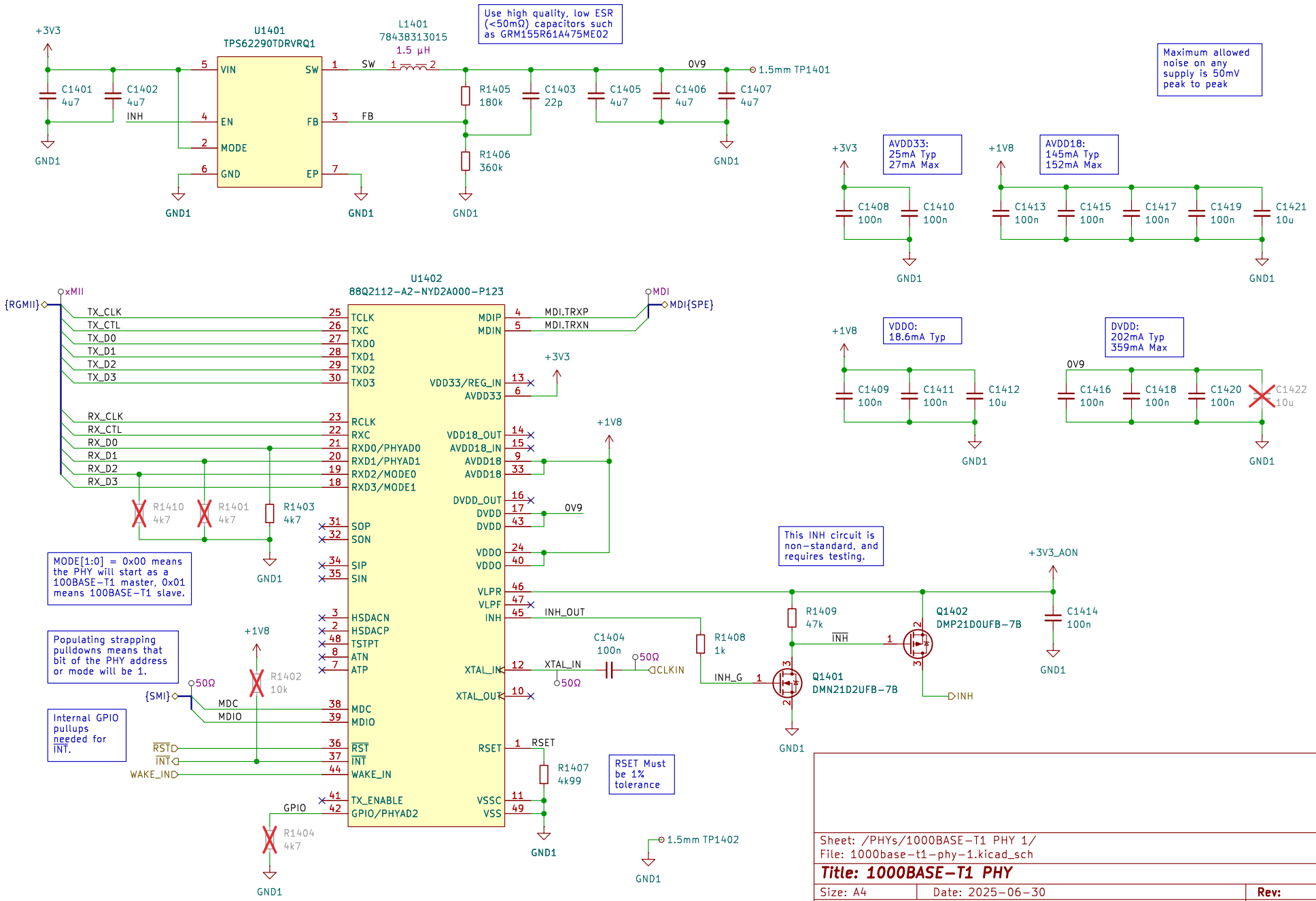


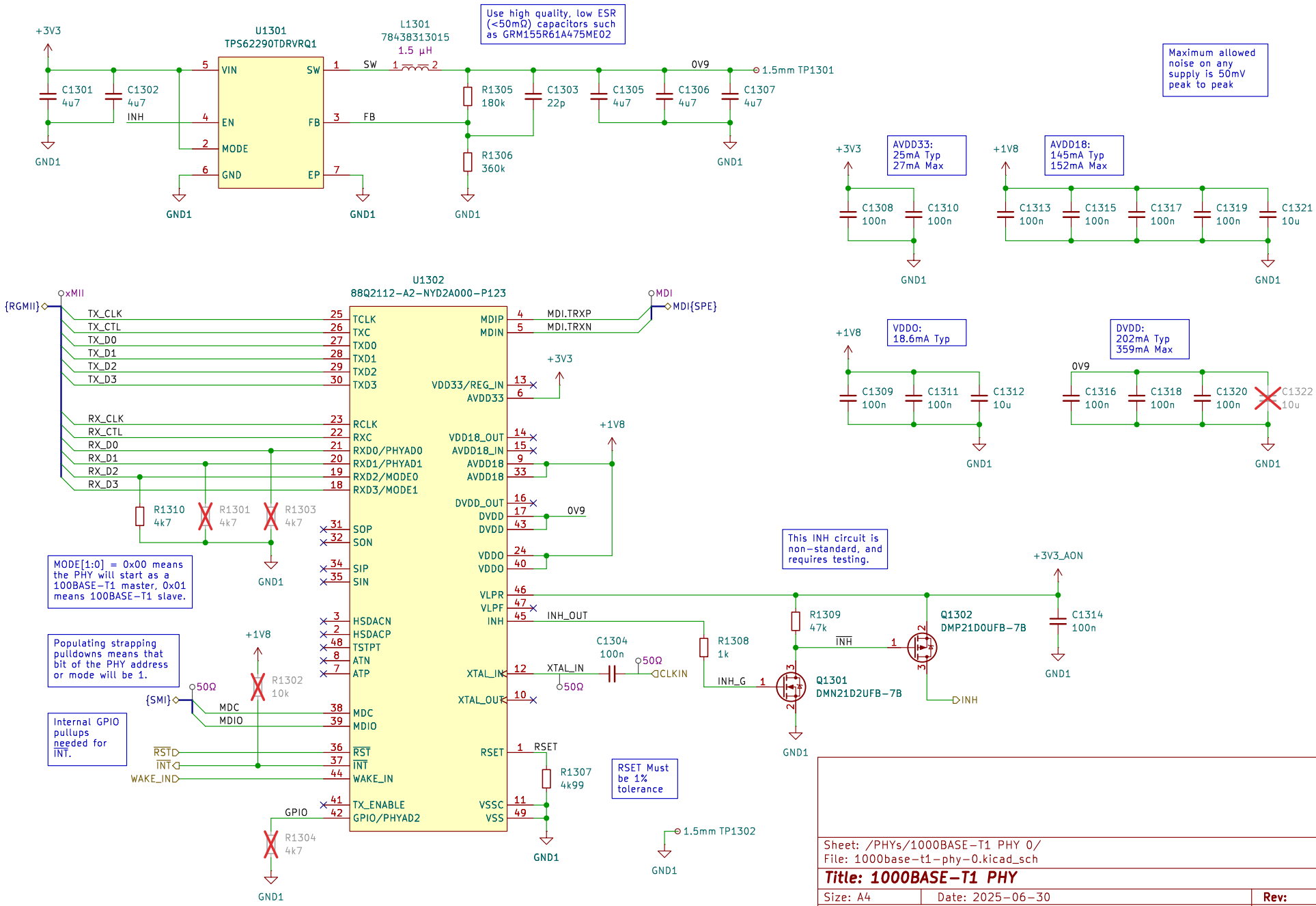
Sheet: /PHYs/10BASE-T1S PHY/
File: 10base-t1s-phy.kicad_sch

Title: 10BASE-T1S PHY

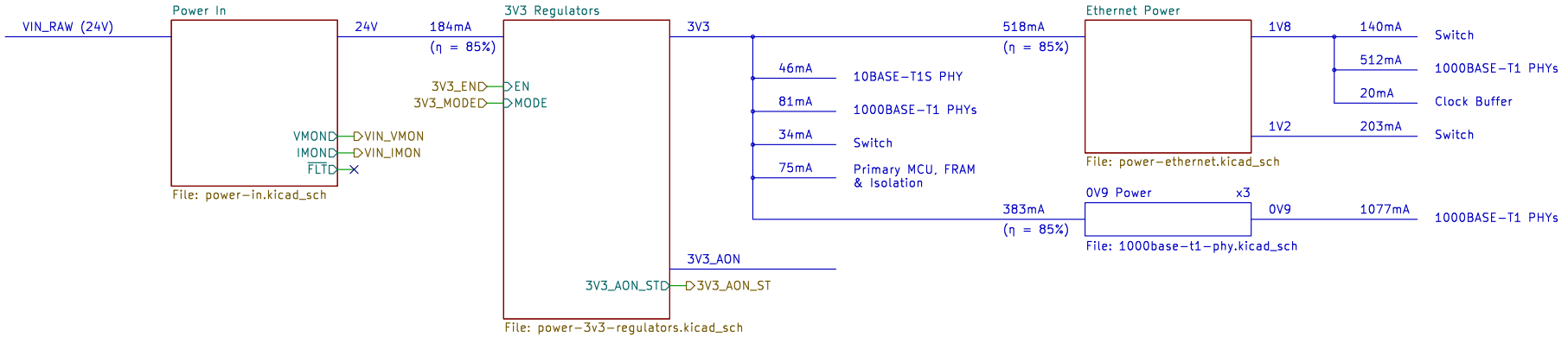
Size: A4	Date: 2025-06-30	**Rev:**
KiCad E.D.A. 9.0.3		Id: 16/26


Use high quality, low ESR (<50mΩ) capacitors such as GRM155R61A475ME02
U1501
TPS62290TDRVRQ1
L1501
78438313015
1.5 µH
+3V3
C1501 4u7
C1502 4u7
INH
VIN
EN
MODE
GND
SW
FB
EP
R1505 180k
R1506 360k
C1503 22p
C1505 4u7
C1506 4u7
C1507 4u7
0V9
1.5mm TP1501
GND1
Maximum allowed noise on any supply is 50mV peak to peak
AVDD33: 25mA Typ 27mA Max
AVDD18: 145mA Typ 152mA Max
C1508 100n
C1510 100n
C1513 100n
C1515 100n
C1517 100n
C1519 100n
C1521 10u
U1502
88Q2112-A2-NYD2A000-P123
xMII
{RGMII}
TX_CLK
TX_CTL
TX_D0
TX_D1
TX_D2
TX_D3
RX_CLK
RX_CTL
RX_D0
RX_D1
RX_D2
RX_D3
TCLK
TXC
TXD0
TXD1
TXD2
TXD3
RCLK
RXC
RXD0/PHYAD0
RXD1/PHYAD1
RXD2/MODE0
RXD3/MODE1
SOP
SON
SIP
SIN
HSDACN
HSDACP
TSTPT
ATN
ATP
MDC
MDIO
RST
INT
WAKE_IN
TX_ENABLE
GPIO/PHYAD2
MDIP
MDIN
VDD33/REG_IN
AVDD33
VDD18_OUT
AVDD18_IN
AVDD18
DVDD_OUT
DVDD
VDDO
VLPR
VLPF
INH
XTAL_IN
XTAL_OUT
RSET
VSSC
VSS
MDI.TRXP
MDI.TRXN
MDI
MDI{SPE}
+3V3
+1V8
0V9
R1510 4k7
R1501 4k7
R1503 4k7
R1502 10k
R1504 4k7
R1507 4k99
C1504 100n
50Ω
CLKIN
INH_OUT
INH_G
R1508 1k
R1509 47k
Q1501 DMN21D2UFB-7B
Q1502 DMP21D0UFB-7B
C1514 100n
+3V3_AON
{SMI}
MDC
MDIO
RSET
1.5mm TP1502
VDDO: 18.6mA Typ
DVDD: 202mA Typ 359mA Max
C1509 100n
C1511 100n
C1512 10u
C1516 100n
C1518 100n
C1520 100n
C1522 10u
MODE[1:0] = 0x00 means the PHY will start as a 100BASE-T1 master, 0x01 means 100BASE-T1 slave.
Populating strapping pulldowns means that bit of the PHY address or mode will be 1.
Internal GPIO pullups needed for INT.
This INH circuit is non-standard, and requires testing.
RSET Must be 1% tolerance
Sheet: /PHYs/1000BASE-T1 PHY 2/
File: 1000base-t1-phy-2.kicad_sch
Title: 1000BASE-T1 PHY
Size: A4
Date: 2025-06-30
Rev:
KiCad E.D.A. 9.0.3
Id: 15/26


Use high quality, low ESR (<50mΩ) capacitors such as GRM155R61A475ME02
U1401
TPS62290TDRVRQ1
L1401
78438313015
1.5 µH
+3V3
C1401 4u7
C1402 4u7
INH
VIN
EN
MODE
GND
SW
FB
EP
R1405 180k
C1403 22p
C1405 4u7
C1406 4u7
C1407 4u7
R1406 360k
0V9
1.5mm TP1401
GND1
Maximum allowed noise on any supply is 50mV peak to peak
AVDD33: 25mA Typ 27mA Max
AVDD18: 145mA Typ 152mA Max
+1V8
C1408 100n
C1410 100n
C1413 100n
C1415 100n
C1417 100n
C1419 100n
C1421 10u
U1402
88Q2112-A2-NYD2A000-P123
xMII
{RGMII}
TX_CLK
TX_CTL
TX_D0
TX_D1
TX_D2
TX_D3
RX_CLK
RX_CTL
RX_D0
RX_D1
RX_D2
RX_D3
TCLK
TXC
TXD0
TXD1
TXD2
TXD3
RCLK
RXC
RXD0/PHYAD0
RXD1/PHYAD1
RXD2/MODE0
RXD3/MODE1
MDIP
MDIN
MDI.TRXP
MDI.TRXN
MDI
MDI{SPE}
VDD33/REG_IN
AVDD33
VDD18_OUT
AVDD18_IN
AVDD18
DVDD_OUT
DVDD
VDDO
VLPR
VLPF
INH
XTAL_IN
XTAL_OUT
RSET
VSSC
VSS
SOP
SON
SIP
SIN
HSDACN
HSDACP
TSTPT
ATN
ATP
MDC
MDIO
RST
INT
WAKE_IN
TX_ENABLE
GPIO/PHYAD2
R1410 4k7
R1401 4k7
R1403 4k7
R1402 10k
R1404 4k7
R1407 4k99
R1408 1k
R1409 47k
C1404 100n
50Ω
CLKIN
INH_OUT
INH_G
RSET
VDDO: 18.6mA Typ
DVDD: 202mA Typ 359mA Max
C1409 100n
C1411 100n
C1412 10u
C1416 100n
C1418 100n
C1420 100n
C1422 10u
C1414 100n
+3V3_AON
Q1402 DMP21D0UFB-7B
Q1401 DMN21D2UFB-7B
This INH circuit is non-standard, and requires testing.
MODE[1:0] = 0x00 means the PHY will start as a 100BASE-T1 master, 0x01 means 100BASE-T1 slave.
Populating strapping pulldowns means that bit of the PHY address or mode will be 1.
Internal GPIO pullups needed for INT.
RSET Must be 1% tolerance
{SMI}
GPIO
1.5mm TP1402
Sheet: /PHYs/1000BASE-T1 PHY 1/
File: 1000base-t1-phy-1.kicad_sch
Title: 1000BASE-T1 PHY
Size: A4
Date: 2025-06-30
Rev:
KiCad E.D.A. 9.0.3
Id: 14/26

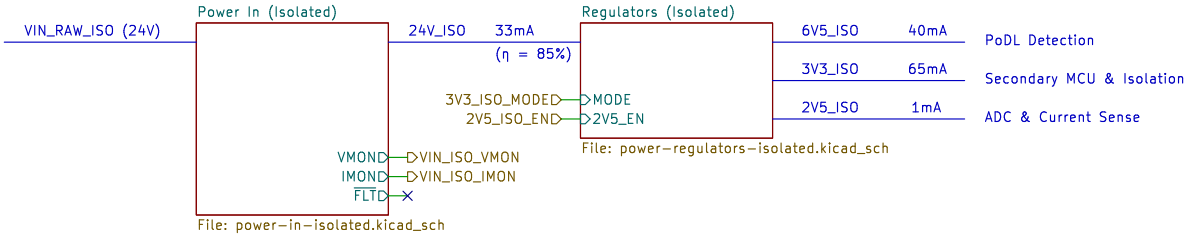

Use high quality, low ESR (<50mΩ) capacitors such as GRM155R61A475ME02
U1301
TPS62290TDRVRQ1
L1301
78438313015
1.5 µH
+3V3
C1301 4u7
C1302 4u7
INH
VIN
EN
MODE
GND
SW
FB
EP
R1305 180k
C1303 22p
C1305 4u7
C1306 4u7
C1307 4u7
R1306 360k
0V9
1.5mm TP1301
GND1
Maximum allowed noise on any supply is 50mV peak to peak
AVDD33: 25mA Typ 27mA Max
AVDD18: 145mA Typ 152mA Max
+1V8
C1308 100n
C1310 100n
C1313 100n
C1315 100n
C1317 100n
C1319 100n
C1321 10u
U1302
88Q2112-A2-NYD2A000-P123
xMII
{RGMII}
TX_CLK
TX_CTL
TX_D0
TX_D1
TX_D2
TX_D3
RX_CLK
RX_CTL
RX_D0
RX_D1
RX_D2
RX_D3
TCLK
TXC
TXD0
TXD1
TXD2
TXD3
RCLK
RXC
RXD0/PHYAD0
RXD1/PHYAD1
RXD2/MODE0
RXD3/MODE1
SOP
SON
SIP
SIN
HSDACN
HSDACP
TSTPT
ATN
ATP
MDC
MDIO
RST
INT
WAKE_IN
TX_ENABLE
GPIO/PHYAD2
MDIP
MDIN
VDD33/REG_IN
AVDD33
VDD18_OUT
AVDD18_IN
AVDD18
DVDD_OUT
DVDD
VDDO
VLPR
VLPF
INH
XTAL_IN
XTAL_OUT
RSET
VSSC
VSS
MDI.TRXP
MDI.TRXN
MDI
MDI{SPE}
R1310 4k7
R1301 4k7
R1303 4k7
MODE[1:0] = 0x00 means the PHY will start as a 100BASE-T1 master, 0x01 means 100BASE-T1 slave.
Populating strapping pulldowns means that bit of the PHY address or mode will be 1.
Internal GPIO pullups needed for INT.
R1302 10k
{SMI}
50Ω
R1304 4k7
R1307 4k99
RSET Must be 1% tolerance
1.5mm TP1302
VDDO: 18.6mA Typ
DVDD: 202mA Typ 359mA Max
C1309 100n
C1311 100n
C1312 10u
C1316 100n
C1318 100n
C1320 100n
C1322 10u
This INH circuit is non-standard, and requires testing.
R1309 47k
R1308 1k
C1304 100n
CLKIN
INH_OUT
INH_G
Q1301 DMN21D2UFB-7B
Q1302 DMP21D0UFB-7B
+3V3_AON
C1314 100n
Sheet: /PHYs/1000BASE-T1 PHY 0/
File: 1000base-t1-phy-0.kicad_sch
Title: 1000BASE-T1 PHY
Size: A4
Date: 2025-06-30
Rev:
KiCad E.D.A. 9.0.3
Id: 13/26

PHY Side Power



Isolation Barrier

Connector Side Power

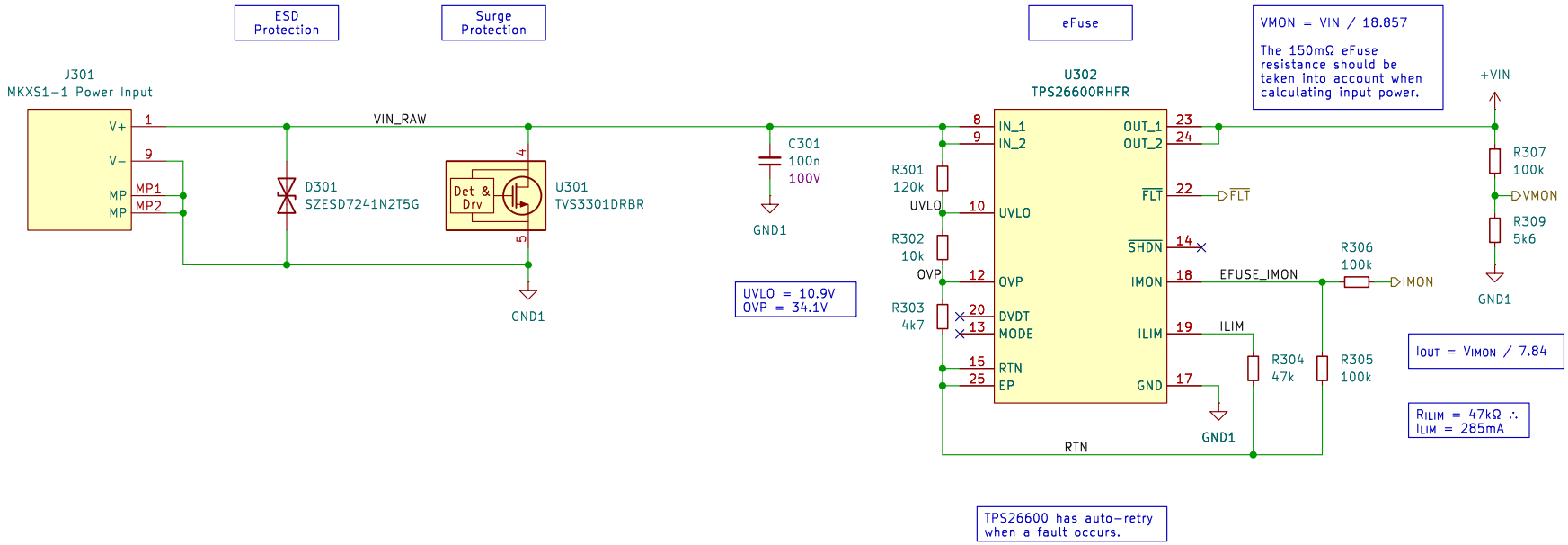


Block diagram of the power supply scheme for both sides of the isolation barrier.

Sheet: /Power/
File: power.kicad_sch

Title: Power

Size: A4	Date: 2025-06-30	**Rev:**
KiCad E.D.A. 9.0.3		Id: 2/26



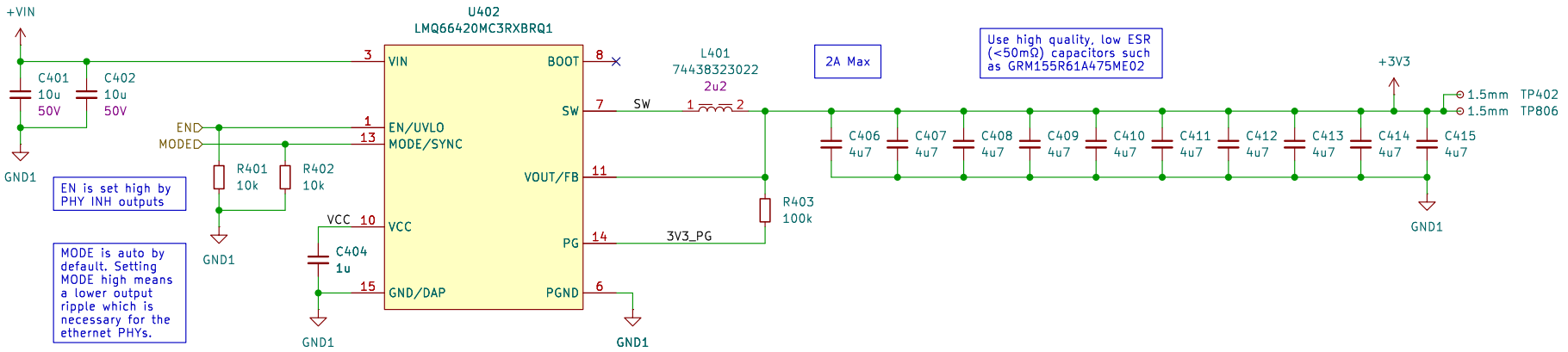
Power input and protection for the PHY side of the PCB.

Sheet: /Power/Power In/
File: power-in.kicad_sch

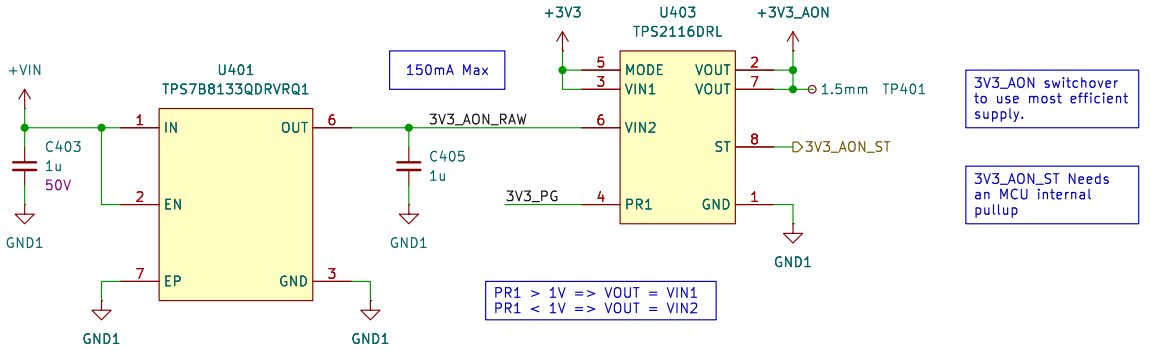
Title: Power In (PHY Side)

Size: A4	Date: 2025-06-30	**Rev:**
KiCad E.D.A. 9.0.3		Id: 3/26

3V3 Main Regulator



3V3 Always on supply

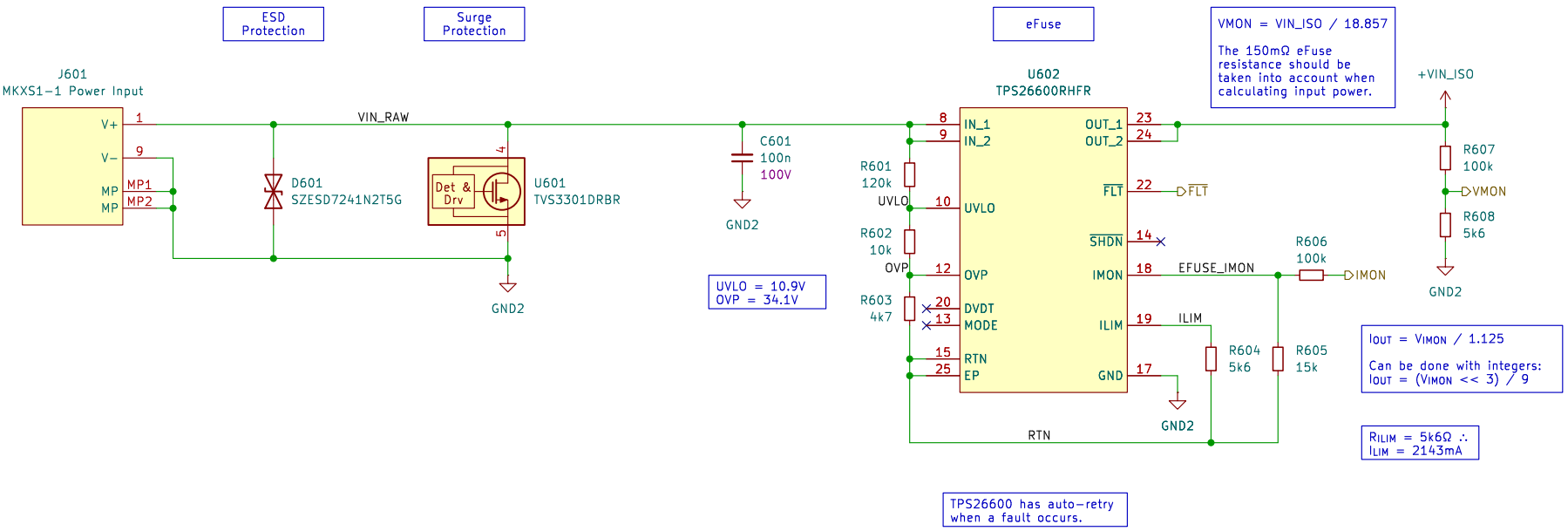


3V3 and 3V3_AON (always on) voltage regulators.

Sheet: /Power/3V3 Regulators/
File: power-3v3-regulators.kicad_sch

Title: 3V3 Regulators (PHY Side)

Size: A4	Date: 2025-06-30	Rev:
KiCad E.D.A. 9.0.3		Id: 4/26



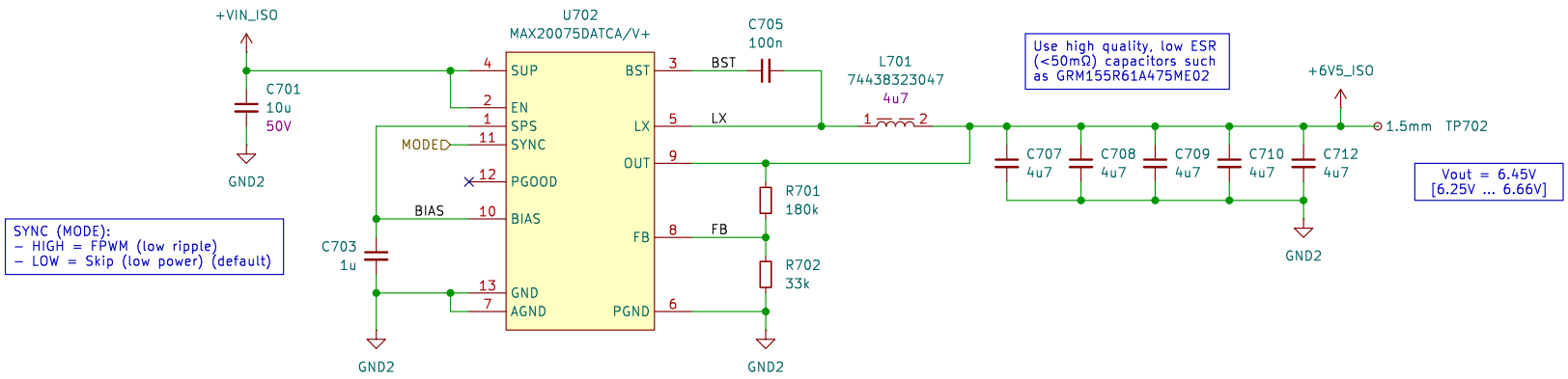
Power input and protection for the connector side of the PCB.

Sheet: /Power/Power In (Isolated)/
File: power-in-isolated.kicad_sch

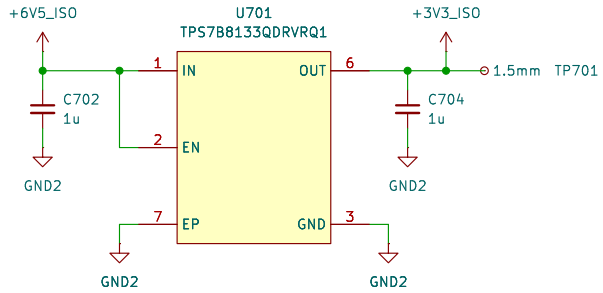
Title: Power In (Connector Side)

Size: A4	Date: 2025-06-30	**Rev:**
KiCad E.D.A. 9.0.3		Id: 6/26

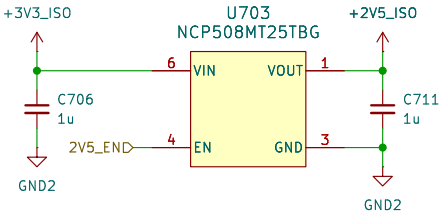
6V5 Regulator



3V3 Regulator



2V5 Regulator



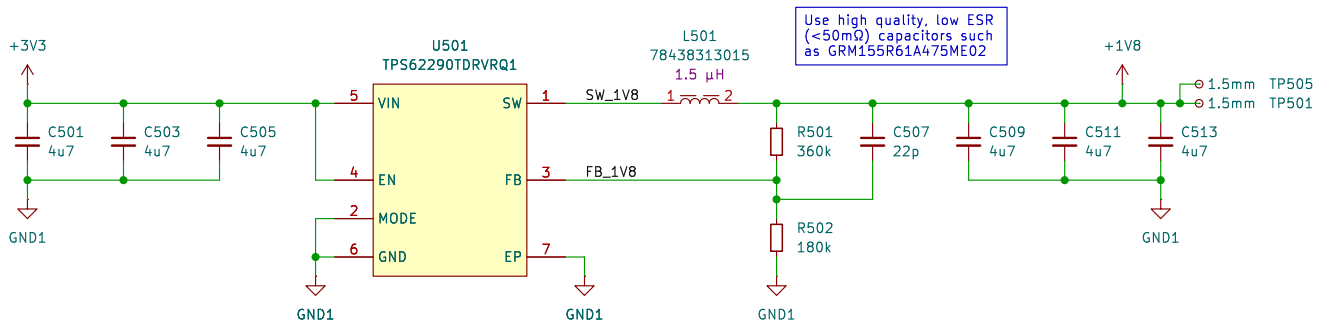
6V5, 3V3 and 2V5 regulators for the connector side of the PCB.

Sheet: /Power/Regulators (Isolated)/
File: power-regulators-isolated.kicad_sch

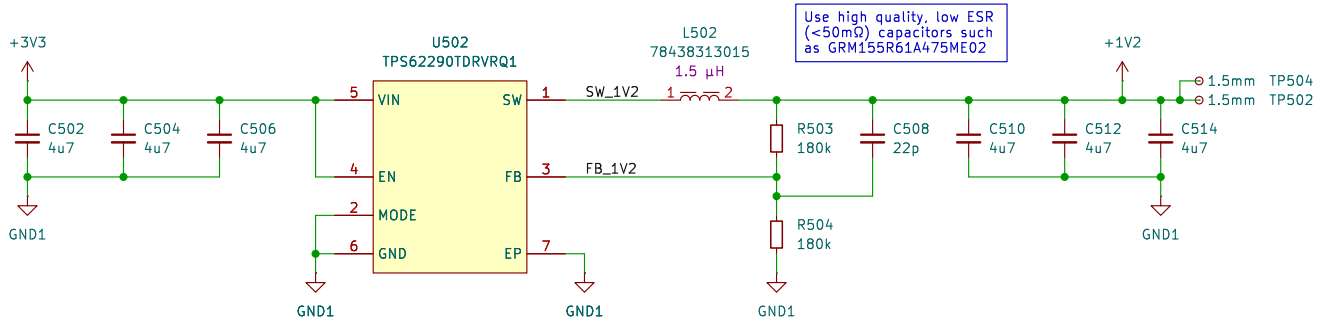
Title: Regulators (Connector Side)

Size: A4	Date: 2025-06-30	Rev:
KiCad E.D.A. 9.0.3		Id: 7/26

1V8 Regulator



1V2 Regulator

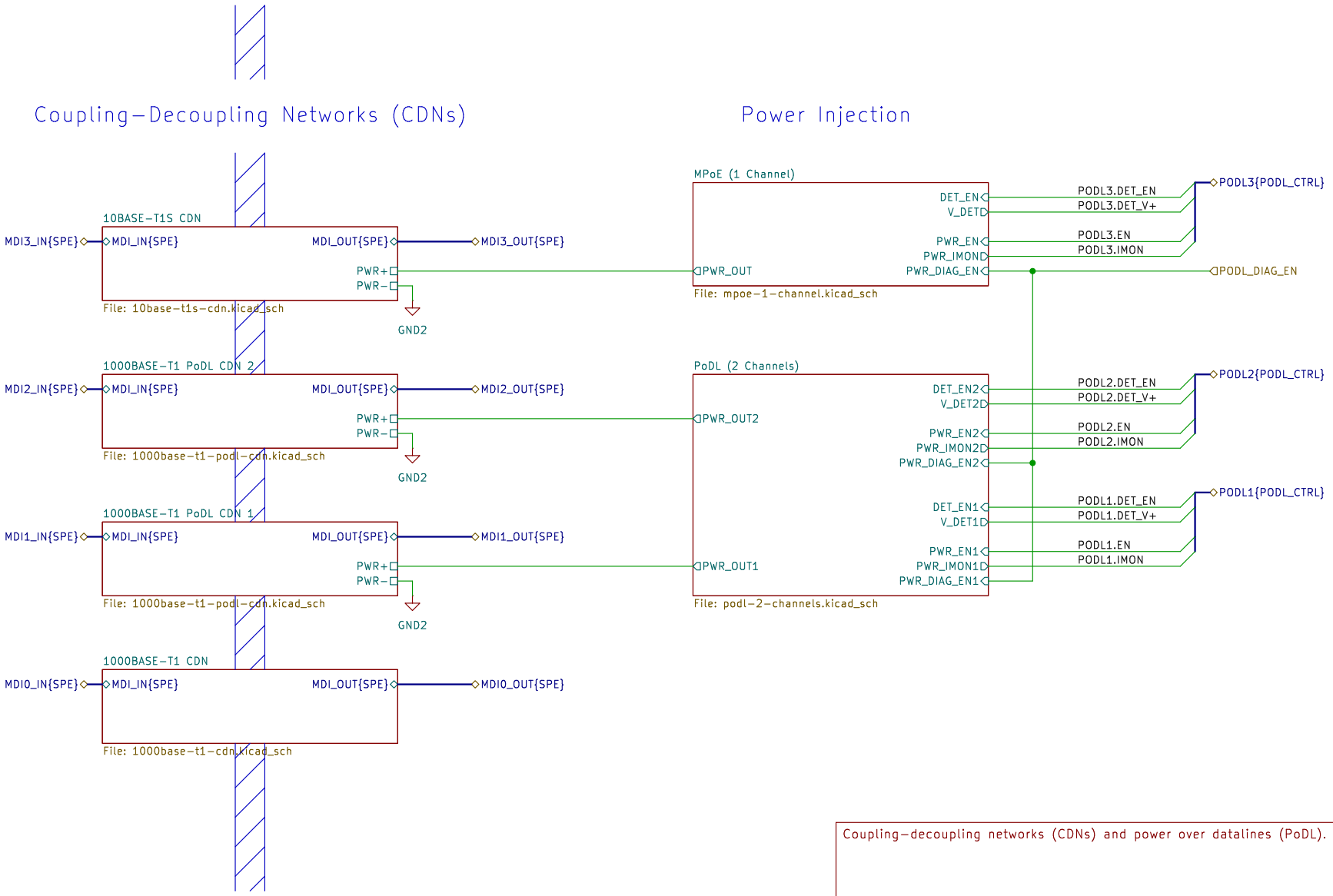


1V8 and 1V2 SMPS for ethernet switch and PHYs.

Sheet: /Power/Ethernet Power/
File: power-ethernet.kicad_sch

Title: Ethernet Power (PHY Side)

Size: A4	Date: 2025-06-30	Rev:
KiCad E.D.A. 9.0.3		Id: 5/26

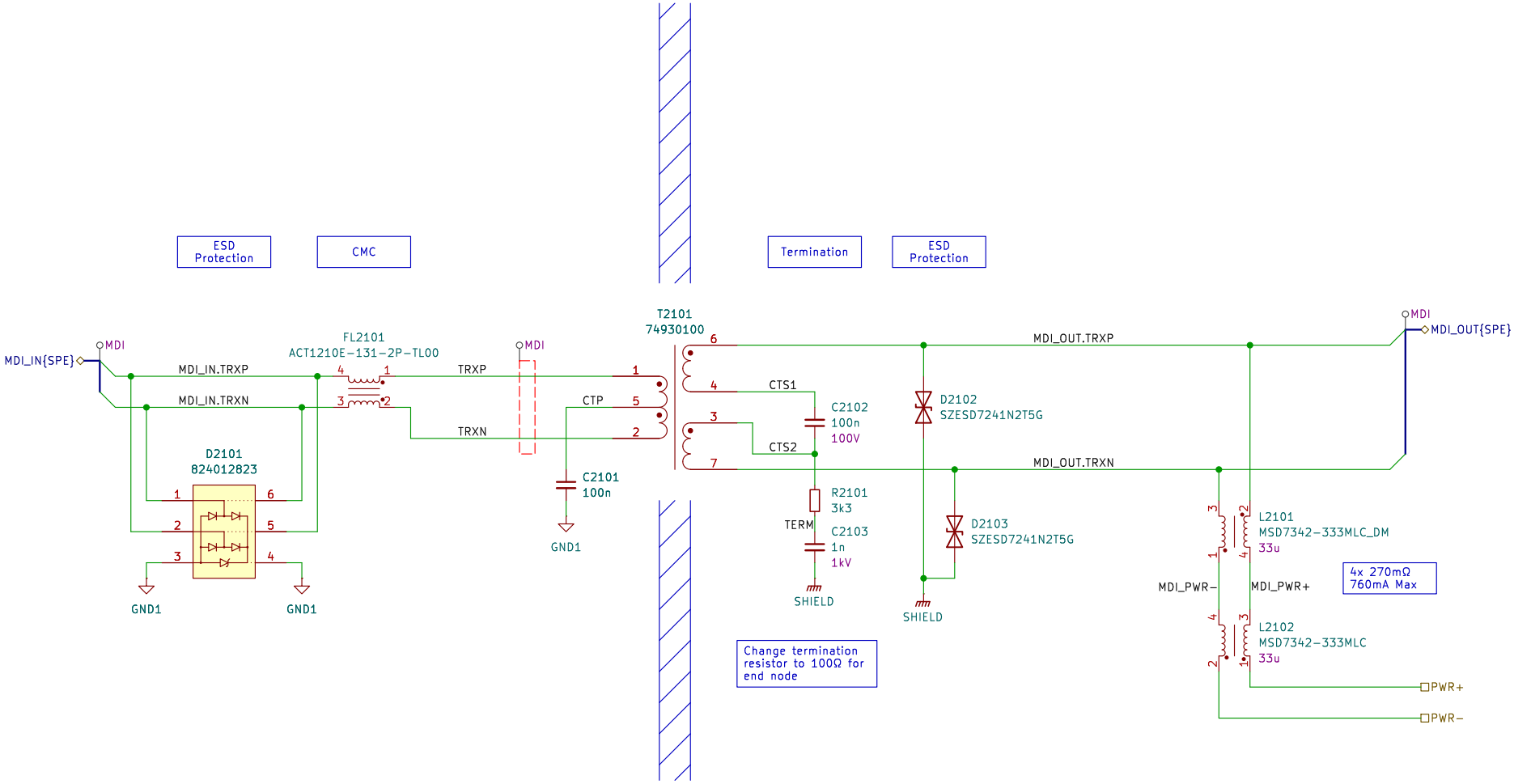


Coupling–decoupling networks (CDNs) and power over datalines (PoDL).

Sheet: /CDNs & PoDL/
File: cdn–podl.kicad_sch

Title: CDNs and PoDL

Size: A4	Date: 2025–06–30	**Rev:**
KiCad E.D.A. 9.0.3		Id: 17/26

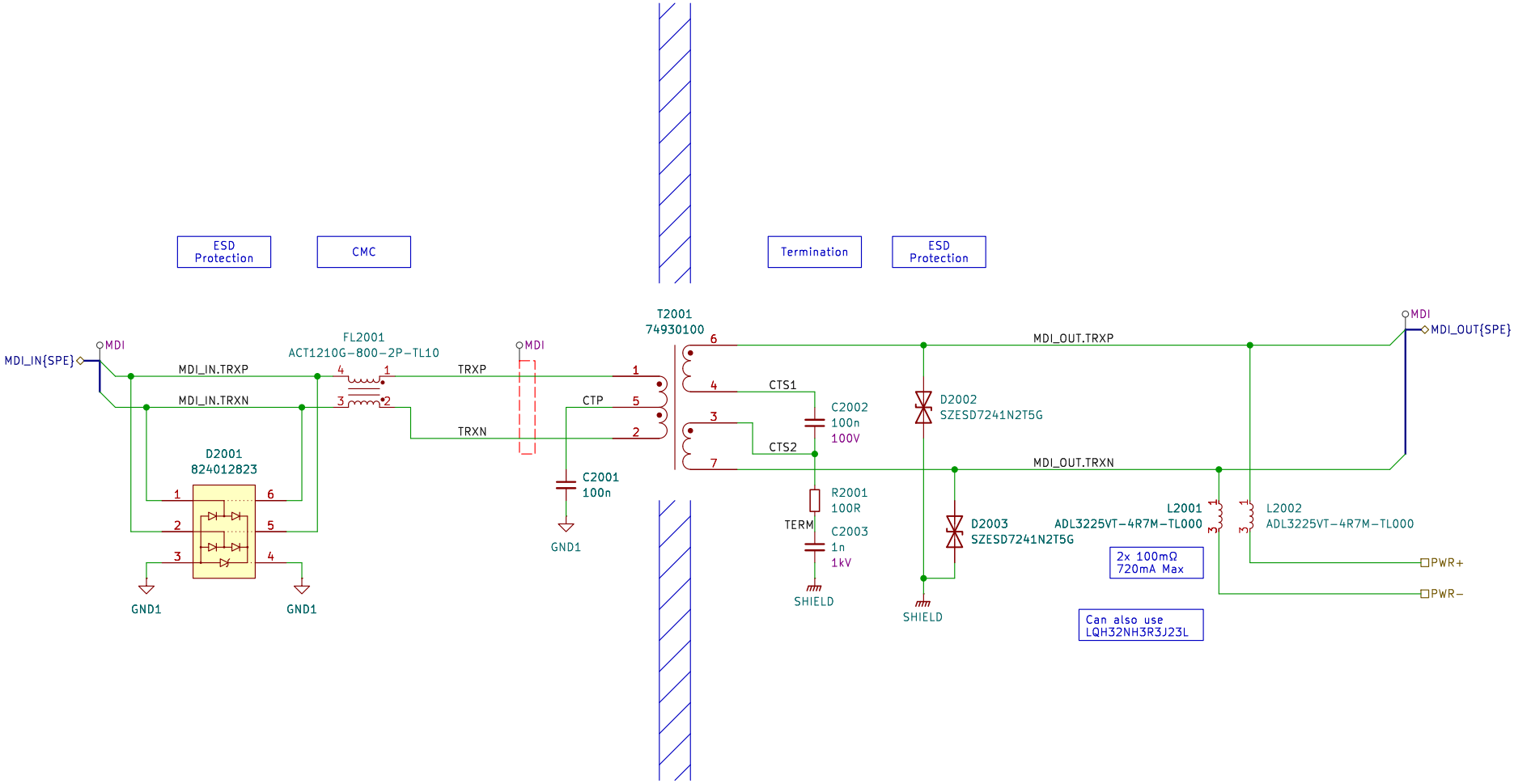


Coupling-decoupling network for 10BASE-T1S with multidrop power over ethernet (MPoE).

Sheet: /CDNs & PoDL/10BASE-T1S CDN/
File: 10base-t1s-cdn.kicad_sch

Title: 10BASE-T1S CDN With MPoE

Size: A4	Date: 2025-06-30	Rev:
KiCad E.D.A. 9.0.3		Id: 21/26

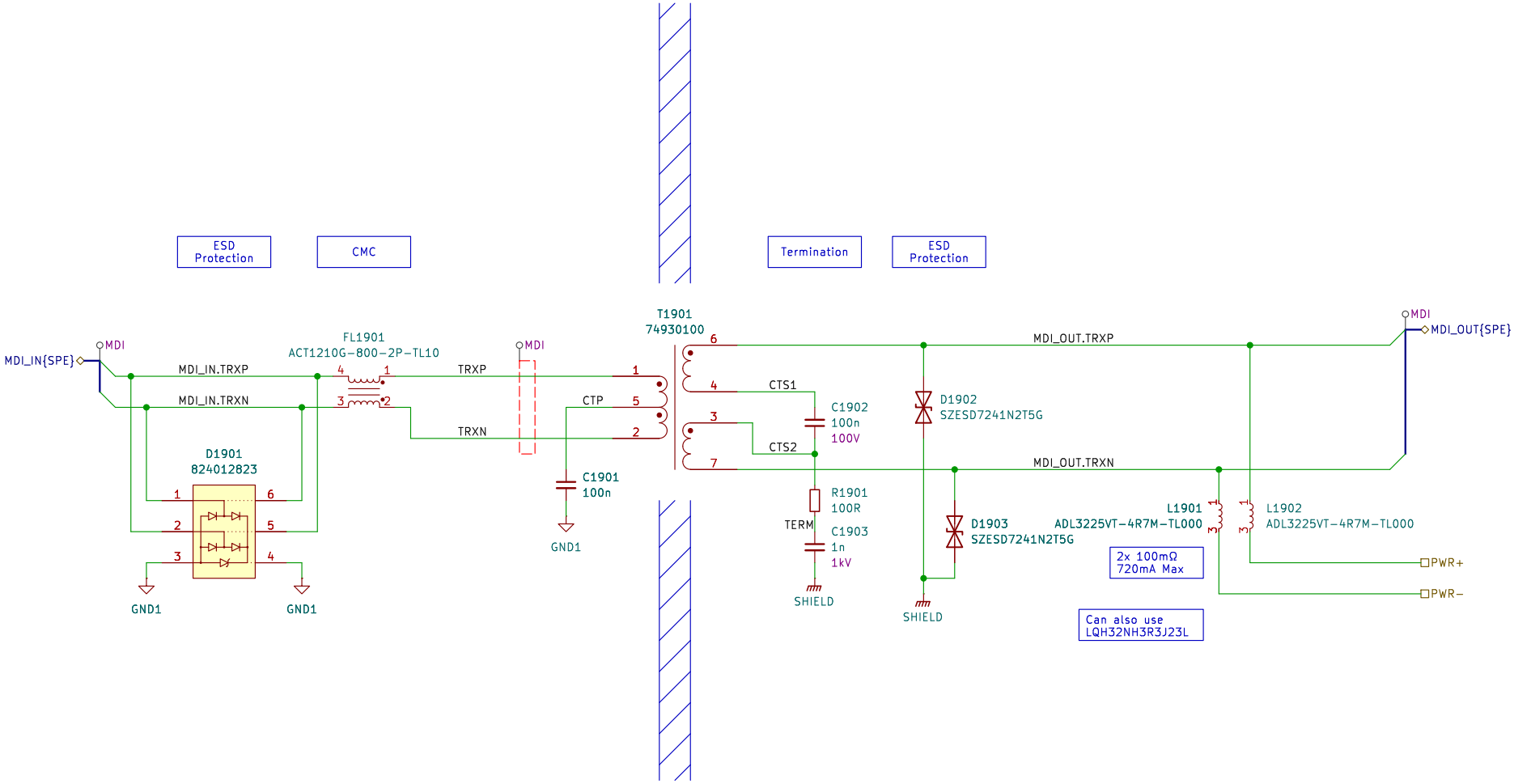


Coupling-decoupling network for 1000BASE-T1 with power over datalines (PoDL).

Sheet: /CDNs & PoDL/1000BASE-T1 PoDL CDN 2/
File: 1000base-t1-podl-cdn.kicad_sch

Title: 1000BASE-T1 CDN With PoDL

Size: A4	Date: 2025-06-30	Rev:
KiCad E.D.A. 9.0.3		Id: 20/26

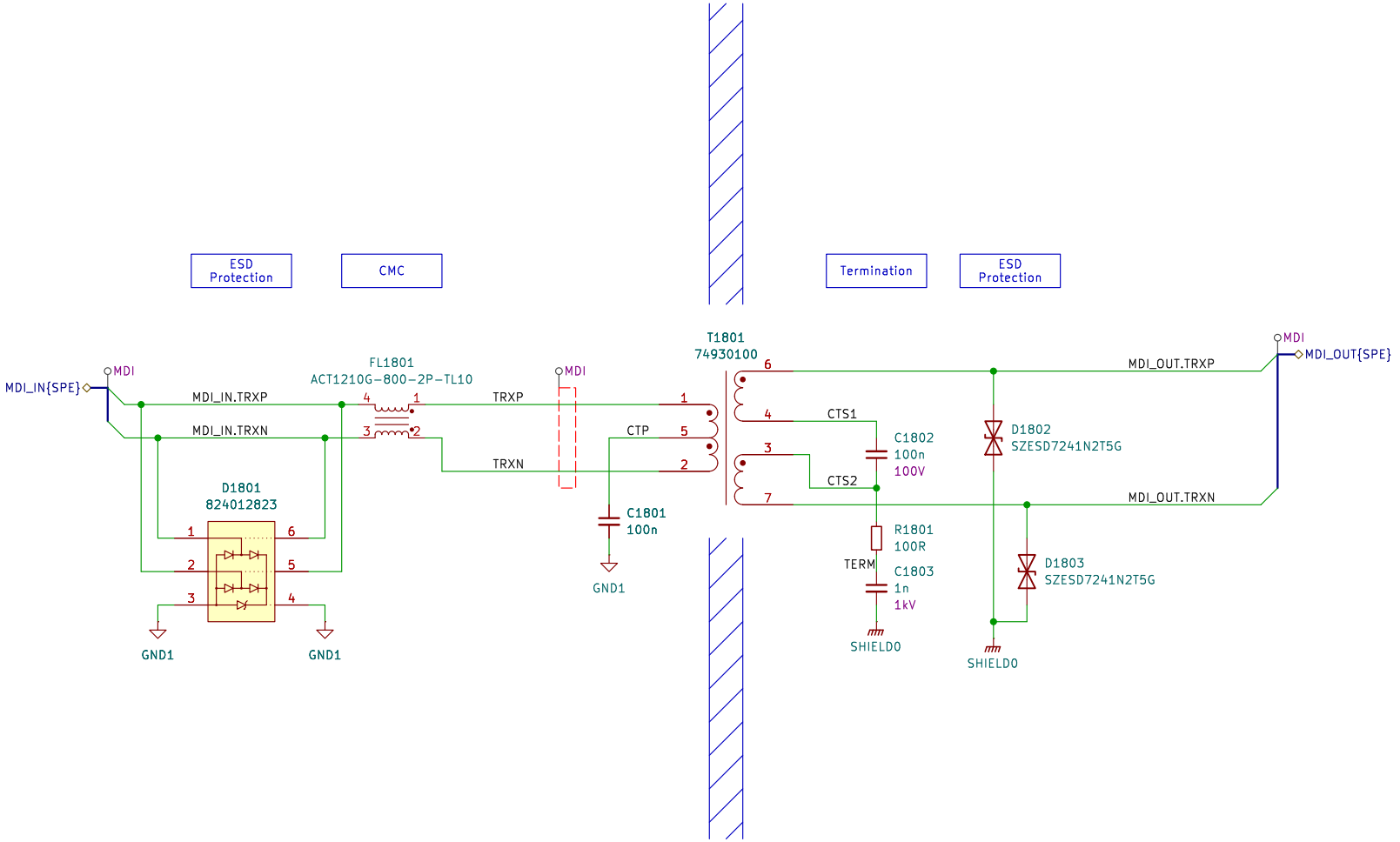


Coupling-decoupling network for 1000BASE-T1 with power over datalines (PoDL).

Sheet: /CDNs & PoDL/1000BASE-T1 PoDL CDN 1/
File: 1000base-t1-podl-cdn.kicad_sch

Title: 1000BASE-T1 CDN With PoDL

Size: A4	Date: 2025-06-30	**Rev:**
KiCad E.D.A. 9.0.3		Id: 19/26

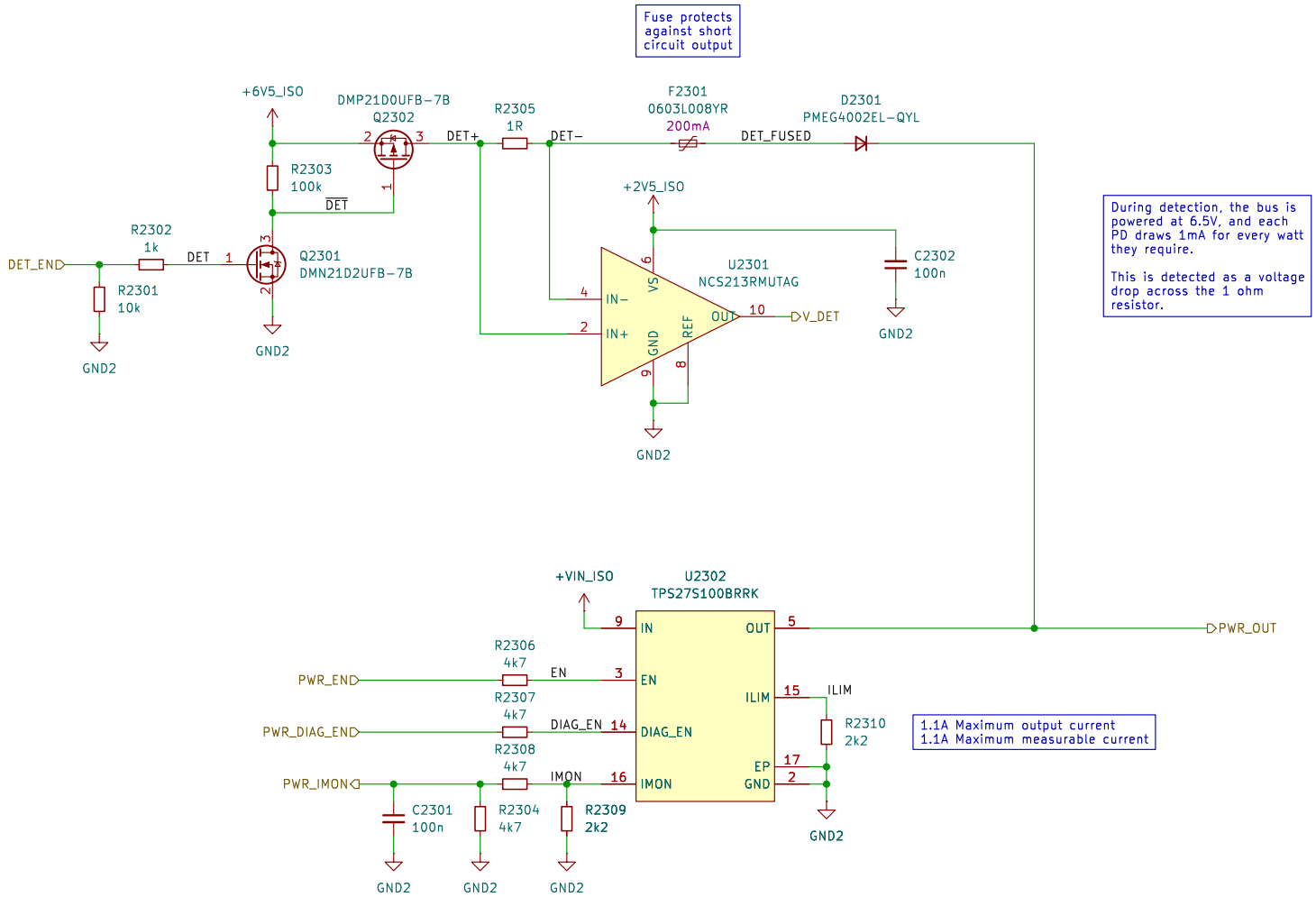


Coupling-decoupling network for 1000BASE-T1

Sheet: /CDNs & PoDL/1000BASE-T1 CDN/
File: 1000base-t1-cdn.kicad_sch

Title: 1000BASE-T1 CDN

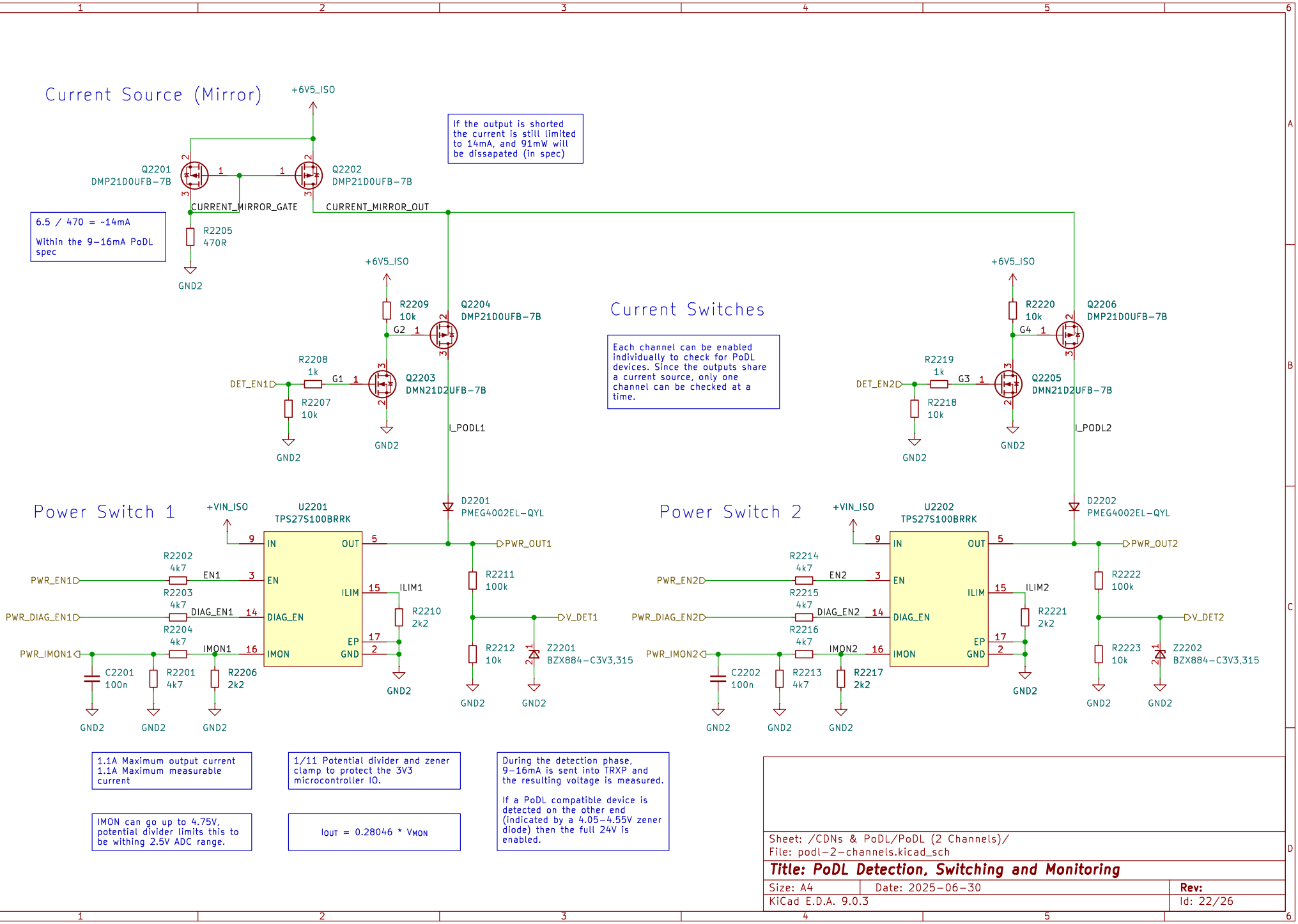
Size: A4	Date: 2025-06-30	**Rev:**
KiCad E.D.A. 9.0.3		Id: 18/26

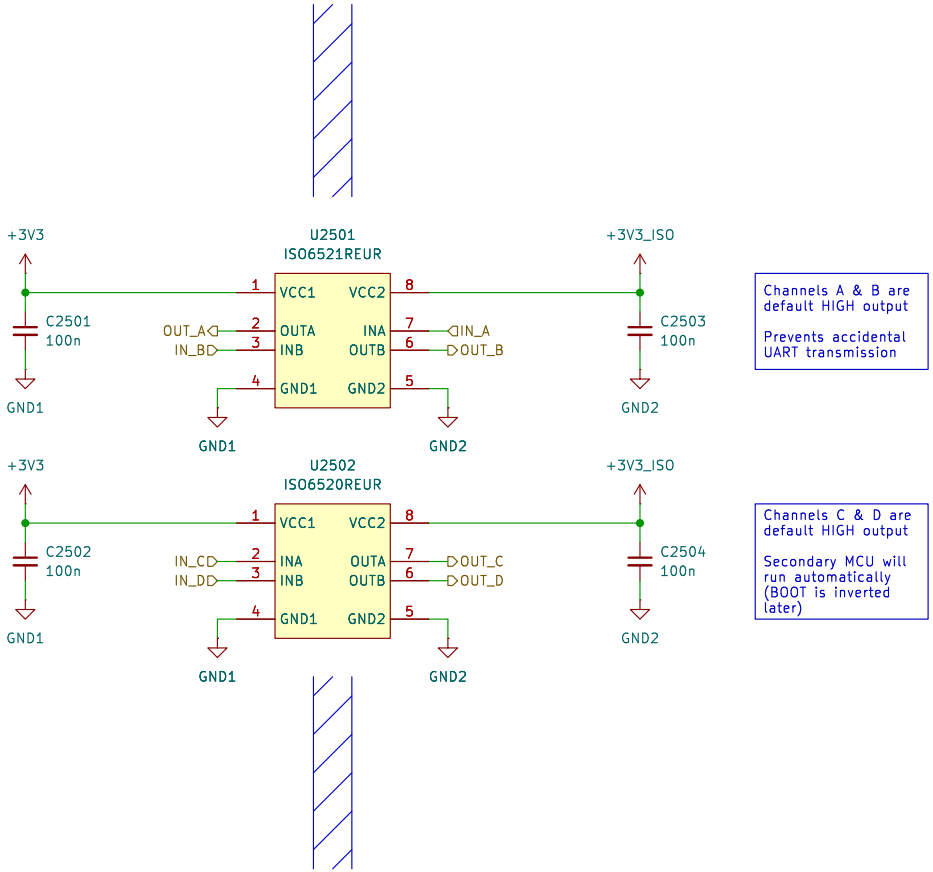


Sheet: /CDNs & PoDL/MPoE (1 Channel)/
File: mpoe-1-channel.kicad_sch

Title: MPoE Detection, Switching and Monitoring

Size: A4	Date: 2025-06-30	Rev:
KiCad E.D.A. 9.0.3		Id: 23/26

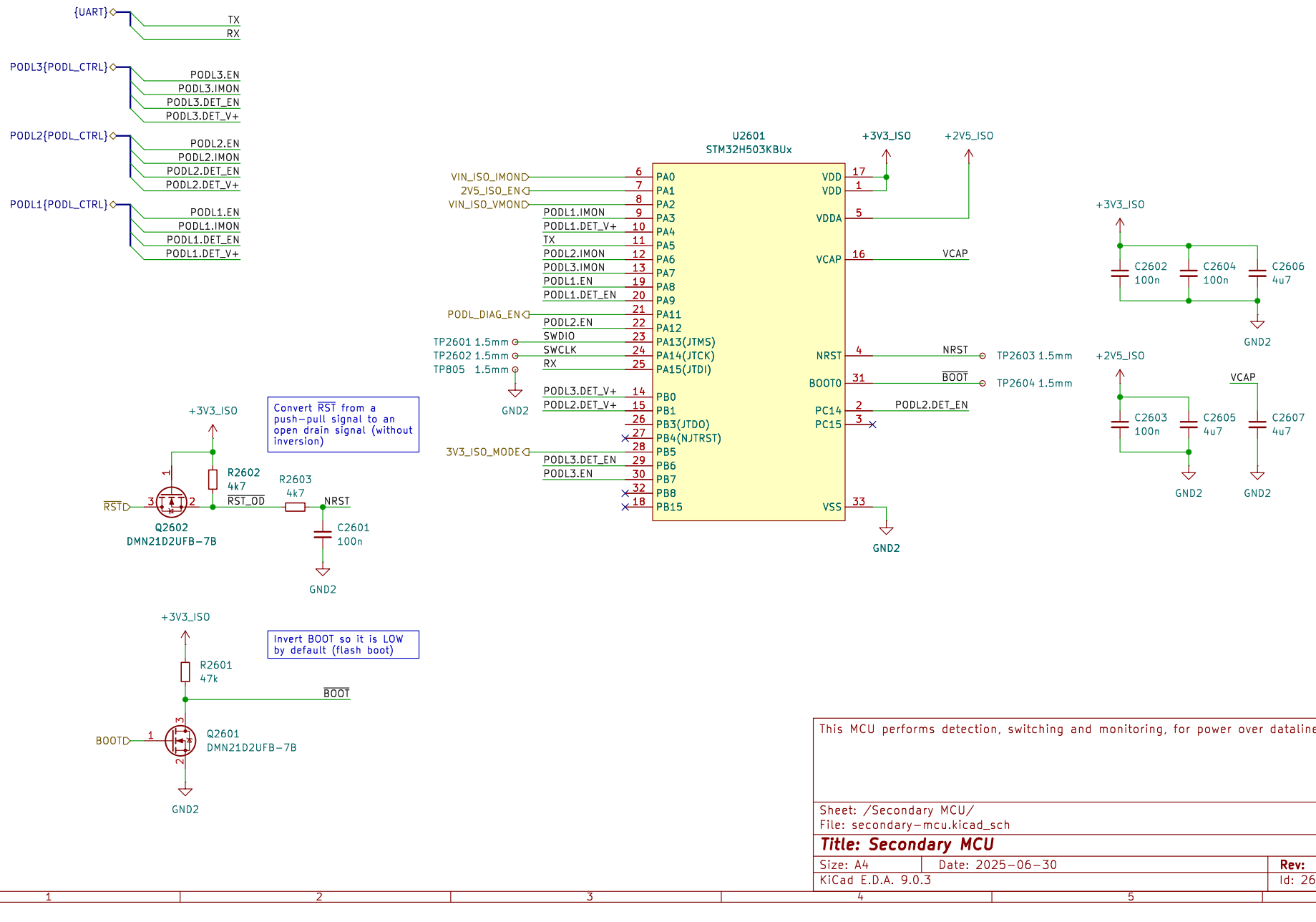

Current Source (Mirror)
+6V5_ISO
If the output is shorted the current is still limited to 14mA, and 91mW will be dissapated (in spec)
Q2201
DMP21D0UFB-7B
Q2202
DMP21D0UFB-7B
CURRENT_MIRROR_GATE
CURRENT_MIRROR_OUT
6.5 / 470 = ~14mA
Within the 9-16mA PoDL spec
R2205
470R
GND2
Current Switches
Each channel can be enabled individually to check for PoDL devices. Since the outputs share a current source, only one channel can be checked at a time.
R2209
10k
Q2204
DMP21D0UFB-7B
G2
R2208
1k
G1
Q2203
DMN21D2UFB-7B
DET_EN1
R2207
10k
I_PODL1
R2220
10k
Q2206
DMP21D0UFB-7B
G4
R2219
1k
G3
Q2205
DMN21D2UFB-7B
DET_EN2
R2218
10k
I_PODL2
Power Switch 1
+VIN_ISO
U2201
TPS27S100BRRK
IN
OUT
EN
ILIM
DIAG_EN
EP
IMON
GND
D2201
PMEG4002EL-QYL
PWR_OUT1
R2202
4k7
EN1
PWR_EN1
R2203
4k7
DIAG_EN1
PWR_DIAG_EN1
R2204
4k7
IMON1
PWR_IMON1
R2210
2k2
ILIM1
R2211
100k
V_DET1
R2212
10k
Z2201
BZX884-C3V3,315
C2201
100n
R2201
4k7
R2206
2k2
Power Switch 2
+VIN_ISO
U2202
TPS27S100BRRK
D2202
PMEG4002EL-QYL
PWR_OUT2
R2214
4k7
EN2
PWR_EN2
R2215
4k7
DIAG_EN2
PWR_DIAG_EN2
R2216
4k7
IMON2
PWR_IMON2
R2221
2k2
ILIM2
R2222
100k
V_DET2
R2223
10k
Z2202
BZX884-C3V3,315
C2202
100n
R2213
4k7
R2217
2k2
GND2
1.1A Maximum output current
1.1A Maximum measurable current
1/11 Potential divider and zener clamp to protect the 3V3 microcontroller IO.
During the detection phase, 9-16mA is sent into TRXP and the resulting voltage is measured.
If a PoDL compatible device is detected on the other end (indicated by a 4.05-4.55V zener diode) then the full 24V is enabled.
IMON can go up to 4.75V, potential divider limits this to be withing 2.5V ADC range.
IOUT = 0.28046 * VMON
Sheet: /CDNs & PoDL/PoDL (2 Channels)/
File: podl-2-channels.kicad_sch
Title: PoDL Detection, Switching and Monitoring
Size: A4
Date: 2025-06-30
Rev:
KiCad E.D.A. 9.0.3
Id: 22/26

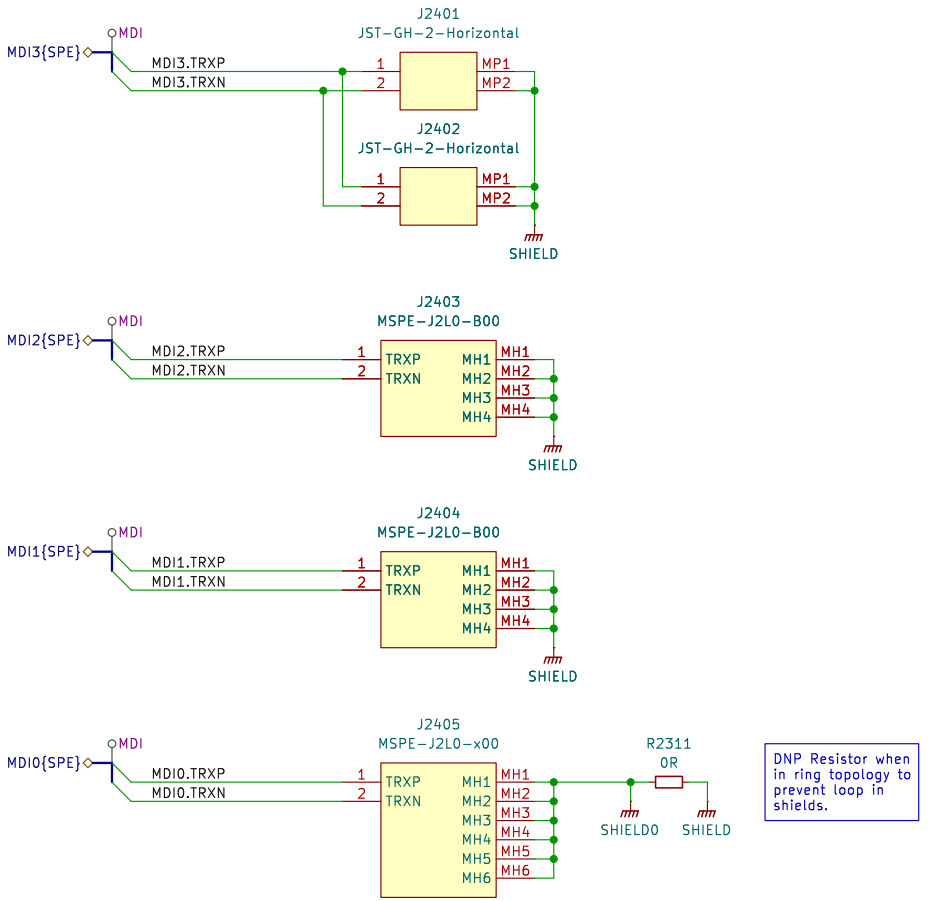


Sheet: /Isolation Crossing/
File: isolation-crossing.kicad_sch

Title: Isolation Crossing

Size: A4	Date: 2025-06-30	**Rev:**
KiCad E.D.A. 9.0.3		Id: 25/26


{UART}
TX
RX
PODL3{PODL_CTRL}
PODL3.EN
PODL3.IMON
PODL3.DET_EN
PODL3.DET_V+
PODL2{PODL_CTRL}
PODL2.EN
PODL2.IMON
PODL2.DET_EN
PODL2.DET_V+
PODL1{PODL_CTRL}
PODL1.EN
PODL1.IMON
PODL1.DET_EN
PODL1.DET_V+
U2601
STM32H503KBUx
VIN_ISO_IMOND
2V5_ISO_EN
VIN_ISO_VMOND
PODL1.IMON
PODL1.DET_V+
TX
PODL2.IMON
PODL3.IMON
PODL1.EN
PODL1.DET_EN
PODL_DIAG_EN
PODL2.EN
SWDIO
SWCLK
RX
PODL3.DET_V+
PODL2.DET_V+
3V3_ISO_MODE
PODL3.DET_EN
PODL3.EN
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PA8
PA9
PA11
PA12
PA13(JTMS)
PA14(JTCK)
PA15(JTDI)
PB0
PB1
PB3(JTDO)
PB4(NJTRST)
PB5
PB6
PB7
PB8
PB15
VDD
VDD
VDDA
VCAP
NRST
BOOT0
PC14
PC15
VSS
+3V3_ISO
+2V5_ISO
VCAP
NRST
BOOT
PODL2.DET_EN
TP2601 1.5mm
TP2602 1.5mm
TP805 1.5mm
TP2603 1.5mm
TP2604 1.5mm
GND2
C2602
100n
C2604
100n
C2606
4u7
C2603
100n
C2605
4u7
C2607
4u7
Convert RST from a push-pull signal to an open drain signal (without inversion)
R2602
4k7
R2603
4k7
RST
RST_OD
Q2602
DMN21D2UFB-7B
C2601
100n
Invert BOOT so it is LOW by default (flash boot)
R2601
47k
BOOT
Q2601
DMN21D2UFB-7B
This MCU performs detection, switching and monitoring, for power over datalines (PoDL).
Sheet: /Secondary MCU/
File: secondary-mcu.kicad_sch
Title: Secondary MCU
Size: A4
Date: 2025-06-30
Rev:
KiCad E.D.A. 9.0.3
Id: 26/26



Sheet: /Ethernet Connectors/		
File: ethernet-connectors.kicad_sch		
Title: Ethernet Connectors		
Size: A4	Date: 2025-06-30	**Rev:**
KiCad E.D.A. 9.0.3		Id: 24/26