VLSI Design - Phase 01

Main Objective: **Select or write VHDL code, evaluate its suitability for the VLSI Design flow, and the potential range of performance considering area and power trade-offs**

Part 1:

Select a reference VHDL design: you can either 1) write a design to implement a somewhat complex arithmetic/logic functionality, or 2) reuse a block from a difference source.

Discuss your selection with a TA or your instructor.

The chosen code must be equipped by a functional testbench. Perform behavioural simulation of your code on ModelSim. Use the rgb2grayscale tutorial as your reference.

Part 2:

Perform a synthesis at a reference frequency of 10MHz on the CMOS 45nm stdcell technology node. If your deisgn has multiple clocks, please discuss this with your instructor or TA.

Determine the area in um^2 and the number of equivalent gates in your design. In principle, the number of kiloGates should be between 20 and 100. If your design does not fit within this range, please discuss this issue with your instructor or TA.

Note: Gate count is obtained by dividing the design area in um by the area of a NAND2 gate (which in CMOS45 is approximately 0.8um^2).

Be aware that your design at this stage may be susceptible to many unforseen design problems, which you will likely need instructor assistance. Be prepared to start early and allow time for support, and even a change in the target design. **It is your responsibility to have a working design prior to the deadline – no extensions will be granted.**

Part 1 & 2 due: January 25th (no submission required)

Part 3:

Using the rgb2grayscale tutorial as a reference, complete a full analysis of the area vs speed, and power vs speed performance of your circuit. Provide appropriate graphs that describe the trade-offs. You must vary speed to see the trade-offs of your core.

Select a target frequency for your design based on your analysis, and provide a detailed report in your powerpoint slides of: 1) the timing performance of your design (include a description of the critical path), 2) area occupation (Kgates and um^2), 3) power consumption estimated by the synthesis process, and 4) provide a comparison of the graphs above

Part 4:

-Perform post synthesis simulation of your design, verifying correctness.

-Perform a complete analysis by repeating the steps from part 2, and power analysis of your post synthesis with VCD file back-annotation describing the main blocks contributing to consumption. Describe the critical path of your design in the conditions chosen from Part 3.

-What is the most suitable design parameters for your core based on the elbow plots?

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Deliverables

Prepare a powerpoint presentation (max 5 slides including title slide), and a .tgz file which includes all the files required to replicate your results from steps 1- 4.

To be completed and uploaded to canvas by February 1st . We will have a grading session as listed on the semester schedule – you will be required to present and demonstrate your work.

Please commit a .tgz or zip file, which includes the pdf version of your ppt slides/report, your source HDL files, and all synthesis and simulation scripts before **Feb 1st @ 11:59pm**.

Grading

Grading Rubric [/100]

[/20] Completeness of presentation, slides, information is clear and appropriate

[/20] Sound results - reported performance is correct and justifiable (area, graphs, area timing information, and leakage/dynamic power consumption stats).

[/50] Completeness of results, all files provided (all design steps required have been performed correctly [step 2: 15%, step 3: 25%, step 4: 10%])

[/10] Demo questions (individually) + lab attendance