VLSI Design - Phase 02

Main Objective: **Design a stdcell library using HSPICE, performing a full timing characteriziation. A reference circuit will be used to test the efficiency of the library designed, which will be used to refine your stdcell library.**

Part 1:

Refer to the **ensc450-tutorial2_HSPICE.pdf** tutorial provided on Canvas. Complete the tutorial and be sure to read the support documentation. Once complete:

Write a HSPICE stdcell library consisting of at least one inverter, one NAND and one NOR gate. Start by building a minimal library composed by a schematic (.cir file) of the cells INV_X1, NOR_X1 and NAND_X1 gates, and perform the necessary simulations in order to build your library file as described in the tutorial. Sweep Ttrin/ Cload values to build your .lib file. Use the appropriate transistor types (i.e. stacked, common source etc) as required. You are encouraged to use design macros provided in the example files to ease your work (i.e. see lab2_comb_stdcell.cir file).

Once you have completed these circuit files and sweeps, use the liberty file (in the db form, instructions below in Note5 to compile the .lib -> .db) to synthesize your VHDL design used in phase 1. Measure the maximum frequency and relative area (**neglect power information in this lab**).

Note1: All your timings should come from HSPICE simulations. **Manually calculate the area of your cells supposing each unit of Wn used is 1um^2**. Manually calculate the input capacitance of each node of each cell supposing the unit C (MOS with W=Wn) is = 1fF. Fill in the .lib file (part IV of the tutorial) with the values you calculate.

Note 2: Your library will not contain FFs, so the tool will use “theoretical” FFs, defined as *FFGEN* that have no delay or timing properties. This will not be a problem - in this context we only care about the combinational cells you are defining.

Note3: You do not need to perform post-synthesis simulation – we are only collecting synthesis result.

Note 4: Select the worst case conditions for your simulation: **1.05V, SS transistors, 125C**

Note 5: Compile the (.lib) liberty file with the following command in the terminal*:

dc_shell-xg-t -shell lc_shell

lc_shell> read_lib <file.lib>

lc_shell> write_lib **<library name>** -format db -output <file.db>

lc_shell> exit (when ready to exit the library compiler)

*ensure you open a new terminal and source tutorial1 scripts prior to running dc_shell

<library_name> is the name of your new .db you’d like to create

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Part 2:

Extend your stcell library by designing the schematic and characterizing the cells NAND_X4, NOR_X4, and INV_X4, plus one (or more) cells of your choice (develop the X1 and X4 versions). Write the liberty file and compile the .db file for the extended library. Synthesize the Phase 1 VHDL using this second library that contains x1 and x4 drive strengths of the stdcell. Compare the timing and area performance of your phase 1 VHDL design based on this second synthesis activity. Also consider that these spice models are developed at 180nm tech lib.

Overall, compare and discuss your core's performance and area for the following:

x1 stdcell lib vs lab1

x1+x4 stccell lib vs lab1

X1 stdcell lib vs x1+x4 stdcell lib

Deliverables

Prepare a powerpoint presentation (max 5 slides including title slide), and a .zip/.tar/.tgz file which includes all the files required to replicate your results.

To be completed and uploaded to canvas by February 22nd.

We will have a grading session as listed on the semester schedule – you will be required to present and demonstrate your work.

Please commit a .zip/.tar/.tgz file, which includes the pdf version of your ppt slides/report, your source HDL files, all synthesis and simulation scripts, and datasheets containing your values before **Feb 22nd @ 11:59pm**. All files should be contained in the file to replicate your results.

Grading

Grading Rubric [/100]

[/20] Completeness of presentation (reported performance is correct, information is clear, in an appropriate style, and justifiable)

[/20] Circuit (.cir) files, .tr0 files, and correctness of stdcell design. Include your reports generated per circuit.

[/20] Correctness of library characterization (include all files required to replicate results, .lib, .db etc)

[/30] Correctness of proposed synthesis results [step 1: 15%, step 2: 15%]. Include all required files to replicate results.

[/10] Demo questions + lab attendance