Lab 2:

Why?

The **objective** of lab2 is to design a custom liberty (.lib) file, containing parameters of a stdcell library you have designed. You will measure various parameters of your stdcells using HSPICE, and use these values to compile your .lib file. The .lib will be translated to a .db file using lc_shell, which will be included in your synth.tcl file (versus the nangate_..._slow.db file), and re-synthesize your lab1 vhdl core to compare results.

.lib file structure

The .lib file itself consists of several Look Up Tables (LUTs) which resemble the following structure:

```
cell_fall(Propagation_Delay) {
index_1 ("1, 2");
index_2 ("2, 10");
values ("0.106,0.246","0.231,0.437");
```

This example provides a template for a given cell's tpdf, one of many LUTs in the lib file (per gate). You must fill out the "values" row, specifying your cell's tpdf. These values are obtained using the .cir/.inc files you sweep with HSPICE. The dc_shell tool will then read and use the .lib LUT information you provide to determine the best gate(s) for your design during synthesis.

In this example, index_1 refers to input transition time, and index_2 to the capacitance load. Accordingly, the value 0.106 signifies a 0.106ns tpdf for the given cell when the input transition time = 1ns, and capacitance load = 2fF. 0.246 signifies a 0.246ns delay for the cell when the input transition time = 1ns, and capacitance load = 10fF, etc. It is your job to fill these values in the liberty file. You may leave the (1,2)(2,10) values as provided in the template, and use these values to sweep your stdcells and fill in the LUTs accordingly.

Note that the .lib has other parameters as well which you must fill (area, etc). Refer to both the tutorial and lab document for specifications, and to **spicelib_180_tt_120_25C.lib** as a good template.

Why do we need .cir and .inc files then?

The initial .cir files you create will help you a) verify the correct functionality per x1 gate, b) determine if you have properly sized the transistors for x4 drive, and c) measure various values of your stdcell, such as tpdf, and tpdr, for inclusion in your .lib file.

You may use .inc files to define your cells, their respective terminals, logic behaviour, and any parameters to pass to the gate (such as width). You may then integrate all your cell definitions

into a main .cir file, and sweep for different input transition and Cload values required of the .lib file (versus running the *hspice* command *n*stdcells*2Cload*2input* transition times).

It's a very good idea to refer to the **comb_stdcell_liberty2.cir** file as an example of instantiating cells in a main file, and sweeping your variables for various stdcells at once.