VLSI Design - Phase 03

Main Objective: **To complete layouts for a stdcell library, extracting the schematic parameters and using them to adjust your liberty file definitions. Use your reference design to test the efficiency of your refined stdcell library.**

Part 1:

Complete a full layout for a skewed inverter.

Refer to the **Tutorial3-layout.pdf** tutorial provided on Canvas which provides a step-by-step manual layout using Cadence Virtuoso.

Perform a full layout for a set of cells to develop a stdcell library: Every group must perform a layout for an inverter x1 *unskewed* (tutorial provided is skewed), NOR x1, NAND x1.

Perform and complete the layout activity for the stdcell your group used for Lab2 (x1 version). Update the liberty file from phase 2 (suggest to copy the lib and rename to lab3, as you will require the original lab2 for comparison) with the timing information extracted from these cell layouts. All necessary specifications are provided in Tutorial3-layout.pdf.

Make an independent lib file, called <name_of_lab3_lib>.lib which only contains the cells you have designed in this lab.

Note: in the case that your design is not DRC or LVS free, clearly state this in your report – do not hide this. Results of this characterization will be distributed to the class and compared.

Part 2:

Perform a new synthesis activity for your reference design core. Your lab3 lib file should contain all information of your layout cells (inverter, NOR, NAND and chosen stdcell). Compare the following:

1. lab2 x1+ x4 lib vs lab3 lib 2. lab3 lib vs lab1 lib 3. lab2 x1+x4+lab3 lib vs lab1 lib

Note: you can **not** have two cells with the same name in a synthesis run. Therefore add the suffix "_lay" to the new layout cells you have designed in your lib files.

Provide a comparison of elbow plots and optimal design point for possibilities listed above. Consider performance, area, and power where applicable.

Ensure for all Spice simulations, there is a consistent value of PVT. PVT impacts silicon performance, and therefore we must maintain consistency between cells to avoid introducing sources of errors in your assignment.

Deliver ables

Prepare a powerpoint presentation (max 6 slides including title slide), and a .zip/.tar/.tgz file which includes all the files required to replicate your results. Include a README so that your TAs may follow your design when marking.

To be completed and uploaded to canvas by March 15th @ 11:59pm.

We will have a grading session as listed on the semester schedule – you will be required to present and demonstrate your work.

VLSI Design - Phase 03

Grading

Grading Rubric [/100]

[/20] Completeness of presentation – all necessary information is visible, all plots and explanations are provided. Group members are capable of describing the layout appropriately, cells and schematics, related to the design.

[/30] Sound results – required performance results are correct, justified (area and timing of synthesis design and cell layout). Required results are visible. Working design.

[/40] Completeness of results – All required design steps have been performed correctly. All HPSICE steps performed correctly [20]. Layout activity is functional, DRC and LVS free of errors [20] All files provided may be used to replicate results. Proof of results obtained is required

[/10] Demo Question – individual during presentation + lab attendance