

VLSI Design - Phase 04

Main Objective: To complete a full Place & Route (P&R) for your core design, using both a GUI and scripting method with Cadence Innovus.

Part 1:**Complete a full Place & Route (P&R) for your design.**

Refer to the **ensc450-tutorial4-PlaceRoute.pdf** tutorial provided on Canvas. This is a continuation of the rgb2grayscale tutorial from lab1, now introducing you to back-end (BE) design. Ensure you understand all the scripts and commands. Go through all the report files; sometimes an error will generate but will not be indicated at the end.

Next, complete the full P&R activity for your phase 1 design using the cmos 45nm stdcell technology. Adapt all Innovus scripts and GUI inputs to your design. In particular, adapt the SDC constraint file definition, as it will likely be different from the Phase 1 version (consider “min” conditions).

When completing the design, ensure that:

1. The size of the design is as small as possible (consider density)
2. There are no timing violations for the frequency selected
3. There are no DRC (geometry) violations

Part 2:**Report your results:**

- Report all information on your design, including area, cell density, frequency, slack, and a description of the critical path.
- Create one .tcl script which runs all your scripts. Measure the CPU time required to run all the P&R scripts sequentially.
- Compare your P&R results to your Front-End (FE) phase 1 results and discuss area, timing and power using elbow plots for illustration
- Report all information regarding your clock tree: Max skew, latency, the number of levels, number of buffers, number of FF (aka sinks).
- Perform a post-layout simulation with the final netlist, and your original testbench. Ensure that your design works as expected and make note of it in your report.
- Report power consumption (average and testbench vcd), and compare to FE results in lab1.
- Compare your P&R results with your previous FE results at the same optimal frequency and working conditions. Find the new optimal timing for your core considering P&R

Deliverables

Prepare a powerpoint presentation (max 5 slides including title slide) discussing your results. Create a .zip/.tar/.tgz file which includes all the files required to replicate your results.

To be completed and uploaded to canvas by April 2nd @ 11:59pm.

We will have a grading session as listed on the semester schedule – you will be required to present and demonstrate your work. Please sign up for your demo.

VLSI Design - Phase 04**Grading****Grading Rubric [/100]**

[/20] Completeness and clarity of presentation – all necessary information is visible, clear, in an appropriate style, demonstrating all required results

[/20] Sound results – required reports are complete, with realistic and optimized results. Required results are visible. Working design.

[/50] Completeness of design and results – All required design steps have been performed correctly. Files correct, working design. All files provided may be used to replicate results, with evidence of all results given (reports, xlsx etc).

[/10] Demo Question(s) + lab attendance