CS223 Laboratory Assignment 3

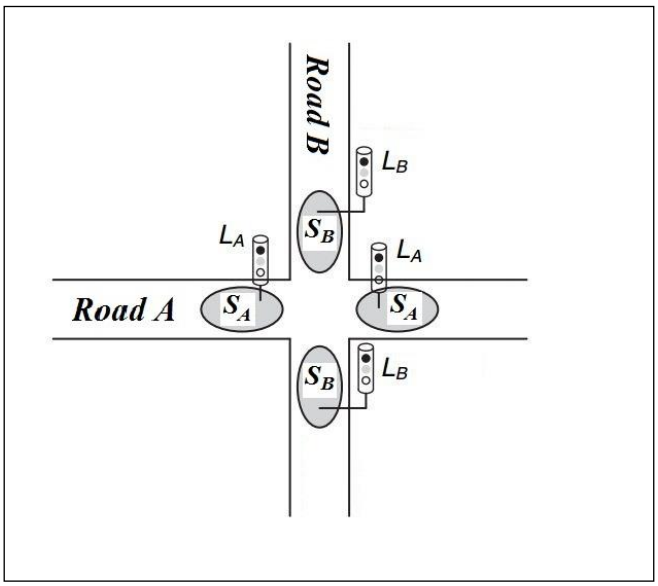
Traffic Light System

Lab dates and times:
Section 1: 14.11.2016 Monday 08:40-12:25
Section 2: 8.11.2016 Tuesday 08:40-12:25
Section 3: 14.11.2016 Monday 13:40-17:25
Section 4: 8.11.2016 Tuesday 13:40-17:25
Section 5: 10.11.2016 Thursday 08:40-12:25
Section 6: 11.11.2016 Friday 08:40-12:25

Location: EA Z04 (in the EA building, straight ahead past the elevators)
Groups: Each student will do the lab individually. Group size = 1

Traffic Light System

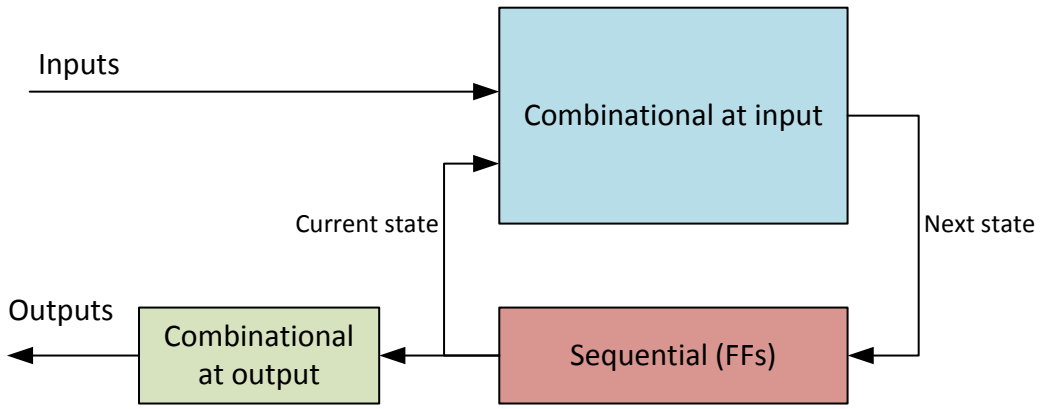
In a community, people need stop signs and traffic lights to slow down drivers from going to fast. To reduce danger at the intersections, time for switching red light to green light and green light to red light should be regulated carefully. Traffic light system is similar to the example in pages 124-129 in the text book, but with some improvement. The roads in which intersect are Road A and Road B. There are sensors SA and SB installed in each road to sense the traffic. Each sensor will be TRUE if traffic present and FALSE if the road is empty. There are two traffic lights LA and LB to control the traffic. The lights may change every 3 seconds depending on the sensors. If a sensor output is TRUE, the lights will not change until it is set to FALSE. If a light is green and sensor is false it will turn to yellow and then red. Both lights will be red for 3 seconds and then red light will turn yellow 3 seconds and then turn green.



Preliminary Report (45 points)

A number of tasks in the today's lab need advance preparation. These advance designs and SystemSystemverilog models should be prepared in advance, and assembled neatly into a Preliminary Design Report. You should make your report as neat as possible, using A4 paper, with a printed cover page and printed pages for the SystemSystemverilog codes. Of course you will need a copy of your designs and SystemSystemverilog programs with you at all times in the lab: to work with, to refer to, to possibly correct and change, to discuss with the TA, to use in debugging. The Preliminary Design Report will be turned in at the start of lab. Therefore, you must make a photocopy of it before you come to the lab. Cover page includes the followings: course name and code number, the number of the lab, your name and student ID, date, number of your trainer pack.

a) Sketch your improved Moore state machine transition diagram, state encodings, state transition table, output table, next state and output equations and your Finite State Machine schematic.
b) How many flip-flops you need to implement this problem?
c) Implement combinational logic at input (blue block in below Figure) by using multiplexers. Implement combinational logic at output (green block in below Figure) by using decoders. You are allowed only to use inverters out of two blocks where needed.



General Moore state machine (Hoffman model)

Simulation (20 Points)

Enter Systemverilog module to Xilinx Vivado software. Prepare a testbench for it and run it. In the simulation, try all possible variation through SA and SB sensors and observe the LA and LB traffic lights. Call your TA to evaluate your work.

Implementation on FPGA (35 Points)

In this part you are going to implement your code on FPGA and have a demo.

1) Slow down the clock rate to at 3 seconds (0.333 Hz) to see the change in the lights. Remember original frequency of BASYS3's clock is 100 MHz.

Hint: use below template for clock division:

```
always@ (posedge clk) begin
        count <= count + 1;
        if (count==D) //D: last value for counter
                count <= N'd0; //N: length of counter
        if (count==N'd0)
                clk_en <= 1'b1;
        else
                clk_en <= 1'b0;
end

always@ (posedge clk)
if (clk_en==1'b1) begin
        ....
        ....
end
```

2) Use LEDs on BASYS3 board for outputs of LA and LB traffic lights.
   Red: *** (three leds)
   Green: ** (two leds)
   Yellow: * (one led)
3) The SA and SB sensors will be two left most switches. The sensor will be active as long as the switch is set to 1.

Now test your code and show the result to your TA.

Submit your code for MOSS similarity testing

Finally, when you are done and before leaving the lab, you need to upload the file *StudentID_SSystemSystemverilog.txt* created in the Implementation with FPGA part. Be sure that the file contains exactly and only the codes which are specifically detailed above. Don't include the codes which are given to you. If you have multiple files, just copy and paste them in order, one after another inside text file. Check the specifications! Even if you didn't finish, or didn't get the SystemSystemSystemverilog part working, you must submit your code to the Unilica Assignment for similarity checking. Your codes will be compared against all the other codes in all sections of the class, by the MOSS program, to determine how similar it is (as an indication of plagiarism). So be sure that the code you submit is code that you actually wrote yourself! All students must upload their code to the 'Unilica>Assignment' specific for your section. Check submission time and don't miss it before leaving the lab. After taking a backup of your work, don't forget to delete it from computer. Because students of other sections will work with your system too.

Clean Up!

1) Clean up your lab station, and return all the parts, wires, the Beti trainer board, etc. Leave your lab workstation.

2) CONGRATULATIONS! You are finished with this lab and are one step closer to becoming a computer engineer.

NOTES

--Advance work on this lab, and all labs, is strongly suggested.

--Be sure to read and follow the Policies for CS223 labs, posted in Unilica.

LAB POLICIES

1. There are three computers in each row in the lab. Don't use middle computers, unless you are allowed by lab supervisor.
2. You borrow a Lab-board containing the development board, connectors, etc. in the beginning. The lab supervisor takes your signature. When you are done, return it to her, otherwise you will be responsible and lose points.
3. Each Lab-board has a number. You must always use the same trainer board pack throughout the semester.
4. You must be in the lab, working on the lab, from the time lab starts until you finish and leave. (Bathroom and snack breaks are the exception to this rule). Absence from the lab, at any time, is counted as absence from the whole lab that day.
5. No cell phone usage during lab. Tell friends not to call during the lab hours--you are busy learning how digital circuits work !.
6. Internet usage is permitted only to lab-related technical sites. No Facebook, Twitter, email, news, video games, etc--you are busy learning how digital circuits work !.
7. If you come to lab later than 20 minutes, you will loose that session completely.
8. When you are done, DO NOT return IC parts into the IC boxes, where you've taken them first. Just put them inside your lab pack box. Lab coordinator will check and return them later.