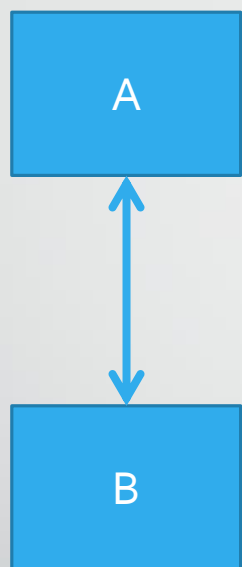


Performance Analysis of a PDEVs Simulator Supporting Multiple Synchronization Protocols

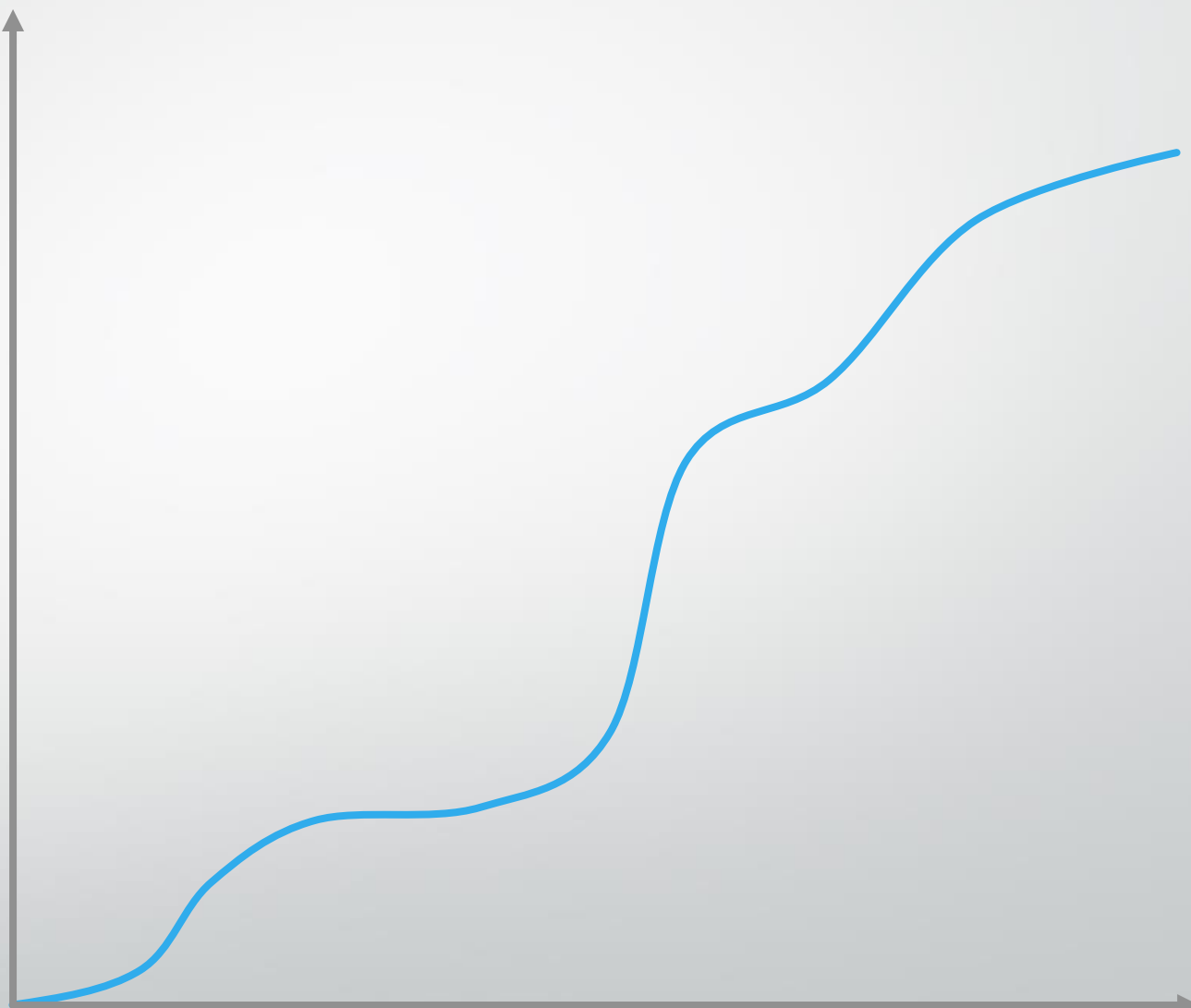
Ben Cardoen, Stijn Manhaeve, Tim Tuijn

Yentl Van Tendeloo, Kurt Vanmechelen,
Hans Vangheluwe, Jan Broeckhove

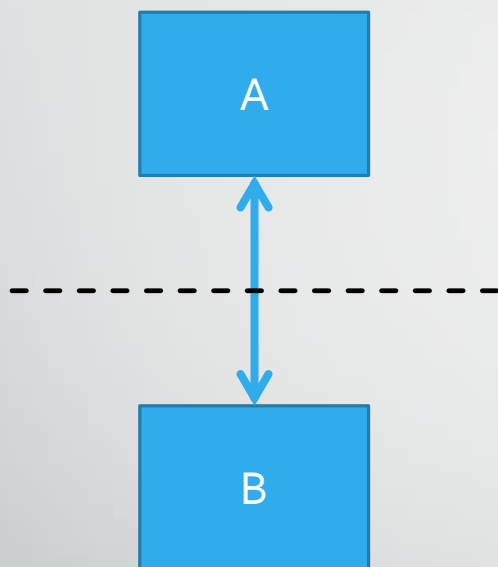




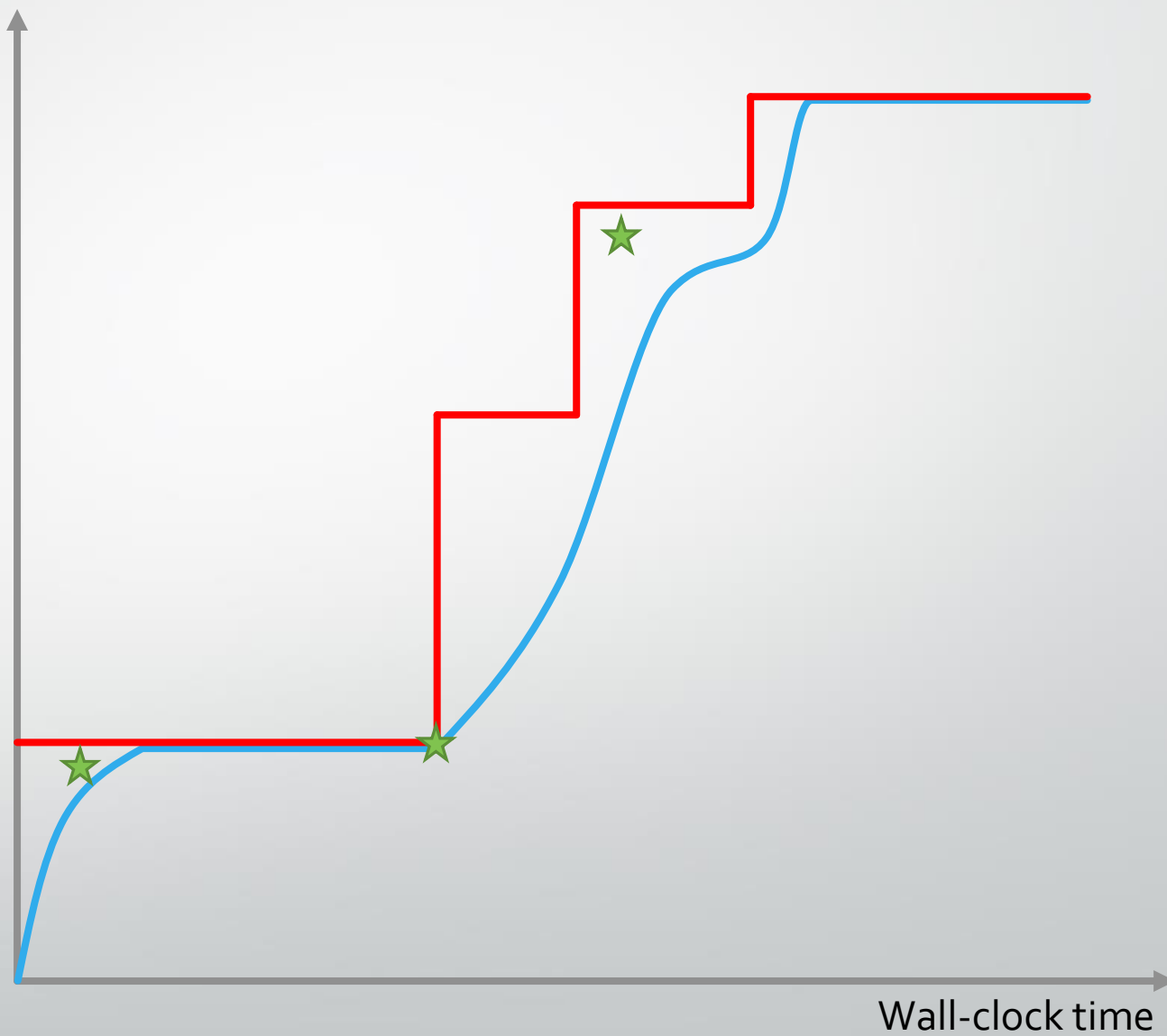
Simulated time

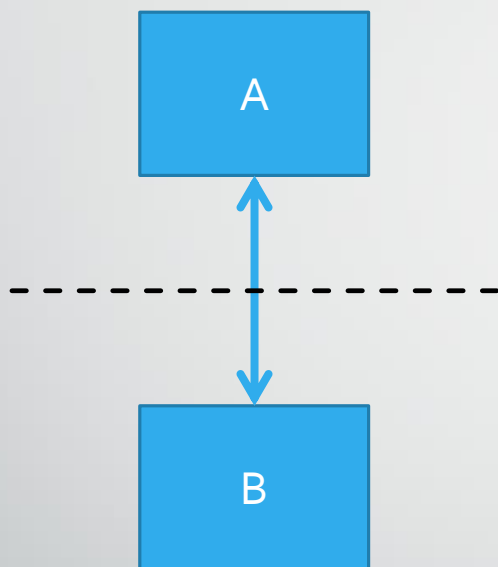


Wall-clock time

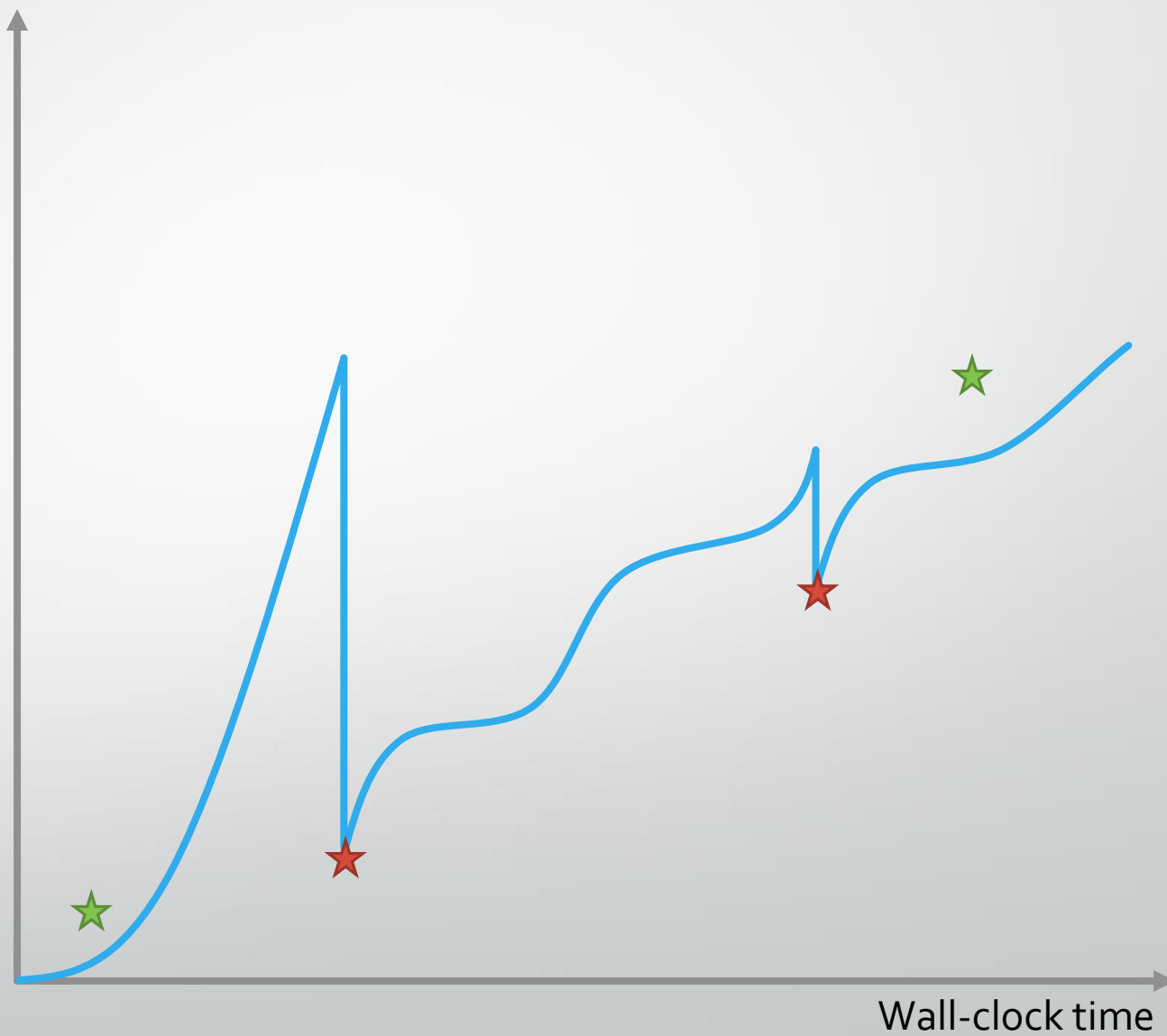


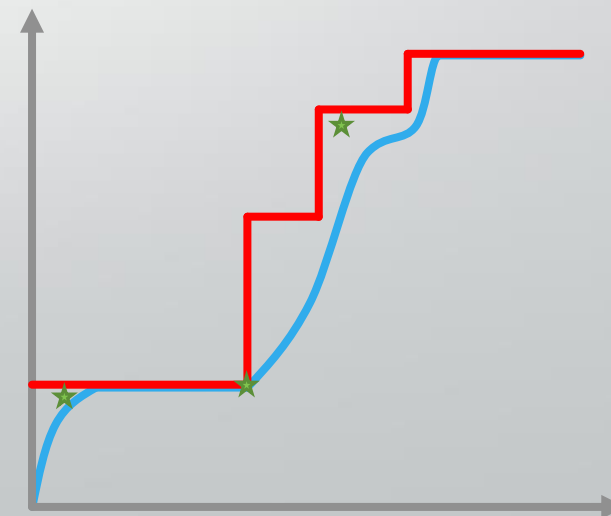
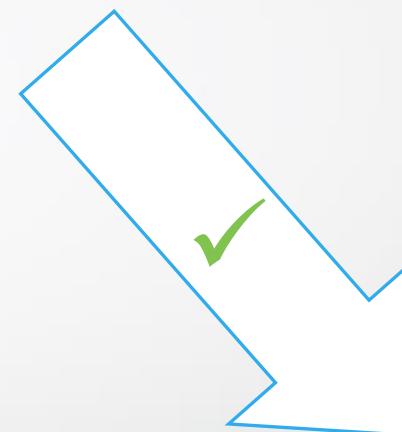
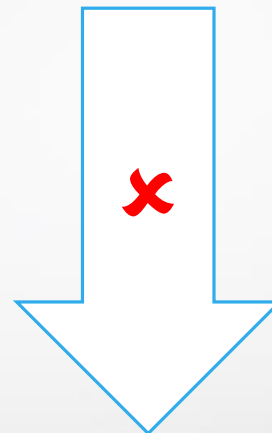
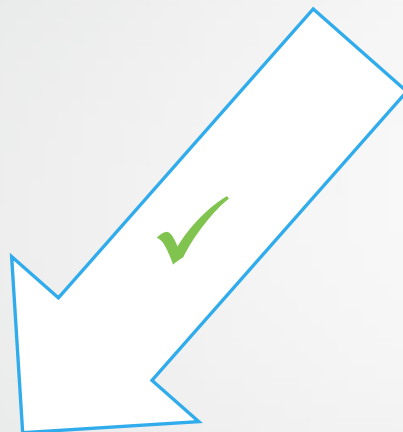
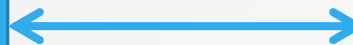
Simulated time @ A





Simulated time @ A







Kernel

Sequential

Conservative

Optimistic

...



km/h

40

60

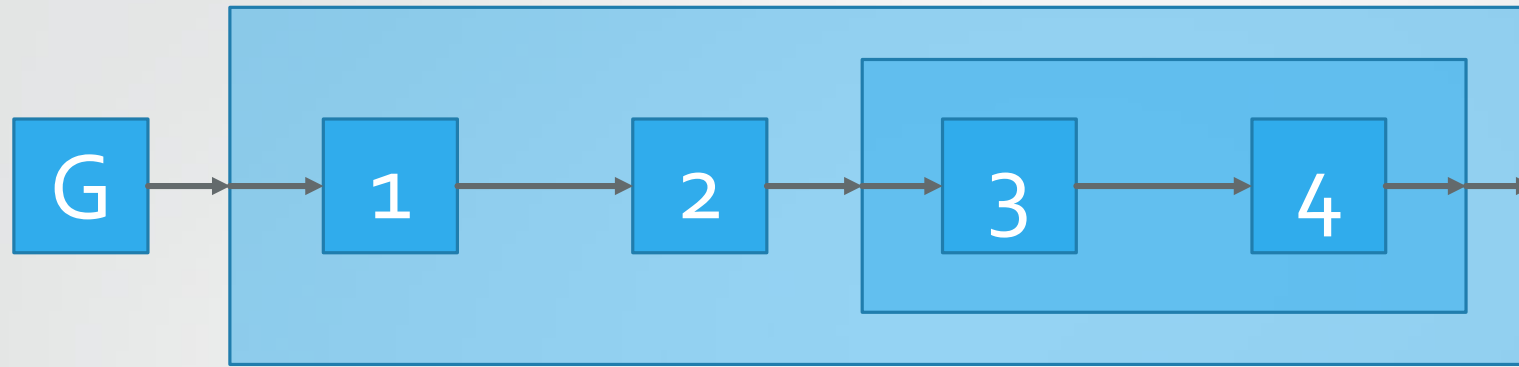
80

100

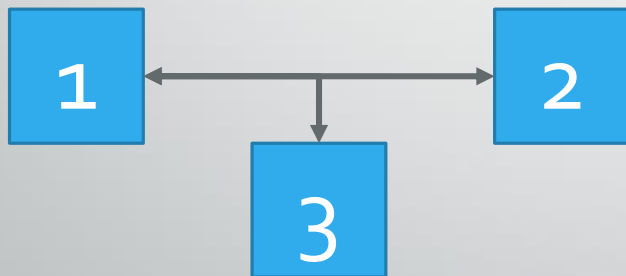
120

140

Queue



Interconnect



PHOLD



