UF Herbert Wertheim College of Engineering
UNIVERSITY *of* FLORIDA

POWERING THE NEW ENGINEER TO TRANSFORM THE FUTURE

Department of Electrical & Computer Engineering

Digital Logic And Computing Systems

Chapter 02 – Logic Gates

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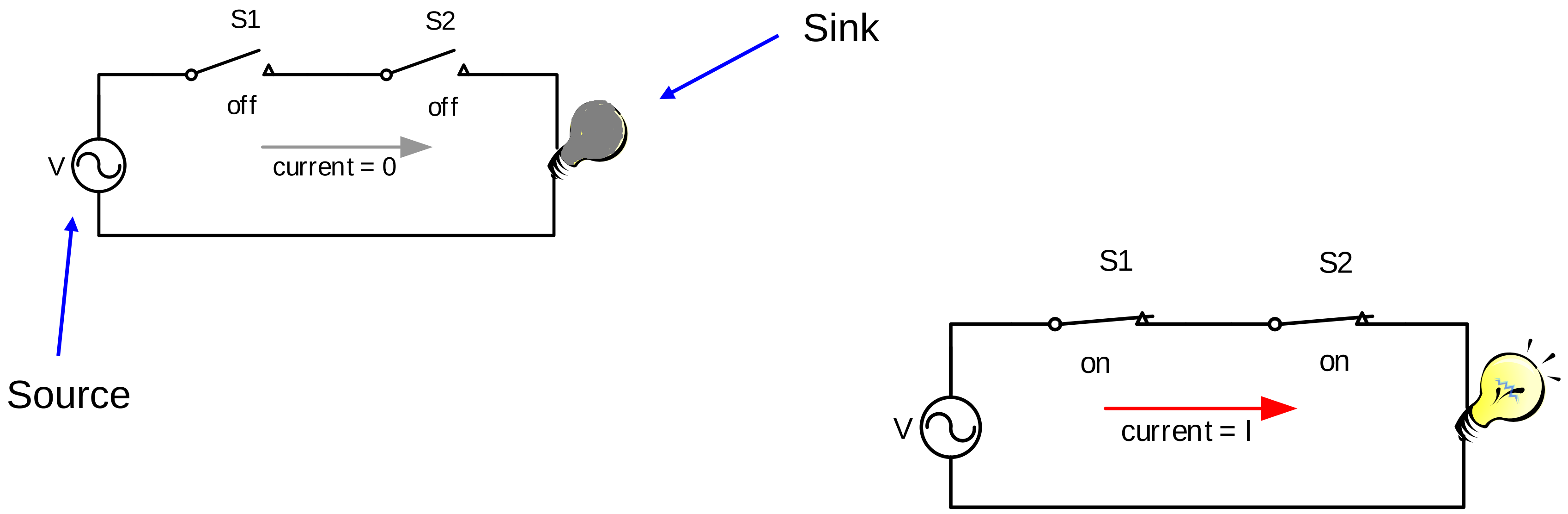
Agenda

- Basic Gates
- Gate composition
- Possible combinations
- Gates with multiple input

Basic Gate - Switch

- Switches are basic components used to model digital systems
  - Two possible states: {open, closed} resp. {off, on} resp. {0,1}, {L,H}, {0V,5V}

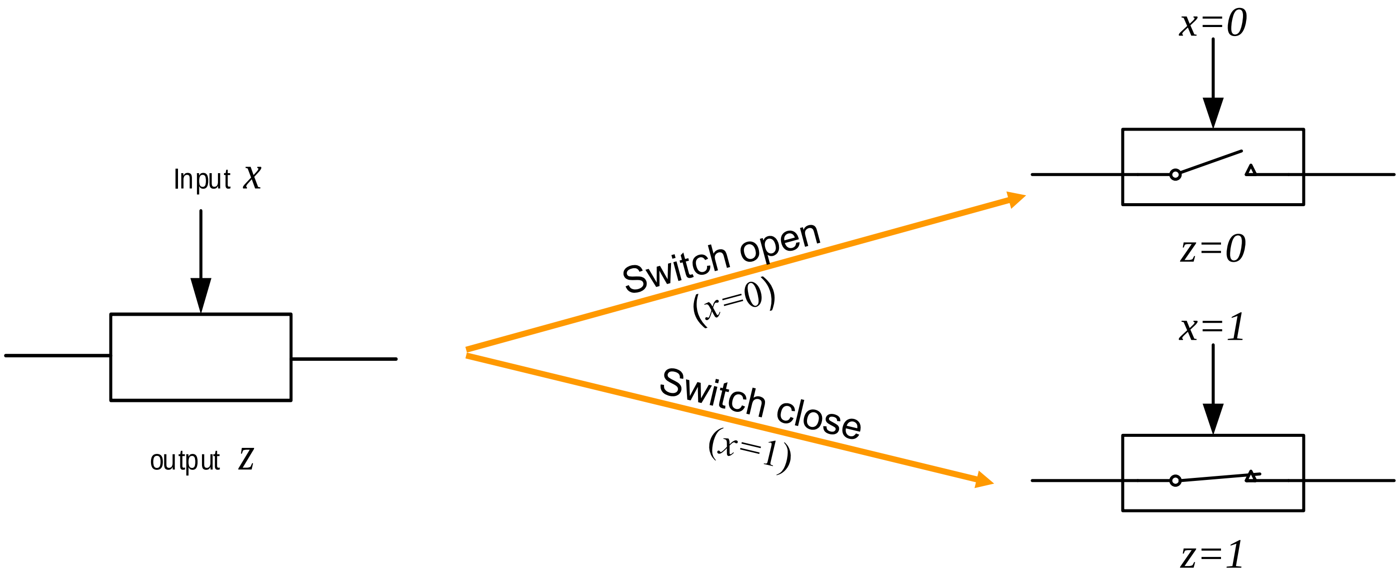


Sink

Source

Basic Gates – Switch

- Modelling ideal switches
  - Abstraction: X, Z in $\{0,1\}$
  - Quality (ideal) of switches depends on the technology



Basic Gates – AND

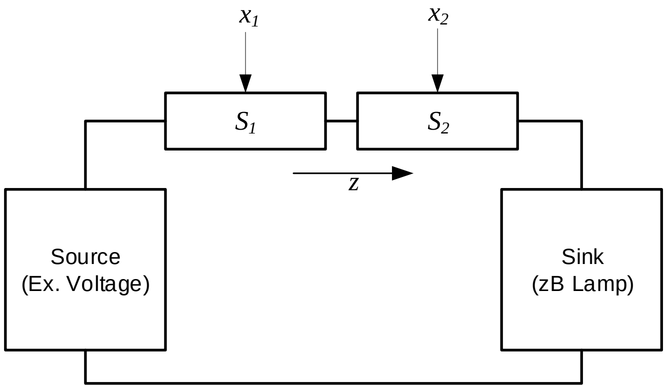
- "If the weather is nice tomorrow and my brother is available, then we will go swimming"
- We will go swimming (z) corresponds to logical conjunction (AND-operation) of
  - X_1 = the weather is nice tomorrow and
  - X_2 = my brother is available
- AND-Truth table

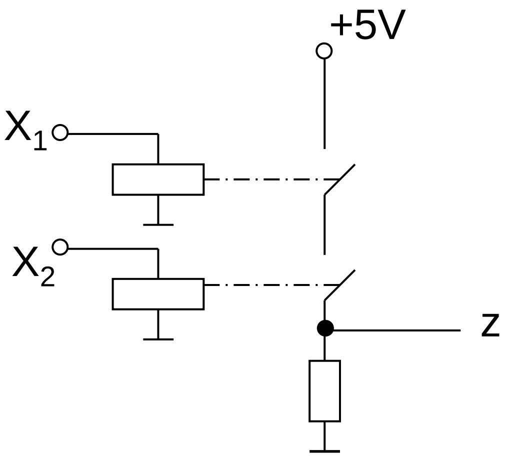
x_1	x_2	z
0	0	0
0	1	0
1	0	0
1	1	1

- AND-Gates are circuit components that implement AND-operations

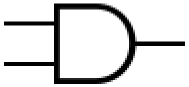
Basic Gates – AND

- Representation: series

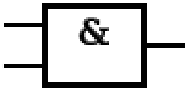




- Notation and Symbol
  - Switch (Boolean) algebra: $Z = X_1 \cdot X_2 = X_1 \wedge X_2 = X_1 \& X_2$



American National Sandard Institute (ANSI)



International Electronic Comission (IEC)

Basic Gates – OR

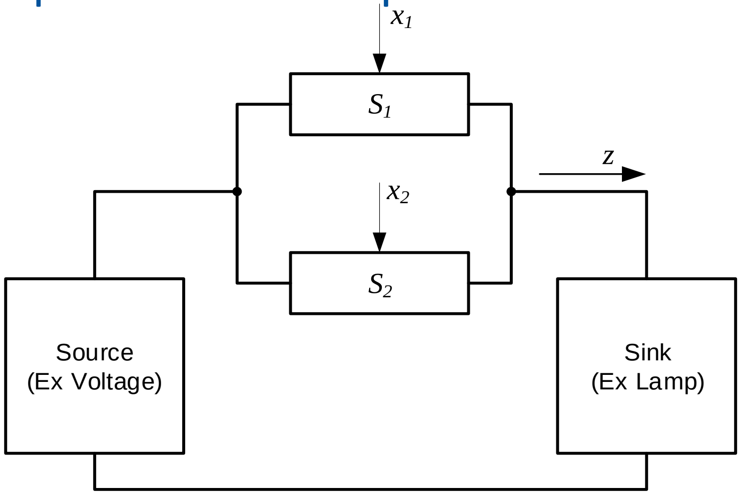
- "Our party will be successful if many girls attend, or the DJ does a good job".
- Our party will be successful (Z) corresponds to a logical disjunction (OR-operation) of
  - X_1 = many girls attend our party and
  - X_2 = the DJ does a good job
- Truth table

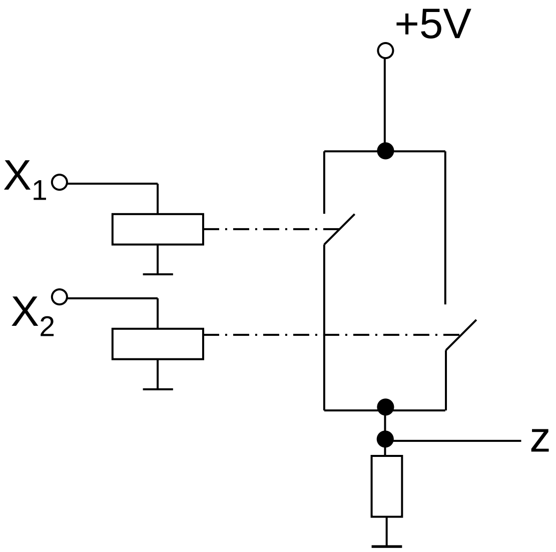
x_1	x_2	z
0	0	0
0	1	1
1	0	1
1	1	1

- OR-Gates are circuit elements that implement OR-operations

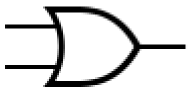
Basic Gates – OR

- Representation as parallels





- Notation and Symbol:
  - Switch (Boolean) algebra: $Z = X_1 + X_2 = X_1 \vee X_2$



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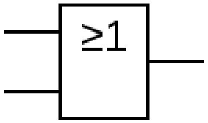


IEC

Basic Gates – NOT

- "If my mother visits today, then I will not go out".
  - Going out (z) is the negation (NOT-relation) of

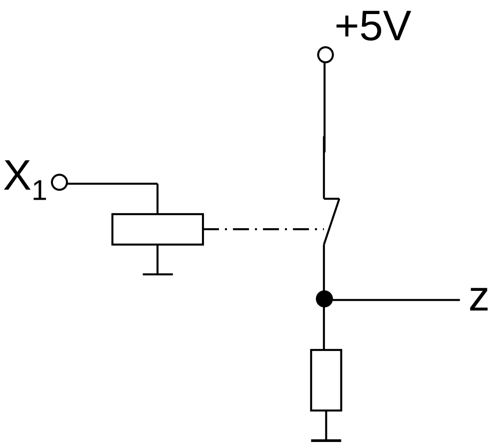
  X_1 = My mother visits today

- NOT Truth table

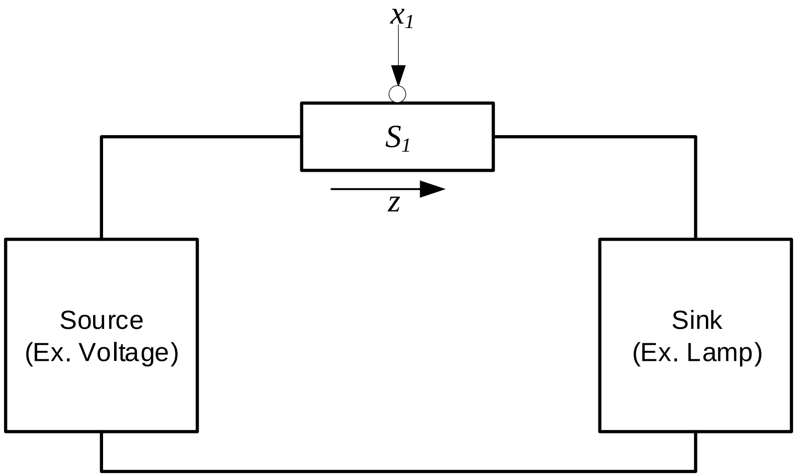
x_1	z
0	1
1	0

- A NOT-Gate is a circuit that implements the NOT-operation

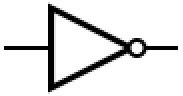
Basic Gates – NOT

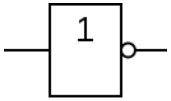


- Representation



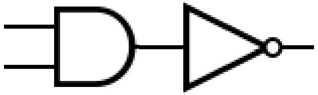
- Notation and Symbol:
  - Switch (Boolean)algebra: $Z = \neg X = \overline{X}$





Gate Composition – NAND

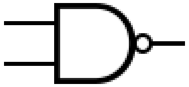
- A NAND-Gate can be built as serial composition of an AND-Gate and a NOR-gate



- Truth table

x_1	x_2	x	z
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

- Symbol:
  - Switch (Boolean) algebra: $Z = \overline{X_1 \wedge X_2}$
  - The bubble indicates a NOT



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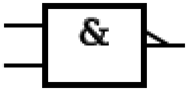

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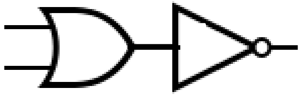
Gate Composition – NOR

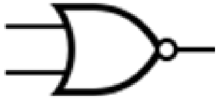
- A NOR-Gate can be built as serial composition of an OR-Gate and a NOT-gate



- Truth table

x_1	x_2	x	z
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

- Symbol:
  - Switch (Boolean) algebra: $Z = \overline{X_1 \vee X_2}$



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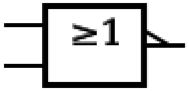

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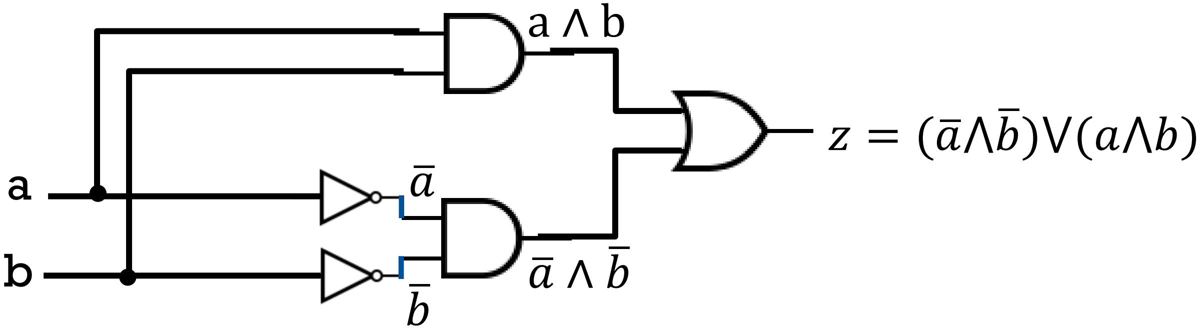
Gate Composition – XNOR

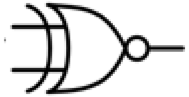
- XNOR-Gate (equivalence) has output 1 if and only if the two inputs are equal
- Construction



- Truth table

a	b	$\bar{a}$	$\bar{b}$	$a \land b$	$\bar{a} \land \bar{b}$	z
0	0	1	1	0	1	1
0	1	1	0	0	0	0
1	0	0	1	0	0	0
1	1	0	0	1	0	1

Symbol:



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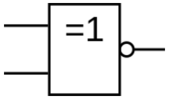

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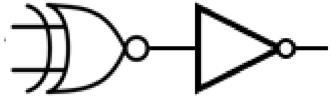
Gate Composition – XOR

- A XOR-Gate (Exclusive OR) has output 1 if and only if the two inputs are different

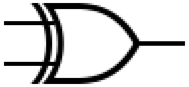


- XOR can be built as serial composition of XNOR and NOT gates

- Truth table

x_1	x_2	z
0	0	0
0	1	1
1	0	1
1	1	0

Symbol:



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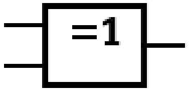

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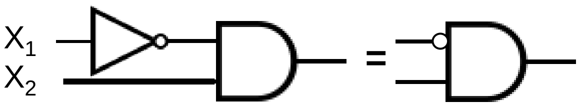
Possible Combinations

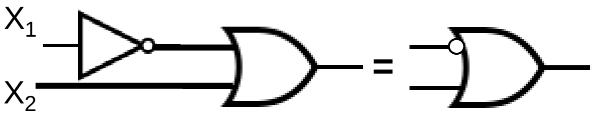
- 16 possible 2-input functions
  - In general, with n-input:
    - 2^n possible result values for 1 functions
    - 2^{2^n} possible functions

x_1	x_2	z_1	z_2	z_2	z_2	z_5	z_2	z_7	z_8	z_2	z_{10}	z_{11}	z_{12}	z_{13}	z_{14}	z_{15}	z_{16}
0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
1	0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
		Constant 0	NOR	Inhibition x_1	Negation x_1	Inhibition x_2	Negation x_2	XOR	NAND	AND	XNOR	Identity x_2	Implication x_1	Identity x_1	implication x_2	OR	constant 1

Inhibition x_1 =

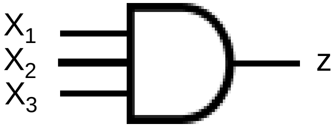


Implication x_1 =



Gates with more than 2 inputs

- Gates with more than 3 inputs can be implemented as combination of 2-input gates
- for 3 inputs $x_1, x_2, x_3,$ all 4 cases of x_1, x_2 can be combined with $x_3 = 0$ and with $x_3 = 1$ → 8 cases (ie. Z = $(X_1 \cdot X_2) \cdot X_3$)
- Example: $Z = X_1 \wedge X_2 \wedge X_3$



x_3	x_1	x_2	z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

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