Digital Logic and Computer Systems

EEL 3701C

Midterm Exam

Monday, February 24th, 2020

08:20 PM – 10:20 PM

Name: _____

Student ID: _____

Problem 1	Problem 2	Problem 3	Total
/24	/20	/09	/53, %

Problem #1 (General Understanding, 24 pts)

1) Why are binary systems preferred to ternary (base-3) despite their optimality? **(1 pts)**

Binary is easy to realize

2) Name 1 universal gate and explain why it is considered such. Feel free to use Boolean algebra and/or circuit designs in your answer. **(2 pt)**

- NAND and NOR gates are universal. Every sum of product can be realized only with NAND or only with NOR.

3) In Computing and communication systems, it is often the case that a value stored or transmitted is not the same as the value retrieved or received later.

   1) Explain the potential causes? **(1 pts)**

- Noises, signal interference, damage on device

   2) Explain an approach to detect cases of fault in such systems **(2 pts)**

- Fault-tolerant implementation. For instance using parity bit appended on a word to detect if a bit error has occurred.

4) Explain the difference between a flip flop (FF) and a latch (**1 pts)**

Fliflops react to the edge of the clock. Latches react to the level of the control signal.

Fliflops are edge-triggered while latches are level-triggered.

5) Why is (S=1, R=1) an invalid input for an SR-FF **(1 pts)**?

When s=1 and r=1 and the output was previously (0,0) the next state is undefined

6) The following character sequence must be transmitted over a communication line: **DiGiTal**. Using **even** block parity, show the bit sequence that must be transmitted to detect and correct single-bit errors **(6 pts)**?

D = 44 = 0100 0100, i = 69 = 0110 1001, G = 47 = 0100 0111, T = 54 = 0101 0100, a = 61 = 0110 0001, l = 6C = 0110 1100

Block encoding, even parity

0100 0100 0
0110 1001 0
0100 0111 0
0110 1001 0
0101 0100 1
0110 0001 1
0110 1100 0
0101 1010 Checksum

Or

00000000 Checksum
11111111
01010110
00001001
01010011
10101010
00100001
01110100
0000110

Do the following operation in binary 14.37 - 17.15 **(4 pts)**

Binary of 14 is 1110

Binary of 0.37: 010111

0.37 × 2 = 0 + 0.74
0.74 × 2 = 1 + 0.48
0.48 × 2 = 0 + 0.96
0.96 × 2 = 1 + 0.92
0.92 × 2 = 1 + 0.84
0.84 × 2 = 1 + 0.68
0.68 × 2 = 1 + 0.36
0.36 × 2 = 0 + 0.72
0.72 × 2 = 1 + 0.44

Binary of 14.37 is 001110.010111

Binary of 17 is 10001 and Binary of 0.15 is 0.001

0.15x2 = 0 + 0.3
0.3 x 2 = 0 + 0.6
0.6 x 2 = 1 + 0.2
0.2 x 2 = 0 + 0.4
0.4 x 2 = 0 + 0.8
0.8 x 2 = 1 + 0.6
0.6 x 2 = 1 + 0.2
0.2 x 2 = 0 + 0.4
0.4 x 2 = 0 + 0.8

Binary of 17.15 is 010001.001001
And the 2's complement is 101110.110111

Now, 001110.010111 + 101110.110111 = **111101. 001110**
Decimal of 111101. 001110 is - 2^5 + 2^4 + 2^3 + 2^2 + 2^0 + 2^(-3) + 2^(-4) + 2^(-5)
= **-**32 + 16 + 8 + 4 + 1 + 0.125 + 0.0625 + 0.03125 = **-2.78**

7) Draw the circuit represented by the following VHDL statements **(2 pts)**

T1 <= not A and not B and C0;

T2 <= not A and B and C1;

T3 <= A and not B and C2;

T4 <= A and B and C3;

F <= T1 or T2 or T3 or T4;

8) Draw the circuit represented by the following VHDL statements **(2 pts)**

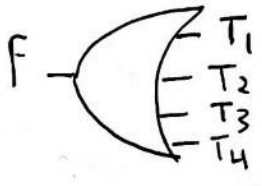
T1 <= not A and not B and C0;

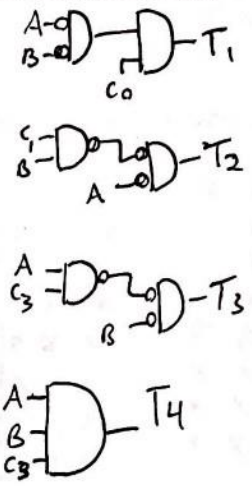
T2 <= not A and B and C1;

T3 <= A and not B and C2;

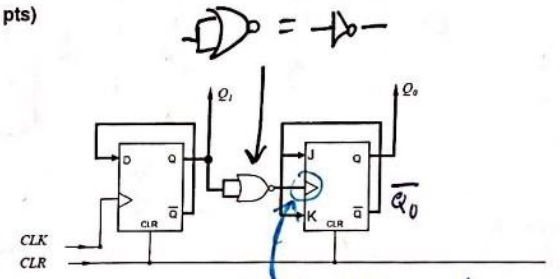
T4 <= A and B and C3;

F <= T1 or T2 or T3 or T4;

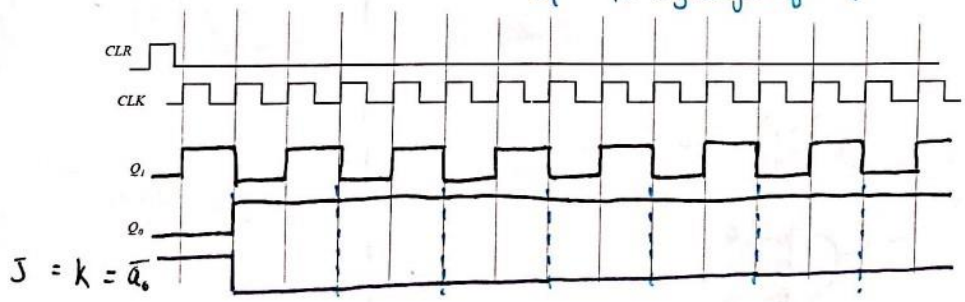




9) Given is the following serially connected **D-FF** and **JK-FF**. Complete the timing diagram of the figure below **(4 pts)**



$\overline{Q_1}$ ∴ falling edge of Q_1



∴ J = k = 1

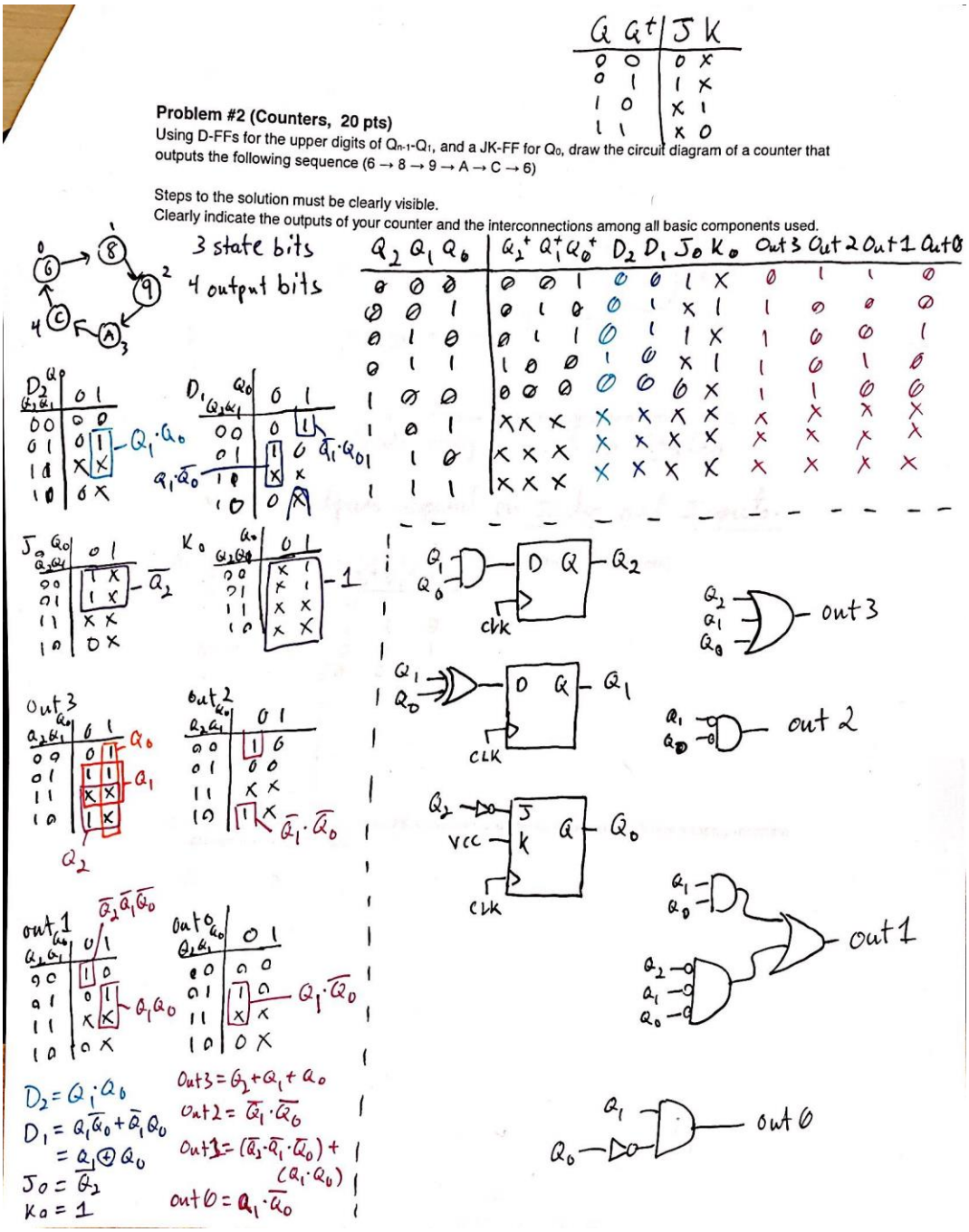
or J = k = ∅

J	K	Q	Q+	
0	∅	0	0	
∅	0	1	1	all other edges
1	1	0	1	1st edge
1	1	1	0	

Problem #2 (Counters, 20 pts)

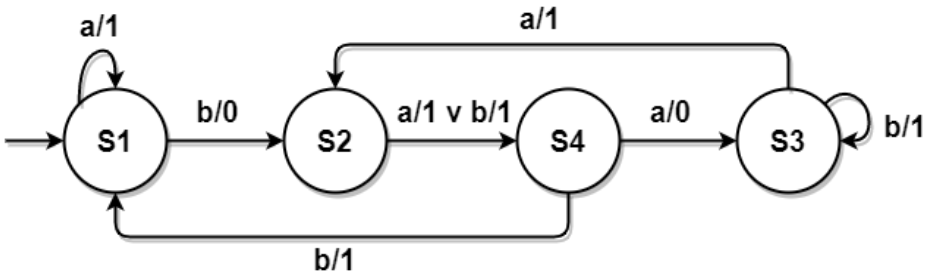
Using D-FFs for the upper digits of Q_{n-1}-Q_1, and a JK-FF for Q_0, draw the circuit diagram of a counter that outputs the following sequence (6 → 8 → 9 → A → C → 6)

Steps to the solution must be clearly visible.
Clearly indicate the outputs of your counter and the interconnections among all basic components used.



Problem #3 (Automata and Control Path, 9 pts)
Use the following diagram for **a-d**

a) What is the main difference between Moore and Mealy finite state machines? **(1 pt)**



b) Is the following automaton a Moore or Mealy ? Explain. **(1 pt)**
c) Draw the state transition table of the automata **(2 pts)**
d) Convert the automaton into an equivalent Moore machine **(5 pts)**

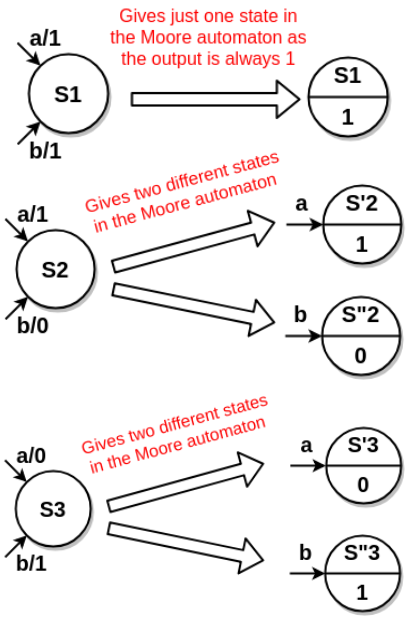
Solution:

a) The main difference resides in that in Moore finite state machines, the output depends only on the current state, while with Mealy, the output depends both on the current state and current inputs.
b) Mealy automaton
c) Here is the transition table:

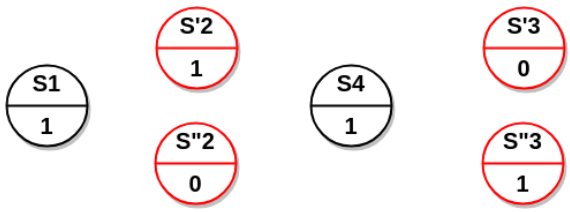
δ/λ	**a**	**b**
S_I**= S1**	S1/1	S2/0
S2	S4/1	S4/1
S3	S2/1	S3/1
S4	S3/0	S1/1

d) Let us convert the automaton into an equivalent Moore machine.

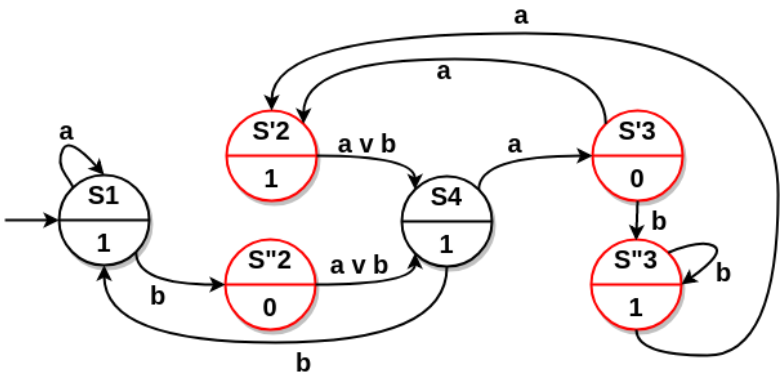
We start by identifying the states from the automaton with more than one incident edge in order to check if new states will be inserted. The following images summarize the findings:



S1 and S3 generate each 2 new states. Now we have the following states:



The corresponding Moore automaton is therefore:



ASCII Translation Table

Dec	Bin	Hex	Char	Dec	Bin	Hex	Char	Dec	Bin	Hex	Char	Dec	Bin	Hex	Char
0	0000 0000	00	[NUL]	32	0010 0000	20	space	64	0100 0000	40	@	96	0110 0000	60	`
1	0000 0001	01	[SOH]	33	0010 0001	21	!	65	0100 0001	41	A	97	0110 0001	61	a
2	0000 0010	02	[STX]	34	0010 0010	22	"	66	0100 0010	42	B	98	0110 0010	62	b
3	0000 0011	03	[ETX]	35	0010 0011	23	#	67	0100 0011	43	C	99	0110 0011	63	c
4	0000 0100	04	[EOT]	36	0010 0100	24	$	68	0100 0100	44	D	100	0110 0100	64	d
5	0000 0101	05	[ENQ]	37	0010 0101	25	%	69	0100 0101	45	E	101	0110 0101	65	e
6	0000 0110	06	[ACK]	38	0010 0110	26	&	70	0100 0110	46	F	102	0110 0110	66	f
7	0000 0111	07	[BEL]	39	0010 0111	27	'	71	0100 0111	47	G	103	0110 0111	67	g
8	0000 1000	08	[BS]	40	0010 1000	28	(	72	0100 1000	48	H	104	0110 1000	68	h
9	0000 1001	09	[TAB]	41	0010 1001	29	)	73	0100 1001	49	I	105	0110 1001	69	i
10	0000 1010	0A	[LF]	42	0010 1010	2A	*	74	0100 1010	4A	J	106	0110 1010	6A	j
11	0000 1011	0B	[VT]	43	0010 1011	2B	+	75	0100 1011	4B	K	107	0110 1011	6B	k
12	0000 1100	0C	[FF]	44	0010 1100	2C	,	76	0100 1100	4C	L	108	0110 1100	6C	l
13	0000 1101	0D	[CR]	45	0010 1101	2D	-	77	0100 1101	4D	M	109	0110 1101	6D	m
14	0000 1110	0E	[SO]	46	0010 1110	2E	.	78	0100 1110	4E	N	110	0110 1110	6E	n
15	0000 1111	0F	[SI]	47	0010 1111	2F	/	79	0100 1111	4F	O	111	0110 1111	6F	o
16	0001 0000	10	[DLE]	48	0011 0000	30	0	80	0101 0000	50	P	112	0111 0000	70	p
17	0001 0001	11	[DC1]	49	0011 0001	31	1	81	0101 0001	51	Q	113	0111 0001	71	q
18	0001 0010	12	[DC2]	50	0011 0010	32	2	82	0101 0010	52	R	114	0111 0010	72	r
19	0001 0011	13	[DC3]	51	0011 0011	33	3	83	0101 0011	53	S	115	0111 0011	73	s
20	0001 0100	14	[DC4]	52	0011 0100	34	4	84	0101 0100	54	T	116	0111 0100	74	t
21	0001 0101	15	[NAK]	53	0011 0101	35	5	85	0101 0101	55	U	117	0111 0101	75	u
22	0001 0110	16	[SYN]	54	0011 0110	36	6	86	0101 0110	56	V	118	0111 0110	76	v
23	0001 0111	17	[ETB]	55	0011 0111	37	7	87	0101 0111	57	W	119	0111 0111	77	w
24	0001 1000	18	[CAN]	56	0011 1000	38	8	88	0101 1000	58	X	120	0111 1000	78	x
25	0001 1001	19	[EM]	57	0011 1001	39	9	89	0101 1001	59	Y	121	0111 1001	79	y
26	0001 1010	1A	[SUB]	58	0011 1010	3A	:	90	0101 1010	5A	Z	122	0111 1010	7A	z
27	0001 1011	1B	[ESC]	59	0011 1011	3B	;	91	0101 1011	5B	[	123	0111 1011	7B	{
28	0001 1100	1C	[FS]	60	0011 1100	3C	<	92	0101 1100	5C	\	124	0111 1100	7C	|
29	0001 1101	1D	[GS]	61	0011 1101	3D	=	93	0101 1101	5D	]	125	0111 1101	7D	}
30	0001 1110	1E	[RS]	62	0011 1110	3E	>	94	0101 1110	5E	^	126	0111 1110	7E	~
31	0001 1111	1F	[US]	63	0011 1111	3F	?	95	0101 1111	5F	_	127	0111 1111	7F	[DEL]