Introduction to performance modeling

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SURF

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UNIVERSITY OF TWENTE.

東京工業大学
Tokyo Institute of Technology

Performance modeling

is the process of building analytical or empirical models to predict and quantify the behavior of applications on HPC systems.

- Aims to identify performance bottlenecks and optimize resource utilization.
- Enables understanding of the impact of system configuration and parameters on application performance.
- Facilitates design decisions for system upgrades or new architecture choices.

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Approaches for performance modeling

- Analytical modeling uses mathematical equations to represent the performance characteristics.
- Empirical modeling uses historical data or benchmarking to build models based on observed behavior.

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Challenges in performance modeling

- Heterogeneous architectures and complex interactions between hardware and software components.
- Scalability issues when modeling large-scale systems with millions of concurrent processes.
- Accuracy and validation of models against empirical performance measurements.
- Model portability across different platforms and architectures.

Exploring HPC through vehicle analogies

Sports car

Family van

Transport truck

Sports car

- Power: $400\,\mathrm{hp}$.
- Passengers: $2\,\mathrm{pax}$.

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Application A

To deliver the maximum power possible.

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Application B

To win a speed race on a racing circuit.

Sports car

- Power: $400\,\mathrm{hp}$.
- Passengers: $2\,\mathrm{pax}$.
- Capacity: $0.5\,\mathrm{m}^3$.
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Family van

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Transport truck

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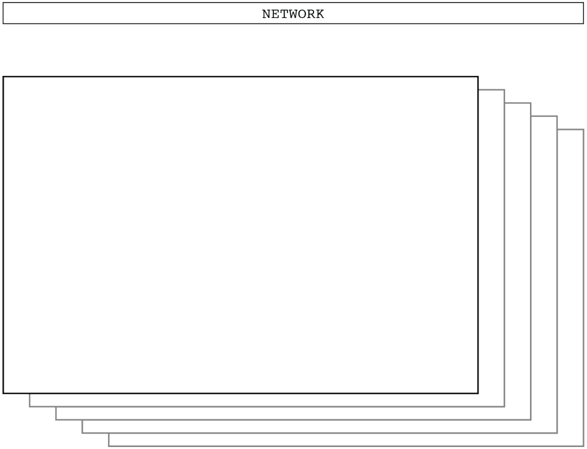
- Speed: $150\,\mathrm{m}/2$.

Application C

To travel from point A to B with 5 passengers.

Hybrid HPC systems

Modern HPC systems consist of multiple hybrid computing nodes interconnected via a communication infrastructure. The nodes are composed of many hardware devices of different architectures, such as central processing unit (CPU) or graphics processing unit (GPU), among others.



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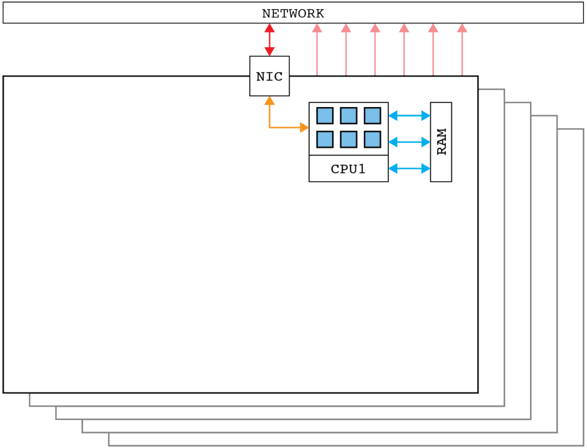

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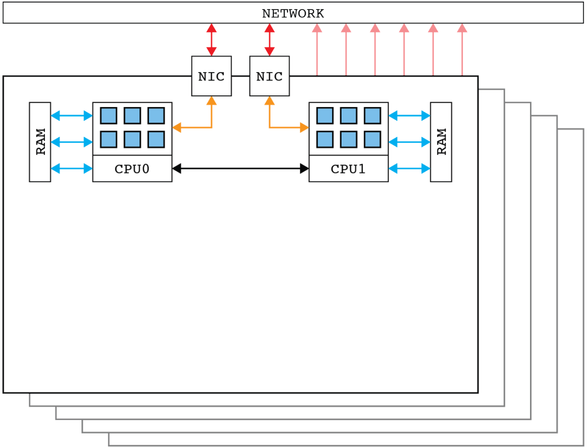

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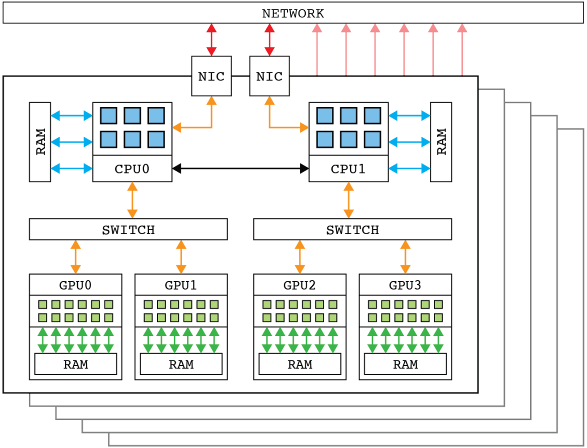
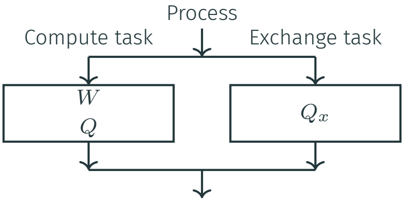


Abstract machine model

Consider computing kernels that perform a vast number of independent operations and memory requests which can be pipelined and parallelized. Distributed-memory parallelization requires large, non-blocking point-to-point messages between subsets of parallel processes that can overlap with bulk computations.



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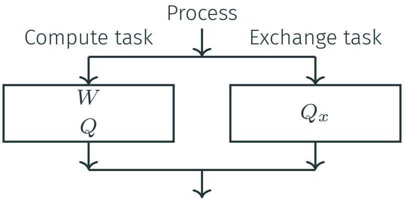

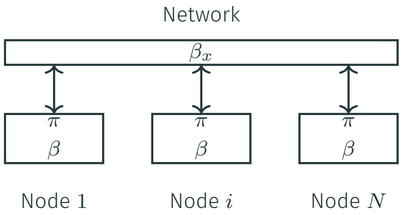

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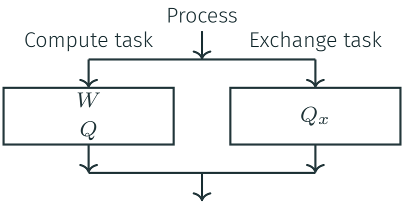

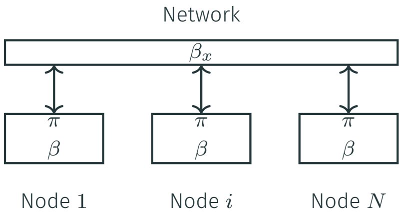

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W	flop	Number of operations
Q	byte	Main memory traffic
Q_x	byte	Network traffic

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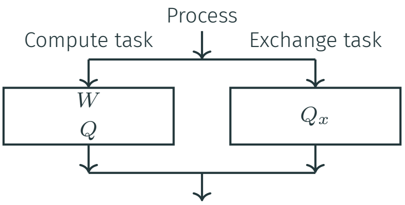

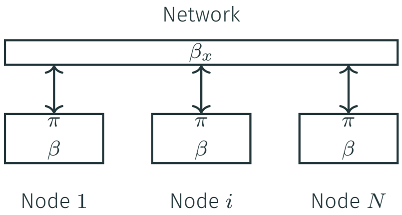

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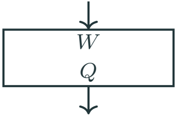
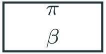
Compute task



Node



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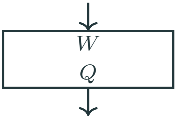

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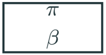

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axpy

The axpy kernel performing the linear combination of two vectors reads:

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where α is a constant, and $\boldsymbol{x}$ and $\boldsymbol{y}$ are two vectors of size n. In such an operation, the processor performs:

- Work (W): n additions and n multiplications, that is, $2n$ floating-point operations.
- Memory traffic (Q): $2n$ elements read and n written, that is, $3n \cdot 8\,\mathrm{bytes}$ in double precision.

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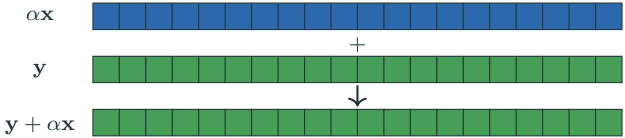

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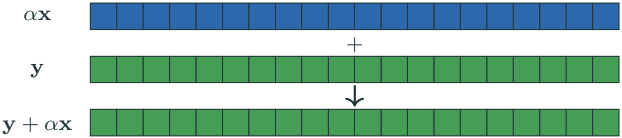

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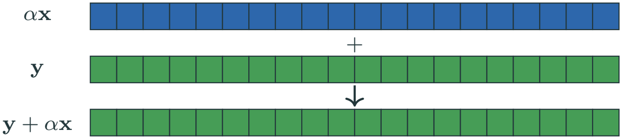

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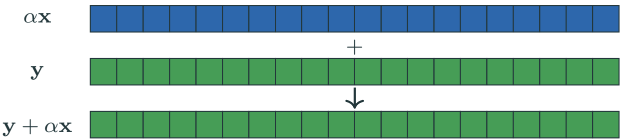

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The time required to execute the kernel:

$$t = max(t^W, t^Q) = max(\frac{2n}{\pi}, \frac{3n \cdot 8}{\beta}).$$

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- Work (W): $mn(k+3)$ additions and multiplications, that is, approximately, $2mnk$ floating-point operations.
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The time required to read and write the data is:

$$t^Q = \frac{Q}{\beta} = \frac{8(mk + kn + 2mn)}{\beta}.$$

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The time required to execute the kernel:

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The roofline model

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Application performance is often considered more relevant than elapsed time itself. Let's divide the work W by t^{RL}:

$$R^{RL} = \frac{W}{t^{RL}} = min\left(\pi, \frac{W}{Q}\beta\right) = min(\pi, I\beta).$$

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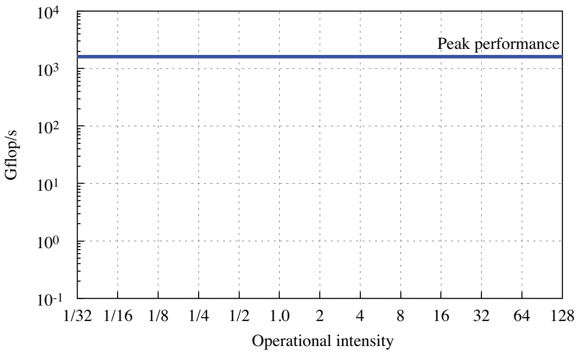

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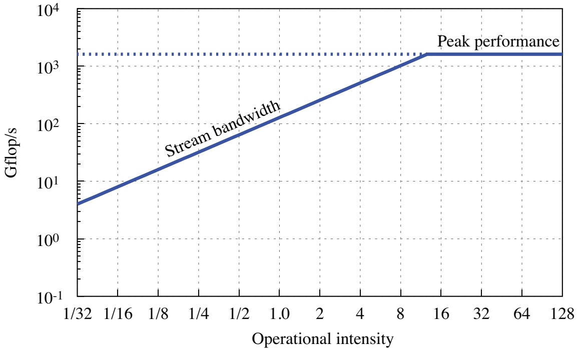

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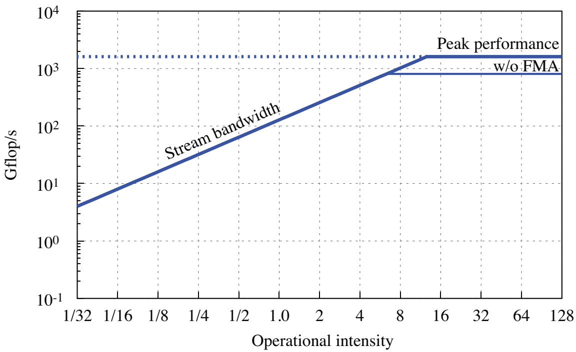

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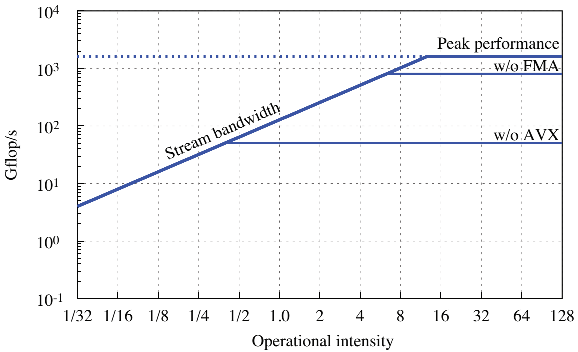

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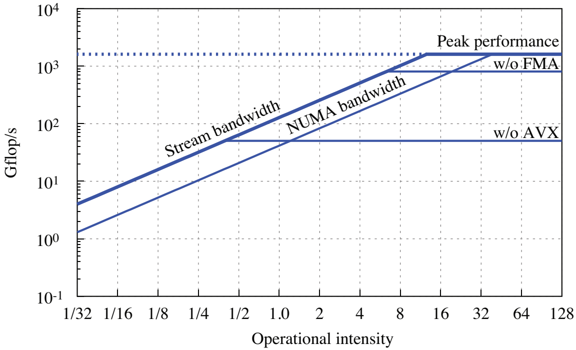

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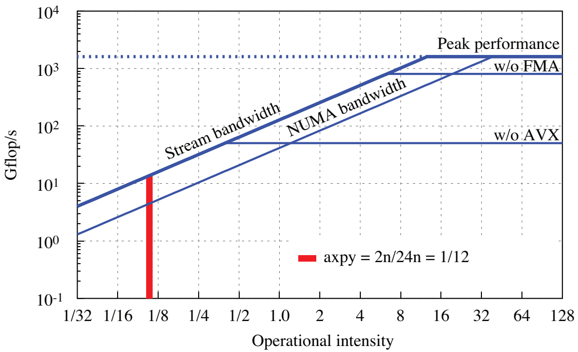

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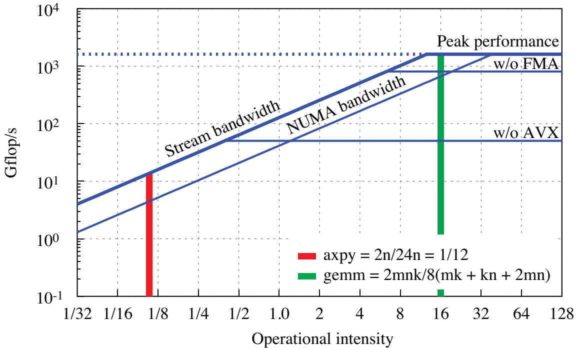

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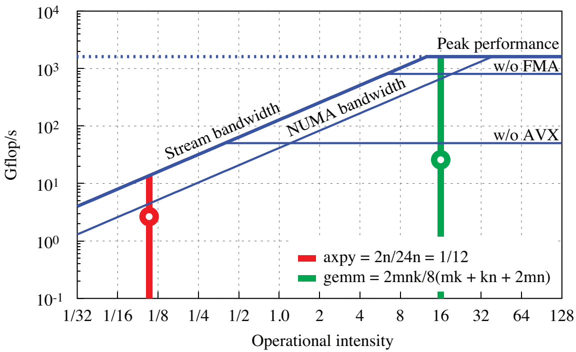

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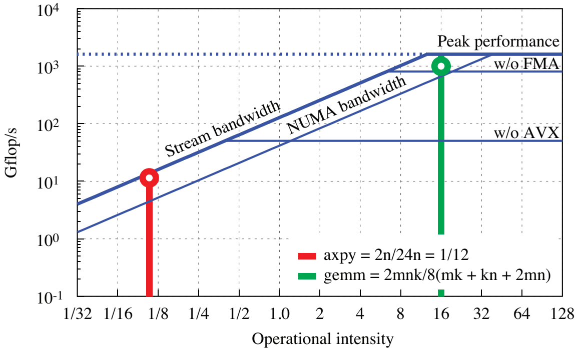

HPCG benchmark, November 2022

Rank	Site	Computer	Cores	HPL Rmax (Pflop/s)	TOP500 Rank	HPCG (Pflop/s)	Fraction of Peak
1	RIKEN Center for Computational Science **Japan**	**Supercomputer Fugaku** — A64FX 48C 2.2GHz, Tofu interconnect D	7,630,848	442.01	2	16.00	3.0%
2	DOE/SC/Oak Ridge National Laboratory **United States**	**Frontier** — AMD Optimized 3rd Generation EPYC 64C 2GHz, Slingshot-11, AMD Instinct MI250X	8,730,112	1102.00	1	14.05	0.8%
3	EuroHPC/CSC **Finland**	**LUMI** — AMD Optimized 3rd Generation EPYC 64C 2GHz, Slingshot-11, AMD Instinct MI250X	2,220,288	309.10	3	3.408	0.8%
4	DOE/SC/Oak Ridge National Laboratory **United States**	**Summit** — IBM POWER9 22C 3.07GHz, Dual-rail Mellanox EDR Infiniband, NVIDIA Volta GV100	2,414,592	148.60	5	2.926	1.5%
5	EuroHPC/CINECA **Italy**	**Leonardo** — Xeon Platinum 8358 32C 2.6GHz, Quad-rail NVIDIA HDR100 Infiniband, NVIDIA A100 SXM4 64 GB	1,463,616	174.70	4	2.567	1.0%

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- Identify parallelism, optimize resource utilization, and improve system efficiency through performance modeling.

Thank you for your attention