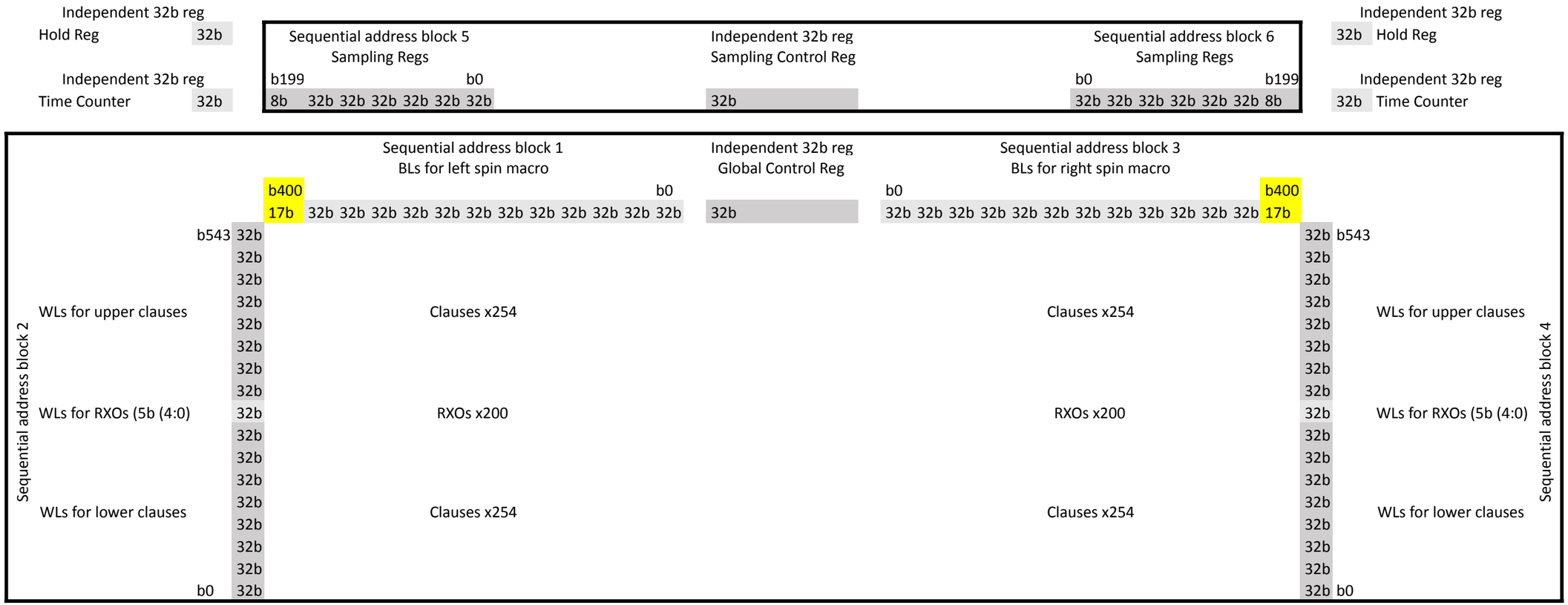

Note: Any non-32b register (ex 8b) is in reality what will be used even thoguh the digital will support 32b. The remaing bits are X and do not need to be wired

Registers

Name:	Size:	Access:	RESET:	Notes:
BL_LEFT<400:0>	401b	R/W	All 0	
WL_LEFT<543:0>	544b	R/W	See Sheet2	b287:261 are left floating in analog core
BL_RIGHT<400:0>	401b	R/W	All 0	
WL_RIGHT<543:0>	544b	R/W	See Sheet2	b287:261 are left floating in analog core
SMPL_DOUT_LEFT<199:0>	200b	R	NA	
SMPL_DOUIT_RIGHT<199:0>	200b	R	NA	
SMPL_TIME_LEFT<31:0>	32b	R	NA	
SMPL_TIME_RIGHT<31:0>	32b	R	NA	
GLBL_CTRL<31:0>	32b	R/W	See Sheet2	
SMPL_CTRL<31:0>	32b	R/W	See Sheet2	
BIAS_CTRL	32b	R/W		DELETED
HOLD_TIME_LEFT<31:0>	32b	R/W	All 1	
HOLD_TIME_RIGHT<31:0>	32b	R/W	All 1	
DIG_CLK	1b	NA	NA	Continous digital core clock shared to analog.
ERRb_LEFT	1b	NA	NA	Continous buffered out at 1.8V.
ERRb_RIGHT	1b	NA	NA	Continous buffered outr at 1.8V.
SMPL_DONE_LEFT	1b	R	NA	Goes to bit 0 of a 32b reg
SMPL_DONE_RIGHT	1b	R	NA	Goes to bit 0 of a 32b reg

Pads:	Count:
VDD	16
VSS	20
VREF_LEFT	1
VCM_LEFT	1
VREF_RIGHT	1
VCM_RIGHT	1
IBIAS_CMP	1
IBIAS_BLD_P	1
IBIAS_MAKE	1
IBIAS_BREAK	1
IBIAS_BLD_N	1
IBIAS_TIA	1

Global Control Reg (GLBL_CTRL<31:0>)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	X	X	X	X	X	X	X	X	X	X	X	CLS_SW_ENb_TOP_LEFT	CLS_SW_ENb_BOT_LEFT	RUN_LEFT	RXO_MODE_LEFT	RXO_RST_LEFT	X	X	X	X	X	X	X	X	X	X	X	CLS_SW_ENb_TOP_RIGHT	CLS_SW_ENb_BOT_RIGHT	RUN_RIGHT	RXO_MODE_RIGHT	RXO_RST_RIGHT
Reset value:	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1

Sampling Control Reg (SMPL_CTRL<31:0>)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	X	X	X	X	X	X	X	X	X	X	SMPL_RSTb_LEFT	SMPL_MODE_LEFT	ERRb_MODE_LEFT	DIG_TRIG_LEFT	CLK_DIV_LEFT<1>	CLK_DIV_LEFT<0>	X	X	X	X	X	X	X	X	X	X	SMPL_RSTb_RIGHT	SMPL_MODE_RIGHT	ERRb_MODE_RIGHT	DIG_TRIG_RIGHT	CLK_DIV_RIGHT<1>	CLK_DIV_RIGHT<0>
Reset value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bias Control Reg

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

DELETED

WL Reg (b543:b0)

543 0

REG_TOP_RSTb, WL<542:1>, REG_BOT_RSTb

	543	. . .	542	541	540	539	538	537	536	535	534	533	532	531	530	529	528	527	526	525	524	523	522	521	520	519	518	517	516	515	514	513	512	. . .	1	0
	REG_TOP_RSTb		WL<542:1>																																	REG_BOT_RSTb
Reset value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RXO WL Reg (b256:b287)

287 . . . 256

	287	286	285	284	283	282	281	280	279	278	277	276	275	274	273	272	271	270	269	268	267	266	265	264	263	262	261	260	259	258	257	256
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X_3	X_2	BIAS	X_1	X_0
Reset value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RXO Internal Reg | **RXO Bias Reg** | **CLS Reg**

7	6	5	4	3	2	1	0
X	X	TIA_DN_N_EN	TIA_DN_P_EN	TIA_UP_N_EN	TIA_UP_P_EN	CPL_INIT	RXO_INIT

7	6	5	4	3	2	1	0
TIA_EN	BLD_N_EN	BLD_P_EN	CMP_EN	X	X	X	X

1	0
CLS_EN	CLS_INV